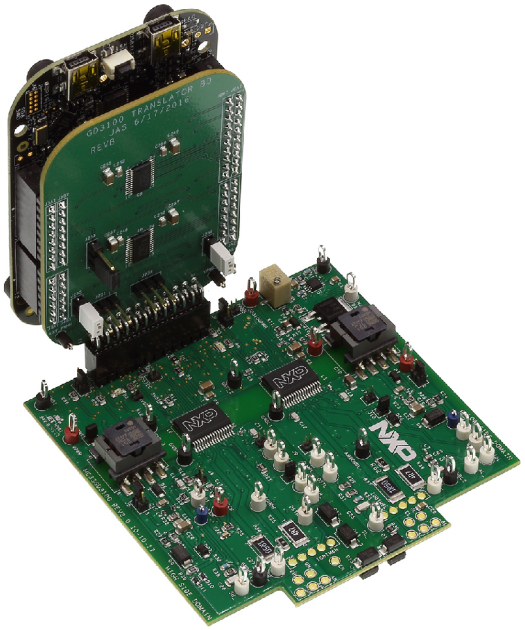
UM11108

FRDM-GD3100EVM half-bridge evaluation board

Rev. 3.0 — 16 August 2018 User guide

1 FRDM-GD3100EVM



aaa-029657

Figure 1. FRDM-GD3100EVM

2 Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

Should this evaluation kit not meet the specifications indicated in the kit, it may be returned within 30 days from the date of delivery and will be replaced by a new kit.

NXP reserves the right to make changes without further notice to any products herein. NXP makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typical”, must be validated for each customer application by customer’s technical experts.

NXP does not convey any license under its patent rights nor the rights of others. NXP products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the NXP product could create a situation where personal injury or death may occur.

Should the Buyer purchase or use NXP products for any such unintended or unauthorized application, the Buyer shall indemnify and hold NXP and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges NXP was negligent regarding the design or manufacture of the part.

3 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. These development boards support a range of analog, mixedsignal, and power solutions. These boards incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

The tool summary page for FRDM-GD3100EVM is at http://www.nxp.com/FRDM-GD3100EVM. The overview tab on this page provides an overview of the device, a list of device features, a description of the kit contents, links to supported devices and a **Get Started** section.

The **Get Started** section provides information applicable to using the the FRDM-GD3100EVM.

- Go to http://www.nxp.com/FRDM-GD3100EVM.
- On the **Overview** tab, locate the **Jump To** navigation feature on the left side of the window.
- Select the **Get Started** link.
  Review each entry in the **Get Started** section.
- Download an entry by clicking on the linked title.

After reviewing the **Overview** tab, visit the other related tabs for additional information:

- **Documentation**: Download current documentation.
- **Software & Tools**: Download current hardware and software tools.
- **Buy/Parametrics**: Purchase the product and view the product parametrics.

After downloading files, review each file, including the user guide which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the **Get Started** section of the **Overview** tab.

3.1 Kit contents/packing list

The FRDM-GD3100EVM contents include:

- Complete assembly of KITGD3100 connected to FRDM-KL25Z
- 3.3 V to 5.0 V translator board
- Cable, USB type A male/type mini B male 3 ft
- Quick start guide

3.2 Required equipment

To use this kit, you need:

- 3.3 V to 5.0 V translator board
- Fuji IGBT 6MBI800XV-075V-01 (M653) or 6MBI800XVB-075 (M6+)
- DC link capacitor compatible with IGBT
  - Panasonic SH film capacitor, EZTZX00456A, DC 500V, 1400 µF (or EZTYL24680HA)
- 50 mil jumpers for configuration
- 50 µH, high current air core inductor for double pulse testing
- HV power supply with protection shield and hearing protection

- 25 V, 1.0 A DC power supply
- Pulse generator
- TEK MSO 4054 500 MHz 2.5 GS/s 4-channel oscilloscope
- Rogowski coil, PEM Model CWT Mini HF60R or CTW MiniHF30 (smaller diameter)
- Two isolated high voltage probes (CAL Test Electric CT2593-1, LeCroy AP030)
- Four low voltage probes
- Two digital voltmeters

3.3 System requirements

The kit requires the following to function properly with the software:

- Windows XP or higher operating system

4 Getting to know the hardware

4.1 Board features

- Capability to connect to Fuji M653 or M6+ IGBT modules for half-bridge evaluations
- Daisy Chain SPI communication capable
- Power supply and fail-safe jumper configurable
- Easy access power, ground and signal test points

4.2 Device features

Table 1. Device features

Device	Description	Features
MC33GD3100	The MC33GD3100 is an advanced single channel gate driver for IGBTs.	• Compatible with current sense and temp sense IGBTs • DESAT detection capability for detecting V_{CE} desaturation condition • Fast short-circuit protection for IGBTs with current sense feedback • Compliant with ASIL C/D ISO 26262 functional safety requirements • SPI interface for safety monitoring, programmability and flexibility • Integrated Galvanic signal isolation • Integrated gate drive power stage capable of 10 A peak source and sink • Interrupt pin for fast response to faults • Compatible with negative gate supply • Compatible with 200 V to 1700 V IGBTs, power range > 125 kW

4.3 Board description

The Freedom KL25Z is microcontroller hardware for interfacing PC with SPIGen software to the SPI programmable registers on the MC33GD3100 devices on the GD3100 half-bridge evaluation board. GD3100 translator board is used to translate 3.3 V signals to 5.0 V signals between MCU hardware and MC33GD3100 gate drivers on the half-bridge evaluation board.

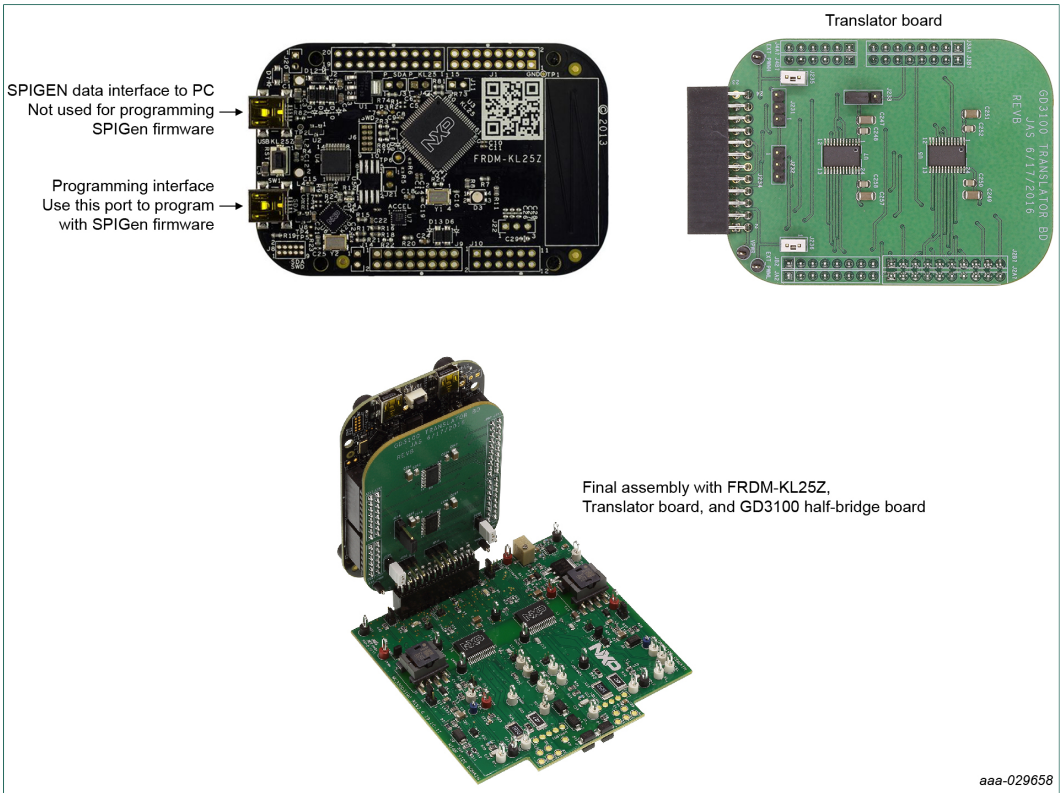


Figure 2. Connecting FRDM-KL25Z, GD3100 half-bridge EVB and translator board

4.3.1 Voltage domains, GD3100 pinout, logic header and IGBT pinout

Low-voltage domain is 12 V VPWR domain that interfaces with the MCU and MC33GD3100 control registers through the 24-pin connector interface.

Low-side driver and high-side driver domains are driver control interfaces to IGBT single phase connections and test points.

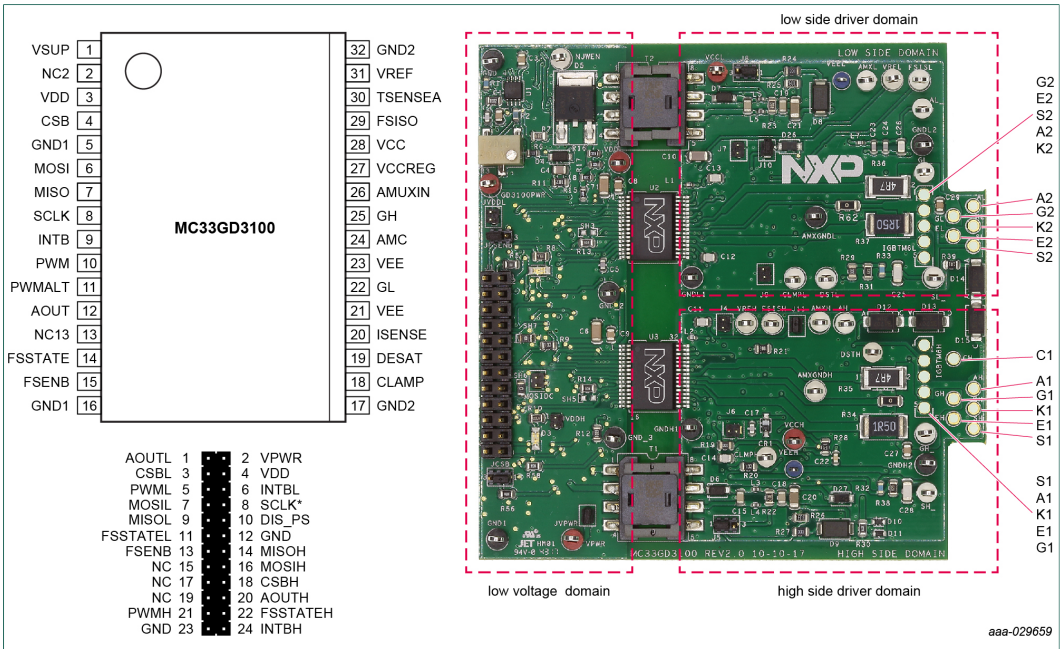


Figure 3. Evaluation board voltage and interface domains

Table 2. 24-pin connector definitions

Pin	Name	Function
1	AOUTL	Duty cycle encoded signal (low-side)
2	VSUP	Power input (+12 V)
3	CSBL	Chip select bar (low-side)
4	VDD	5.0 V power
5	PWML	PWM input (low-side)
6	INTBL	Interrupt bar (low-side)
7	MOSIL	Master out slave in (low-side)
8	SCLK	Serial clock input
9	MISOL	Master in Slave out (low-side)
11	FSSTATEL	Fail-safe state (low-side)
12	GND	Ground
13	FSENB	Fail-safe enable (high-side and low-side)
14	MISOH	Master in slave out
15	NC	No connection
16	MOSIH	Master out slave in
17	NC	No connection
18	CSBH	Chip select bar (high-side)
19	NC	No connection
20	AOUTH	Duty cycle encoded signal (high-side)
21	PWMH	PWM input (high-side)
22	FSSTATEH	Fail-safe state (high-side)
23	GND	Ground
24	INTBH	Interrupt bar (high-side)

4.3.2 Test point definitions

All test points are clearly marked on the evaluation board. Figure 4 shows the location of various test points.

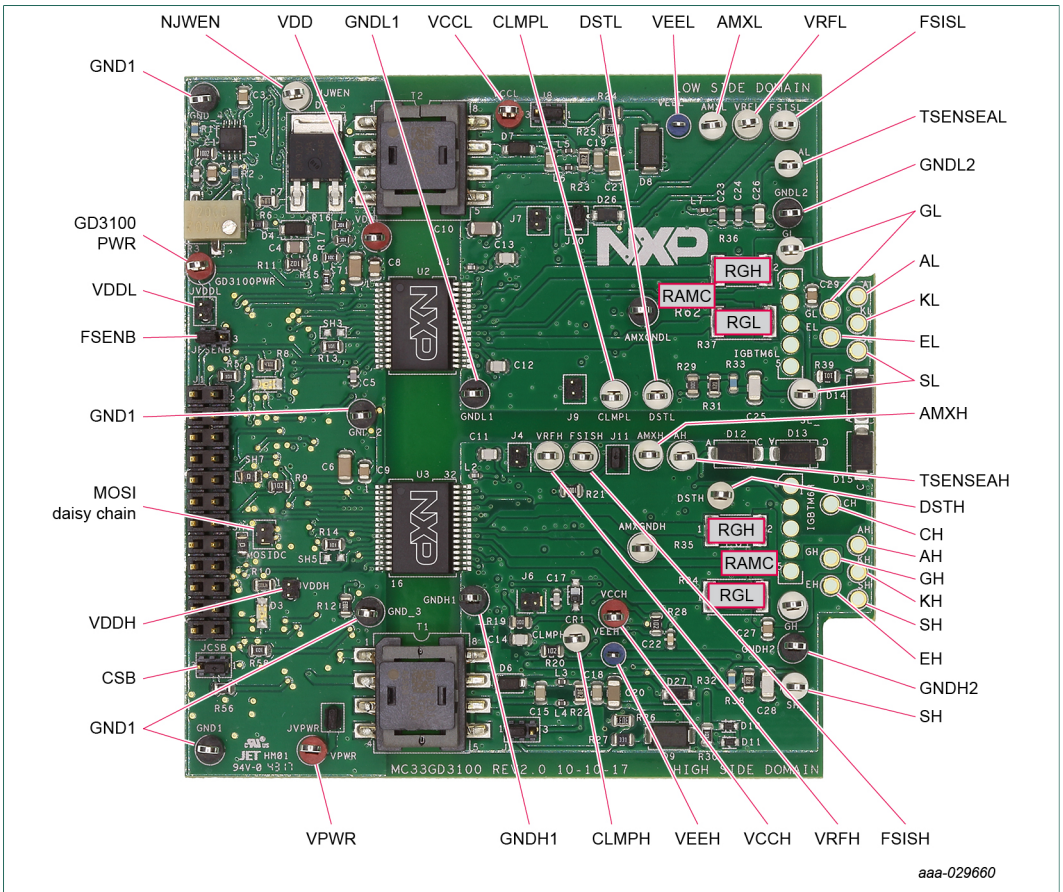


Figure 4. Key test point locations

Table 3. Test point definitions

Test point	Definitions
Low voltage domain	
VPWR	DC voltage source connection point for VSUP power input of MC33GD3100 devices. Typically supplied by vehicle battery +12V DC.
GND1_1,2,3,4	Grounding points for low voltage domain
GD3100PWR	MC33GD3100 VSUP test point
VDDL	MC33GD3100 VDD test point on low-side driver. See data sheet for usage.
NJWEN	Flyback enable test point connected to NJW4140 MOSFET drive switching regulator
Low-side driver domain	
VCCL	Positive voltage supply test point for isolated circuitry and low-side driver gate of IGBT
CLAMPL	V_{CE} sense test point connected to low-side driver clamp pin and circuitry
DSTL	V_{CE} desaturation test point connected to low-side driver DESAT pin and circuitry
VEEL	Negative voltage supply test point for low-side driver gate of IGBT
AMXL	Analog MUX input test point for low-side driver

Test point	Definitions
VREFL	5.0 V reference test point for isolated analog circuitry on low-side driver
FSISOL	Fail-safe state management test point for low-side driver domain
TSENSEAL	Temperature sense test point connected to anode of IGBT temp sense diode and MC33GD3100 TSENSEA input of low-side driver
GNDL1	Low-side driver ground point
GNDL2	Low-side driver ground point
AMXGNDL	Isolated ground test point for AMUXIN of MC33GD3100 low-side driver
GL	IGBT gate test point on low-side driver domain which is the charging pin of IGBT gate
SL	ISENSE test point connected to IGBT current sense and MC33GD3100 low-side driver ISENSE pin
High-side driver domain	
VCCH	Positive voltage supply test point for isolated circuitry and high-side driver gate of IGBT
CLAMPH	V_{CE} sense test point connected to high-side driver clamp pin and circuitry
DSTH	V_{CE} desaturation test point connected to high-side driver DESAT pin and circuitry
VEEH	Negative voltage supply test point for high-side driver gate of IGBT
AMXH	Analog MUX input test point for high-side driver
VREFH	5.0 V reference test point for isolated analog circuitry on high-side driver
FSISOH	Fail-safe state management test point for high-side driver domain
GNDH1	High-side driver ground point
GNDH2	High-side driver ground point
AMXGNDH	Isolated ground test point for AMUXIN of MC33GD3100 high-side driver
GH	IGBT gate test point on high-side driver domain which is the charging pin of IGBT gate
SH	ISENSE test point connected to IGBT current sense and MC33GD3100 high-side driver ISENSE pin

4.3.3 Power supply and fail-safe jumper configuration

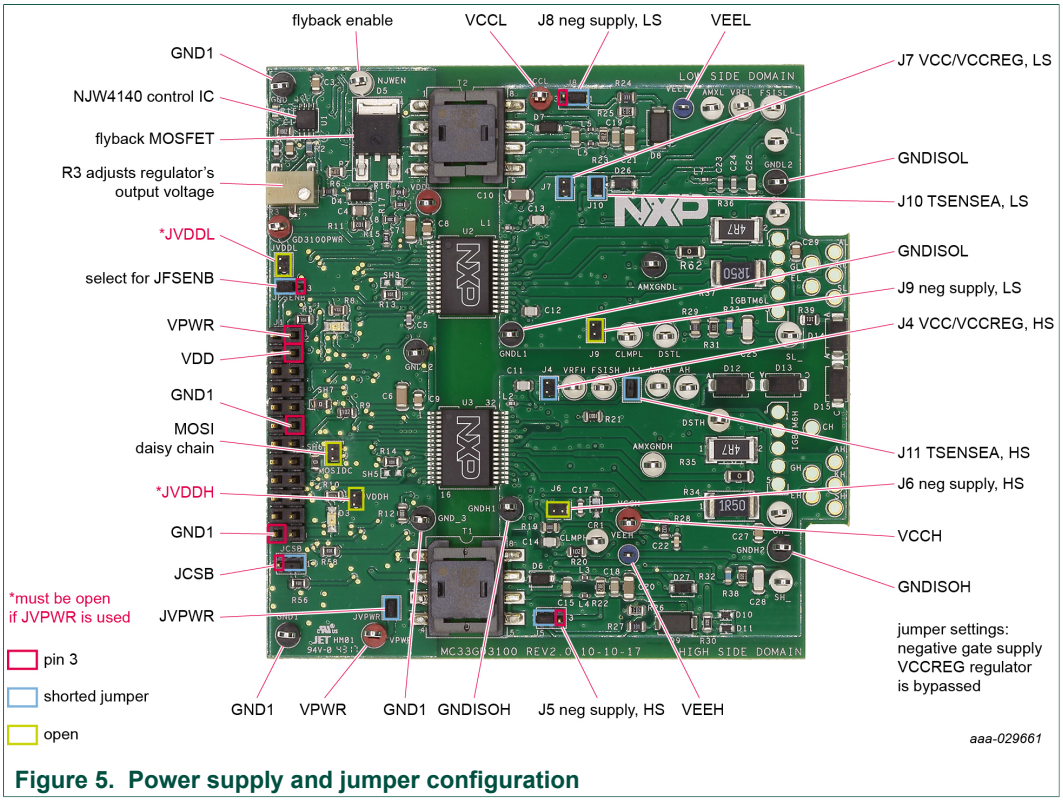


Figure 5. Power supply and jumper configuration

Table 4. Jumper definitions

Jumper	Position	Function
JVPWR	shorted	VSUP = VPWR external 12 V connection
	OPEN	VSUP is isolated from VPWR
JFSENB	1-2	FSENB = H (fail-safe not activated)
	2-3	FSENB = L (fail-safe is activated)
J4	shorted	VCC = VCCREG (HS)
	open	VCC and VCCREG (HS) are separate
J5	1-2	HS neg supply = active
	2-3	HS neg supply = GNDISOH
J6	shorted	HS neg supply = GNDISOH
	open	HS neg supply = active
J7	shorted	VCC = VCCREG (LS)
	open	VCC and VCCREG (LS) are separate
J8	1-2	LS neg supply = active
	2-3	LS neg supply = GNDISOL
J9	shorted	LS neg supply = GNDISOL
	open	LS Neg Supply = active
J10	shorted	TSENSEA LS active
	open	TSENSEA LS non-active (internal test mode only)
J11	shorted	TSENSEA HS active

Jumper	Position	Function
	open	TSENSEA HS non-active (internal test mode only)
JVDDL	shorted	VDDL to VPWR connection Short only when low voltage domain is powered by external 5.0 V
	open	VDDL isolated from external VSUP supply
JVDDH	shorted	VDDH to VPWR connection Short only when low voltage domain is powered by external 5.0 V
	open	VDDH isolated from external VSUP supply
MOSIDC	open	SPI MOSI for use in non-daisy chain mode
	shorted	SPI MOSI for use in daisy chain mode (connects MISOL to MOSIH)
JCSB	1-2	SPI chip select for use in non-daisy chain mode
	2-3	SPI chip select for use in daisy chain mode (connects CSB pins of both GD3100 devices)

4.3.4 Bottom view

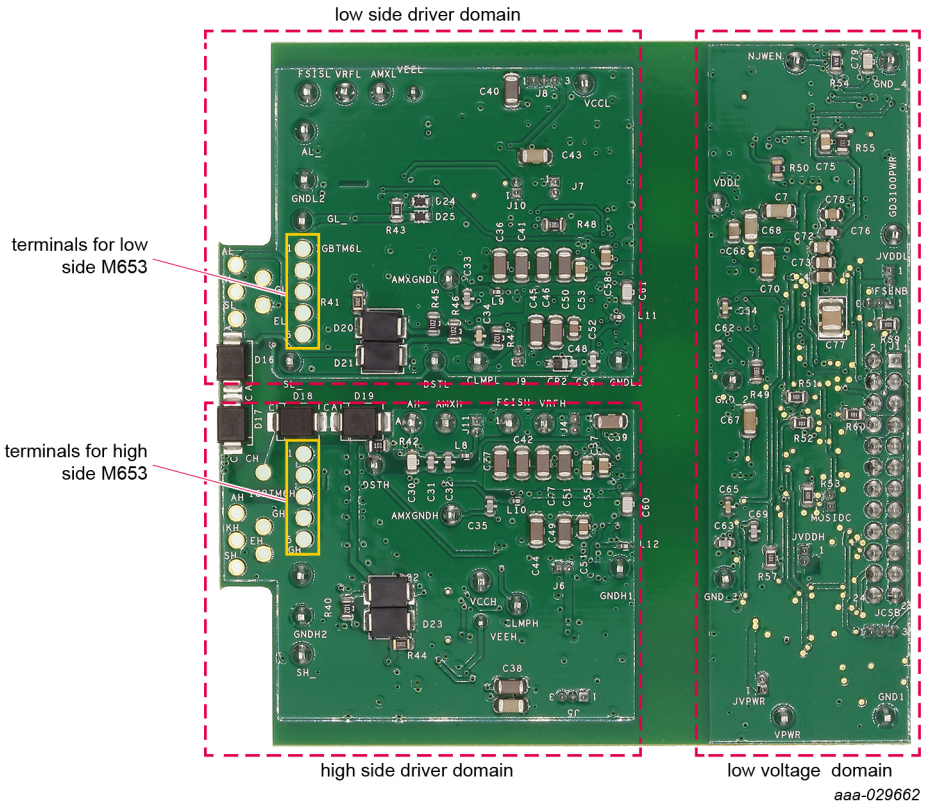


Figure 6. GD3100 evaluation board bottom view

4.3.5 Gate drive resistors

- RGH - gate high resistor in series with the GH pin at the output of the MC33GD3100 high-side driver and IGBT gate that controls the turn-on current for IGBT gate.
- RGL - gate low resistor in series with the GL pin at the output of the MC33GD3100 low-side driver and IGBT gate that controls the turn-off current for IGBT gate.

- RAMC - series resistor between IGBT gate and AMC input pin of the MC33GD3100 high-side/low-side driver for gate sensing and Active Miller clamping.

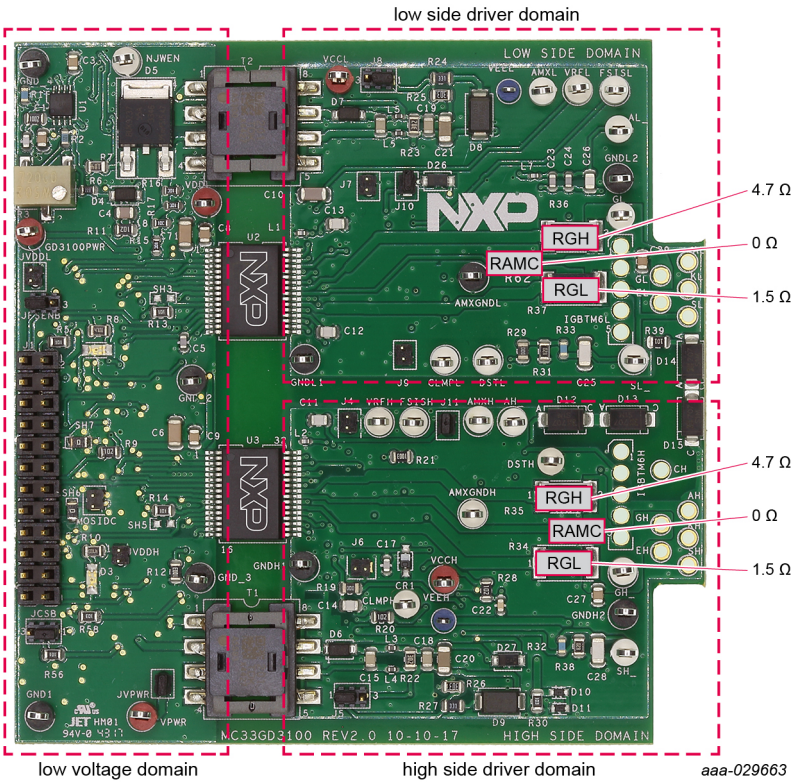


Figure 7. Gate drive resistors

4.3.6 LED interrupt indicators

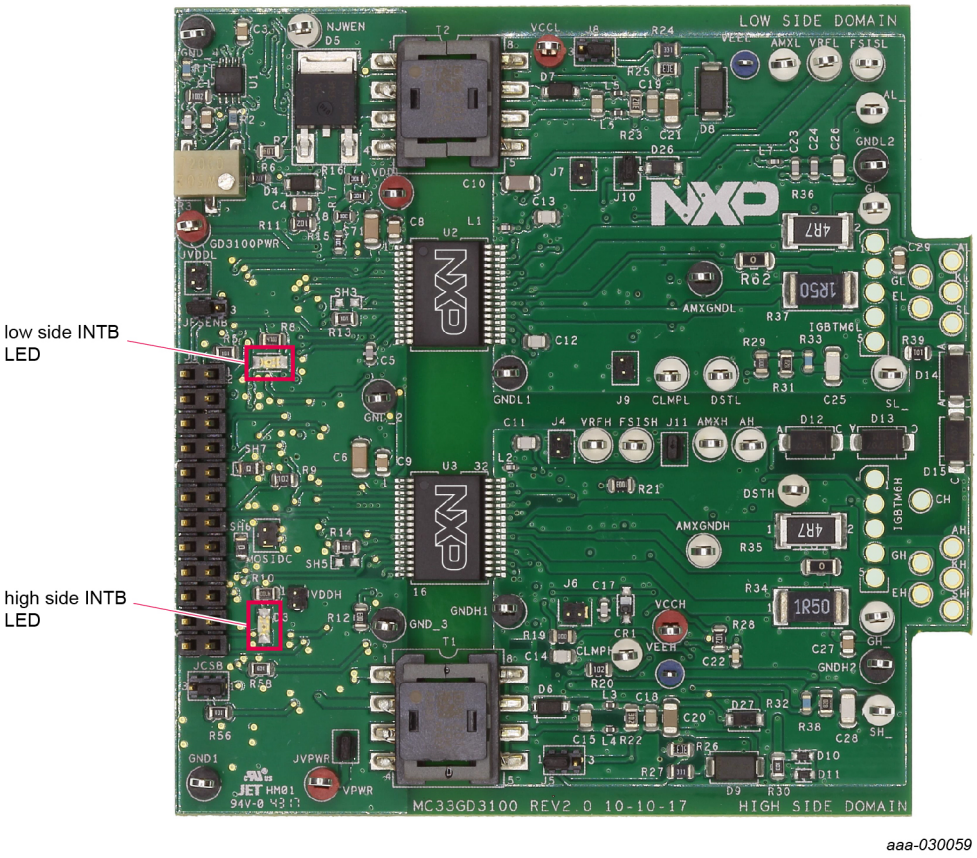


Figure 8. LED interrupt indicators

Table 5. LED interrupt indicators

LED	Description
Low-side INTB	Connected to the INTB output pin of low-side driver indicating reported fault status when on (active low)
High-side INTB	Connected to the INTB interrupt output pin of high-side driver indicating reported fault status when on (active low)

4.3.7 VDD, daisy chain, PWM and PWMALT disconnects; M653 terminals and pinout

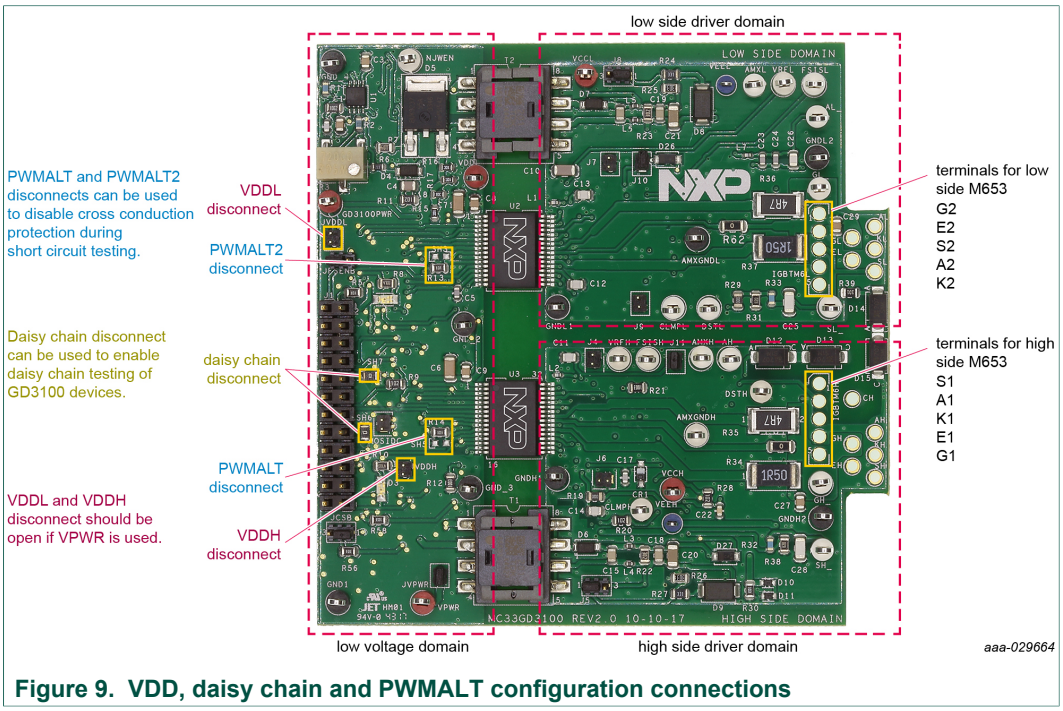


Figure 9. VDD, daisy chain and PWMALT configuration connections

- Disable PWM/PWMALT by changing four components. Remove R13 and R14 (normally populated) AND add SH3 and SH5 (normally open) to disable cross conduction and deadtime protection.
- SH6 and SH7: normally populated/shorted. Remove shorting resistors to enable SPI daisy chain operation in conjunction with JCSB and MOSIDC jumpers.
- JVDDL and JVDDH: **OPEN**
  Connects VPWR to VDD pins. This jumper is shorted only when the low voltage domain is powered by an external 5.0 V supply. When this jumper is in place, VPWR must be 5.0 V.

4.4 Quick start

4.4.1 Scope and purpose

This section provides comprehensive quick start notes for the FRDM-GD3100EVM half-bridge evaluation kit. Within a few minutes it is possible install SPIGEN application on a PC, power up half-bridge evaluation kit, and start SPI communication with the GD3100 devices as well as pass PWM signals for evaluation.

4.4.2 Intended audience

Experienced engineers evaluating MC33GD3100 gate drive device for IGBT control.

4.4.3 Setting up and connecting the evaluation kit

1. Download and install latest SPIGEN software – Windows application from NXP.com to your PC.

2. Assemble the FRDM-GD3100EVM with KL25Z micro board and translator board as shown in Figure 2.
3. Check jumper configuration on the evaluation board. The default jumper configuration (shipped from factory) is setup for non-daisy chain SPI communication with high-side and low-side driver domains VEE negative supply level active as described in Figure 5. Also, ensure jumper J233 is populated on Translator board as in Figure 11 for powering KL25Z micro.
   a. For daisy chain SPI communication of gate drive devices see Figure 9 and use daisy chain test interface section only of SPIGEN GUI GD3100 Mode tab.
4. Start SPIGEN application software on PC. Connect USB cable from PC to USBKL25Z port on KL25Z micro board. A successful connection results in a connection successful pop-up on the PC with SPIGEN application running.
   a. KL25Z micro shipped with proper firmware is already flashed. See Section 6 "Preparing graphical user interface operating environment" for additional details.
5. Next supply 12 V DC power to low voltage domain of evaluation board (12 V DC to VPWR connection point and grounding to GND1 connection point on low voltage domain).
6. Check high-side and low-side driver domain regulated voltage level by checking VCCH and VCCL test points for ~17 V DC with respect to grounding to points GNDH and GNDL in each domain respectively.
   a. If voltage level on VCCH and VCCL are low adjust R3 potentiometer for proper level as shown in Figure 5.
7. With proper PC interface connection and voltage levels, SPI communication can be conducted with MC33GD3100 devices as described in Section 6.1 "SPIGEN GUI" and referencing data sheet for MC33GD3100.
   a. Selecting SPI0 communicates with low-side gate drive device and SPI1 communicates with high-side gate drive device (see Figure 14).
8. To pass an external PWM signal through each gate drive device, remove jumpers J235 and J236 from translator board. Connect external PWM signal to high-side EXT_PWMH or low-side EXT_PWML as described in Figure 11. Gate drive output can be observed on high-side and low-side driver devices on GH_ and GL_ test points respectively.
9. For double pulse and short-circuit testing with an IGBT and inductive load, use pulse test GUI under SPIGEN GUI GD3100 for setting pulse widths using KL25Z micro.
   a. Jumpers J235 and J236 must be installed on Translator board for passing PWM signals from KL25Z micro.
   b. For short-circuit testing, PWMALT and PWMALT2 must be disconnected to disable cross-conduction and deadtime protection as described in Figure 9.

4.5 Kinetis KL25Z freedom board

The Freedom KL25Z is an ultra-low-cost development platform for Kinetis® L Series MCU built on Arm® Cortex®-M0+ processor.

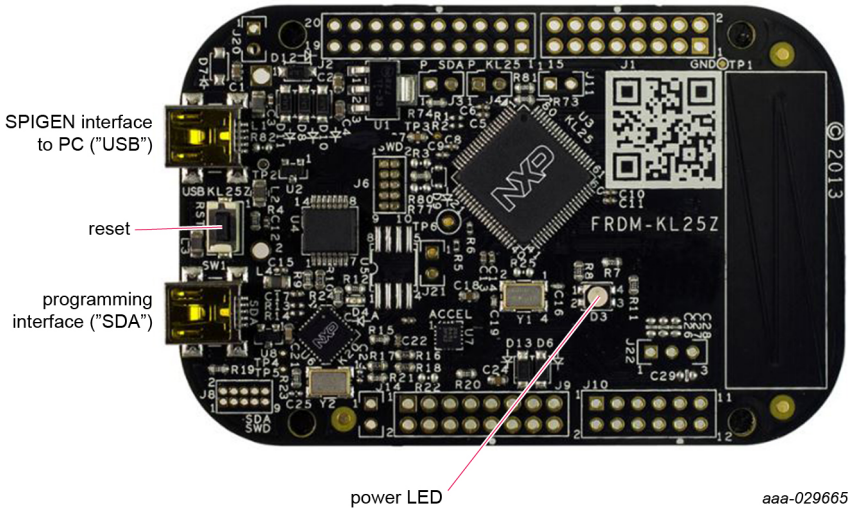


Figure 10. Freedom Development Platform

4.6 3.3 V to 5.0 V translator board

GD3100 translator enables level shifting of signals from 3.3 V to 5.0 V SPI communication.

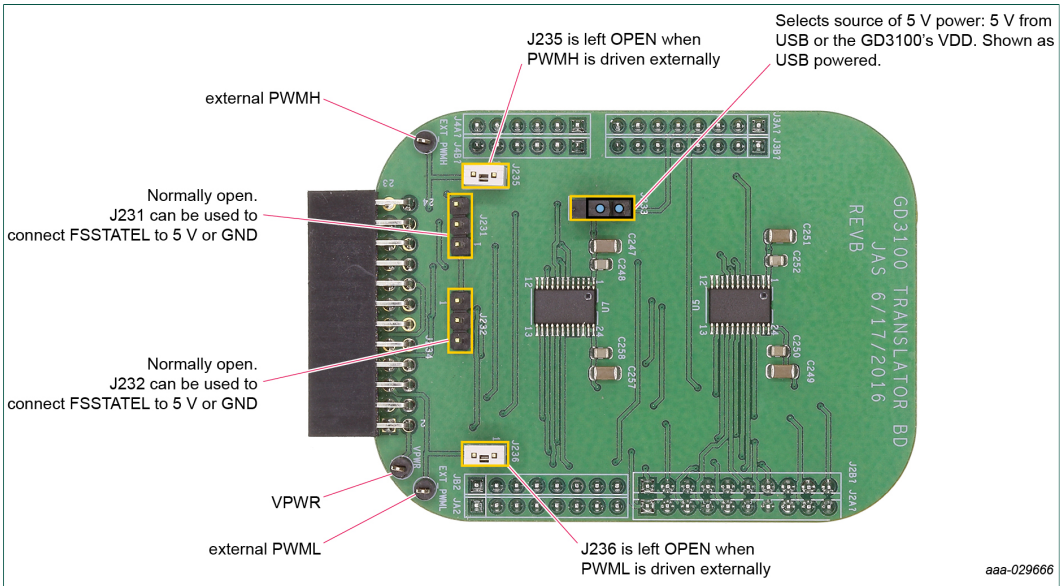


Figure 11. Translator board

5 Configuring the hardware

FRDM-GD3100EVM is connected to U Phase of a Fuji M653 IGBT module with SBE DC Link capacitor as shown in Figure 12. Double pulse and short-circuit testing can be conducted utilizing Windows based PC with SPIGEN software.

Suggested equipments needed for test:

- Rogowski coil high current probe
- High voltage differential voltage probe

- High sample rate digital oscilloscope with probes
- DC link capacitor
- Fuji M653 or M6+ IGBT module
- Windows based PC
- High voltage DC power supply for DC link
- Low voltage DC power supply for VPWR
  - +12 V DC gate drive board low voltage domain
- Voltmeter for monitoring high voltage DC Link supply
- Load coil

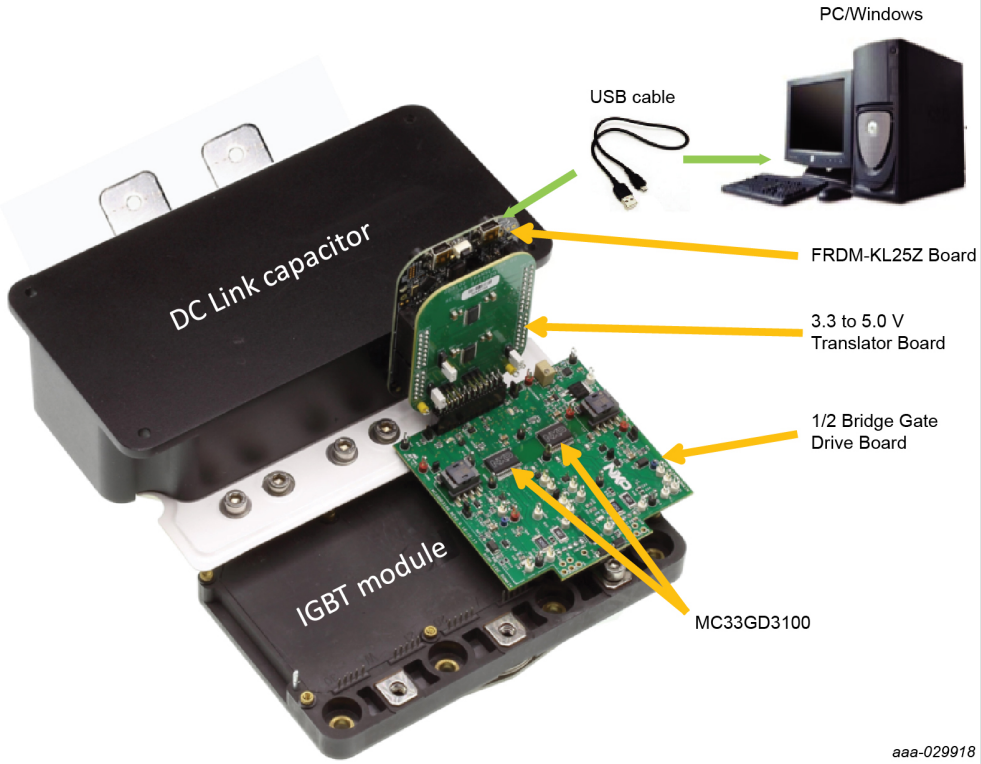


Figure 12. Evaluation board setup

6 Preparing graphical user interface operating environment

1. Install the firmware and MCU code.
   - The kit ships with KL25Z MCU firmware already installed. If for any reason the KL25Z MCU firmware needs to be re-installed follow this procedure. Hold down the reset button on the KL25Z board and connect a mini USB B cable from the PC to the Programming interface SDA USB port. Release the reset button. The PC shows a drive called **E:/BOOTLOADER** or something similar. Copy the SDA file (*MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA*) to the **E:/BOOTLOADER** drive.
   - Unplug and re-plug the USB cable to the same location to restart and activate the new firmware (do not hold the reset button this time). The drive name changes to **E:/FRDM-KL25Z** or something similar. Copy the file *UsbSpiDongleKL25Z_GD3100_545.srec* to the **E:/FRDM-KL25Z** drive. Unplug USB

cable. Firmware files are available with SPIGEN install which can be downloaded from NXP.com and can be found in SPIGEN install directory folder.

2. Run *SPIGEN SPI generator software installer* to install SPIGEN on PC.
3. Run SPIGEN with KL25Z board connected.
   - Connect the PC to the mini USB B cable into the “USBKL25Z” USB port on the KL25Z board.
   - Open the SPIGen software on the PC. At the bottom of the page you should see *SPI dongle Firmware Ver. 5.4.5* or something similar.

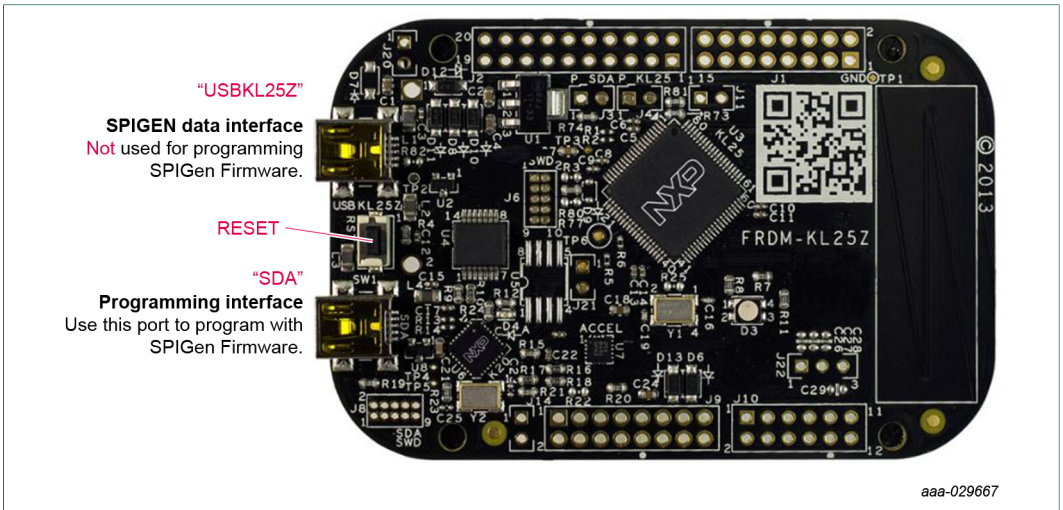


Figure 13. FRDM-KL25Z setup and interface

6.1 SPIGEN GUI

See Figure 14 for SPIGEN Graphical User Interface for MC33GD3100 internal register read and write access. It also includes the daisy chain read and write access when configured for daisy chain operation on certain MC33GD3100 registers.

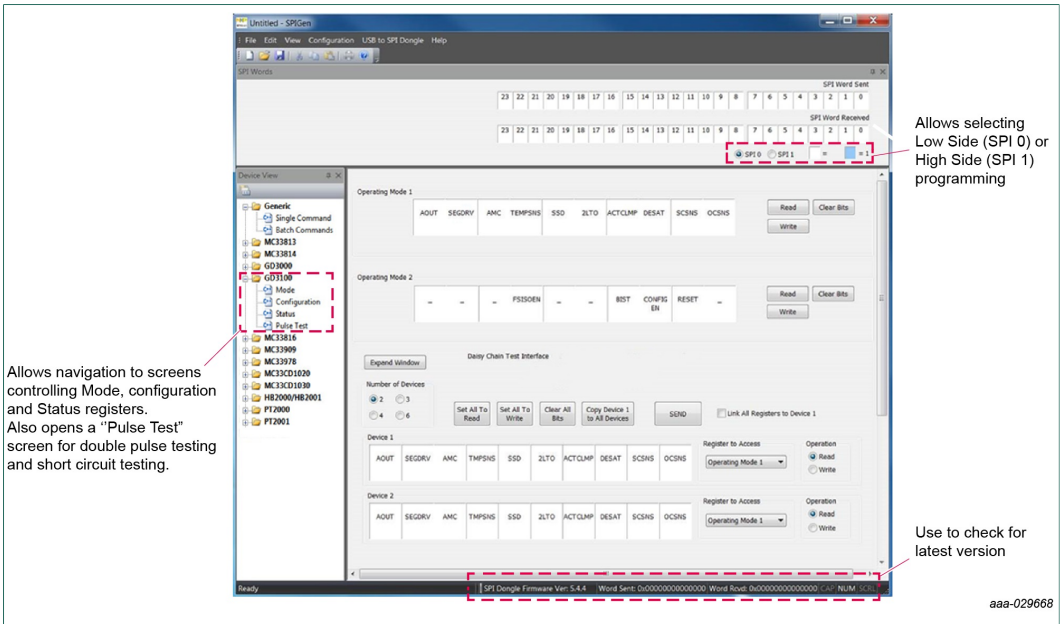
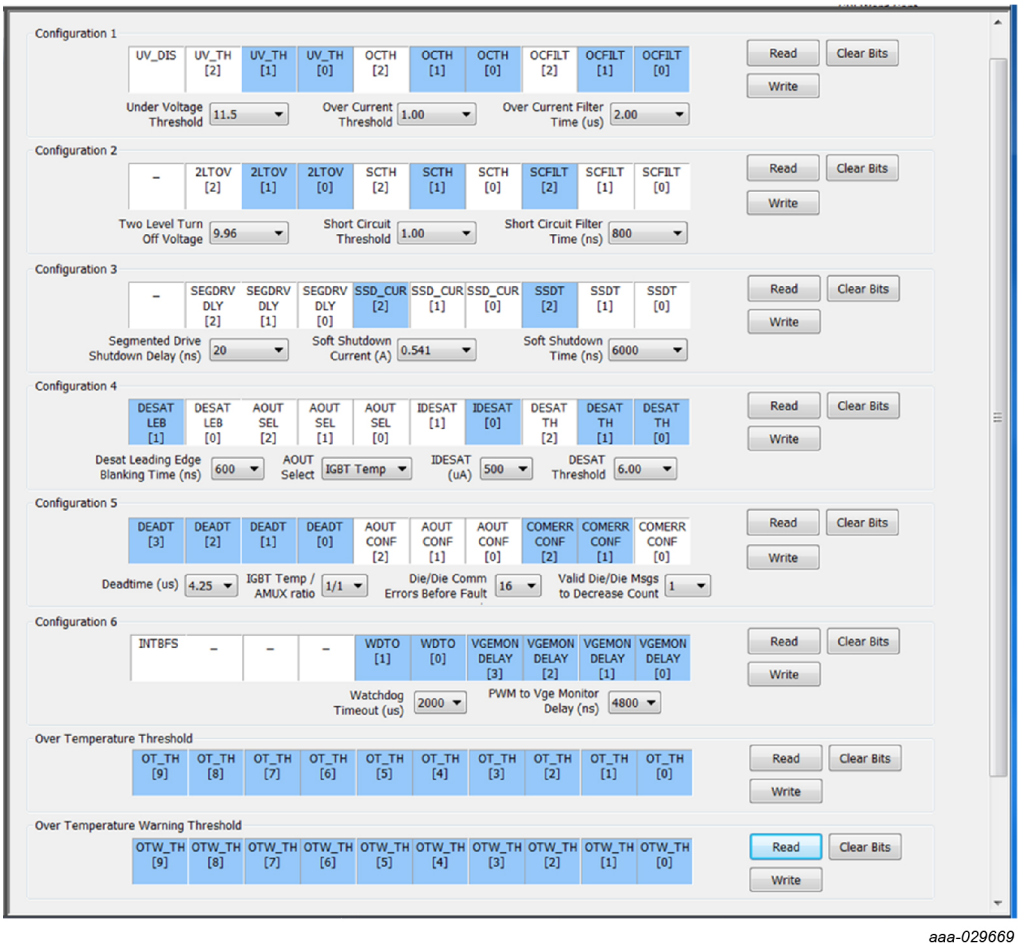


Figure 14. SPIGEN GUI

6.1.1 Configuration register

See MC33GD3100 data sheet for SPI configuration register descriptions.



aaa-029669

Figure 15. Configuration register window

6.1.2 Status and mask register

See MC33GD3100 data sheet for SPI configuration register descriptions.

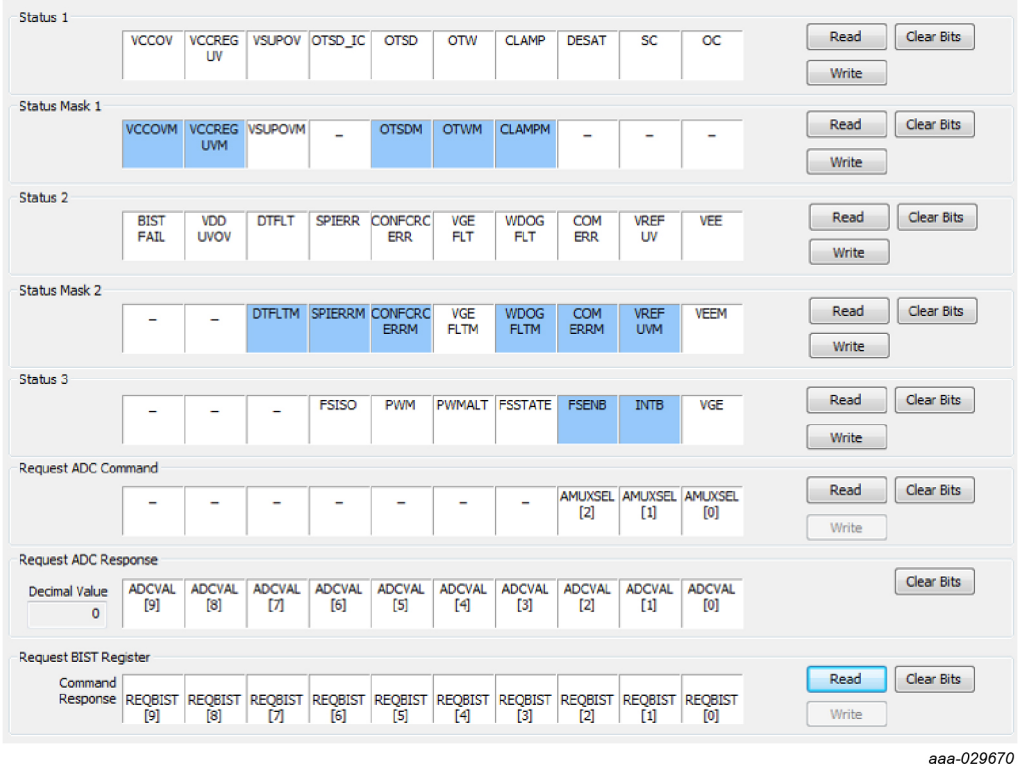


Figure 16. Status and mask register window

6.1.3 Double pulse and short-circuit test

See MC33GD3100 data sheet for SPI configuration register descriptions.

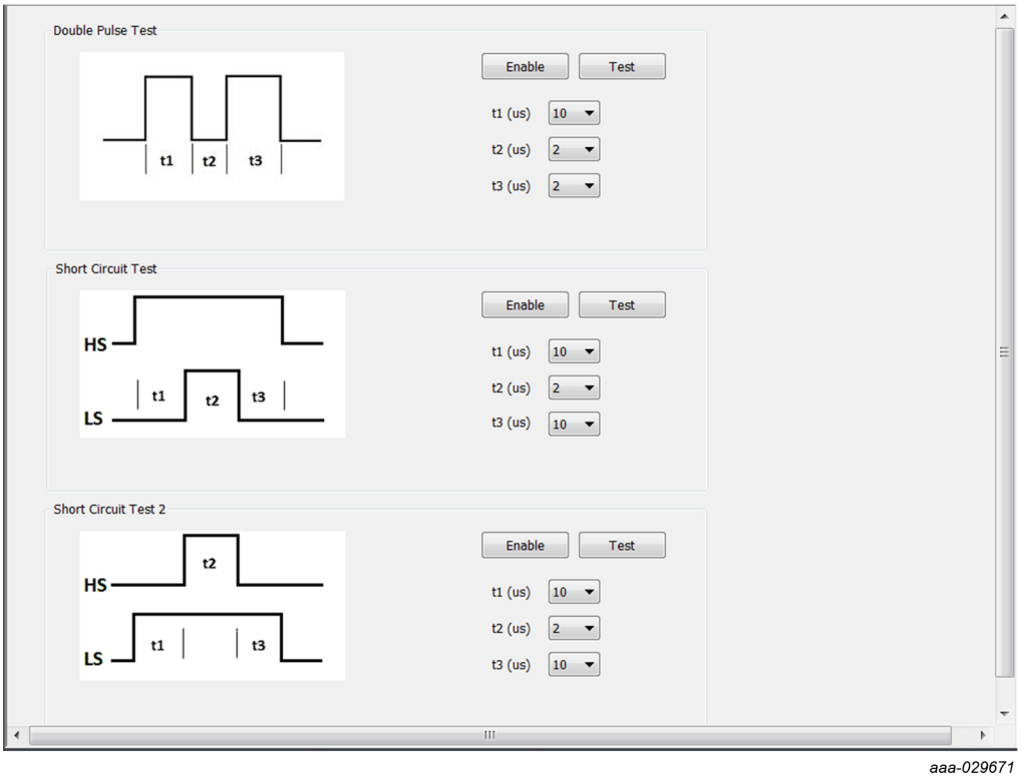


Figure 17. Double pulse and short circuit test window

7 Schematics, board layout and bill of materials

The board schematics, board layout and bill of materials are available at http://www.nxp.com/FRDM-GD3100EVM on the Overview tab under Get Started.

8 References

Following are URLs where you can obtain information on related NXP products and application solutions:

NXP.com support pages	Description	URL
FRDM-GD3100EVM	Tool summary page	http://www.nxp.com/FRDM-GD3100EVM
GD3100	Product summary page	http://www.nxp.com/GD3100

Revision history

Revision history

Rev	Date	Description
v.1	20180430	• Initial version
v.2	20180716	• Added Section 4.4
v.3	20180816	• Updated firmware install notes and changed firmware version to 5.4.5 in Section 6

9 Legal information

9.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

9.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

9.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

SafeAssure — is a trademark of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 16 August 2018