UG325: Class 3 Isolated Evaluation Board for the Si3404

The Si3404 isolated Flyback topology based evaluation board is a reference design for a power supply in a Power over Ethernet (PoE) Powered Device (PD) application.

This Si3404-ISO-FB EVB maximum output level is Class 3 power (η x 15.4 W).

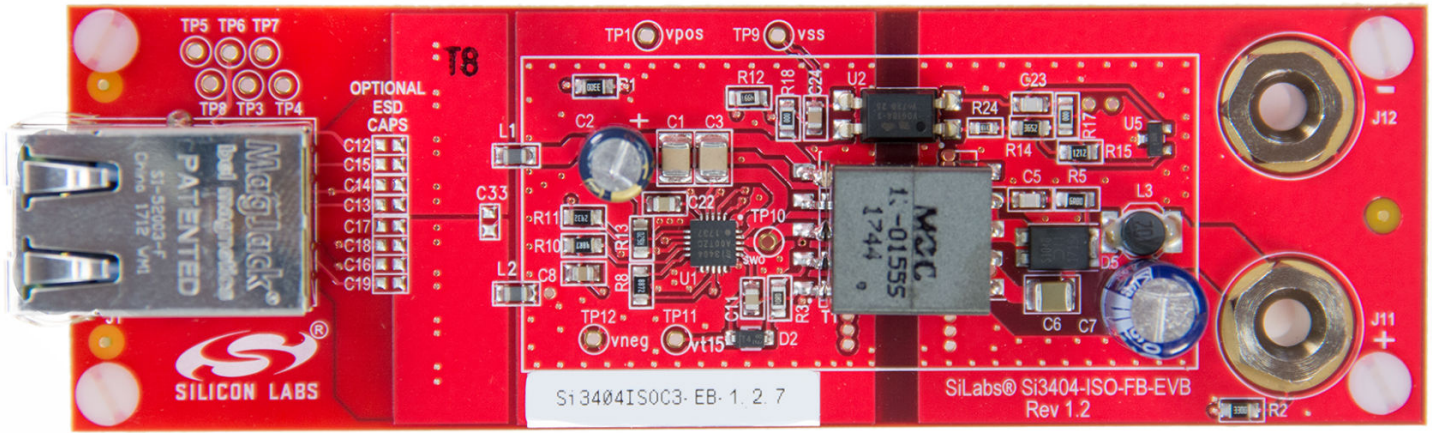
The Si3404-ISO-FB EVB board is shown below. The Si3404 IC integrates an IEEE 802.03af compatible PoE interface as well as a current control based dc/dc converter.

The Si3404 PD integrates a detection circuit, classification circuit, dc/dc switch, hot-swap switch, TVS overvoltage protection, dynamic soft-start circuit, cycle-by-cycle current limit, thermal shutdown, and inrush current protection.

The switching frequency of the converter is tunable by an external resistor.

KEY FEATURES

- IEEE 802.03af Compatible
- Very Small Application PCB Surface
- High Efficiency
- High Integration
- Low-Profile 4 x 4 mm 20-pin QFN
- Thermal Shutdown Protection
- Low BOM Cost
- Transient Overvoltage Protection



1. Kit Description

The Si3404-ISO-FB isolated Flyback topology based evaluation board is a reference design for power supplies in Power over Ethernet (PoE) Powered Device (PD) applications. The Si3404 device is described more completely in the data sheet and application notes. This document describes the evaluation board.

The Si3404-ISO-FB EVB is shown on the cover page. The schematic is shown in Figure 2.3 Si3404 Isolated Flyback EVB Schematic: 5 V, Class 3 PD on page 4, and the layout is in 16. Board Layout. The dc output is at connectors J11(+) and J12(–).

Boards are shipped configured to produce 5 V output voltage but can be configured for different output voltages, such as 3.3 or 12 V, for example, by changing resistors R14, R15, and a few other components. Refer to “AN1130: Using the Si3406/Si34061/Si34062 PoE + and Si3404 PoE PD Controller in Isolated and Non-Isolated Designs” for more information. The preconfigured Class 3 signature can also be modified, which is described as well in AN1130.

The silicon type diode bridge can be replaced with Schottky type diode bridges to achieve higher overall board efficiency.

To compensate the reverse leakage of the Schottky type diodes at high temperature, the recommended detection resistor should be adjusted to the values listed in the following table:

Table 1.1. Recommended Detection Resistor Values

External Diode Bridge	R_{DET}
Silicon Type	24.3 kΩ
Schottky Type	24.9 kΩ

2. Getting Started: Powering Up the Si3404-ISO-FB Board

Ethernet data and power are applied to the board through the RJ45 connector (J1). The board itself has no Ethernet data transmission functionality, but, as a convenience, the Ethernet transformer secondary-side data is brought out to test points.

The design can be used in Gigabit (10/100/1000) systems as well by using PoE RJ45 Magjack, such as type L8BE-1G1T-BFH from Bel Fuse.

Power may be applied in the following ways:

- Using an IEEE 802.3-2015-compliant, PoE-capable PSE, such as Trendnet TPE-1020WS
- Using a laboratory power supply unit (PSU):
  - Connecting a dc source between blue/white-blue and brown/white-brown of the Ethernet cable (either polarity), (End-span) as shown below:

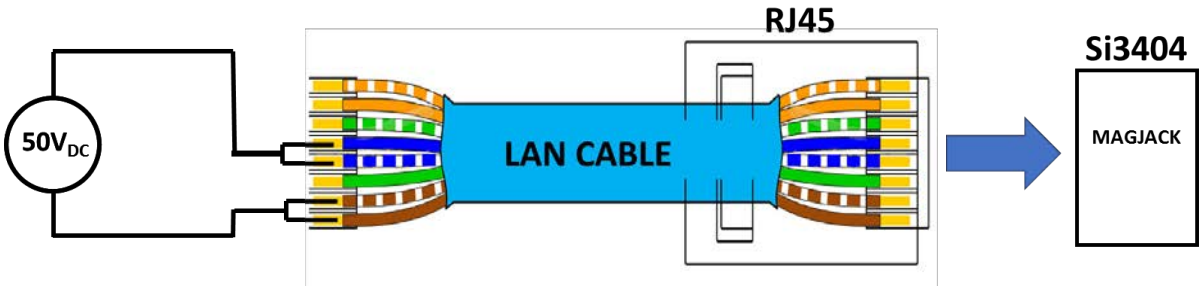


Figure 2.1. Endspan Connection using Laboratory Power Supply

  - Connecting a dc source between green/white-green and orange/white-orange of the Ethernet cable (either polarity), (Mid-span) as shown below:

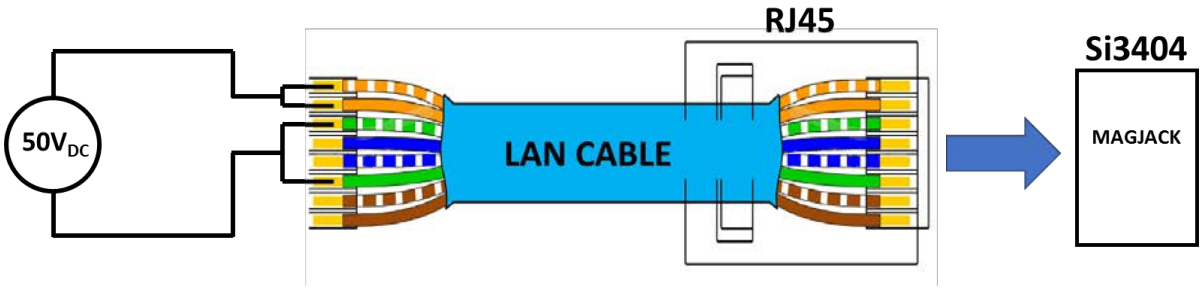


Figure 2.2. Midspan Connection using Laboratory Power Supply

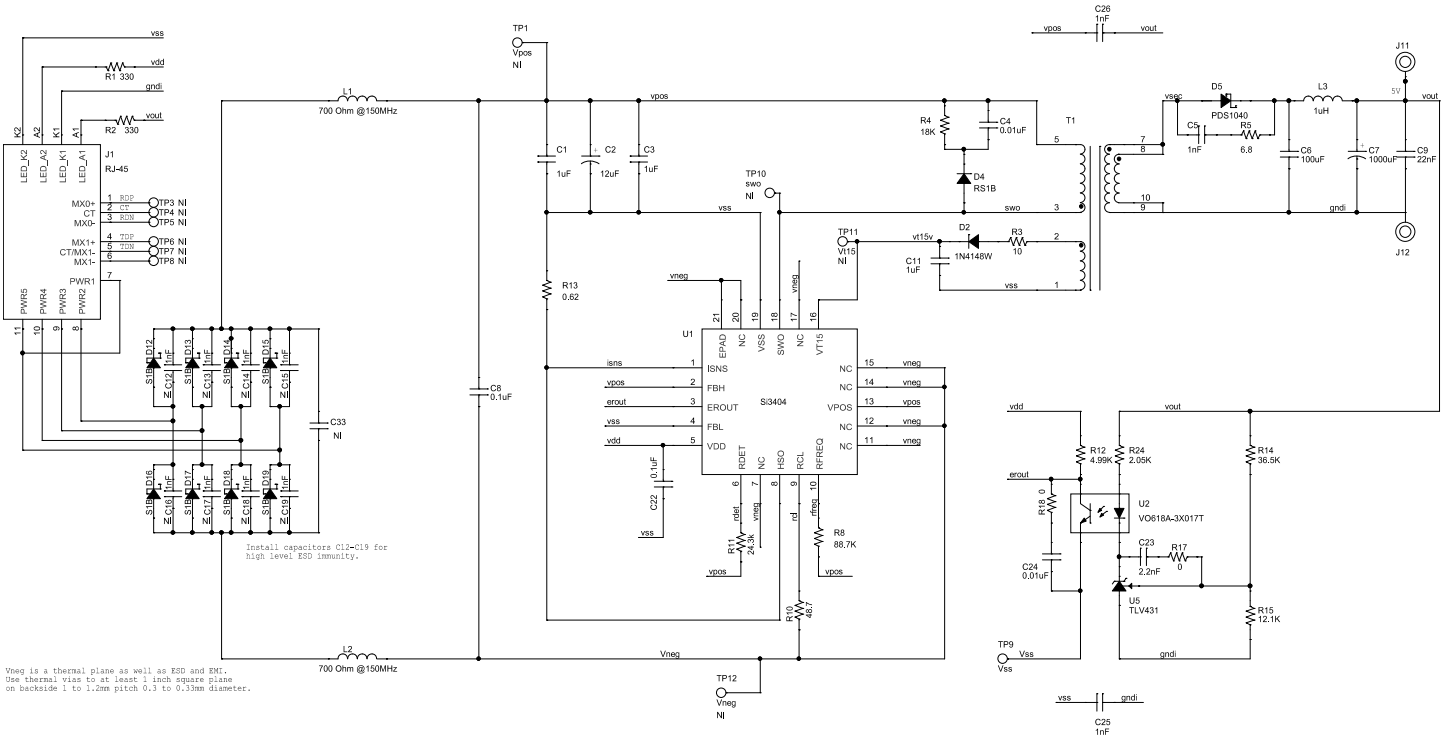


Figure 2.3. Si3404 Isolated Flyback EVB Schematic: 5 V, Class 3 PD

3. Overall EVB Efficiency

The overall efficiency measurement data of the Si3404-ISO-FB EVB board is shown below. The input voltage is 50 V, and the output voltage is 5 V.

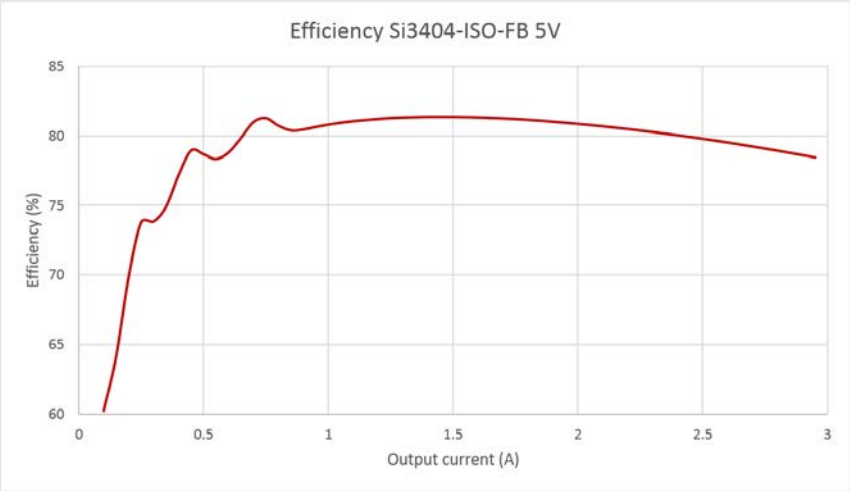


Figure 3.1. Si3404 Isolated Flyback EVB Overall Efficiency: 50 V Input, 5 V Output, Class 3

Note: The chart shows overall EVB efficiency. The voltage drop on the standard silicon diode bridge is included.

4. SIFOS PoE Compatibility Test Results

The Si3404-ISO-FB EVB board has been successfully tested with PDA-300 Powered Device Analyzer from SIFOS Technologies. The PDA-300 Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at PoE Powered Devices (PD's).

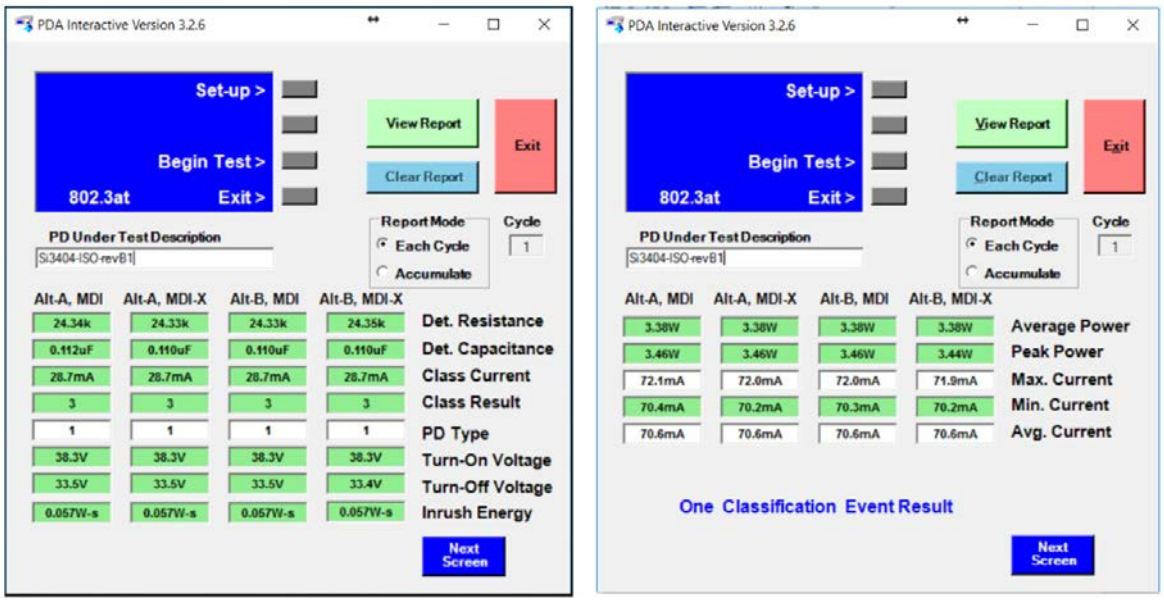


Figure 4.1. Si3404 Isolated Flyback PD SIFOS PoE Compatibility Test Results

5. Feedback Loop Phase and Gain Measurement Results (Bode Plots)

The Si3404 device integrates a current mode controlled switching mode power supply controller circuit. Therefore, the application is a closed-loop system. To guarantee a stable output voltage of a power supply and to reduce the influence of input supply voltage variations and load changes on the output voltage, the feedback loop should be stable.

To verify the stability of the loop, the loop gain and loop phase shift has been measured.

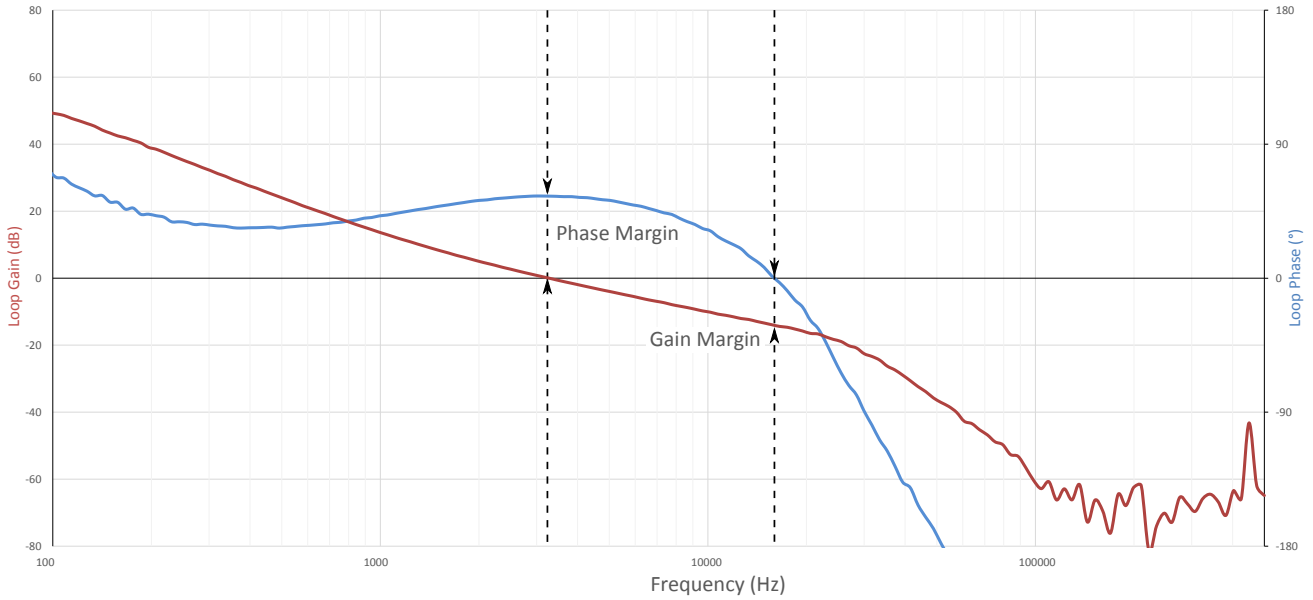


Figure 5.1. Si3404ISOFB-EVB Measured Loop-Gain and Phase Shift

Table 5.1. Measured Loop Gain and Phase Shift

	Frequency	Gain	Phase
Cursor 1 (Phase Margin)	3.3 kHz	0 dB	55°
Cursor 2 (Gain Margin)	16 kHz	–14 dB	0 °

6. Step Load Transient Measurement Results

The Si3404-ISO-FB EVB board's output has been tested with a step load function to verify the converters output dynamic response.

Step load: from 0.3A to 2.4A output current;	Step load: from 2.4A to 0.3A output current;

Figure 6.1. Si3404 Isolated Flyback EVB PD Output Step Load Transient Test

7. Output Voltage Ripple

The Si3404-ISO-FB EVB output voltage ripple has been measured in both no load and heavy load conditions.

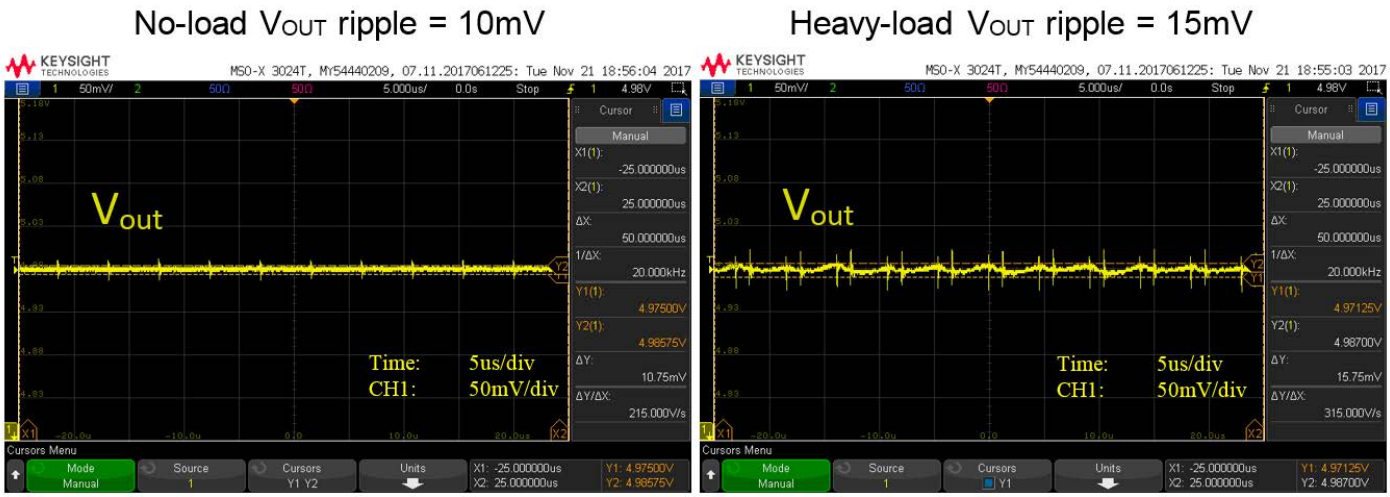


Figure 7.1. Si3404 Isolated Flyback EVB Output Voltage Ripple at No Load (Left) and Heavy Load (Right) Conditions

8. Soft-Start Protection

The Si3404 device has an integrated dynamic soft-start protection mechanism to avoid stressing the components by the sudden current or voltage changes associated with the initial charging of the output capacitors.

Figure 8.1. Si3404 Isolated Flyback EVB Output Voltage Soft-Start at Low Load (Left) and Heavy Load (Right) Conditions

9. Output Short Protection

The Si3404 device has an integrated output short protection mechanism, which protects the IC itself and the surrounding external components from overheating in the case of electrical short on the output.

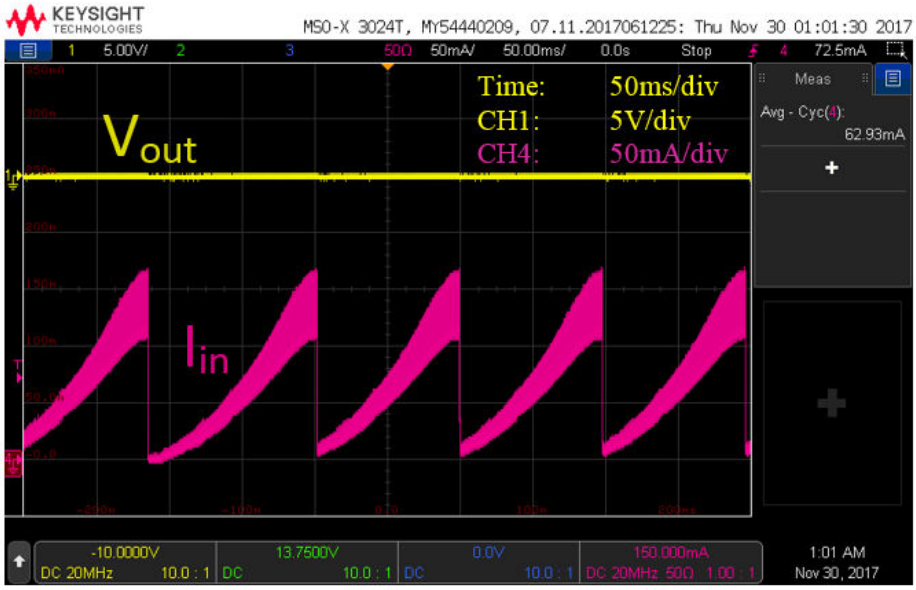


Figure 9.1. Si3404 Isolated Flyback EVB Output Short Circuit Protection

10. Pulse Skipping at No-Load Condition

The Si3404 device has an integrated pulse skipping mechanism to ensure ultra-low power consumption at no load condition.

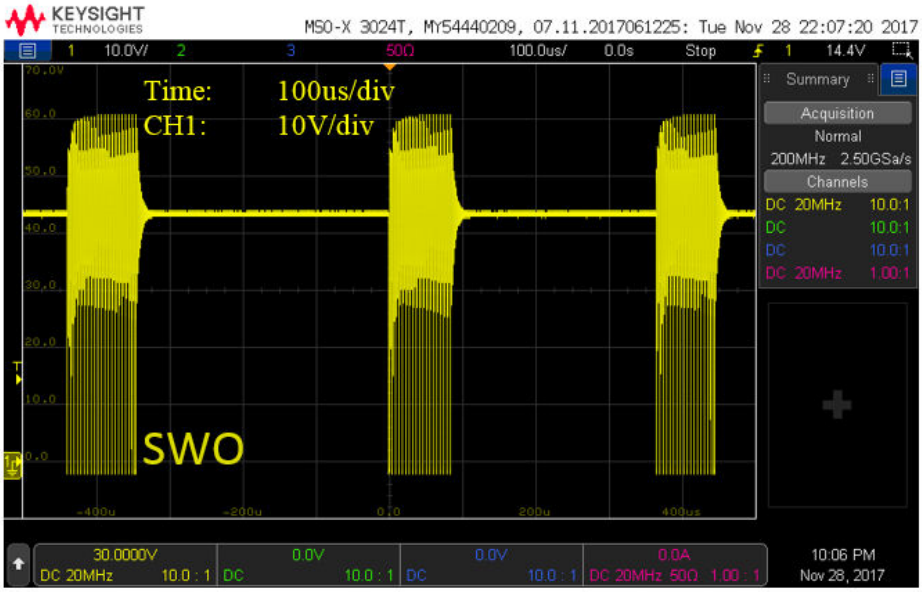


Figure 10.1. Si3404 Pulse Skipping at No-load Condition: SWO Waveform

11. Adjustable EVB Current Limit

For additional safety, the Si3404 has an adjustable EVB current limit feature. The EVB current limit through the ISNS pin measures the voltage on R_{SENSE}. When V_{ISNS} = –270 mV (referenced to V_{SS}), the current limit circuit restarts the circuit to protect the application.

The EVB current limit for this Class 3 application can be calculated with the following formula:

$$R_{SENSE} = 0.62\Omega$$

$$I_{LIMIT} = \frac{270mV}{0.62\Omega} = 435mA$$

Equation 1. EVB Current Limit

12. Tunable Switching Frequency

The switching frequency of the oscillator is selected by choosing an external resistor (RFREQ) connected between RFREQ and VPOS pins. The following figure will aid in choosing the RFREQ value to achieve the desired switching frequency.

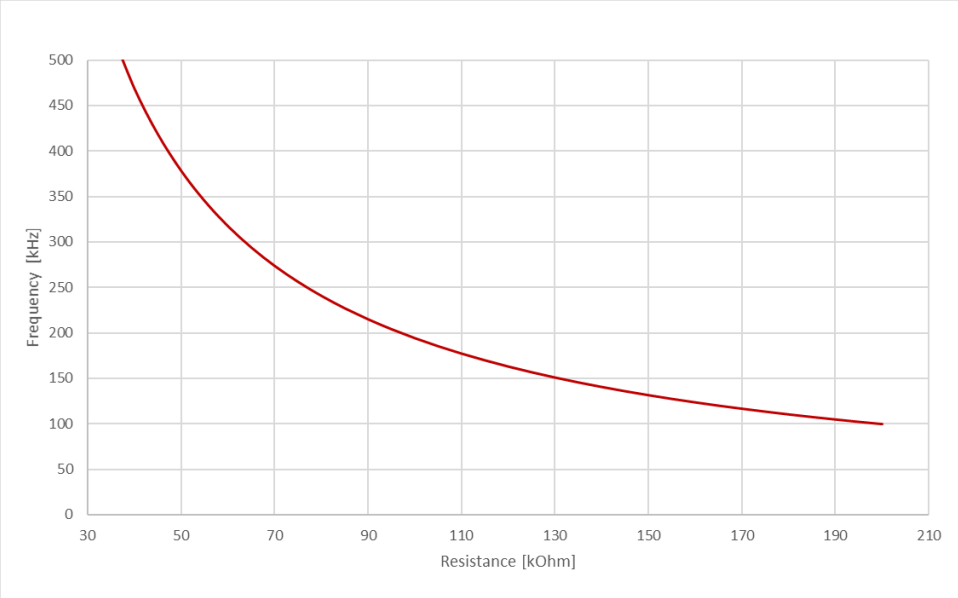


Figure 12.1. Switching Frequency vs R_{FREQ}

The selected switching frequency for this application is 220 kHz, which is achieved by setting the RFREQ resistor to 88.7 kΩ.

13. Discontinuous (DCM) and Continuous (CCM) Current Modes

At low-load the converter works in discontinuous current mode (DCM), at heavy load the converter runs in continuous current mode (CCM). At low-load the SWO voltage waveform has a ringing waveform, which is typical for a DCM operation.

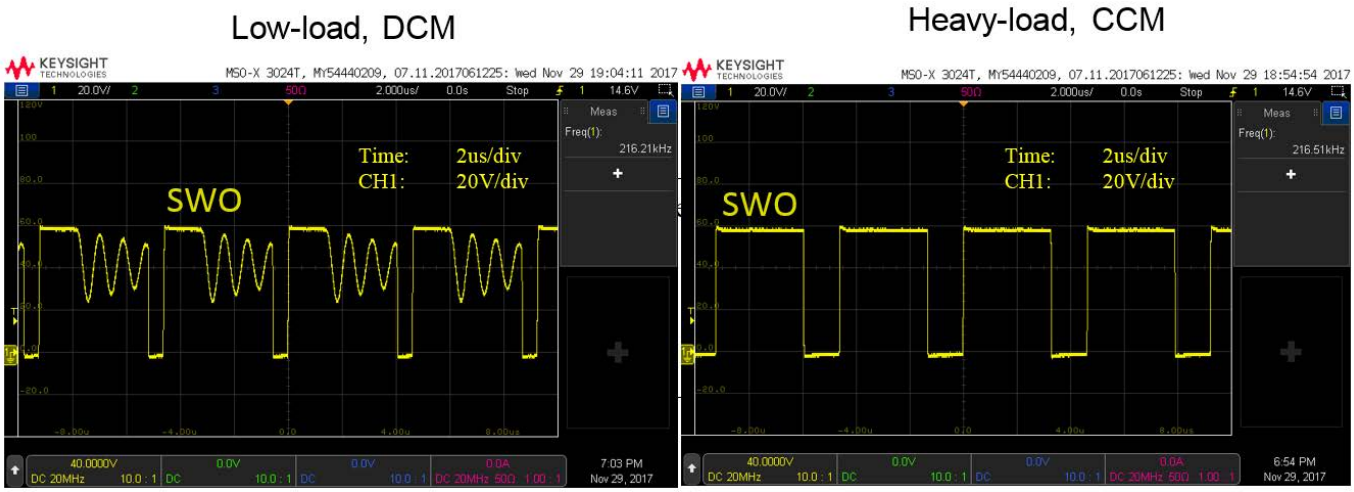


Figure 13.1. Si3404-ISO-FB SWO Waveform in Discontinuous Current Mode (DCM) at Low Load (Left) and in Continuous Current Mode (CCM) at Heavy Load (Right)

14. Radiated Emissions Measurement Results

Radiated emissions have been measured of the Si3404-ISO-FB EVB board with 50 V input voltage and full load connected to the output – 12.5 W.

As shown below, the Si3404-ISO-FB EVB is fully compliant with the international EN 55022 class B emissions standard.

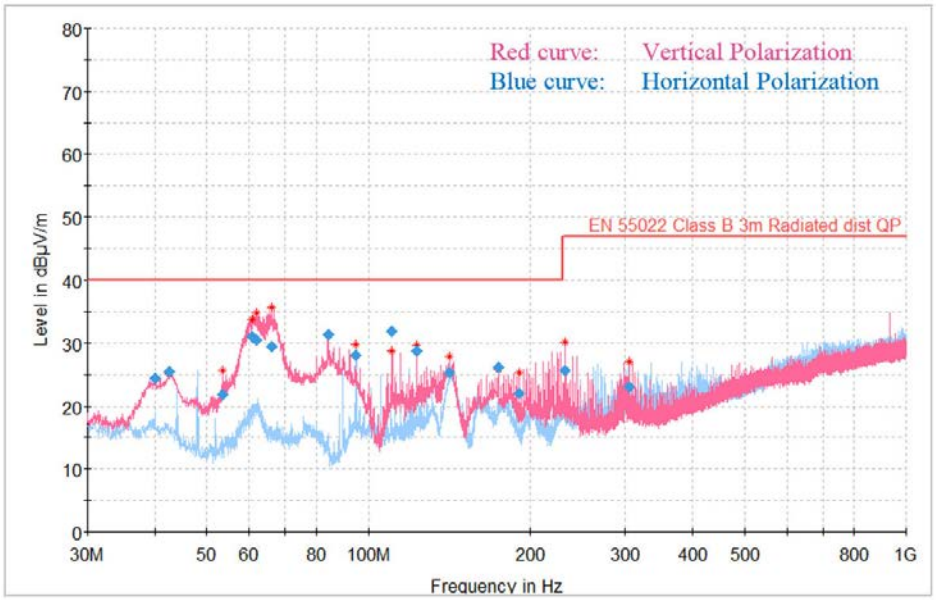


Figure 14.1. Si3404 Isolated Flyback EVB Radiated Emissions Measurements Results; 50 V Input, 5 V Output, 12.5 W Output Load

14.1 Radiated EMI Measurement Process

The EVB is measured at full load with peak detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a red curve (vertical polarization) and a blue curve (horizontal polarization). Next, specific frequencies are selected (red stars) for quasi-peak measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The results of this quasi-peak detector measurement are the blue rhombuses.

The blue rhombuses represent the final result of the measurement process. To have passing results, the blue rhombuses should be below the highlighted EN 55022 Class B limit.

15. Conducted Emissions Measurement Results

The Si3404-ISO-FB EVB board's conducted emissions have been measured, the result is shown below.

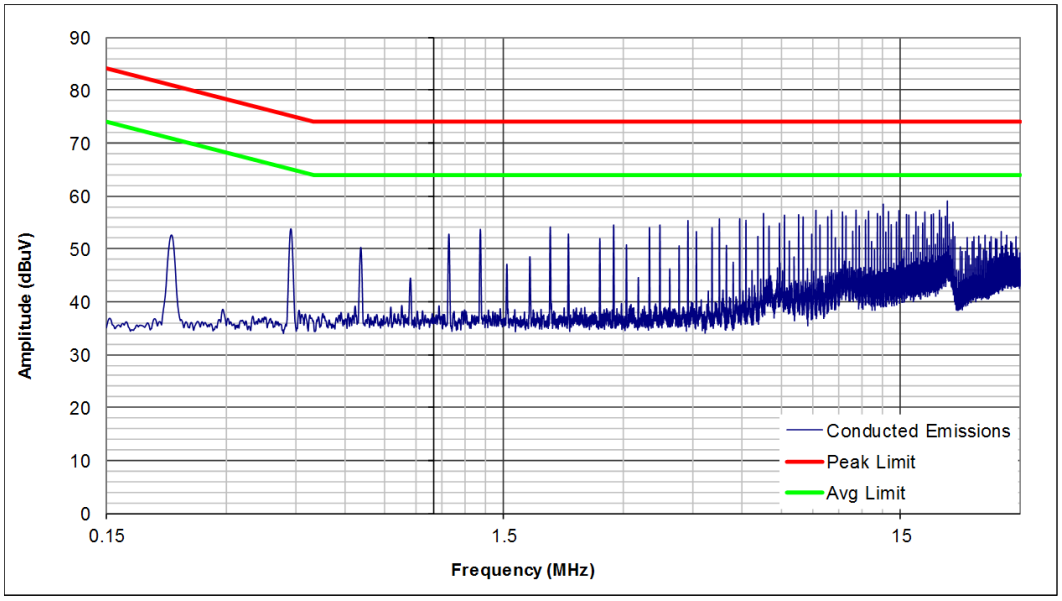


Figure 15.1. Si3404 Isolated Flyback EVB Conducted Emissions Measurements Results; 50 V Input, 5 V Output, 12.5 W Output Load

16. Board Layout

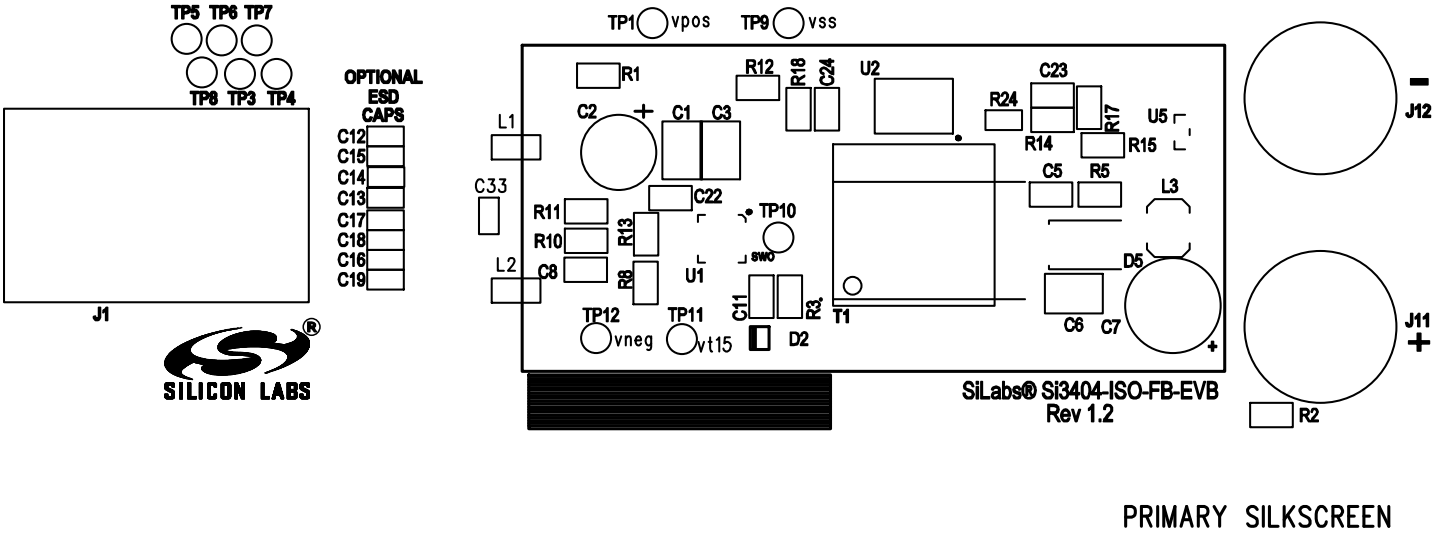


Figure 16.1. Top Silkscreen

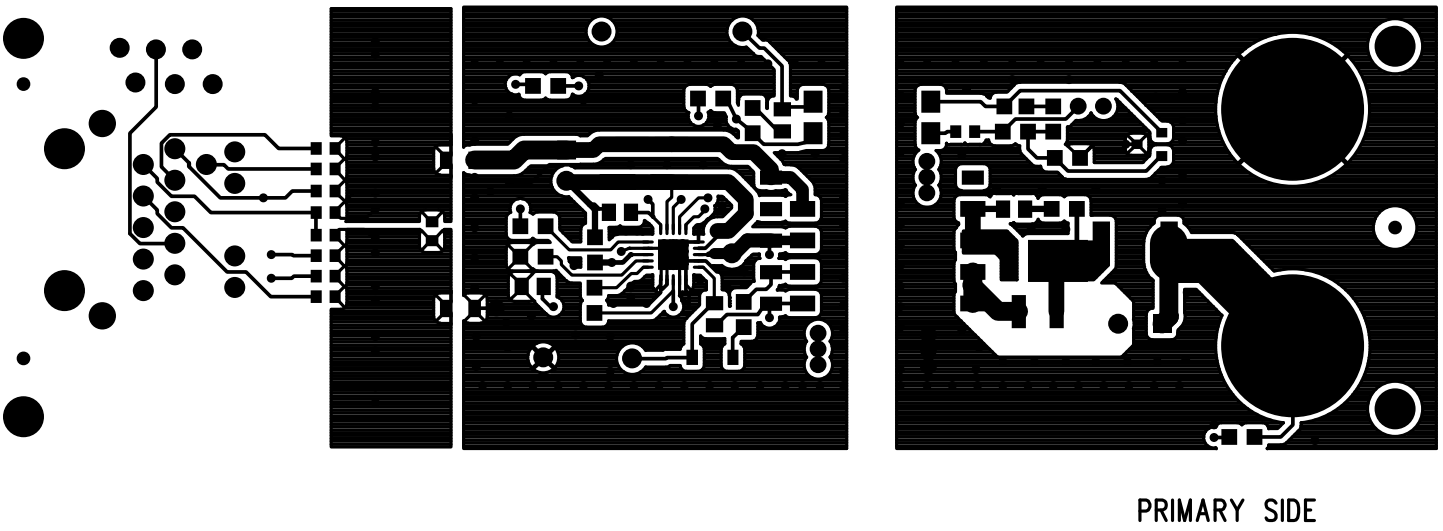


Figure 16.2. Top Layer

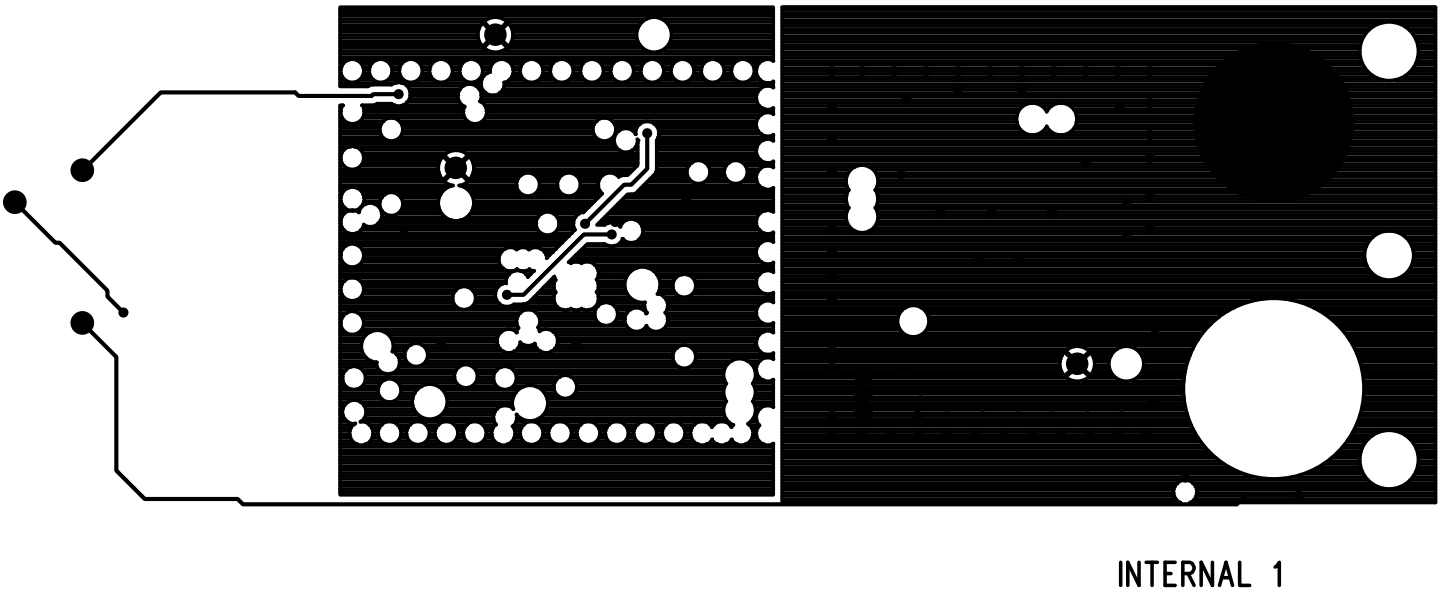


Figure 16.3. Internal 1 (Layer 2)

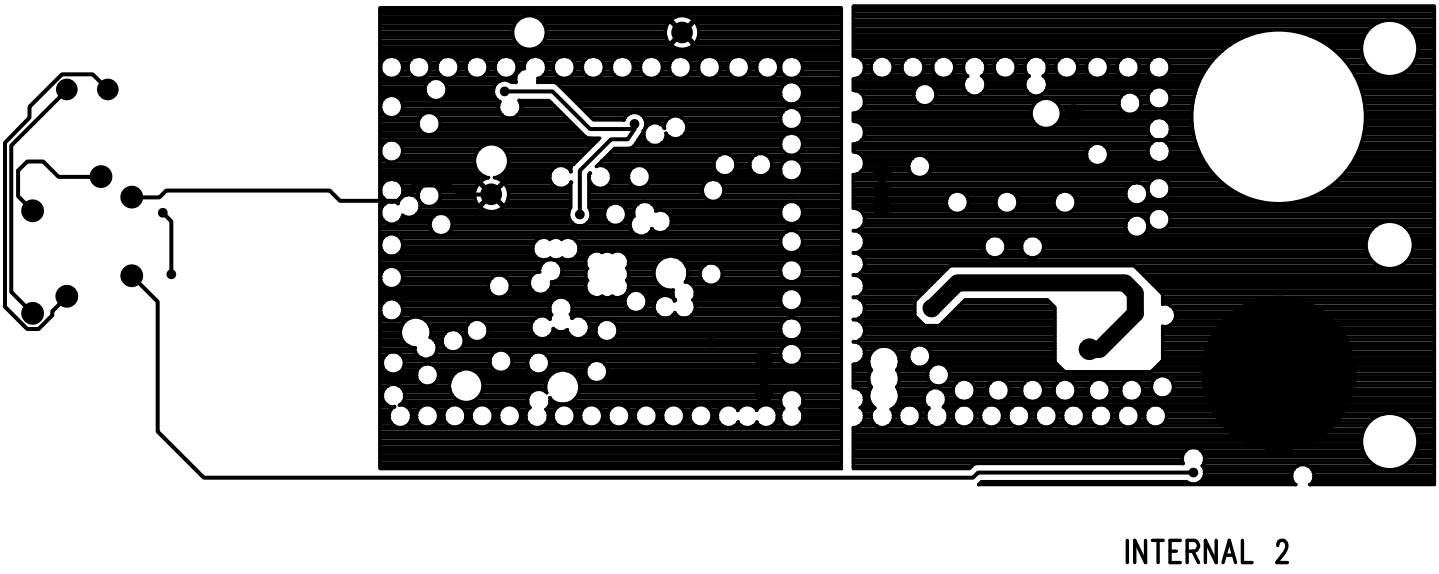


Figure 16.4. Internal 2 (Layer 3)

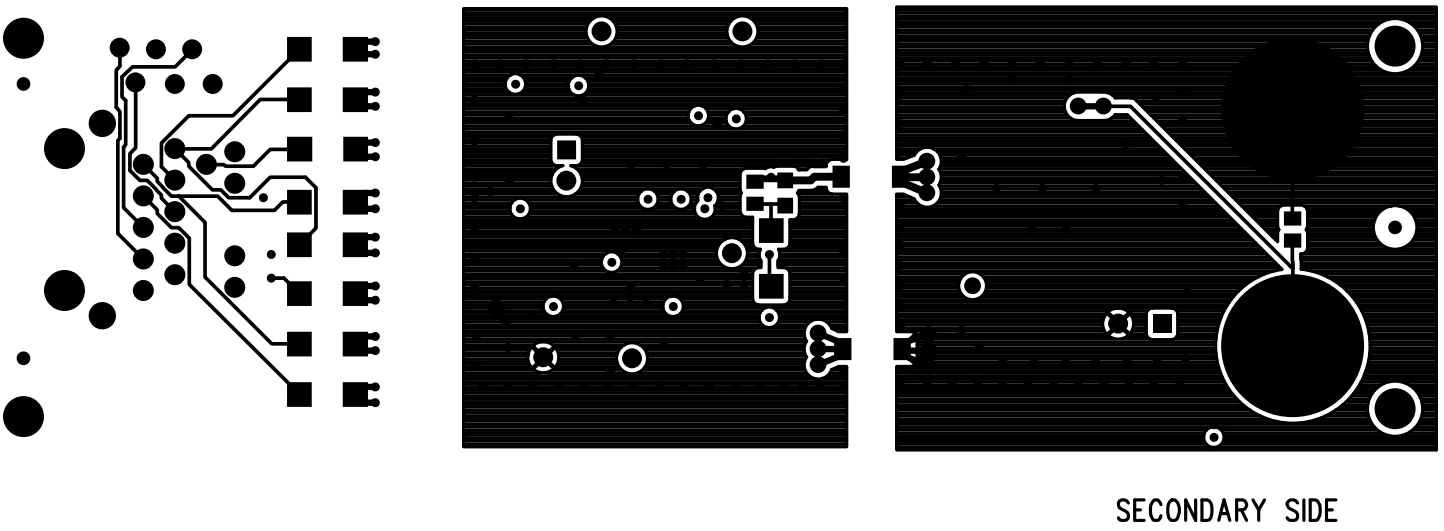


Figure 16.5. Bottom Layer

17. Bill of Materials

The table below is the BOM listing for the standard 5 V output evaluation board with option PoE Class 3.

Table 17.1. Si3404ISOC3 Evaluation Board Bill of Materials

Qty	Value	Ref	Rat-ing	Volt-age	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
2	C1, C3	1 µF		100 V	±10%	X7R	C1210	C1210X7R101-105K	Venkel
1	C11	1 µF		25 V	±20%	X5R	C0805	CC0805MKX5R8BB105	Yageo
1	C2	12 µF		100 V	±20%	Alum_Elec	C2.5X6.3MM-RAD	EEUFC2A120	Panasonic
1	C22	0.1 µF		16 V	±10%	X7R	C0805	C0805X7R160-104K	Venkel
1	C23	2.2 nF		50 V	±10%	C0G	C0805	C0805C0G500-222K	Venkel
1	C24	0.01 µF		16 V	±10%	X7R	C0805	C0805C103K4RAC-TU	KEMET
2	C25, C26	1 nF		3000 V	±10%	X7R	C1808	C1808X7R302-102K	Venkel
1	C4	0.01 µF		100 V	±10%	X7R	C0805	C0805X7R101-103K	Venkel
1	C5	1 nF		50 V	±1%	C0G	C0805	C0805C0G500-102F	Venkel
1	C6	100 µF		6.3 V	±10%	X5R	C1210	C1210X5R6R3-107K	Venkel
1	C7	1000 µF		6.3 V	±20%	Alum_Elec	C3.5X8MM-RAD	ECA0JM102	Panasonic
1	C8	0.1 µF		100 V	±10%	X7R	C0805	C0805X7R101-104K	Venkel
1	C9	22 nF		25 V	±5%	C0G	C0805	C0805C0G250-223J	Venkel
8	D12, D13, D14, D15, D16, D17, D18, D19	S1B	1.0A	100 V		Single	DO-214AC	S1B	Fairchild
1	D2	1N4148W	300mA	100 V		Single	SOD-123	1N4148W-7-F	Diodes Inc.
1	D4	RS1B	1.0A	100 V		Stand-ard	DO-214AC	RS1B	Fairchild
1	D5	PDS1040	10A	40 V		Schottky	POWERDI-5	PDS1040-13	Diodes Inc.
1	J1	RJ-45				Recep-tacle	RJ45-SI-52004	SI-52003-F	Bel
2	J11, J12	BND_POST	15A			BANA-NA	BANANA-JACK	101	ABBATRON HH SMITH
2	L1, L2	742792040	2000 mA	700 Ω @150MHz		SMT	L0805	742792040	Wurth
1	L3	1 µH	2.9A		±20%	Shielded	IND-6.6X4.45MM	DO1608C-102ML_	Coilcraft
2	R1, R2	330 Ω	1/10W		±1%	Thick-Film	R0805	CR0805-10W-3300F	Venkel
1	R10	48.7 Ω	1/8W		±1%	Thick-Film	R0805	CRCW080548R7FKTA	vishay

Qty	Value	Ref	Rat-ing	Volt-age	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
1	R11	24.3 kΩ	1/8W		±1%	Thick-Film	R0805	CRCW080524K3FKEA	vishay
1	R12	4.99 kΩ	1/10W		±1%	Thick-Film	R0805	CR0805-10W-4991F	Venkel
1	R13	0.62 Ω	1/8W		±1%	Thick-Film	R0805	RL0805FR-070R62L	Yageo
1	R14	36.5 kΩ	1/10W		±1%	Thick-Film	R0805	CR0805-10W-3652F	Venkel
1	R15	12.1 kΩ	1/10W		±1%	Thick-Film	R0805	CR0805-10W-1212F	Venkel
2	R17, R18	0 Ω	2A			Thick-Film	R0805	CR0805-10W-000	Venkel
1	R24	2.05 kΩ	1/16W		±1%	Thick-Film	R0603	CR0603-16W-2051F	Venkel
1	R3	10 Ω	1/10W		±1%	Thick-Film	R0805	CR0805-10W-10R0F	Venkel
1	R4	18 kΩ	1/10W		±5%	Thick-Film	R0805	CR0805-10W-183J	Venkel
1	R5	6.8 Ω	1/8W		±1%	Thick-Film	R0805	RC0805FR-076R8L	Yageo
1	R8	88.7 kΩ	1/8W		±1%	Thick-Film	R0805	CRCW080588K7FKEA	Vishay
4	SO1, SO2, SO3, SO4	Standoff				HDW		2397	SPC Technol-ogy
1	T1	TOEP13-0155S1	15W	100V			XFMR-EP13-SMT	TOEP13-0155S1	MenTech
1	U1	Si3404		120V		PD	QFN20N4X4P0.5	Si3404-A-GM	SiLabs
1	U2	VO618A-3X017T					SO4N10.16P2.54-AKEC	VO618A-3X017T	Vishay
1	U5	TLV431				SHUNT	TLV431-DBZ	TLV431BCDBZR	TI
Not-Installed Components									
9	C12, C13, C14, C15, C16, C17, C18, C19, C33	1 nF		100 V	±10%	X7R	C0603	C0603X7R101-102K	Venkel
11	TP1, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12	BLACK				LOOP	TESTPOINT	5001	Keystone

18. Appendix—Si3404-ISO-FB Design and Layout Checklist

Although the EVB design is pre-configured as a Class 3 PD with 5 V output, the schematics and layouts can easily be adapted to meet a wide variety of common output voltages and power levels.

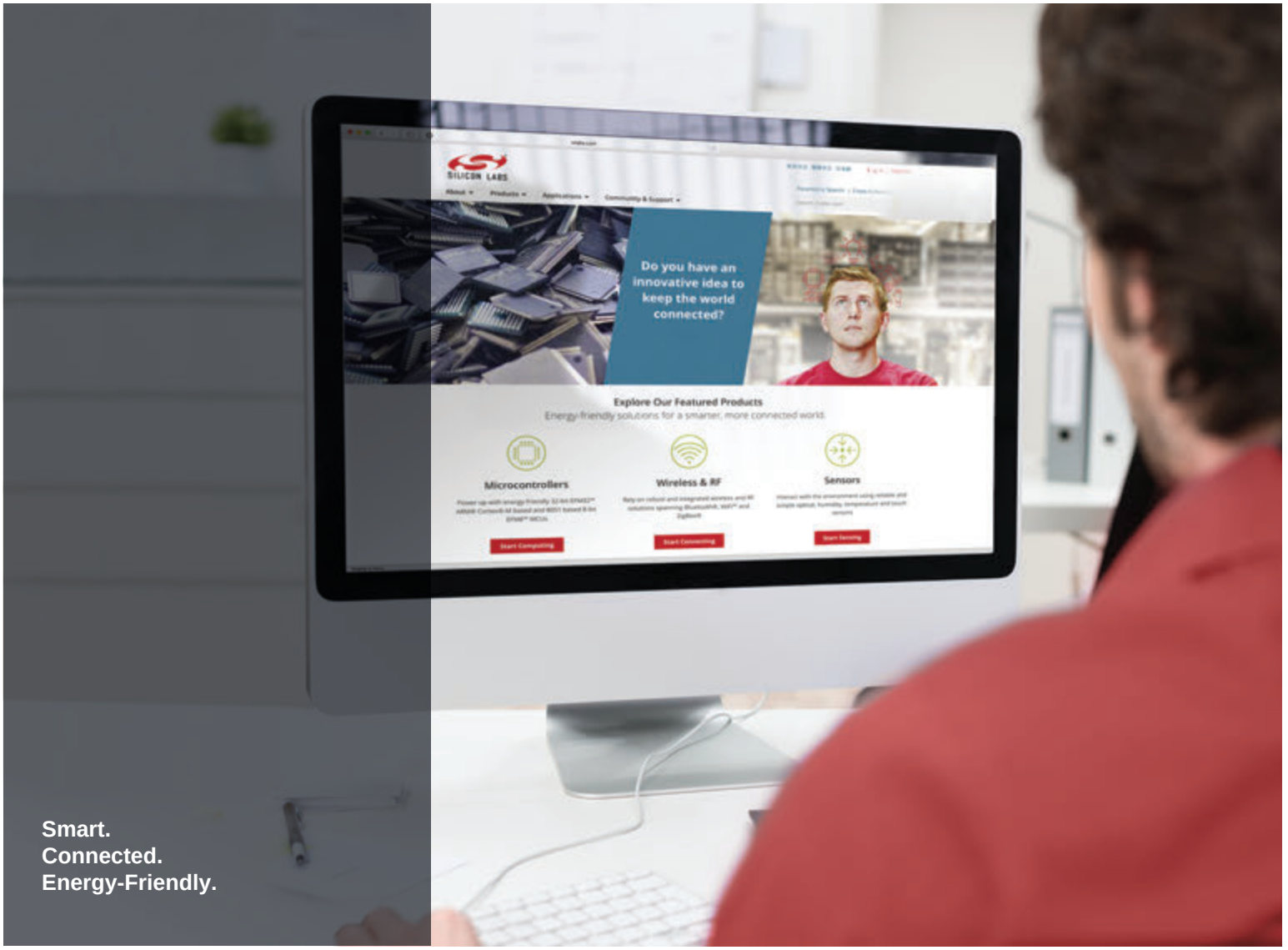
The complete EVB design databases for the standard 5 V/Class 3 configuration are located at www.silabs.com/PoE link. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

Below is a recommended design checklist that can assist in trouble-free development of robust PD designs.

Refer also to the Si3404-ISO-FB data sheet and AN1130 when using the following checklist.

1. Design Planning Checklist:
   a. Determine if your design requires an isolated or non-isolated topology. For more information, see AN1130.
   b. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si3404-ISO-FB into your system design process.
   c. Determine your load's power requirements (i.e., VOUT and IOUT consumed by the PD, including the typical expected transient surge conditions). In general, to achieve the highest overall efficiency performance of the Si3404-Isolated Flyback, choose the highest output voltage option used in your PD and then post regulate to the lower supply rails, if necessary.
   d. Based on your required PD power level, select the appropriate class resistor RCLASS value by referring to AN1130.
2. General Design Checklist:
   a. ESD caps (C12–C19 in Figure 2.3 Si3404 Isolated Flyback EVB Schematic: 5 V, Class 3 PD on page 4) are strongly recommended for designs where system-level ESD (IEC6100-4-2) must provide >15 kV tolerance.
   b. If your design uses an AUX supply, be sure to include a 3 Ω surge limiting resistor in series with the AUX supply for hot insertion. Refer to AN1130 when AUX supply is 48 V.
   c. Non-standard PoE injectors turns on the PD without detection and classification phases. In most cases, dV/dt is not controlled and could violate IEEE requirements. To ensure robustness with those injectors, please include a 2 x 3 ohm resistors in series with L1 and L2.
   d. Silicon Labs recommends the inclusion of a minimum load (250 mW) to avoid the PSE port being disconnected by the PSE. If your load is not at least 250 mW, add a resistor load to dissipate at least 250 mW.
3. Layout Guidelines:
   a. Make sure VNEG pin of the Si3404 is connected to the backside of the QFN package with an adequate thermal plane, as noted in the data sheet and AN1130.
   b. Keep the trace length from SWO to VSS as short as possible. Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere.
   c. Usually, one standard via handles 200 mA of current. If the trace needs to conduct a significant amount of current from one plane to the other, use multiple vias.
   d. Keep the circular area of the loop from the Switcher FET output to the inductor or transformer and returning from the input filter capacitors (C1–C3) to VSS as small a diameter as possible. Also, minimize the circular area of the loop from the output of the inductor or transformer to the Schottky diode and returning through the first stage output filter capacitor back to the inductor or transformer as small as possible. If possible, keep the direction of current flow in these two loops the same.
   e. Keep the high power traces as short as possible.
   f. Keep the feedback and loop stability components as far from the transformer/inductor and noisy power traces as possible.
   g. If the outputs have a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together, and then connect to the plane at a single point.

To help ensure first-pass success, contact our customer support by submitting a help ticket and uploading your schematics and layout files for review.



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