

Final Product Change Notification

Issue Date: 09-Feb-2019 Effective Date: 10-May-2019

Dear Emma Tempest,

Here's your personalized quality information concerning products Premier Farnell PLC purchased from NXP.

For detailed information we invite you to <u>view this</u> notification online

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QUALITY

201901014F01

Management Summary

Microcontroller products LPC5410xUK49 version "C" includes a die revision to fix errata issues and an upgraded bump process.

Change Category

[X] Assembly	[X] Product Marking	[] Test Location	[X] Design
Process			
[X]	[X] Mechanical	[]Test	[] Errata
Assembly	Specification	Process	
Materials	•		
[] Assembl	v[]	[]Test	[] Electrical
Location	Packing/Shipping/Labeli	ng Equipment	
			coverage
[] Other			
	Assembly Process [X] Assembly Materials [] Assembl Location	Assembly Process [X] [X] Mechanical Assembly Specification Materials [] Assembly[] Location Packing/Shipping/Labeli	Assembly Location Process [X] [X] Mechanical []Test Assembly Specification Process Materials [] Assembly[] [] Test Location Packing/Shipping/Labeling Equipment

LPC5410xUK49 in WLCSP49 Package Change from Rev "B" to Rev "C"

Description of Change

Microcontroller products LPC5410xUK49 in WLCSP49 package will change from version "B" to version "C". Changes included a die revision to fix errata issues and an upgraded bump process.

The following functional changes were made to product version "C":

- IRC frequency tolerance improvement over temperature to resolve errata IRC.1 as defined in the device errata sheet.
- System clock frequency improved to resolved errata Frequency.1 as defined in the device errata sheet.

The following bump process changes were made to product version "C":

- Under Bump Metal (UBM) and Re-Distribution Layer (RDL) change from a sputter to a plated process.
- Back side protection (BSP) material changes from 40um to 25um thickness.
- Overall maximum package thickness changes from 0.58mm to 0.565mm (see package drawing in attached datasheet).

A revised data sheet, LPC5410x v2.10 is available at https://www.nxp.com/docs/en/data-sheet/LPC5410X.pdf.

Reason for Change

- 1) To fix errata IRC.1 and Frequency.1.
- 2) The sputter UBM process is outdated and has been obsoleted by the assembly vendor. The assembly process is being ugraded to the current process already qualified by the LPC5411xUK49.

Identification of Affected Products

Top side marking

The change applies to product version "C" visible on the top side marking.

Product Availability

Sample Information

Samples are available upon request

Production

Planned first shipment 10-May-2019

Anticipated Impact on Form, Fit, Function, Reliability or Quality

Product overall height is reduced by 15um due to change in back side protection thickness.

Product functionality changes to fix errata issues IRC.1 and Frequency.1.

Data Sheet Revision

A new datasheet will be issued

Disposition of Old Products

Existing inventory will be shipped until depleted

Additional information

Affected products and sales history information: see attached file

Self qualification: <u>view online</u> Additional documents: <u>view online</u>

Timing and Logistics

In compliance with JEDEC J-STD-046, your acknowledgement of this change is expected by 11-Mar-2019.

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please <u>contact NXP "Global Quality Support Team"</u>.

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

For specific questions on this notice or the products affected please contact our specialist directly:

Name Tim Camenzind

Position Senior Quality Engineer e-mail address tim.camenzind@nxp.com

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Customer Focus, Passion to Win.

NXP Quality Management Team.

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