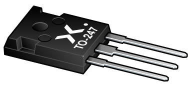


GAN063-650WSA

650 V, 50 mΩ Gallium Nitride (GaN) FET

3 April 2019 — Product data sheet

1. General description

The GAN063-650WSA is a 650 V, 50 mΩ Gallium Nitride (GaN) FET. It is a normally-off device that combines Nexperia's state-of-the-art high-voltage GaN HEMT and low-voltage silicon MOSFET technologies — offering superior reliability and performance. AEC-Q101 qualified.

2. Features and benefits

- Ultra-low reverse recovery charge
- Simple gate drive (0 V to +10 V or 12 V)
- Robust gate oxide (±20 V capability)
- High gate threshold voltage (+4 V) for very good gate bounce immunity
- Very low source-drain voltage in reverse conduction mode
- Transient over-voltage capability (800 V)
- AEC-Q101 qualified

3. Applications

- Hard and soft switching converters for industrial and datacom power
- Bridgeless totempole PFC
- PV and UPS inverters
- Servo motor drives

4. Quick reference data

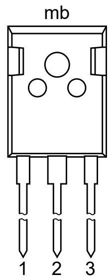
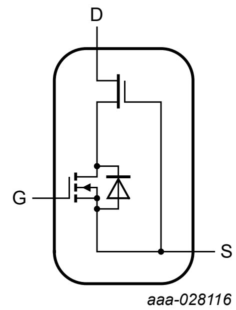
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 175 °C		-	-	650	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	34.5	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	143	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	50	60	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 400 V; V_{GS} = 10 V; T_j = 25 °C		-	4	-	nC
$Q_{G(tot)}$	total gate charge			-	15	-	nC
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V; Fig. 14		-	125	-	nC

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 **TO-247 (SOT429)**	
2	S	source		
3	D	drain		
mb	S	mounting base; connected to source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GAN063-650WSA	TO-247	plastic, single-ended through-hole package; 3 leads; 5.45 mm pitch; 20.45 mm x 15.6 mm x 4.95 mm body	SOT429

7. Marking

Table 4. Marking codes

Type number	Marking code
GAN063-650WSA	GAN063-650WSA

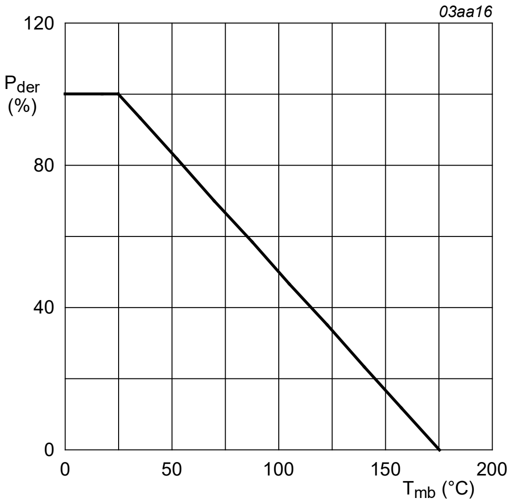
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

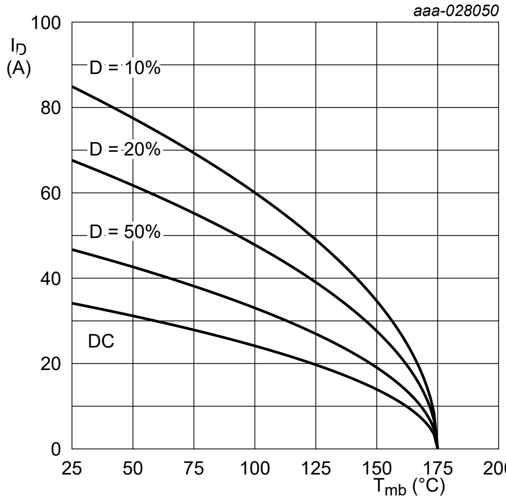
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 175 °C		-	650	V
V_{TDS}	transient drain to source voltage	pulsed; t_p = 1 μs; δ_{factor} = 0.01		-	800	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	143	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	34.5	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	24.4	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C; Fig. 3		-	150	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C; V_{GS} = 0 V		-	34.5	A

Symbol	Parameter	Conditions		Min	Max	Unit
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	150	A



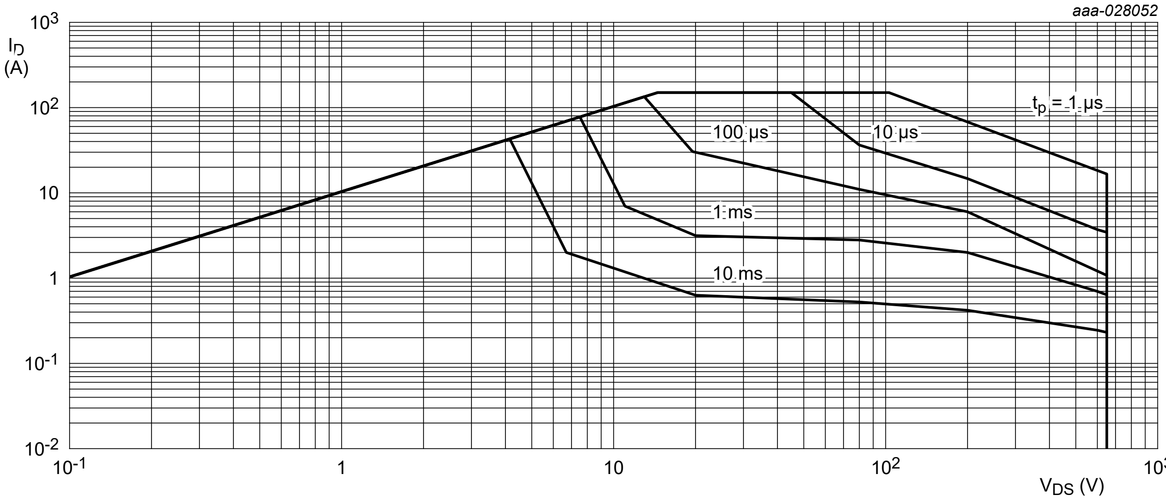
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq$ 10 V; Pulse witdh ≤ 10 µs

Fig. 2. Drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	-	1.05	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air		-	-	40	K/W

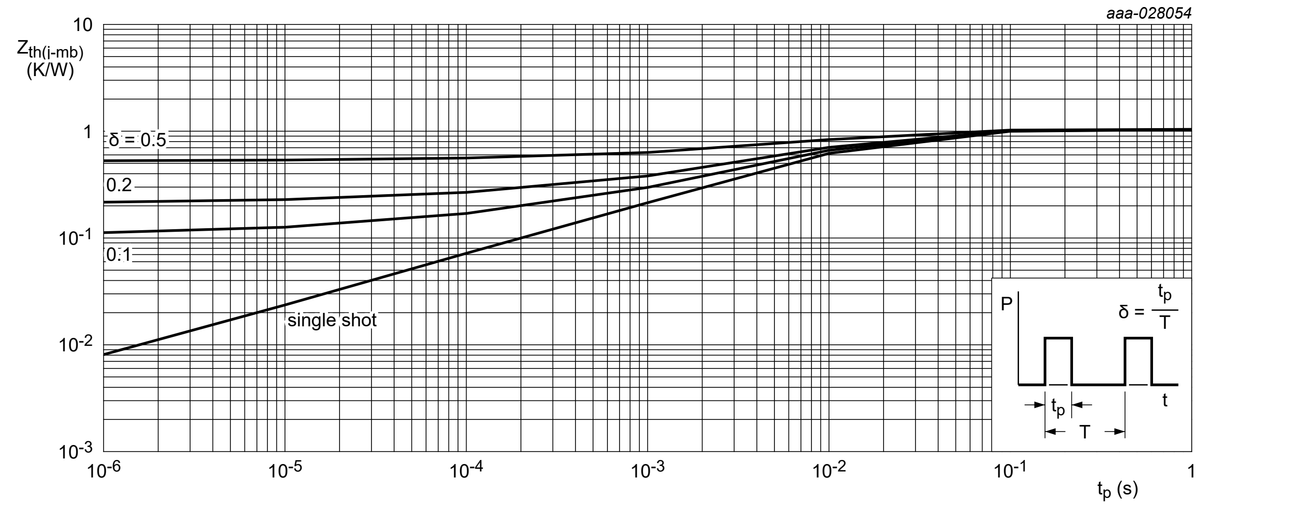


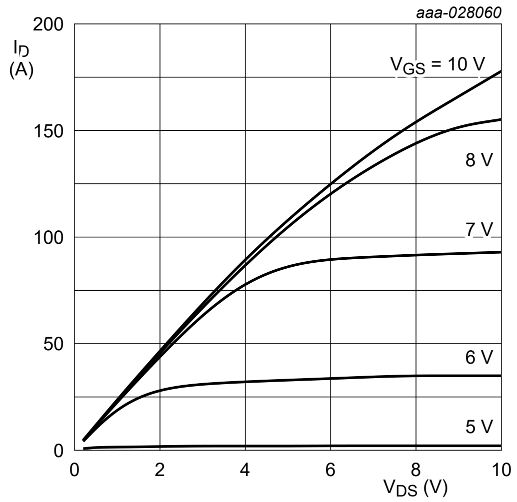
Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

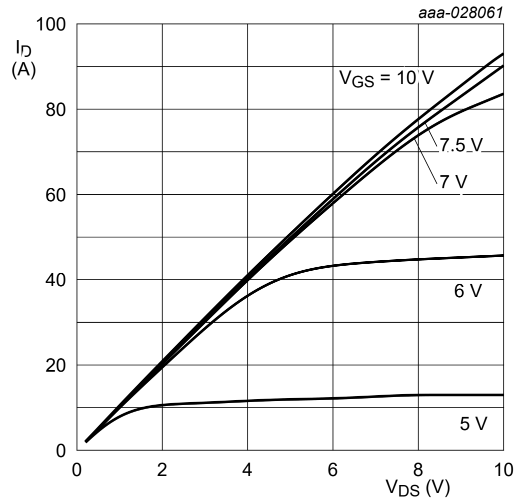
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		3.4	3.9	4.5	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 9		2.2	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 9		-	-	5.2	V
I_{DSS}	drain leakage current	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C		-	2	25	µA
		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 175 °C		-	25	-	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	50	60	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 10		-	120	-	mΩ
R_G	gate resistance	f = 1 MHz		-	2.3	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 400 V; V_{GS} = 10 V; T_j = 25 °C		-	15	-	nC
Q_{GS}	gate-source charge			-	6	-	nC
Q_{GD}	gate-drain charge			-	4	-	nC
C_{iss}	input capacitance	V_{DS} = 400 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 11		-	1000	-	pF
C_{oss}	output capacitance			-	130	-	pF
C_{rss}	reverse transfer capacitance			-	8	-	pF
$C_{o(er)}$	effective output capacitance, energy related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C; Fig. 12		-	190	-	pF
$C_{o(tr)}$	effective output capacitance, time related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C		-	310	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 400 V; R_L = 16 Ω; V_{GS} = 12 V; $R_{G(ext)}$ = 40 Ω		-	57	-	ns
t_r	rise time			-	10	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(off)}$	turn-off delay time			-	88	-	ns
t_f	fall time			-	11	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 400 V		-	125	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 13		-	1.9	-	V
		I_S = 12.5 A; V_{GS} = 0 V; T_j = 25 °C		-	1.35	-	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -1000 A/µs; V_{GS} = 0 V; V_{DS} = 400 V; Fig. 14		-	54	-	ns
Q_r	recovered charge			-	125	-	nC



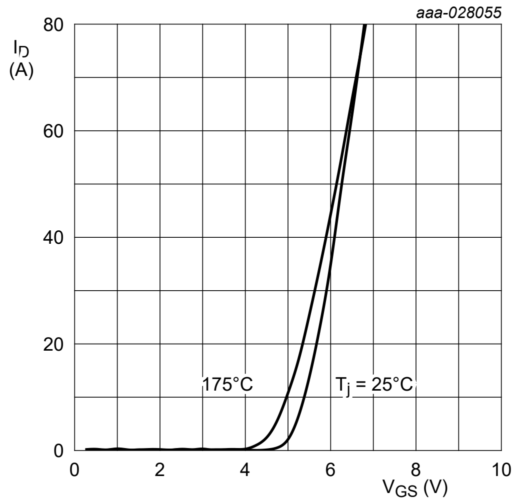
T_j = 25 °C

Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values



T_j = 175 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



V_{DS} = 10 V

Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

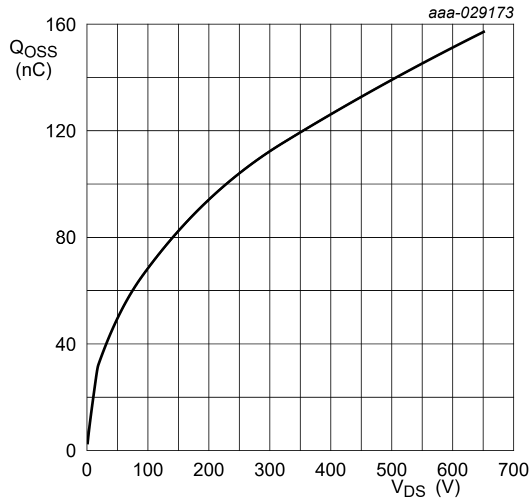
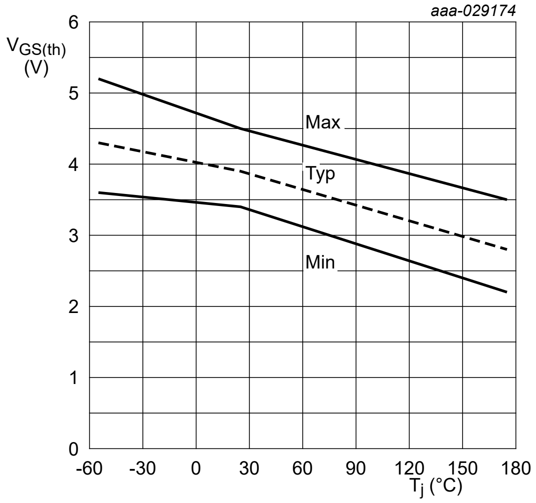
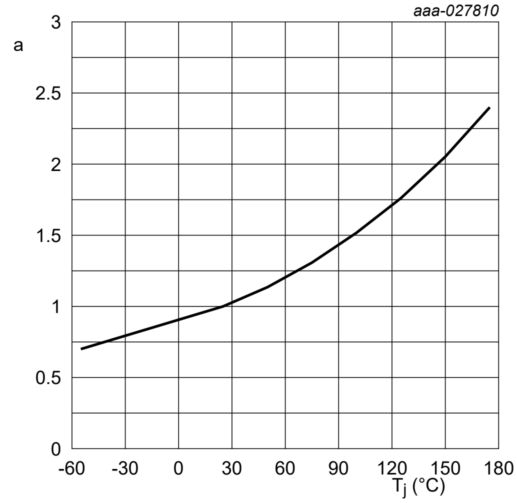


Fig. 8. Typical QOSS



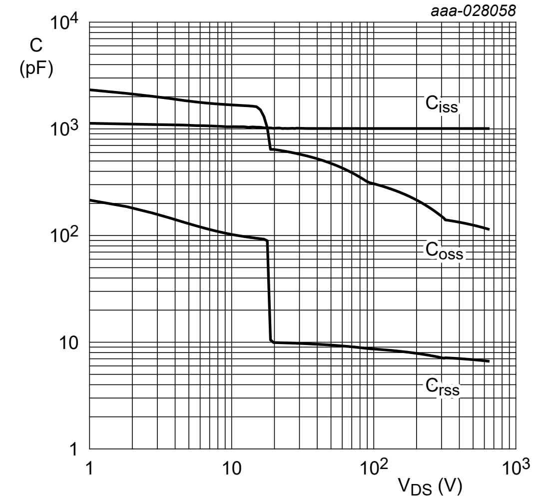
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 9. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon}\,(25°C)}$$

Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature



V_{GS} = 0 V; f = 1 MHz

Fig. 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

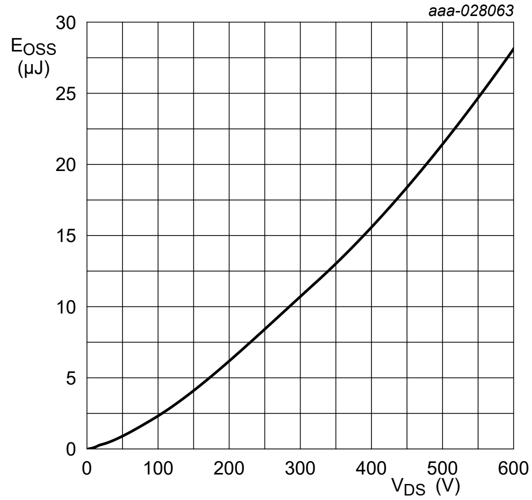
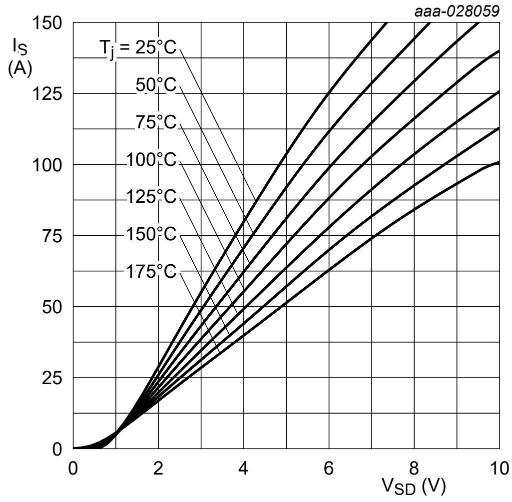


Fig. 12. Typical COSS Stored Energy



V_{GS} = 0 V

Fig. 13. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

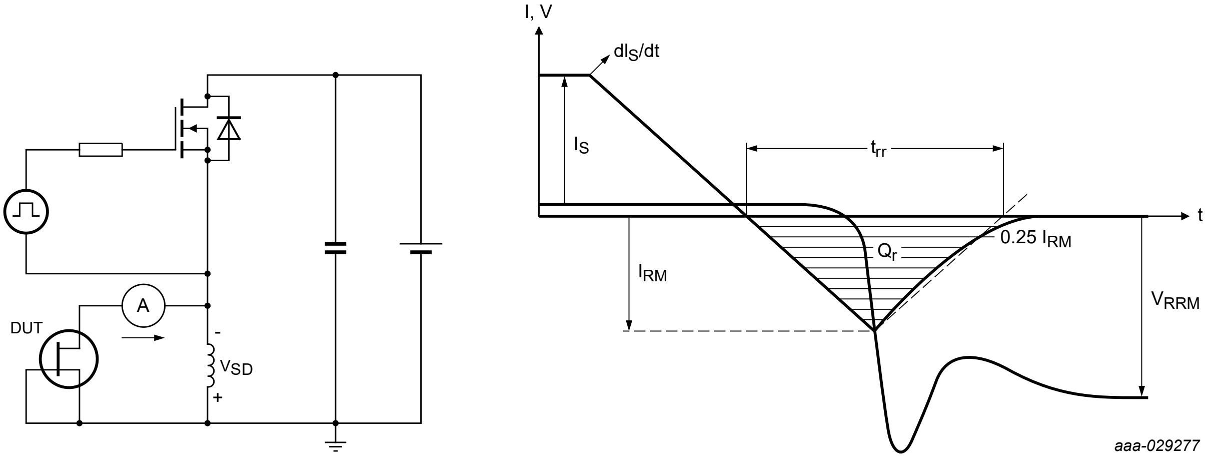


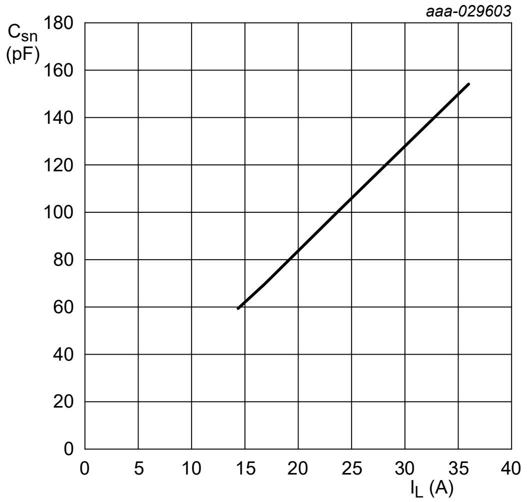
Fig. 14. Diode reverse recovery test circuit and waveform

11. Application information

To achieve maximum efficiency and stability when switching high currents, a switching node RC snubber (R_{sn}, C_{sn}) is recommended. For I_L < 14 A, a switching-node snubber is not required.

C_{SN} is taken from the graph.

R_{SN} should be selected to achieve a time constant of 1 ns; e.g. if C_{SN} = 100 pF, R_{SN} = 1 ns / 100 pF = 10 Ω.



R_G = 30 Ω; τ = R_{SN} × C_{SN} = 1 ns

Fig. 15. Snubber capacitance as function of load current

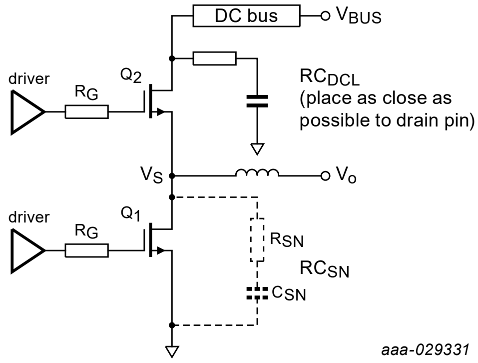
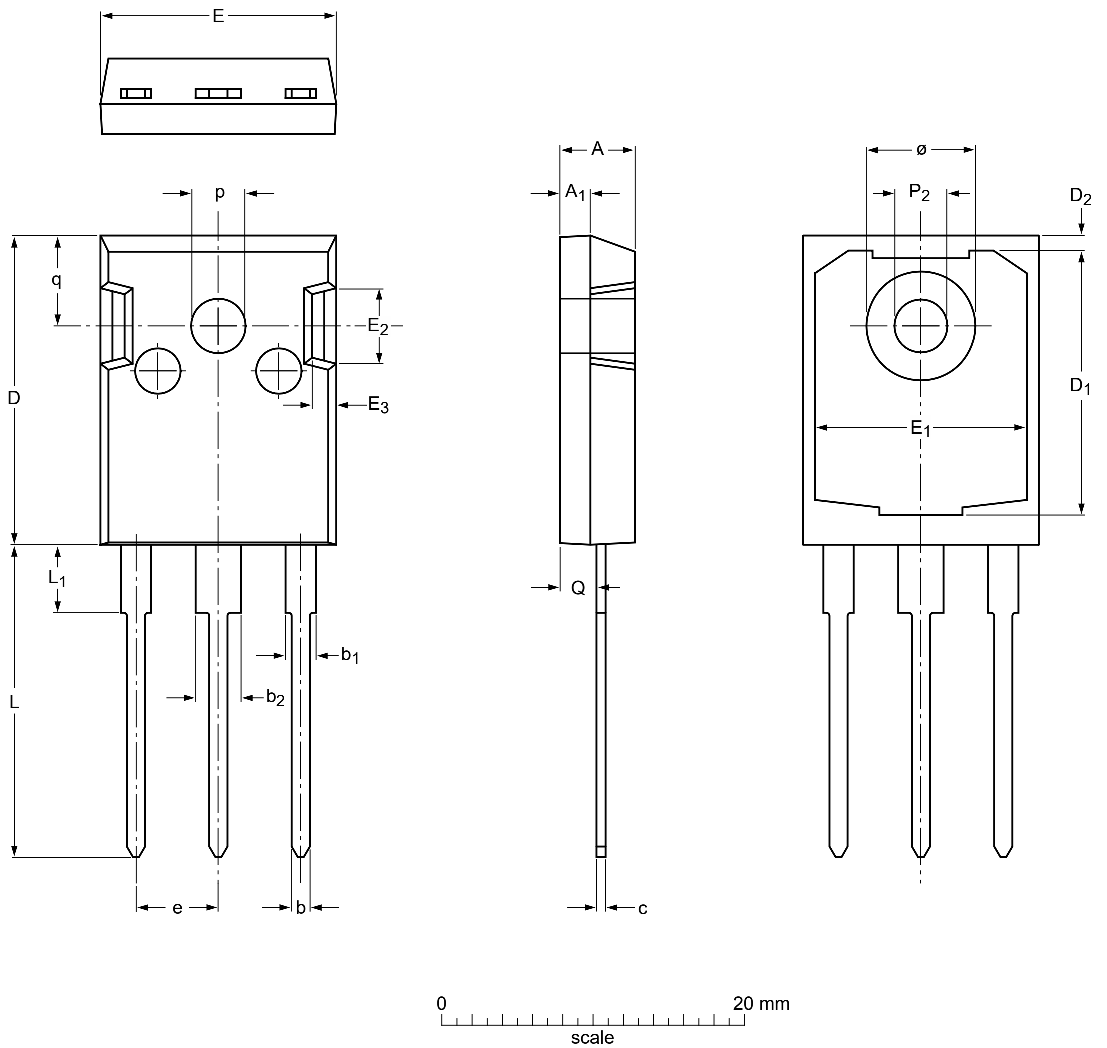


Fig. 16. DC-link snubber circuit

Note: A DC-link snubber is recommended in all cases. Optimal is 20 nF in series with 4 Ω, most easily achieved with parallel combination 10 nF and 8 Ω. This snubber lowers the Q factor of any resonance in the bus. That resonance will act as a load on the high gain amplifier that is the GaN FET and can lead to instability. For very high current, an RC snubber is recommended for the switching node. This will increase switching loss, so this is only recommended at high power levels where the losses are a very small percentage of the total power.

12. Package outline

Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3-lead TO-247 **SOT429**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	b	b_1	b_2	c	D	D_1	D_2	E	E_1	E_2	E_3	e(1)	L	L_1	P_2	p	Q	q	ø
mm	max	5.20	2.10	1.40	2.20	3.20	0.70	20.6	17.68	1.20	15.75	14.22	5.20	1.80		20.90	4.75	3.60	3.70	2.60	6.18	7.30
	nom														5.45							
	min	4.70	1.90	1.00	1.80	2.80	0.50	20.3	17.28	0.80	15.45	13.82	4.80	1.40		20.40	4.25	3.40	3.50	2.20	5.78	7.10

Note

1. Basic spacing between centers.

sot429_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT429		TO-247				~~04-09-14~~ 13-03-25

Fig. 17. Package outline TO-247 (SOT429)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

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