

CAB450M12XM3

1200V, 450A All-Silicon Carbide Conduction Optimized, Half-Bridge Module

V_{DS}	1200 V
I_{DS}	450 A

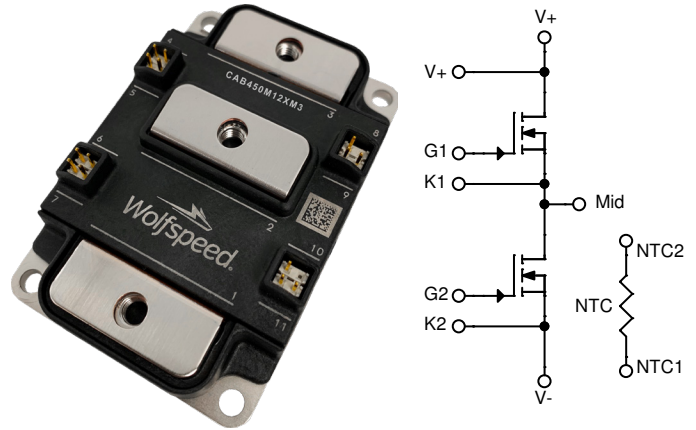
Technical Features

- High Power Density Footprint
- High Junction Temperature (175 °C) Operation
- Low Inductance (6.7 nH) Design
- Implements Conduction Optimized Third Generation SiC MOSFET Technology
- Silicon Nitride Insulator and Copper Baseplate

Applications

- Motor & Traction Drives
- Vehicle Fast Chargers
- Uninterruptable Power Supplies
- Smart-Grid / Grid-Tied Distributed Generation

Package 80 x 53 x 19 mm



System Benefits

- Terminal layout allows for direct bus bar connection without bends or bushings enabling a simple, low inductance design.
- Isolated integrated temperature sensing enables high-level temperature protection.
- Dedicated drain Kelvin pin enables direct voltage sensing for gate driver overcurrent protection.

Key Parameters ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{DS\ max}$	Drain-Source Voltage			1200	V		
$V_{GS\ max}$	Gate-Source Voltage, Maximum Value	-4		+19		AC frequency $\geq 1\text{Hz}$.	Note 1
$V_{GS\ op}$	Gate-Source Voltage, Recommended Op. Value	-4		+15		Static	
I_{DS}	DC Continuous Drain Current			450	A	$V_{GS} = 15\text{V}$, $T_c = 25^\circ\text{C}$, $T_{vj} \leq 175^\circ\text{C}$	Fig. 20
			409			$V_{GS} = 15\text{V}$, $T_c = 90^\circ\text{C}$, $T_{vj} \leq 175^\circ\text{C}$	Note 2
I_{SD}	DC Source-Drain Current			450		$V_{GS} = 15\text{V}$, $T_c = 25^\circ\text{C}$, $T_{vj} \leq 175^\circ\text{C}$	
$I_{SD\ BD}$	DC Source-Drain Current (Body Diode)		225			$V_{GS} = -4\text{V}$, $T_c = 25^\circ\text{C}$, $T_{vj} \leq 175^\circ\text{C}$	
$I_{DS\ (pulsed)}$	Maximum Pulsed Drain-Source Current			900		t_{Pmax} limited by T_{jmax} $V_{GS} = 15\text{V}$, $T_c = 25^\circ\text{C}$	
$I_{SD\ (pulsed)}$	Maximum Pulsed Source-Drain Current			900			
$T_{Vj\ op}$	Maximum Virtual Junction Temperature under Switching Conditions	-40		175	$^\circ\text{C}$		

Note 1 If MOSFET body diode is not used, $V_{GS\ max} = -8/+19\text{V}$

Note 2 Assumes $R_{THJC} = 0.11^\circ\text{C/W}$ and $R_{DS(on)} = 4.6\text{m}\Omega$. Calculate $P_D = (T_{vj} - T_c) / R_{THJC}$. Calculate $I_{D_MAX} = \sqrt{(P_D / R_{DS(on)})}$

MOSFET Characteristics (Per Position) ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, I_D = 200\ \mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.6		$V_{DS} = V_{GS}, I_D = 132\ \text{mA}$	
			2.0			$V_{DS} = V_{GS}, I_D = 132\ \text{mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		5	200	μA	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$	
I_{GSS}	Gate-Source Leakage Current		0.05	1.3		$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance (Devices Only)		2.6	3.7	m Ω	$V_{GS} = 15\text{ V}, I_D = 450\text{ A}$	Fig. 2
			4.6			$V_{GS} = 15\text{ V}, I_D = 450\text{ A}, T_J = 175^\circ\text{C}$	Fig. 3
g_{fs}	Transconductance		355		S	$V_{DS} = 20\text{ V}, I_{DS} = 450\text{ A}$	Fig. 4
			360			$V_{DS} = 20\text{ V}, I_{DS} = 450\text{ A}, T_J = 175^\circ\text{C}$	
E_{On}	Turn-On Switching Energy, $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ $T_J = 175^\circ\text{C}$		11.0 11.7 13.0		mJ	$V_{DS} = 600\text{ V},$ $I_D = 450\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V},$ $R_{G(ext)} = 0.0\ \Omega,$ $L = 13.6\ \mu\text{H}$	Fig. 11 Fig. 13
E_{Off}	Turn-Off Switching Energy, $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ $T_J = 175^\circ\text{C}$		10.1 11.3 12.1				
$R_{G(int)}$	Internal Gate Resistance		2.5		Ω		
C_{iss}	Input Capacitance		38.0		nF	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V},$ $V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$	Fig. 9
C_{oss}	Output Capacitance		1.5				
C_{rss}	Reverse Transfer Capacitance		90				
Q_{GS}	Gate to Source Charge		355		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 450\text{ A}$ Per IEC60747-8-4 pg 21	
Q_{GD}	Gate to Drain Charge		500				
Q_G	Total Gate Charge		1330				
R_{thJC}	FET Thermal Resistance, Junction to Case		0.11	0.13	$^\circ\text{C}/\text{W}$		Fig. 17

Body Diode Characteristics (Per Position) ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Body Diode Forward Voltage		4.7		V	$V_{GS} = -4\text{ V}, I_{SD} = 450\text{ A}$	Fig. 7
			4.2			$V_{GS} = -4\text{ V}, I_{SD} = 450\text{ A}, T_J = 175^\circ\text{C}$	
t_{rr}	Reverse Recovery Time		52		ns	$V_{GS} = -4\text{ V}, I_{SD} = 450\text{ A}, V_R = 600\text{ V}$ $di/dt = 8\text{ A/ns}, T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge		6.6				
I_{rr}	Peak Reverse Recovery Current		195				
E_{rr}	Reverse Recovery Energy $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ $T_J = 175^\circ\text{C}$		0.2		mJ	$V_{DS} = 600\text{ V}, I_D = 450\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V}, R_{G(ext)} = 0.0\ \Omega,$ $L = 13.6\ \mu\text{H}$	Fig. 14
			1.1				
			1.9				

Temperature Sensor (NTC) Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R ₂₅	Rated Resistance		4.7		kΩ	T _{NTC} = 25 °C
ΔR/R	Tolerance of R ₂₅			±1	%	
P ₂₅	Maximum Power Dissipation			50	mW	

Steinhart-Hart Modified Coefficients for R/T Computation: $\frac{1}{T} = A + B \times \ln\left(\frac{R}{R_{25}}\right) + C \times \ln^2\left(\frac{R}{R_{25}}\right) + D \times \ln^3\left(\frac{R}{R_{25}}\right)$

	A	B	C	D
T _{NTC} < 25 °C	3.3540E-03	3.0013E-04	5.0852E-06	2.1877E-07
T _{NTC} ≥ 25 °C	3.3540E-03	3.0013E-04	5.0852E-06	2.1877E-07

Module Physical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R ₃₋₁	Package Resistance, M1		0.72		mΩ	T _c = 125 °C, Note 3
R ₁₋₂	Package Resistance, M2		0.63			T _c = 125 °C, Note 3
L _{Stray}	Stray Inductance		6.7		nH	Between Terminals 2 and 3
T _c	Case Temperature	-40		125	°C	
W	Weight		175		g	
M _s	Mounting Torque	2.0	3.0	4.0	N-m	Baseplate, M4 bolts
		2.0	4.0	5.0		Power Terminals, M5 bolts
V _{isol}	Case Isolation Voltage	4.0			kV	AC, 50 Hz, 1 min
CTI	Comparative Tracking Index	600				
	Clearance Distance	12.5			mm	From 2 to 3, Note 4
		11.5				From 1 to Baseplate, Note 4
		5.7				From 2 to 5, Note 4
		13.7				From 5 to Baseplate, Note 4
	Creepage Distance	14.7				From 2 to 3, Note 4
		14.0				From 1 to Baseplate, Note 4
		14.7				From 2 to 5, Note 4
		14.3				From 5 to Baseplate, Note 4

Note 3 Total Effective Resistance (Per Switch Position) = MOSFET R_{DS(on)} + Switch Position Package Resistance.

Note 4 Numbers reference the connections from the Schematic and Package Dimensions sections of this document.

Typical Performance

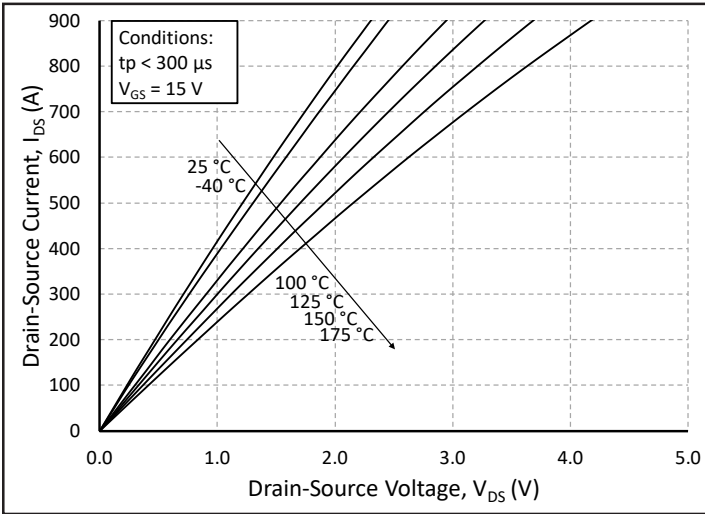


Figure 1. Output Characteristics for Various Junction Temperatures

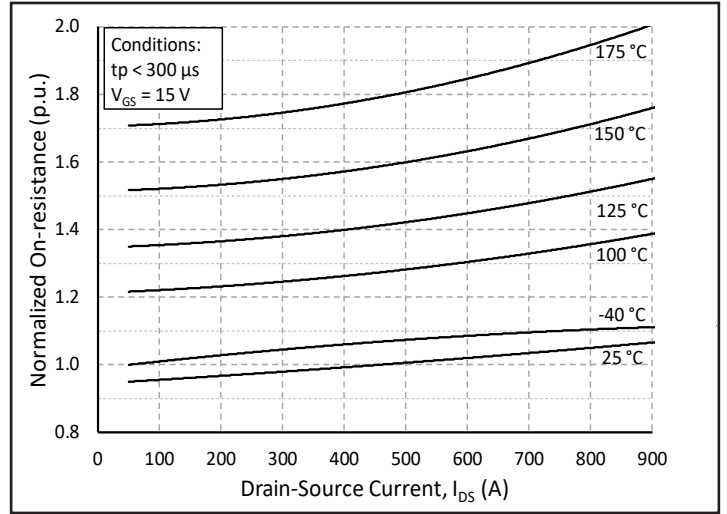


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

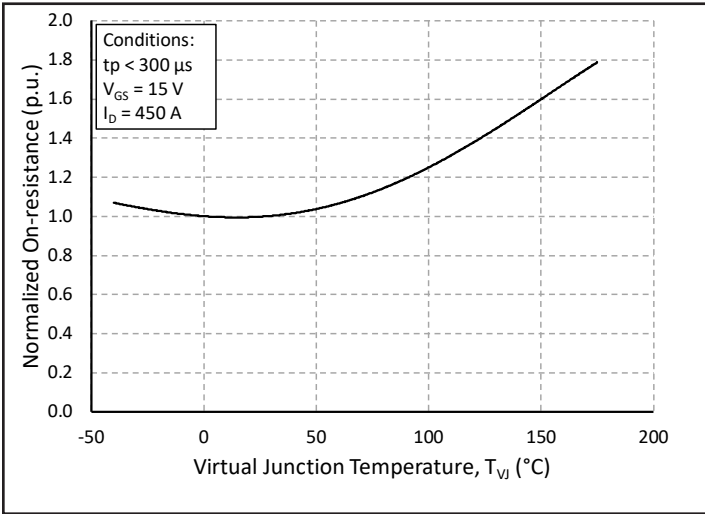


Figure 3. Normalized On-State Resistance vs. Junction Temperature

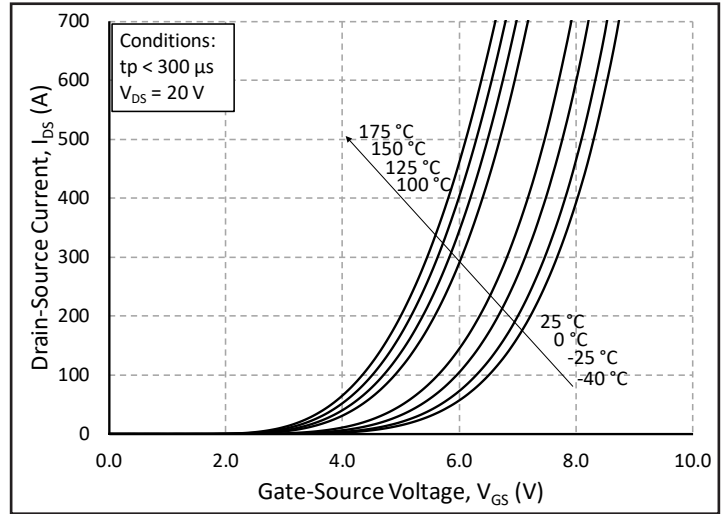


Figure 4. Transfer Characteristic for Various Junction Temperatures

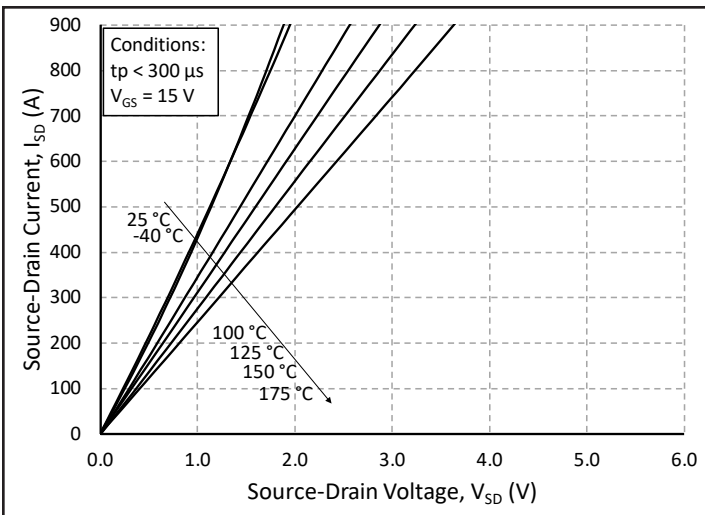


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 15$ V

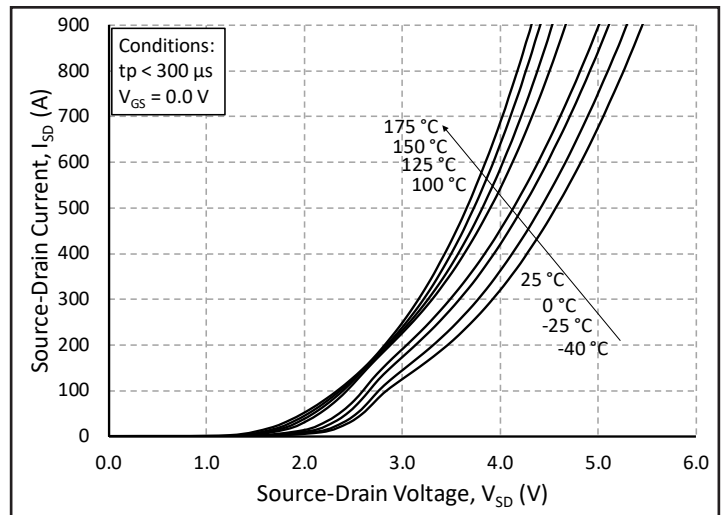


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0$ V (Body Diode)

Typical Performance

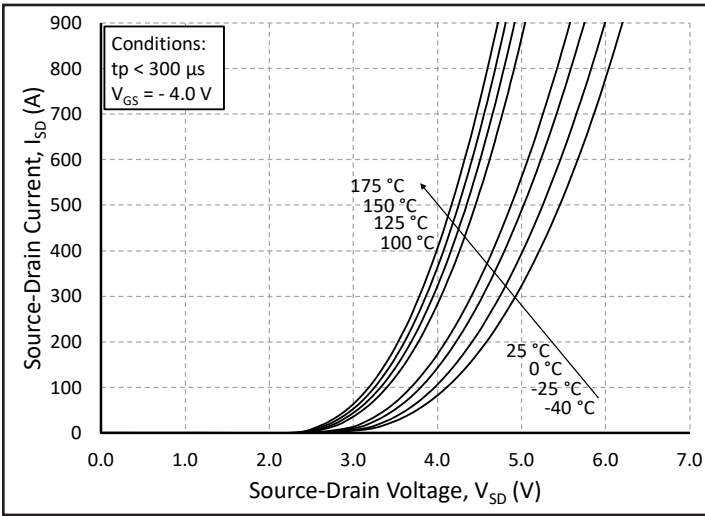


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -4\text{ V}$ (Body Diode)

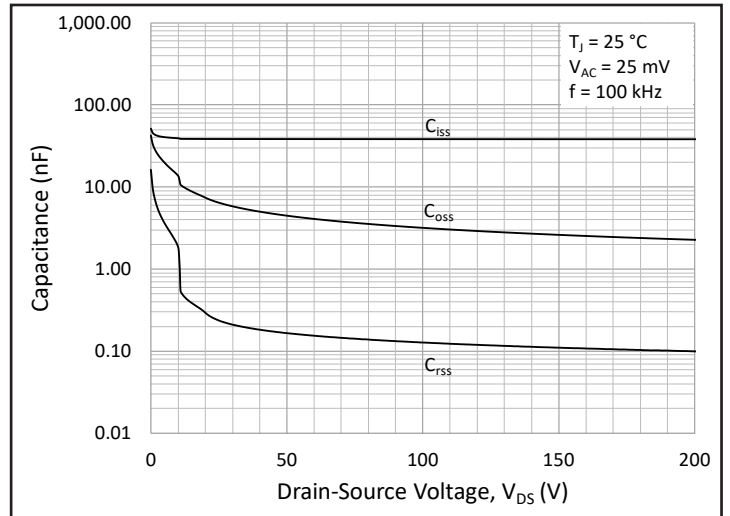


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

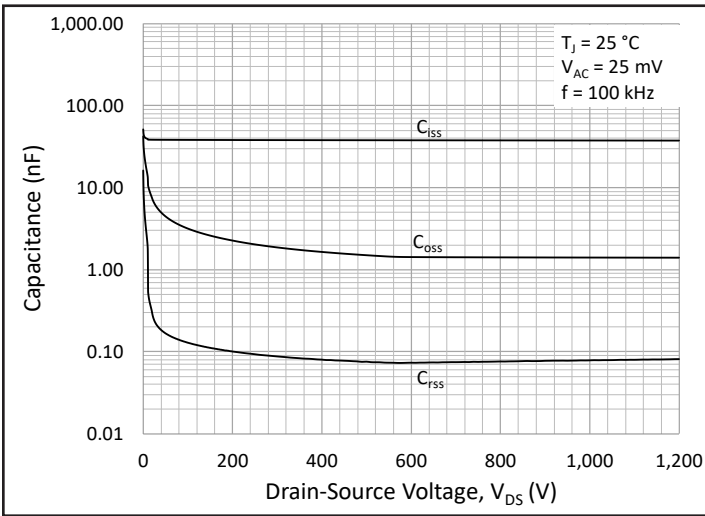


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

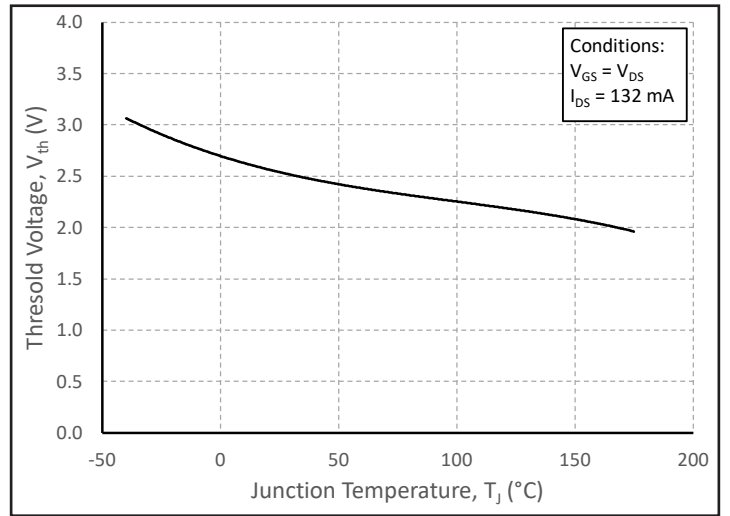


Figure 10. Threshold Voltage vs. Junction Temperature

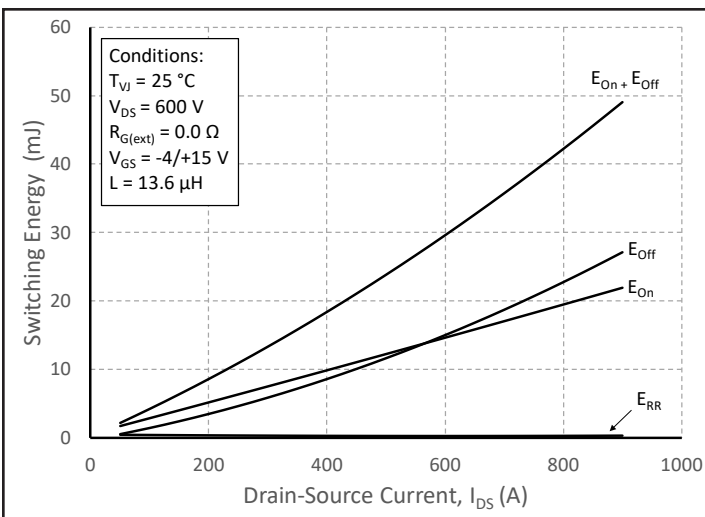


Figure 11. Switching Energy vs. Drain Current ($V_{DS} = 600\text{ V}$)

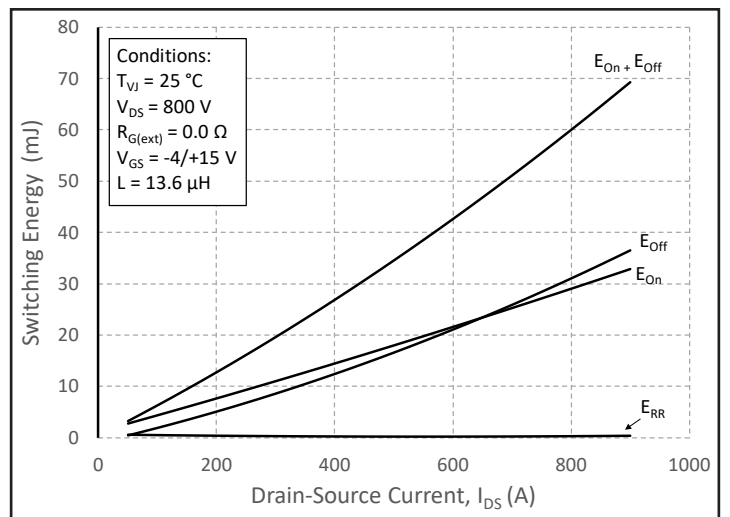


Figure 12. Switching Energy vs. Drain Current ($V_{DS} = 800\text{ V}$)

Typical Performance

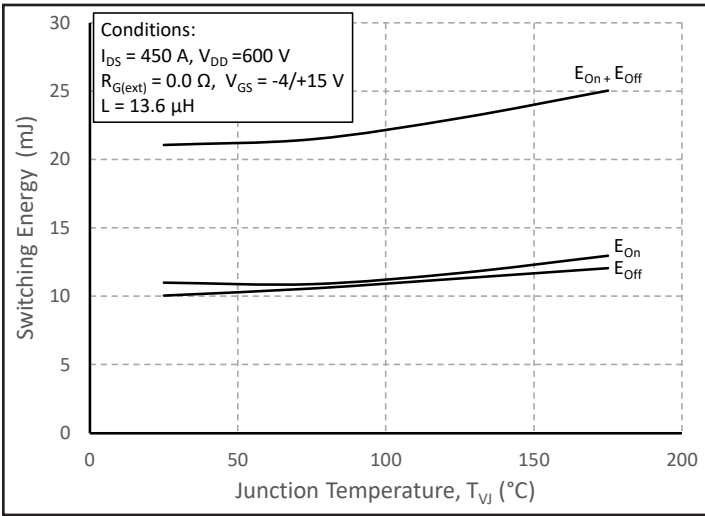


Figure 13. MOSFET Switching Energy vs. Junction Temperature

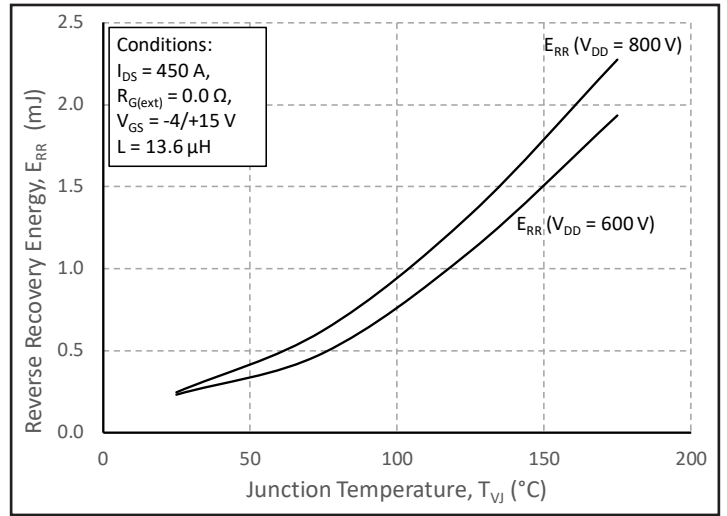


Figure 14. Reverse Recovery Energy vs. Junction Temperature

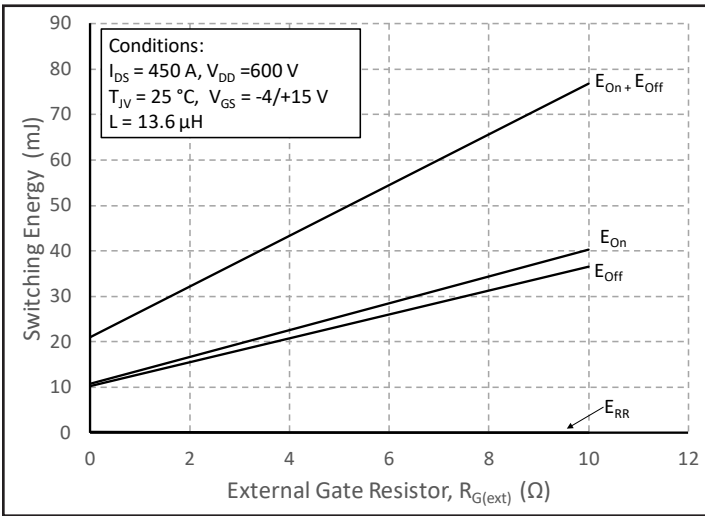


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

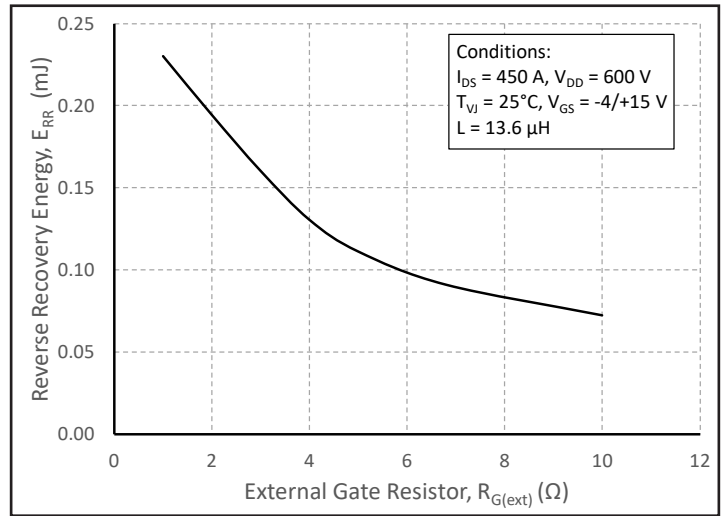


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

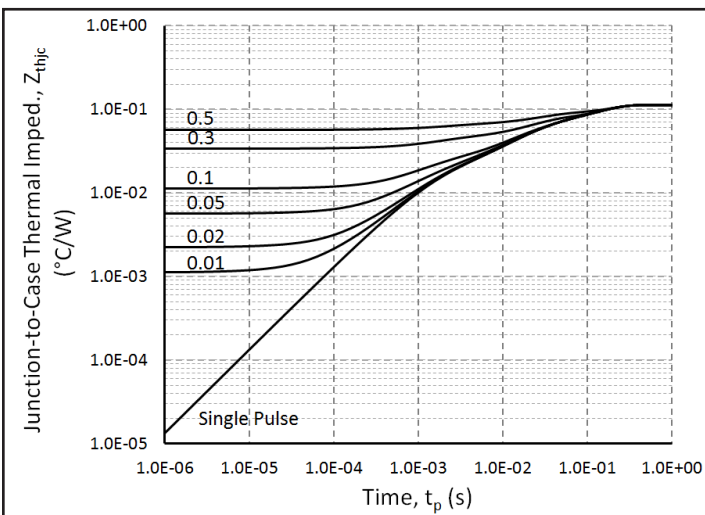


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, Z_{thJC} (°C/W)

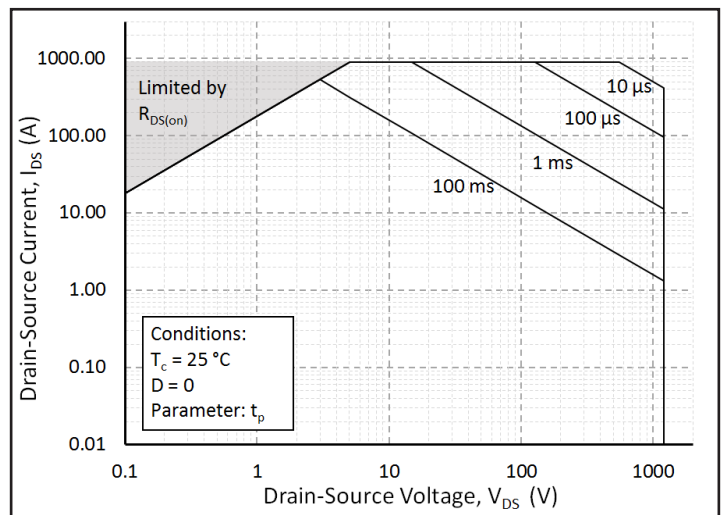


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

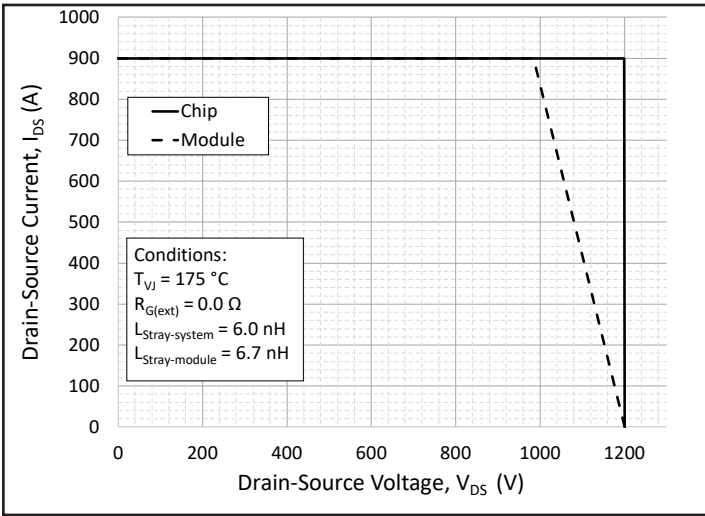


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

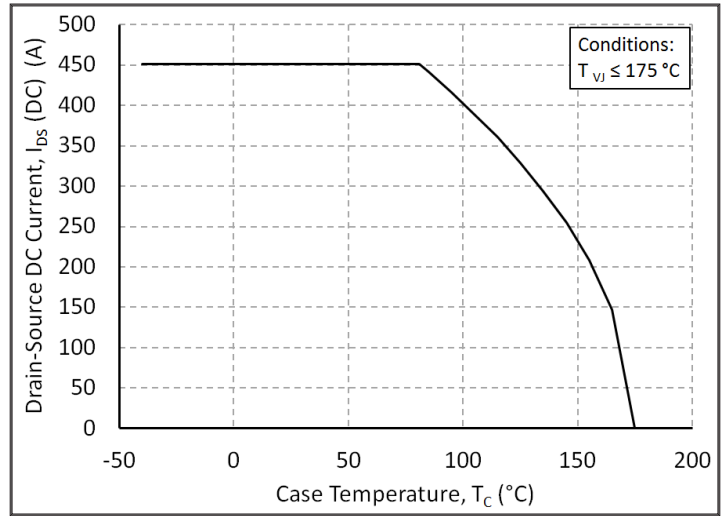


Figure 20. Continuous Drain Current Derating vs. Case Temperature

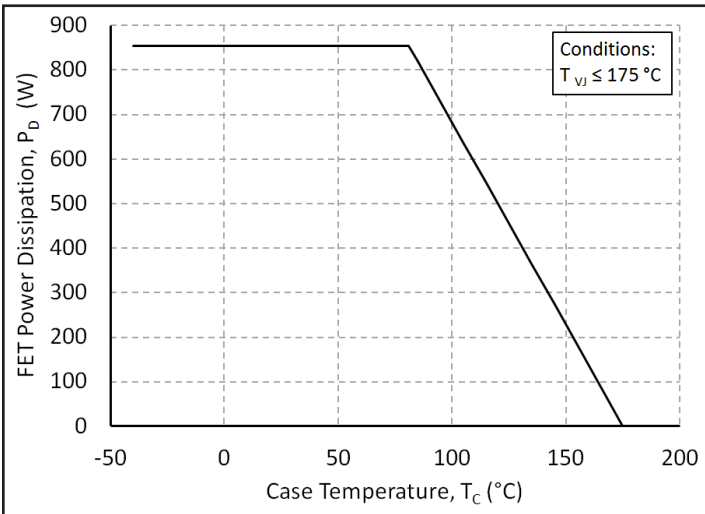


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

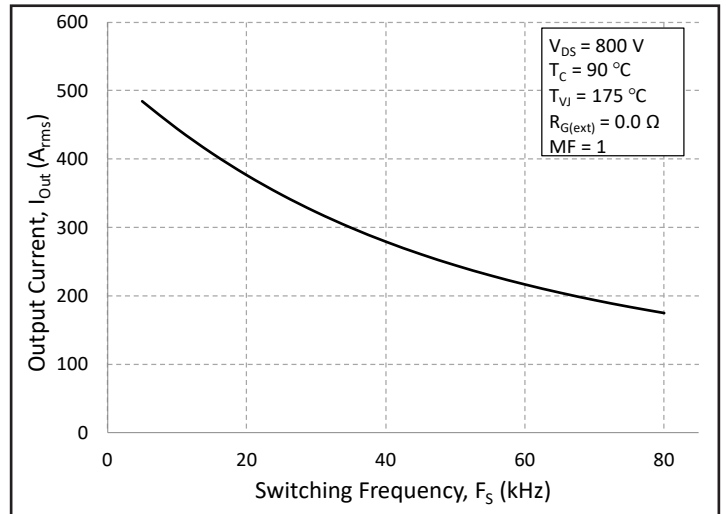
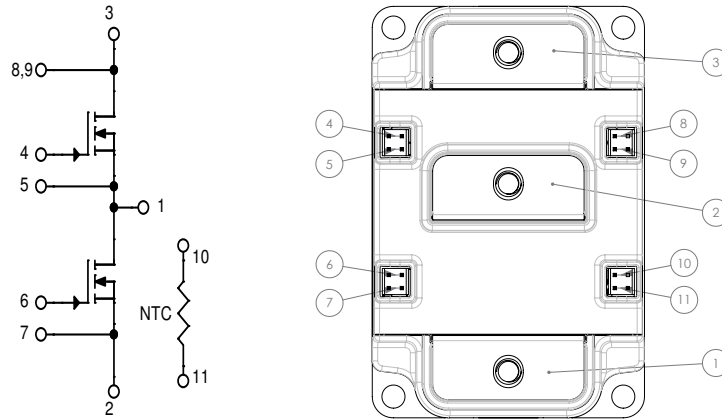


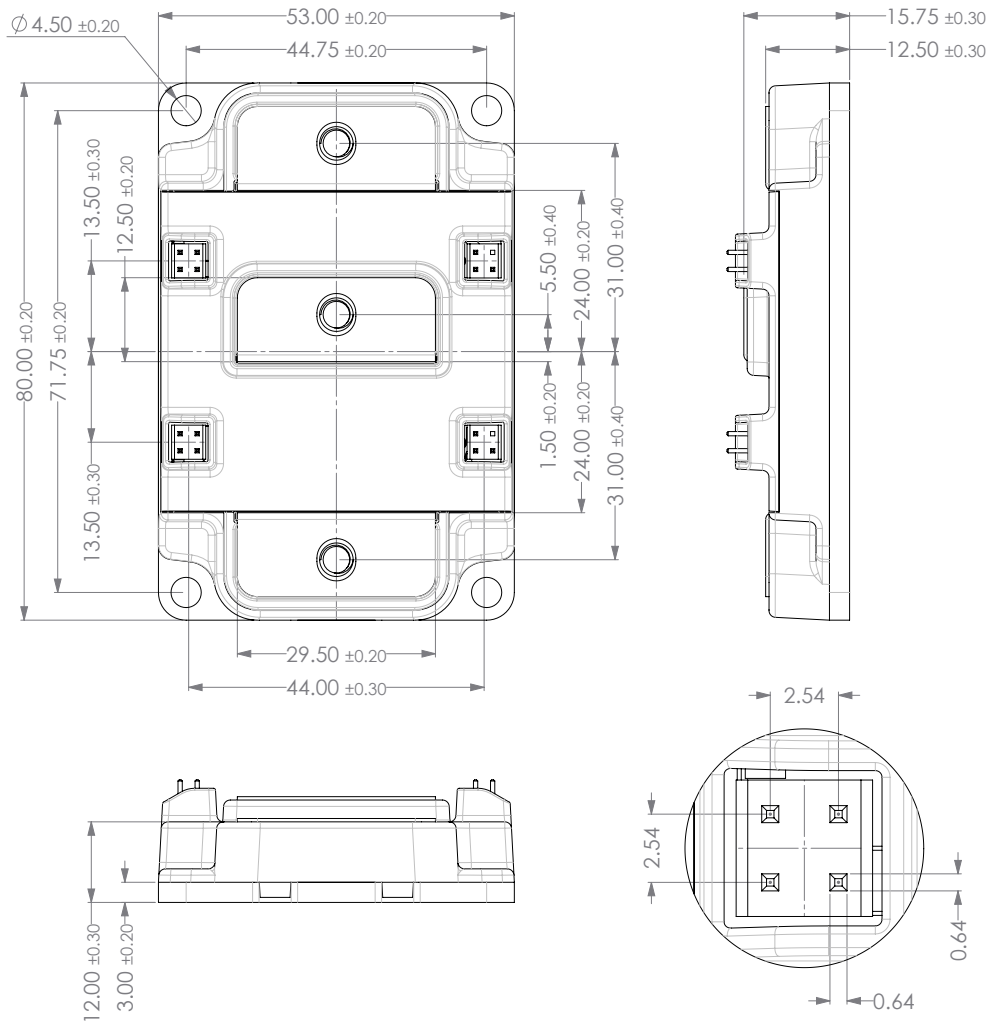
Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)



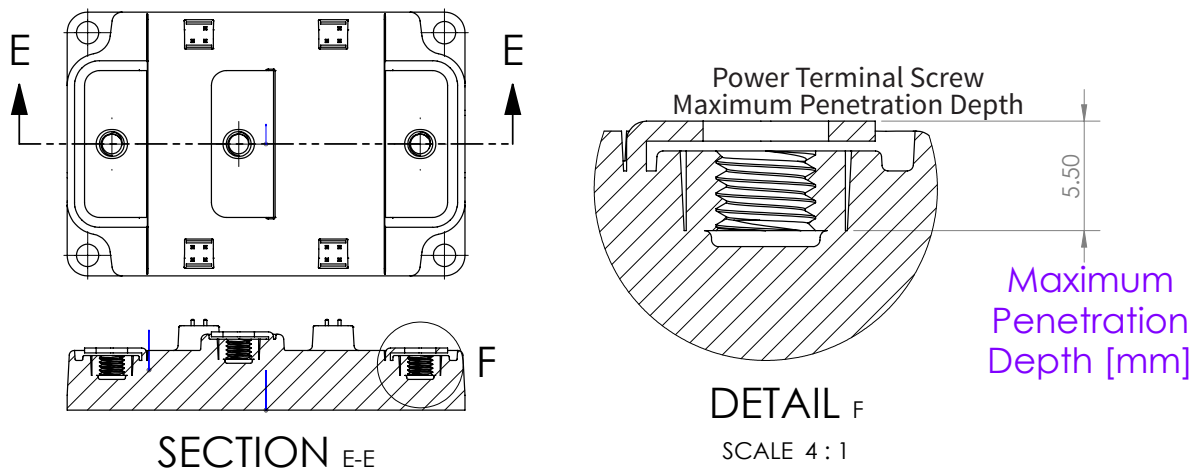
Schematic and Pin Out



Package Dimension (mm)



Package Dimension (mm)



Supporting Links & Tools

- [CGD12HBXMP: XM3 Evaluation Gate Driver](#)
- [CGD12HB00D: Differential Transceiver Board for CGD12HBXMP](#)
- [CRD300DA12E-XM3: 300 kW Inverter Kit for Conduction-Optimized XM3 \(CPWR-AN30\)](#)
- [KIT-CRD-CIL12N-XM3: Dynamic Performance Evaluation Board for the XM3 Module \(CPWR-AN31\)](#)
- [CPWR-AN28: Module Mounting Application Note](#)
- [CPWR-AN29: Thermal Interface Material Application Note](#)

Notes

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.
- The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.

