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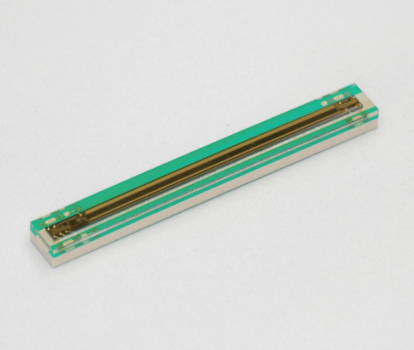


CMOS linear image sensor

S12443

Pixel size: 7 × 125 μm, 2496 pixels, small package

The S12443 is a CMOS linear image sensor with a compact yet 2496-pixel long photosensitive area (effective photosensitive area length: 17.472 mm). The pixel size is 7 × 125 μm.

Features

- **Pixel size: 7 × 125 μm**
- **2496 pixels**
- **Effective photosensitive area length: 17.472 mm**
- **3.3 V single power supply operation**
- **Built-in timing generator allows operation with only start and clock pulse inputs.**
- **Simultaneous charge integration for all pixels**
- **Variable integration time function (electronic shutter function)**
- **Video data rate: 10 MHz max.**
- **Small input terminal capacitance: 5 pF**

Applications

- **Barcode readers**
- **Position detection**
- **Image reading**
- **Encoders**

Structure

Parameter	Specification	Unit
Number of pixels	2496	-
Pixel pitch	7	μm
Pixel height	125	μm
Photosensitive area length	17.472	mm
Package	Glass epoxy	-
Seal material	Silicone resin	-

Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd	Ta=25 °C	-0.3 to +6	V
Clock pulse voltage	V(CLK)	Ta=25 °C	-0.3 to +6	V
Start pulse voltage	V(ST)	Ta=25 °C	-0.3 to +6	V
Operating temperature*1	Topr		-40 to +85	°C
Storage temperature*1	Tstg		-40 to +85	°C
Reflow soldering conditions*2	Tsol		Peak temperature 260 °C, 3 times (see P.9)	-

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to the product within the absolute maximum ratings.

*1: No dew condensation
When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

*2: JEDEC level 2a

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	3.15	3.3	3.45	V
Clock pulse voltage	High level	V(CLK)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	V
Start pulse voltage	High level	V(ST)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	V

Input terminal capacitance (Ta=25 °C, Vdd=3.3 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse input terminal capacitance	C(CLK)	-	5	-	pF
Start pulse input terminal capacitance	C(ST)	-	5	-	pF

Electrical characterisitics [Ta=25 °C, Vdd=3.3 V, V(CLK)=V(ST)=3.3 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	f(CLK)	200 k	5 M	10 M	Hz
Data rate	DR	-	f(CLK)	-	Hz
Output impedance	Zo	70	-	260	Ω
Current consumption*3 *4	I	14	21	30	mA

*3: f(CLK)=10 MHz
*4: Current consumption increases as the clock pulse frequency increases. The current consumption is 8 mA typ. at f(CLK)=200 kHz.

Electrical and optical characterisitics [Ta=25 °C, Vdd=3.3 V, V(CLK)=V(ST)=3.3V, f(CLK)=10 MHz]

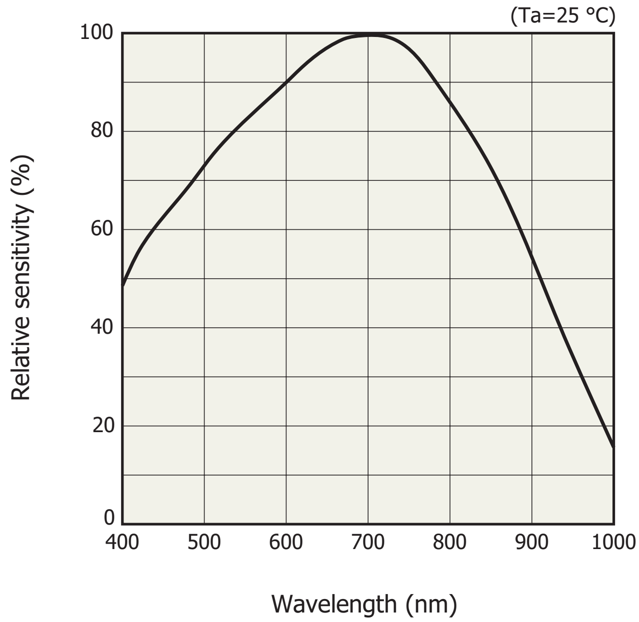
Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	λ	400 to 1000			nm
Peak sensitivity wavelength	λp	-	700	-	nm
Photosensitivity*5	Sw	-	500	-	V/(lx·s)
Conversion efficiency*6	CE	-	25	-	μV/e$^-$
Dark output voltage*7 *8	Vd	0	0.4	4.0	mV
Saturation output voltage*8	Vsat	1.5	2.0	2.8	V
Readout noise	Nread	0.4	1.2	2.0	mV rms
Dynamic range 1*9	Drange1	-	1666	-	times
Dynamic range 2*10	Drange2	-	5000	-	times
Output offset voltage	Vo	0.4	0.7	1.0	V
Photoresponse nonuniformity*5 *11	PRNU	-	-	±10	%
Image lag*12	IL	-	-	0.1	%

*5: Measured with a tungsten lamp of 2856 K
*6: Output voltage generated per one electron
*7: Integration time=10 ms
*8: Difference from Vo
*9: Drange1 = Vsat/Nread
*10: Drange2 = Vsat/Vd
Integration time=10 ms
Dark output voltage is proportional to the integration time and so the shorter the integration time, the wider the dynamic range.
*11: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 2490 pixels excluding 3 pixels each at both ends, and is defined as follows:
PRNU= ΔX/X × 100 (%)
X: average output of all pixels, ΔX: difference between X and maximum output or minimum output
*12: Signal components of the preceding line data that still remain even after the data is read out in a saturation output state.
Image lag increases when the output exceeds the saturation output voltage.

Appearance inspection standards

Parameter	Test criterion	Inspection method
Foreign matter on photosensitive area	10 µm max.	Automated camera

Spectral response (typical example)



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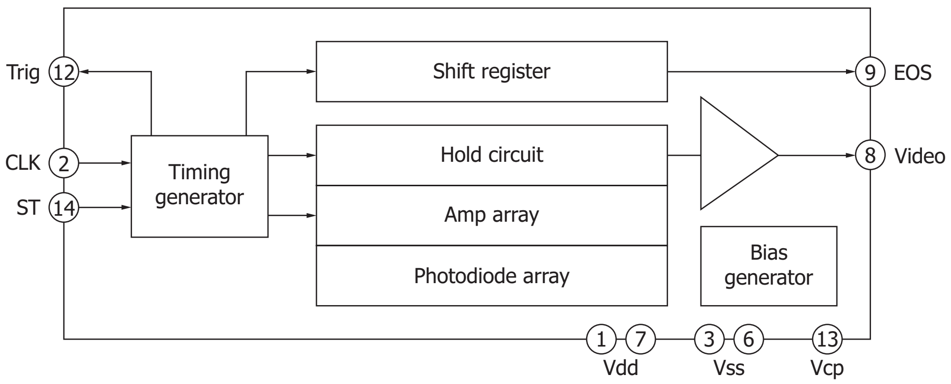
Block diagram



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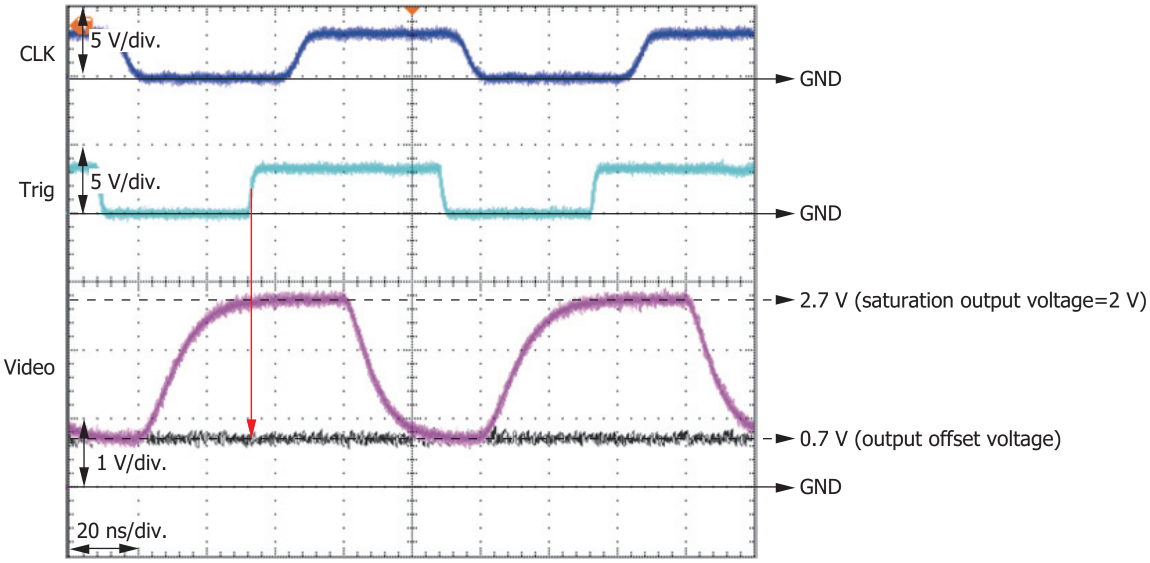
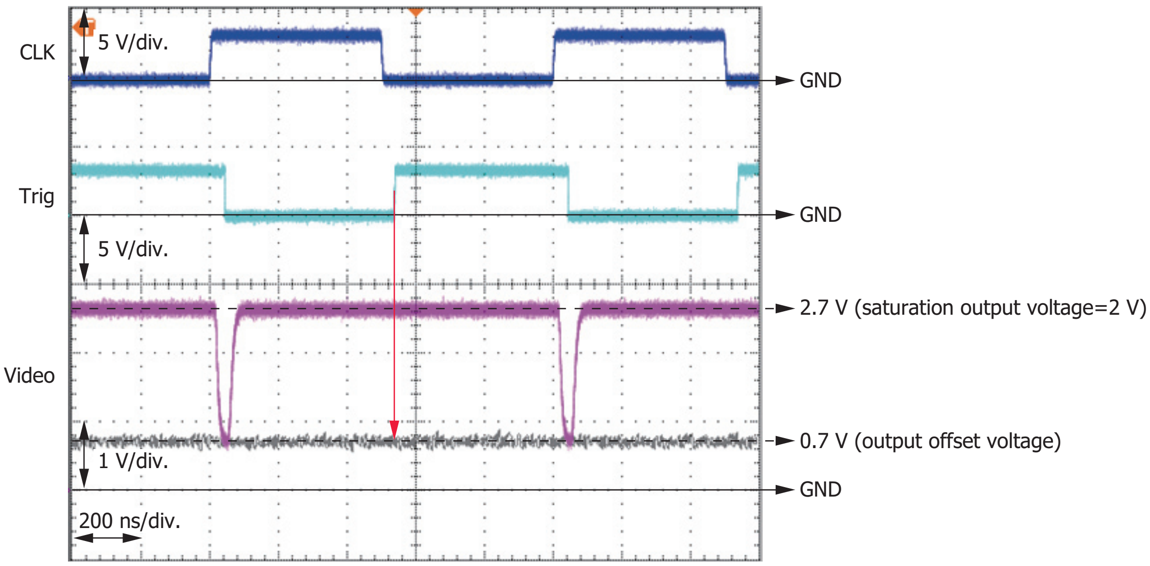
Output waveforms of one pixel

The timing for acquiring the video signal is synchronized with the rising edge of Trig pulse (See red arrow below.).

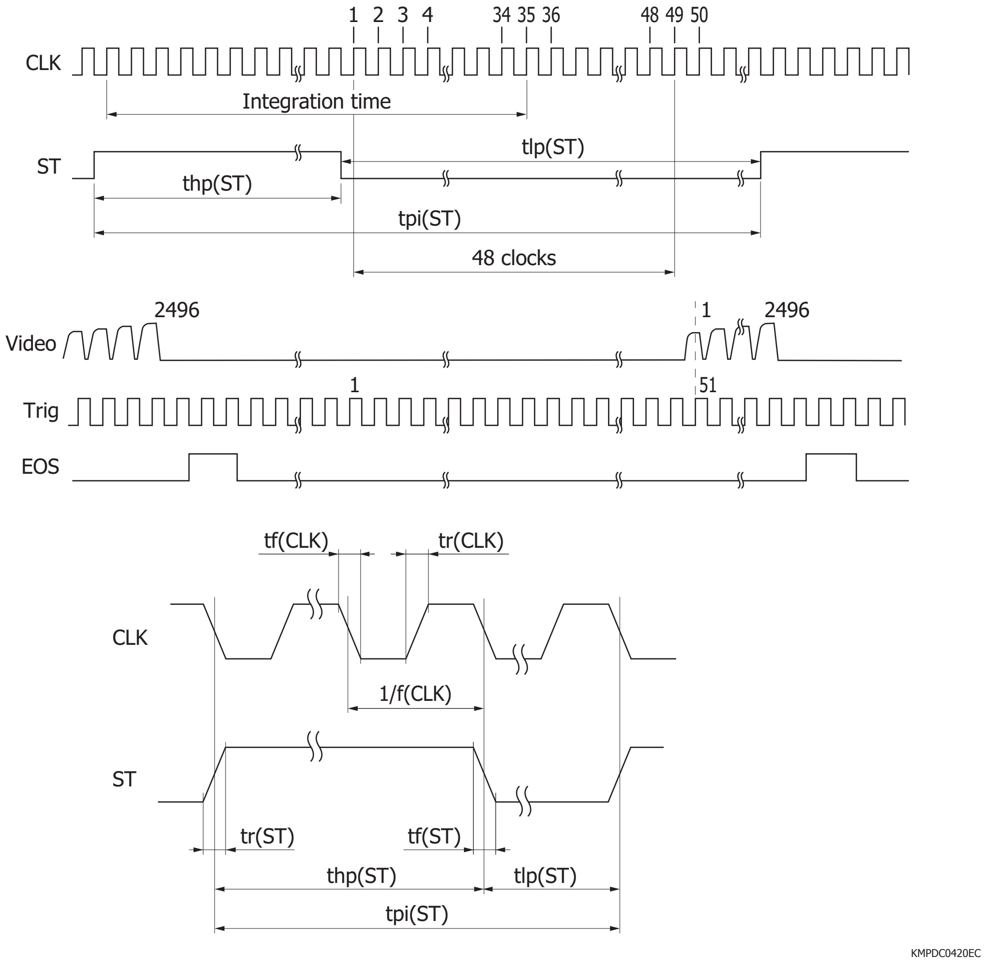
f(CLK)=DR=10 MHz



f(CLK)=DR=1 MHz



Timing chart

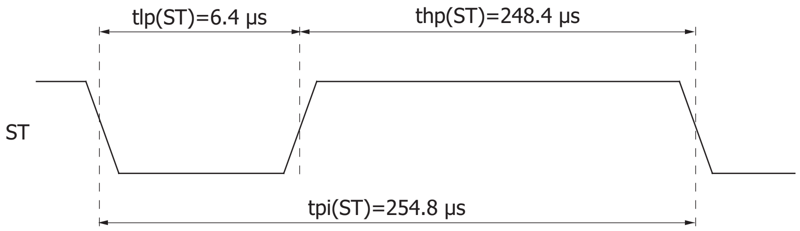


Parameter	Symbol	Min.	Typ.	Max.	Unit
Start pulse cycle*13	tpi(ST)	70/f(CLK)	-	-	s
Start pulse high period*13 *14	thp(ST)	6/f(CLK)	-	-	s
Start pulse low period	tlp(ST)	64/f(CLK)	-	-	s
Start pulse rise and fall times	tr(ST), tf(ST)	0	10	30	ns
Clock pulse duty ratio	-	45	50	55	%
Clock pulse rise and fall times	tr(CLK), tf(CLK)	0	10	30	ns

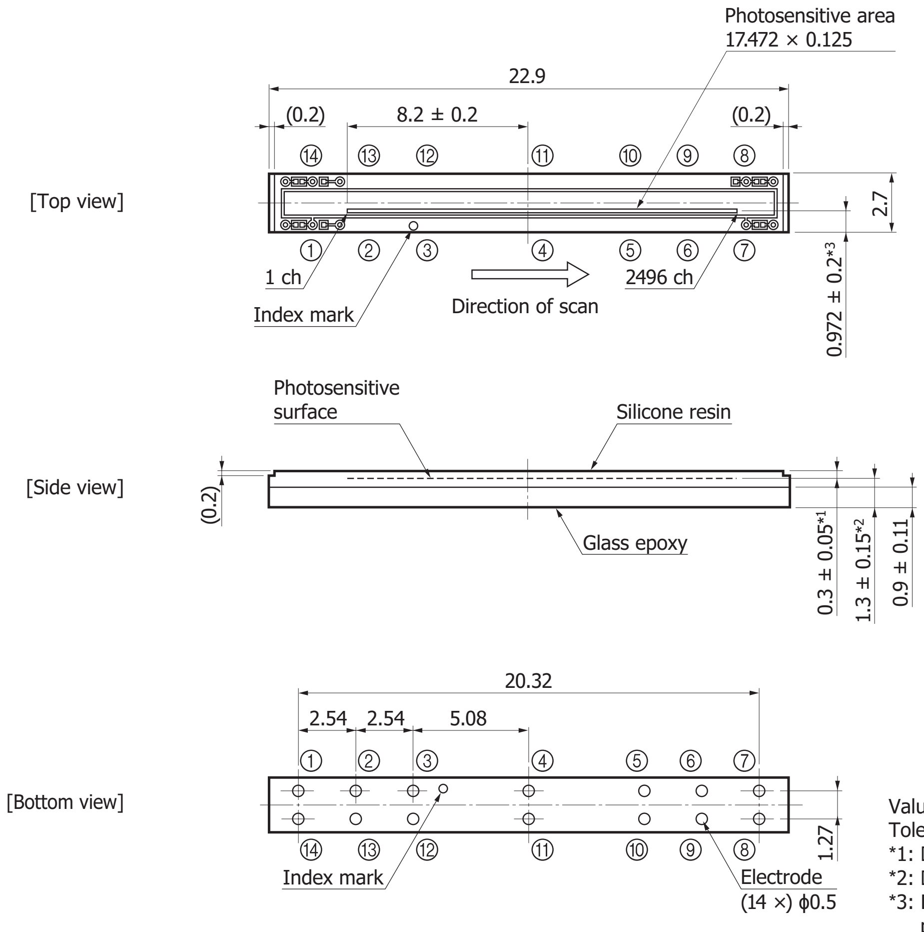
*13: Dark output increases if the start pulse cycle or the start pulse high period is lengthened.
*14: The integration time equals the high period of ST plus 34 CLK cycles.
The shift register starts operation at the rising edge of CLK immediately after ST goes low.
The integration time can be changed by changing the ratio of the high and low periods of ST.
If the first Trig pulse after ST goes low is counted as the first pulse, the Video signal is acquired at the rising edge of the 51st Trig pulse.

Operation example

This example assumes that the clock pulse frequency is maximized (video data rate is also maximized), the time of one scan is minimized, and the integration time is maximized.
Clock pulse frequency = Video data rate = 10 MHz
Start pulse cycle = 2548/f(CLK) = 2548/10 MHz = 254.8 μs
High period of start pulse = Start pulse cycle - Start pulse's low period min.
= 2548/f(CLK) - 64/f(CLK) = 2548/10 MHz - 64/10 MHz = 248.4 μs
Integration time is equal to the high period of start pulse + 34 cycles of clock pulses, so it will be 248.4 + 3.4 = 251.8 μs.



Dimensional outline (unit: mm)



Values in parentheses indicate reference values.
Tolerance unless otherwise noted: ±0.1
*1: Distance from package surface to photosensitive surface
*2: Distance from package bottom to photosensitive surface
*3: Distance from package side surface to center of photosensitive area

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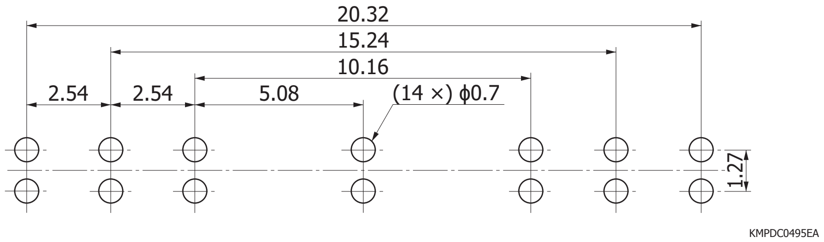
Pin connections

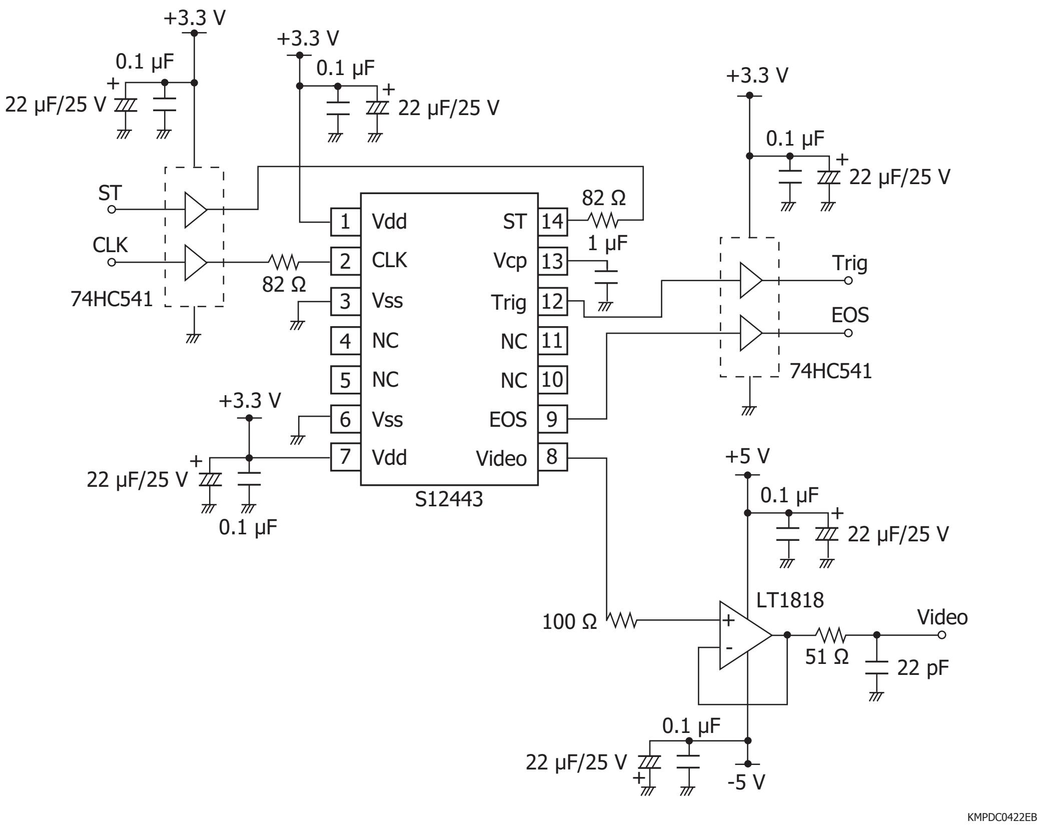
Pin no.	Symbol	I/O	Description
1	Vdd	I	Supply voltage
2	CLK	I	Clock pulse
3	Vss	-	GND
4	NC	-	No connection
5	NC	-	No connection
6	Vss	-	GND
7	Vdd	I	Supply voltage
8	Video	O	Video signal
9	EOS	O	End of scan
10	NC	-	No connection
11	NC	-	No connection
12	Trig	O	Trigger pulse
13	Vcp	I	Bias voltage for booster circuit*15
14	ST	I	Start pulse

*15: Voltage of approx. 5.5 V, which was boosted by the chip's internal booster circuit, appears at the terminal. To maintain the voltage, insert a capacitor of about 1 μF between GND and Vcp.

Recommended land pattern (unit: mm)



Application circuit example



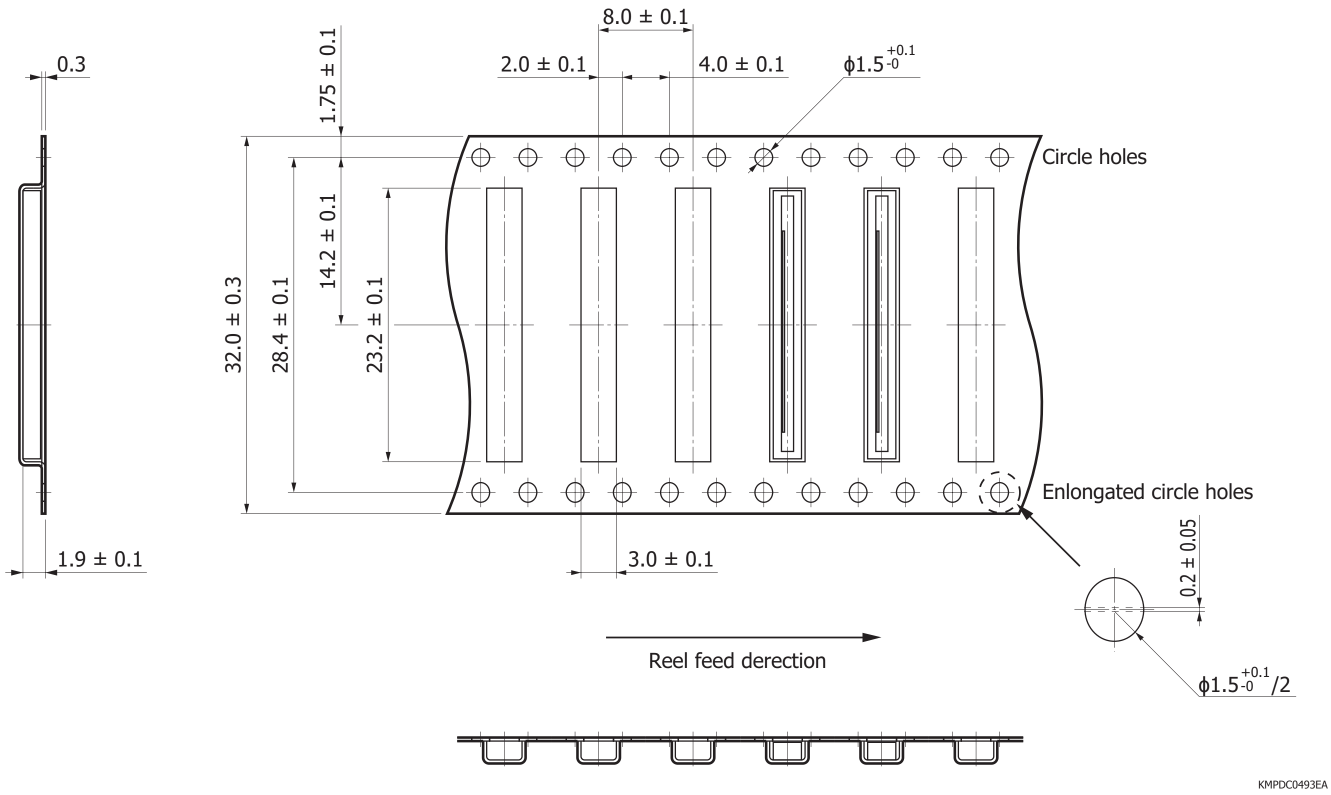
Standard packing specifications

■ Reel (conforms to JEITA ET-7200)

Dimensions	Hub diameter	Tape width	Material	Electrostatic characteristics
330 mm	100 mm	32 mm	Plastic*16	Conductive

*16: Compound of polyacetylene, polypyrrole, polythiophene and polyaniline

■ Embossed (unit: mm, material: plastic*16, conductive)



■ Packing quantity

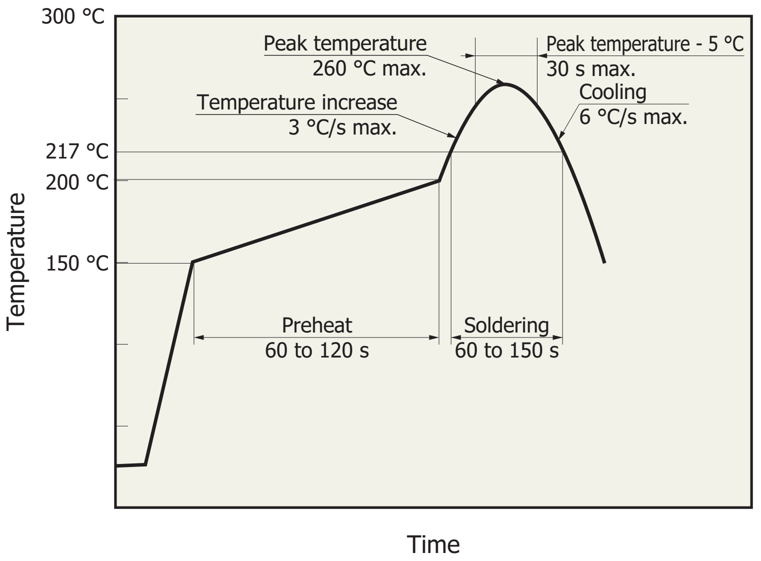
1000 pcs/reel

Packing specifications may vary on orders less than 1000 pieces.

■ Packing type

Reel and desiccant in moisture-proof packing (vaccum-sealed)

Recommended temperature profile for reflow soldering (typical example)



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· This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 4 weeks.
· The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. Before actual reflow soldering, check for any problems by tesitng out the reflow soldering methods in advance.

Precautions

(1) Electrostatic countermeasures
· This device has a built-in protection circuit as a safeguard against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools.
· Protect this device from surge voltages which might be caused by peripheral equipment.

(2) Package handling
· The photosensitive area of this device is sealed and protected by transparent resin. When compared to a glass faceplate, the surface of transparent resin may be less uniform and is more likely to be scratched. Be very careful when handling this device and also when designing the optical systems.
· Dust or grime on the light input window might cause nonuniform sensitivity. To remove dust or grime, blow it off with compressed air.

(3) Surface protective tape
· Protective tape is affixed to the surface of this product to protect the photosensitive area. After assembling the product, remove the tape before use.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

· Disclaimer
· Image sensor
· Surface mount type products
· Resin-sealed CMOS linear image sensors

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