Wireless Power Consortium Qi Compliant
AirFuel Alliance PMA Compliant

Wireless Power Receiver IC

BD57016GWL

General Description

BD57016GWL is a stand-alone wireless power receiver IC.

The device integrates a fully synchronous rectifier circuit with low-impedance FETs, Qi compliant and PMA compliant packet controller, adjustable regulated voltage output, and an open-drain output pin to communicate with the power transmitter using amplitude modulation.

BD57016GWL is targeted at mobile applications implementing wireless charging compliant to the Qi standard and the PMA standard.

Key Specifications

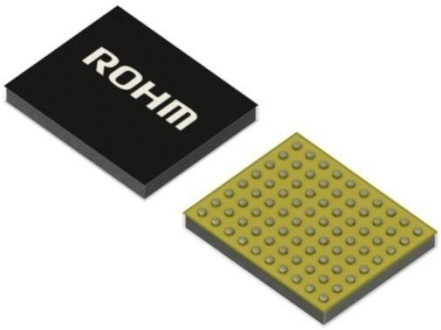
- Maximum Input Voltage: 20.0 V
- 7 Programmable Output Voltages: 5.0 V to 12.0 V
- Maximum Input/ Output Current: 1.5 A (Max)
- AC Input Frequency Range: 100 kHz to 480 kHz
- Operating Temperature Range: -25 °C to +85 °C

Package

	W (Typ) x D (Typ) x H (Max)
UCSP50L4C (80pin)	4.2 mm x 3.4 mm x 0.57 mm (0.4 mm pitch)

Features

- Low Impedance FET Rectifier
- High Efficiency Fully Synchronous Rectifier
- Supports Qi Standard Ver1.2 (BPP, EPP) and PMA Standard SR1
- Automatic Detection of Qi / PMA, or Selection by External Pin
- Open-Drain Output pin for Modulation
- TX-RX Coil Position Gap Alarm



Applications

Qi and/or PMA Compliant Devices

- Smart Phones
- Cell Phones
- Hand-held Mobile Devices

Typical Application Circuit

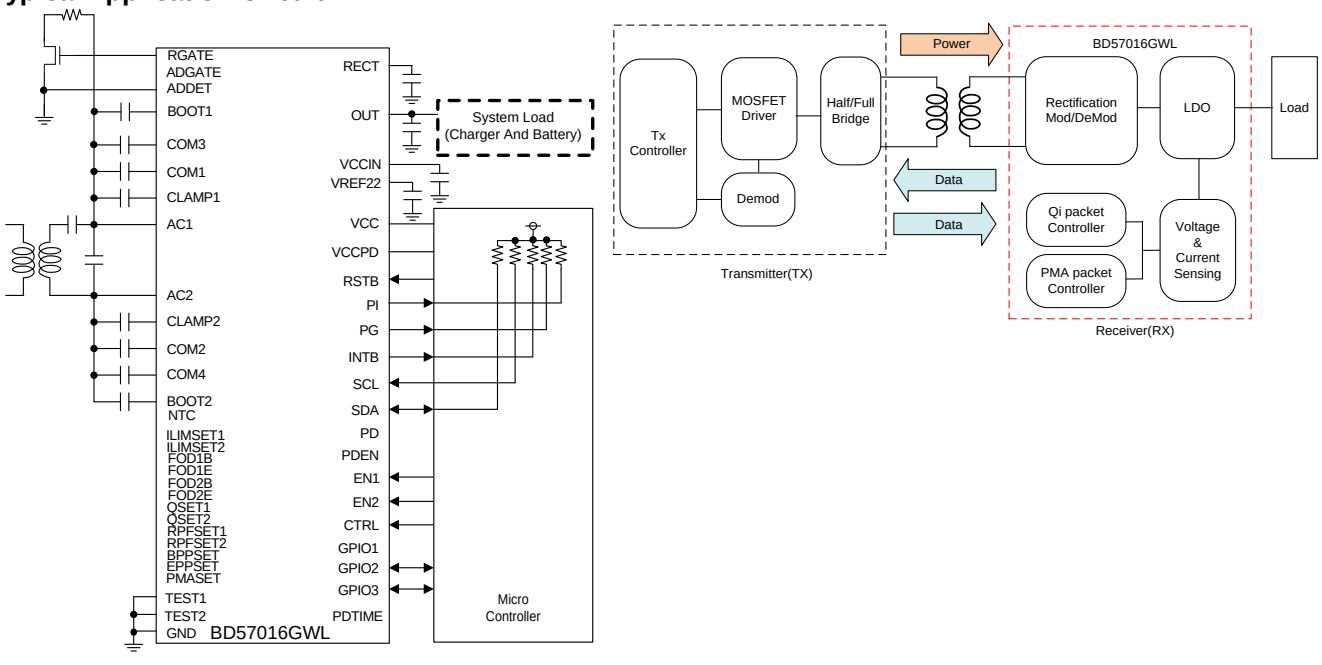


Figure 1. Wireless Power Transfer System

Contents

General Description 1
Features 1
Applications 1
Key Specifications 1
Package 1
Typical Application Circuit 1
Contents 2
Absolute Maximum Ratings 3
Recommended Operating Conditions 3
Electrical Characteristics 4
Pin Configuration 6
Pin Description 6
Block Diagram 9
Description of Blocks 10
Typical Performance Curves 48
Timing Chart 50
I/O Equivalence Circuits 51
Thermal/Heat Loss 53
Operational Notes 54
Ordering Information 56
Marking Diagram 56
Physical Dimension and Packing Information 57
Revision History 58

Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit
RECT, OUT, AC1, AC2, COM1, COM2, COM3, COM4, CLAMP1, CLAMP2 Voltage	V_{INOUT_H1}	-0.3 to +20	V
BOOT1, BOOT2 Voltage	V_{INOUT_H2}	-0.3 to +26	V
BOOT1-AC1, BOOT2-AC2 Voltage	V_{BOOT_AC}	-0.3 to +7.0	V
PG, PI, INTB, SDA, SCL, TEST1, TEST2, EN1, EN2, PMASET, BPPSET, EPPSET, CTRL, RGATE, PD, PDEN Voltage	V_{INOUT_L1}	-0.3 to +7.0	V
VCC, VCCIN, GPIO1-3, VREF22 FOD1B, FOD1E, FOD2B, FOD2E OUTSET, NTC, ILIMSET1, ILIMSET2, RSTB, QSET1, QSET2, PDTIME, VCCPD Voltage	V_{INOUT_L2}	-0.3 to +4.5	V
ADDET, ADGATE Voltage	V_{AD_H1}	-0.3 to +28	V
Input/ Output Rating Current	I_{MAX}	1.5*(Note 1)*	A
PG, PI, INTB Pin Rated Current	I_{MAX_PG}	15	mA
Power Dissipation	Pd	1.71*(Note 2)*	W
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB board with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Applies to AC1, AC2, RECT, GND terminals when all of them are connected to a common pattern on the PCB.

(Note 2) If mounted on a standard ROHM PCB (PCB size: 54 mm x 62 mm x 1.6 mm), reduce by 13.12 mW/°C (Ta ≥25 °C).

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	Topr	-25	-	+85	°C
Rectified Voltage Range	V_{RECT}	0	-	15	V
AC1, AC2 Input Peak Voltage Range	V_{AC1}, V_{AC2}	0	-	15	V
Capacitance between RECT and GND	C_{RECT}	20	-	-	µF

Electrical Characteristics (Unless otherwise specified V_{IN}=12 V Ta=25 °C)

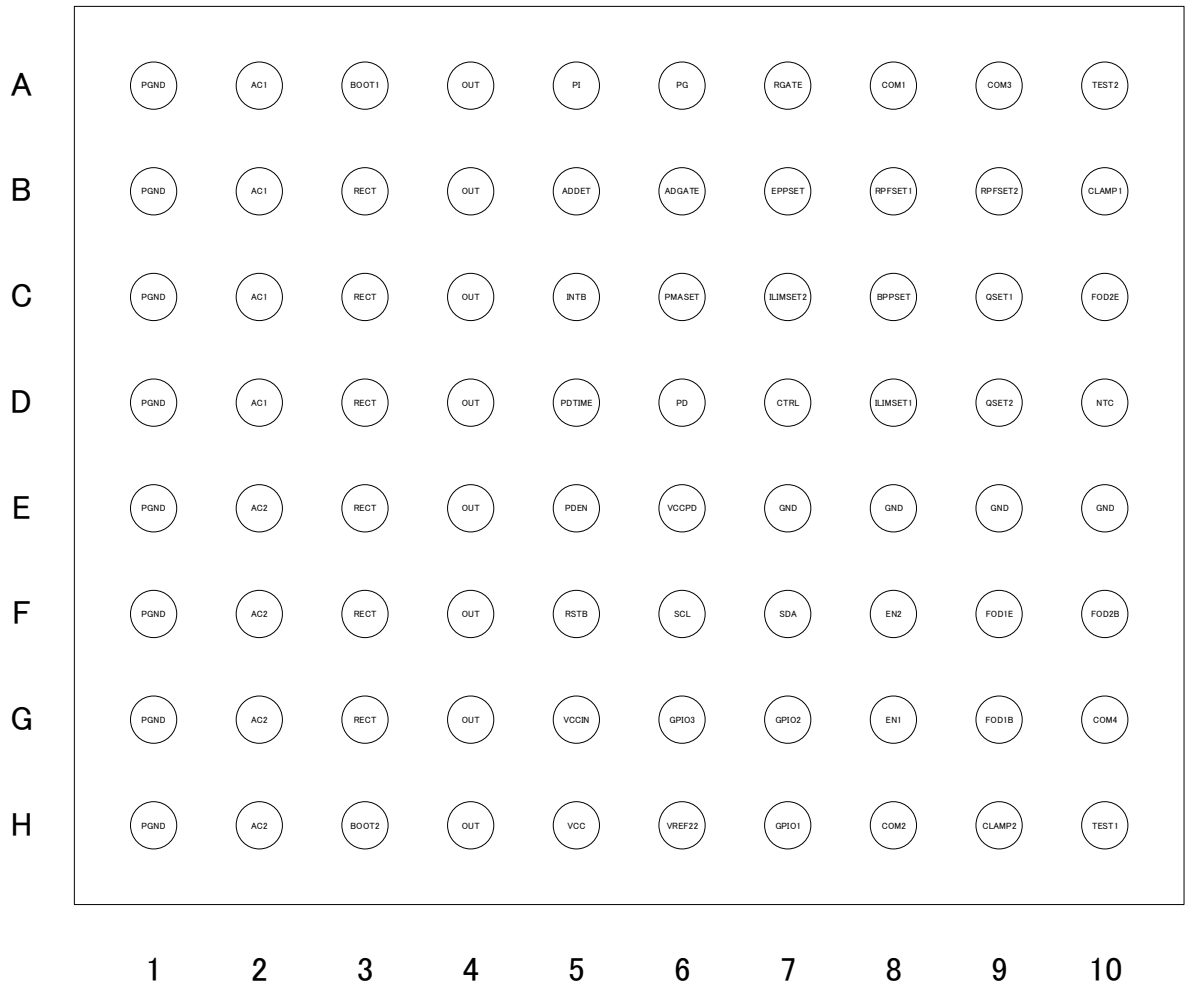
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Operating Circuit Current1	I_{RECT1}	-	44	50	mA	V_{RECT}=5.0 V, OUT off.
Operating Circuit Current2	I_{RECT2}	-	27	35	mA	V_{RECT}=5.0 V, OUT on
OUT Pin Quiescent Current (wireless charging is disabled)	I_{OUT}	-	50	100	µA	V_{OUT}=5.0 V, V_{RECT}=0 V ADDET=OPEN
Protection Circuit						
RECT Under Voltage Lockout	V_{RECTUV}	2.5	2.6	2.7	V	V_{RECT}:0 V to 5 V
Hysteresis on UVLO RECT Terminal	$V_{RECTUVHYS}$	150	300	450	mV	V_{RECT}:5 V to 0 V
RECT Over Voltage Protection Detection Voltage	V_{RECTOV}	15.6	16.5	17.4	V	V_{RECT}:10 V to 20 V
Hysteresis on RECT Over Voltage Protection	$V_{RECTOVHYS}$	150	300	450	mV	V_{RECT}:20 V to 10 V
LDO Block						
OUT Pin Output Voltage	V_{OUTLDO}	6.86	7.00	7.14	V	I_{LOAD}=100 mA, V_{OUT}=5.0 V setting, V_{RECT}=7.5 V
OUT Pin Output Voltage Accuracy	R_{ATEOUT}	-3	0	+3	%	V_{OUT}=5 V,5.3 V,8 V,9 V, 10 V, 12 V
OUT Pin Load Regulation	dV_{OUT}	-	-	200	mV	I_{LOAD}=0 mA to 500 mA V_{RECT}=7.2 V V_{OUT}=7 V
Maximum Output Current	$I_{LOADMAX}$	-	-	1.5	A	
PADDET Block						
PDTIME Input Off Leak Current	$I_{LEAKPDTIME}$	-	-	2.0	µA	VCCPD=2.65 V, AC2=Open, V_{PDTIME}=2.65 V
PDTIME Detection Voltage	V_{PDDET}	0.4	0.7	1.0	V	
PD Output L Level	V_{PDVOL}	-	0.1	0.2	V	I_{SINK}=1 mA
PD Pin Leak Current	I_{LEAKPD}	-	-	2.0	µA	V_{PD}=2.65 V, AC2=Open, V_{PDTIME}=0 V, V_{PD}=7 V
COM Block						
COM1 to COM4 ON Resistance	R_{ONCOM}	-	1.0	2.5	Ω	
COM1 to COM4 Pin Leak Current	$I_{LEAKCOM}$	-	-	2	µA	V_{COM1} to V_{COM4}=20 V
RGATE Block						
RGATE Pin Output H Level	V_{HRGATE}	4.3	4.8	5.3	V	I_{SOURCE}=-1 mA V_{RECT}=7 V
RGATE Pin Output L Level	V_{LRGATE}	-	0.1	0.5	V	I_{SINK}=1 mA
CLAMP Block						
CLAMP1, CLAMP2 ON Resistance	$R_{ONCLAMP}$	-	1.0	2.5	Ω	
CLAMP1, CLAMP2 Pin Leak Current	$I_{LEAKCLAMP}$	-	-	2	µA	V_{CLAMP1}, V_{CLAMP2}=20 V
Adapter Detection Block						
Adapter Input Detection Threshold Voltage	V_{ADPDET}	3.4	3.6	3.8	V	V_{ADDET}:0 V to 5 V
Adapter Input Detection Hysteresis Voltage	V_{HYS_AD}	200	400	600	mV	V_{ADDET}:5 V to 0 V
Adapter Input Overvoltage Detection Voltage	V_{ADDET_OV}	14.0	14.5	15.0	V	V_{ADDET}:13 V to 16 V
Adapter Input Overvoltage Detection Hysteresis Voltage	$V_{HYS\_AD\_OV}$	500	720	940	mV	V_{ADDET}:16 V to 13 V

Electrical Characteristics - continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
ADDET Pin Input Current	I_{ADDET}	-	150	300	µA	V_{ADDET}=5 V, OUT=OPEN
ADGATE Pin Output L Level	$V_{LADGATE}$	-	0.12	0.25	V	I_{SINK}=1 mA
EN1, EN2, CTRL, PDEN Pin						
EN1, EN2, CTRL Pin L Level Input Voltage	V_{ILMODE}	-	-	0.4	V	
EN1, EN2, CTRL Pin H Level Input Voltage	V_{IHMODE}	1.3	-	-	V	
PMA, QI, EN1, EN2, CTRL Pin Pull Down	R_{IMODE}	-	200	-	kΩ	
PDEN Pin L Level Input Voltage	V_{ILPDEN}	-	-	0.4	V	
PDEN Pin H Level Input Voltage	V_{IHPDEN}	1.3	-	-	V	
RSTB Pin						
RSTB Pin L Level Input Voltage	V_{ILRSTB}	-	-	0.6	V	VCC=2.65 V
RSTB Pin Pull Up Resistance	R_{IRSTB}	-	100	-	kΩ	
RSTB Pin L Level Output Voltage	V_{LRSTB}	-	0.15	0.30	V	I_{SINK}=1 mA
PG, PI, INTB Pin						
PG, PI, INTB Pin Output L Level	V_{LINT}	-	0.25	0.5	V	I_{SINK}=5 mA
PG, PI, INTB Leak Current	$I_{LEAKINT}$	-	-	2	µA	V_{INTB}=7 V
GPIO Pin						
GPIO Pin L Level Input Voltage	V_{ILGPIO}	-	-	VCCx0.3	V	
GPIO Pin H Level Input Voltage	V_{IHGPIO}	VCCx0.7	-	-	V	
GPIO Pull Down Resistance	R_{PDGPIO}	-	100	-	kΩ	
GPIO Pull Up Resistance	R_{PUGPIO}	-	100	-	kΩ	
L Level Output Voltage	V_{OLGPIO}	-	-	VCCx0.2	V	I_{SINK}=1 mA
H Level Output Voltage	V_{OHGPIO}	VCCx0.8	-	-	V	I_{SOURCE}=-1 mA
Serial Interface						
SCL, SDA Pin L Level Input Voltage	V_{ILSCL} V_{ILSDA}	-	-	0.4	V	
SCL, SDA Pin H Level Input Voltage	V_{IHSCL} V_{IHSDA}	1.3	-	-	V	
SCL, SDA Pin L Level Input Current	I_{ILSCL} I_{ILSDA}	-1	-	-	µA	V_{SCL}=V_{SDA}=0 V
SCL, SDA Pin H Level Input Current	I_{IHSCL} I_{IHSDA}	-	-	1	µA	V_{SCL}=V_{SDA}=2.65 V
SDA Pin L Level Output Voltage	V_{OLSDA}	-	-	0.4	V	I_{SINK}=2.5 mA

Pin Configuration

(TOP VIEW)



Pin Description

Pin No.	Pin Name	I/O	Function
A1*(Note 1)*	PGND	Ground	Power ground pin
A2*(Note 1)*	AC1	Input	AC input pin 1
A3	BOOT1	Output	Bootstrap capacitor connection pin 1 for the internal FET driver
A4*(Note 1)*	OUT	Output	LDO output pin
A5	PI	Output	Qi BPP/EPP identification pin
A6	PG	Output	Open drain output pin to notify if LDO output is ON
A7	RGATE	Output	Modulation output pin for PMA If only Qi mode is used, leave the pin OPEN.
A8	COM1	Output	Modulation output pin 1
A9	COM3	Output	Modulation output pin 3
A10	TEST2	Input	Test pin 2 (Usually these pins are connected to GND.)
B1*(Note 1)*	PGND	Ground	Power ground pin
B2*(Note 1)*	AC1	Input	AC input pin 1
B3*(Note 1)*	RECT	Output	Rectifier output pin
B4*(Note 1)*	OUT	Output	LDO output pin
B5	ADDET	Input	External adaptor voltage detection pin*(Note 2)*
B6	ADGATE	Output	External adaptor path gate driver pin

(Note 1) Please connect the pin to common on a board every function, if several pin numbers are assigned to one pin (function).
(Note 2) When the pin is unused, please connect the pin to GND.

Pin Description - continued

Pin No.	Pin Name	I/O	Function
B7	EPPSET	Input	Resistance connection pin for the EPP output voltage setting
B8	RPFSET1	Input	Resistance connection pin 1 for the EPP mode Reference peak frequency setting for Q factor
B9	RPFSET2	Input	Resistance connection pin 2 for the EPP mode Reference peak frequency setting for Q factor
B10	CLAMP1	Input	AC1 clamp protection pin
C1 *(Note 1)*	PGND	Ground	Power ground pin
C2*(Note 1)*	AC1	Input	AC input pin 1
C3*(Note 1)*	RECT	Output	Rectifier output pin
C4*(Note 1)*	OUT	Output	LDO output pin
C5	INTB	Output	Interrupt output pin
C6	PMASET	Input	Resistance connection pin for the PMA output voltage setting
C7	ILIMSET2	Input	Resistance connection pin for the EPP mode Current limit setting
C8	BPPSET	Input	Resistance connection pin for the BPP output voltage setting
C9	QSET1	Input	Resistance connection pin 1 for the EPP mode Q factor setting
C10	FOD2E	Input	Resistance connection pin 1 for the EPP mode foreign object detection adjustment setting. If only PMA mode is used, leave the pin OPEN.
D1*(Note 1)*	PGND	Ground	Power ground pin
D2*(Note 1)*	AC1	Input	AC input pin 1
D3*(Note 1)*	RECT	Output	Rectifier output pin
D4*(Note 1)*	OUT	Output	LDO output pin
D5	PDTIME	Input	PAD detection time setting pin*(Note 2)*
D6	PD	Output	PAD detection output pin
D7	CTRL	Input	Control pin for wireless charging
D8	ILIMSET1	Input	Resistance connection pin for the BPP/PMA mode Current limit setting
D9	QSET2	Input	Resistance connection pin 2 for the EPP mode Q factor setting
D10	NTC	Input	Resistance connection pin for the position gap detection setting*(Note 3)*
E1*(Note 1)*	PGND	Ground	Power ground pin
E2*(Note 1)*	AC2	Input	AC input pin 2
E3*(Note 1)*	RECT	Output	Rectifier output pin
E4 *(Note 1)*	OUT	Output	LDO output pin
E5	PDEN	Input	PAD detection enable pin*(Note 2)*
E6	VCCPD	Power	Power supply for pad detection pin*(Note 2)*
E7*(Note 1)*	GND	Ground	Ground pin
E8*(Note 1)*	GND	Ground	Ground pin
E9*(Note 1)*	GND	Ground	Ground pin
E10*(Note 1)*	GND	Ground	Ground pin

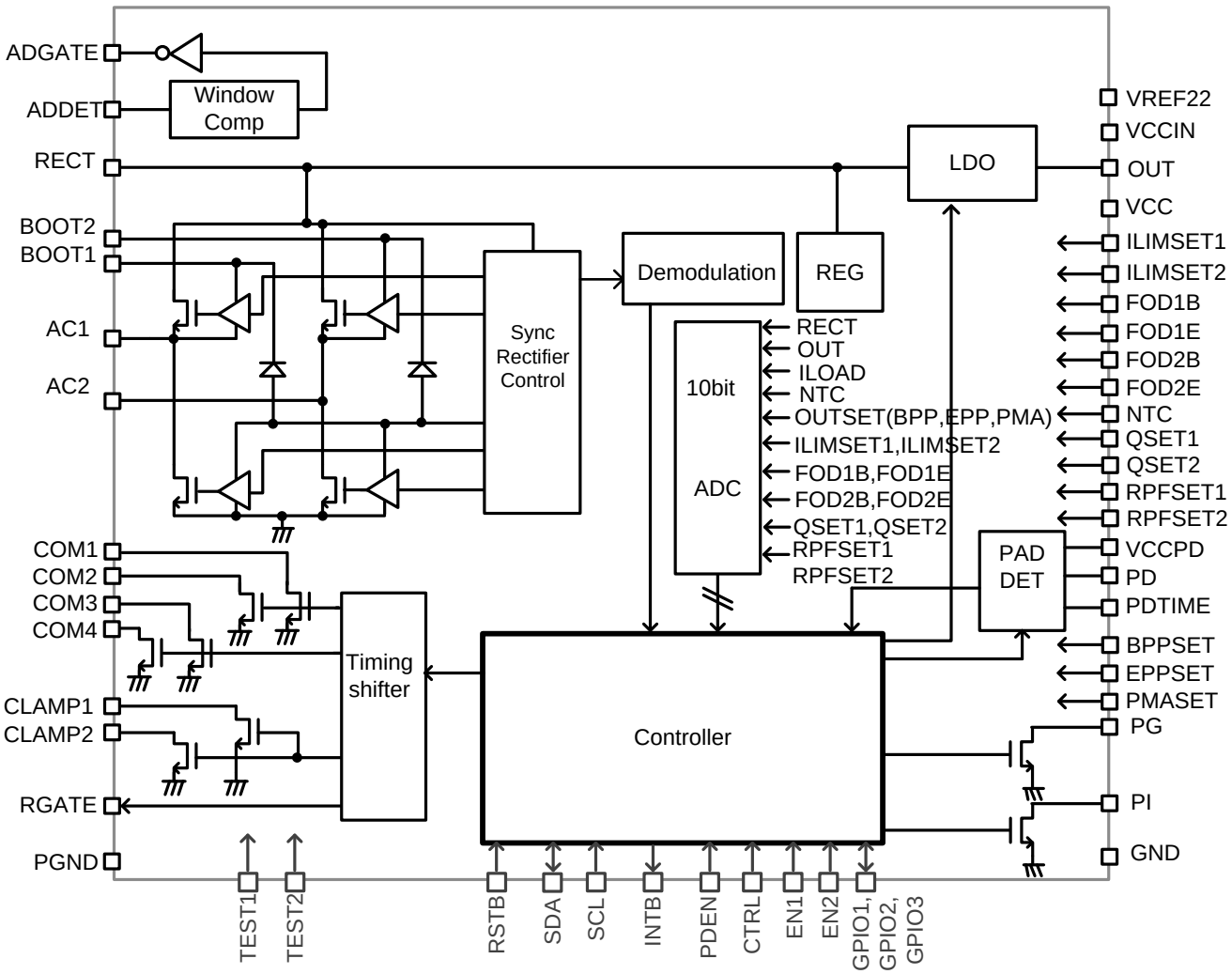
(Note 1) Please connect the pin to common on a board every function, if several pin numbers are assigned to one pin (function).
(Note 2) When the pin is unused, please connect the pin to GND.
(Note 3) When the pin is unused, please leave the pin OPEN.

Pin Description - continued

Pin No.	Pin Name	I/O	Function
F1*(Note 1)*	PGND	Ground	Power ground pin
F2*(Note 1)*	AC2	Input	AC input pin 2
F3*(Note 1)*	RECT	Output	Rectifier output pin
F4*(Note 1)*	OUT	Output	LDO output pin
F5	RSTB	Input/Output	System reset input and output pin*(Note 3)*
F6	SCL	Input	Serial interface clock input pin*(Note 2)*
F7	SDA	Input/Output	Serial interface data input/output pin*(Note 2)*
F8	EN2	Input	Enable pin 2 for wired, wireless or stop charging
F9	FOD1E	Input	Resistance connection pin 1 for the EPP mode foreign object detection adjustment setting. If only PMA mode is used, leave the pin OPEN.
F10	FOD2B	Input	Resistance connection pin 2 for the BPP mode foreign object detection adjustment setting. If only PMA mode is used, leave the pin OPEN.
G1*(Note 1)*	PGND	Ground	Power ground pin
G2*(Note 1)*	AC2	Input	AC input pin 2
G3*(Note 1)*	RECT	Output	Rectifier output pin
G4*(Note 1)*	OUT	Output	LDO output pin
G5	VCCIN	Output	2.5V internal power supply pin
G6	GPIO3	Input/Output	GPIO 3 pin*(Note 4)*
G7	GPIO2	Input/Output	GPIO 2 pin*(Note 4)*
G8	EN1	Input	Enable pin 1 for wired, wireless or stop charging
G9	FOD1B	Input	Resistance connection pin 1 for the BPP mode foreign object detection adjustment setting. If only PMA mode is used, leave the pin OPEN.
G10	COM4	Output	Modulation output pin 4
H1*(Note 1)*	PGND	Ground	Power ground pin
H2*(Note 1)*	AC2	Input	AC input pin 2
H3	BOOT2	Output	Bootstrap capacitor connection pin 2 for the internal FET driver
H4*(Note 1)*	OUT	Output	LDO output pin
H5	VCC	Power	External power supply application pin for LOGIC block*(Note 4)*
H6	VREF22	Output	2.2 V internal REF voltage output pin
H7	GPIO1	Input/Output	GPIO 1 pin*(Note 4)*
H8	COM2	Output	Modulation output pin 2
H9	CLAMP2	Input	AC2 clamp protection pin
H10	TEST1	Input	Test pin 1 (Usually these pins are connected to GND.)

(Note 1) Please connect the pin to common on a board every function, if several pin numbers are assigned to one pin (function).
(Note 2) When the pin is unused, please connect the pin to GND.
(Note 3) When the pin is unused, please leave the pin OPEN.
(Note 4) When the pin is unused, please connect the pin to GND or leave the pin OPEN.

Block Diagram



Description of Blocks

1. Qi BPP/EPP/PMA Operation Mode Selection

BD57016GWL is compliant with both Qi and PMA standards. Qi/PMA operation mode can be set by the automatic judgment with the internal circuit or by an external Pin. The automatic detection of operation mode depends on the carrier frequency from TX during Digital Ping. Furthermore, the operation mode using external pins is shown as follow:

BPPSET pin	EPPSET pin	PMASET pin	Operation Mode
GND short	GND short	GND short	Reserved (Do not use this setting)
Resistance Connection	GND short	GND short	Qi BPP mode (It will not operate in other modes)
GND short	Resistance Connection	GND short	Reserved (Do not use this setting)
Resistance Connection	Resistance Connection	GND short	Qi BPP/EPP mode (It will not operate in other modes)
GND short	GND short	Resistance Connection	PMA mode (It will not operate in other modes)
Resistance Connection	GND short	Resistance Connection	Automatic detection based on the internal circuit (Qi BPP only)
Resistance Connection	Resistance Connection	Resistance Connection	Automatic detection based on the internal circuit

When the Automatic detection of operation mode is selected, the active operation mode can be confirmed using the Mode Status Register (0x83).

Mode Status register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
MODE STATUS	0x83	[7] Reserved [6] PMA_MODE PMA mode detection monitor 0x0: Undetected PMA mode 0x1: Operating in PMA mode [5] QI_MODE Qi BPP mode detection monitor 0x0: Undetected Qi mode 0x1: Operating in Qi mode [4] MODE DETECTION ERROR 0x0: Mode detection No error 0x1: Mode detection error [3:0] Reserved	0x00	R

Reserved bits read an undefined value.

The charge start detection interrupt can be used as an indicator to when to check this register. Refer to section "*16 Interrupt Control Block"* for the data is on the charge start detection interrupt.

Description of Blocks - continued

2. Qi Controller Block

If Qi mode is detected as the operation mode of BD57016GWL, it will proceed to following the Qi compliant Ping phase. In this phase, it will send the Signal Strength value which shows the strength of connection to TX side. Next, BD57016GWL will proceed to the Identification & Configuration phase and the ID information and the necessary information about BD57016GWL will be sent to the TX. When BD57016GWL is set to EPP mode, (set in Qi Power Mode setting register (0x0E) or Resistance Connected the EPPSET pin), it sends the information of the configuration and requests the transition to the Negotiation phase. In this negotiation, if TX returns the ACK message, it will proceed to the Negotiation phase. However, if TX does not return a message, the BD57016GWL will proceed to the Power Transfer phase in the BPP mode and start the power transfer.
In this Negotiation phase, the negotiation information as specified in the Qi standard will be exchanged with the TX in order to transfer power at more than 5 W. If this negotiation succeeds, it will move to the Power Transfer phase at EPP.
A charging mode which BPP or EPP works on can be checked by the PI pin. If the PI pin is L, it is EPP, and if it is H, it means that it is charging in BPP. Furthermore, the same can be also confirmed by checking the Qi Monitor Mode register (0x52).

Qi Monitor Mode register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
MONI_MODE	0x52	[7:1] Reserved [0] POWER_MODE Classification of the operation mode 0x0: Operation in BPP 0x1: Operation in EPP	0x00	R

Reserved bits read “0”

In the Power Transfer Phase, an output voltage that has previously been set is output at the OUT pin and the device is ready to start charging. The charging will be stopped when setting the EN1 pin to “H” and sending the End Power Transfer packet (Charging Complete, EPT) to the TX. The following are the supporting messages regarding EPT packet. The EPT value can be checked in the Qi EPT Code Register (0x0E) when EPT is sent.

End Power Transfer Packet			
Value	**Reason**	**Support**	**Condition**
0x00	Unknown	Send	Adapter Input detection
0x01	Charge Complete	Send	Charge Complete (EN1=H Detection)
0x02	Internal Fault	Send	Internal Temperature Error, ILIMSET1, ILIMSET2, FOD1B, FOD1E, FOD2B, FOD2E pin setting error.
0x03	Over Temperature	Send	External Temperature Error (CTRL=H Detection, Detection for using the information from NTC pin)
0x04	Over Voltage	Not Sent	-
0x05	Over Current	Not Sent	-
0x06	Battery Failure	Not Sent	-
0x07	Reserved	Not Sent	-
0x08	No Response	Send	No convergence to desired point for RECT voltage
0x09	Reserved	Not Sent	-
0x0A	Negotiation Failure	Send	Negotiation can not be done normally
0x0B	Restart Power Transfer	Not Sent	-

When sending this packet, the interrupt could be generated for the external microcontroller.

Qi EPT Code register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
EPT_CODE	0x0E	[7:0] EPT_CODE EPT value (code) When the status is not EPT, this register is 0xFF.	0xFF	R

Description of Blocks - continued

3. PMA Controller Block

When the operation of BD57016GWL is set to PMA mode, BD57016GWL will proceed to the digital Ping phase of PMA. In this phase, BD57016GWL will notify that a device based on PMA exists and sends the ACK Signal to the TX. Next, BD57016GWL proceeds to the Identification phase and sends BD57016GWL ID information to the TX. TX will check the ID Information and if it is correct, it will proceed to the Power Transfer phase. However, if it is incorrect, it will go back to the Digital Ping phase. In the Power Transfer phase, an output voltage is produced in the OUT pin and it charging can start. The charging will be stopped when setting the EN1 pin to “H” and sending a signal of EOC to the TX. When the charging stops, it can also generate an interrupt signal. The detailed reason for stop charging is stored in the PMA EOC Code register (0x0F). Other conditions that produce an End of Charge (EOC) signal are described below.

PMA EOC Code register (Only for PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
EOC_WR	0x0F	[7:0] EOC_CODE Cause of the output EOC. (”1” indicates “Detection”) [7]: ECO_TEMP During NTC detection [6]: EOC_NO_LOAD No Load Detection (continuous for 42 seconds or more)*(Note 1)* [5]: EOC_FULL_CHARGE Full Charge Detection(Low Current Detection for long hours)*(Note 1)* [4]: OUT_UVLO UVLO Detection of Output [3]: EOC_CTRL External Temperature Error (CTRL=H Detection) 150 degrees [2]: EOC_TSD Internal Temperature Error, ILIMSET pin setting Error, OUTSET pin setting Error [1]: EOC_EN1 Charge Complete (EN1=H Detection) [0]: EOC_ADP_DET Adapter Input Detection	0x00	R

(Note 1) These functions are cleared when the device is reset. This setting shall remain in effect with the following registers (EOC_MASK:0x80)

PMA EOC Mask register (Only for PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
EOC_MASK	0x80	[7:4] Reserved [3] MASK_NO LOAD EOC output for the No Load Detection Disable (0x0: Enable 0x1: Disable) [2] MASK_FULL EOC output for the Full Charge Detection Disable (0x0: Enable 0x1: Disable) [1:0] Reserved	0x0C	R/W

Please set an initial value into Reserved bits.

Description of Blocks - continued

4. Rectifier block

By inputting AC signal into both ends of a primary side (TX) coil, a voltage is generated by electromagnetic induction in the secondary side coil. Full-wave rectification is performed after detection of output current from the secondary coil as mentioned above, and using the built-in FET connected to AC1 and AC2 pins. The current detection is done by comparing the AC pin voltage (FET R_{ON} x I_{COIL}) with GND level. The on/off signal of built-in FET will be generating based on this detection signal. The on/off timing of L side FET and H side FET are monitored to prevent a shoot through current. The bootstrap drive system for the Nch FET on H side and L side is adopted for high efficiency. Therefore, the capacitor for voltage maintenance is needed between the BOOT1 (BOOT2) pin and the AC1 (AC2) pin.

5. Low Drop Out (LDO) Block

The OUT pin output voltage can be set through the BPPSET, EPPSET, PMASET pin or through a register
Additionally, the current limit value of the OUT pin can be set through the ILIMSET1, ILIMSET2 pin or through a register.
Regarding the OUT pin output Voltage setting, refer to section "*13. OUTPUT Voltage setting*" for details.
The details of the current limit settings are explained in section "*9. ILIM setting*".

6. A/D Converter Block

When making a packet, each kind of analog signal that is needed for calculation will be converted to digital. The A/D converter uses the 10 bit sequential comparison (SAR) formula. This conversion is processed internally so it cannot be controlled from outside.

7. External Control Input (EN1, EN2, and CTRL)

Charging from wireless supply or wired (adapter) supply can be enabled or disabled using EN1 and EN2.
By default, EN1=L and EN2=L, so both wireless power supply and adapter control are active. When both sources are available, priority is given to the adapter (wired power), wireless power is stopped according to the sequence explained in adapter detection block, and the electrical connection of the path from an adapter is active.

When EN1 becomes H, the Qi mode will produce an End Power Transfer (0x01: Charge Complete) packet and the PMA mode will produce an End of Charge (EOC) packet and wireless power supply will be stopped.

CTRL	Operation
L	Will maintain the normal feed (wireless power supply) condition.
H	During external temperature error, the wireless power transfer will stop because of an EPT or EOC output.

EN1	EN2	Operation
L	L	Both the wireless power charging and external adapter control are enabled. Priority is given to the external adapter. That is, if a sufficient adapter input is detected during wireless power charging, wireless power will immediately stop and only an adapter charging will continue.
L	H	Both the wireless power charging and external adapter control are enabled. Priority is given to the wireless power. That is, if a sufficient adapter input is detected during wireless power charging, adapter charging will immediately stop and only wireless power charging will start.
H	L	Wireless power charging is disabled (OFF). The charge of the adapter is effective.
H	H	Both an adapter and wireless power charging are disabled. That is, in this mode, power cannot be supplied from OUT.

Description of Blocks - continued

8. Adapter Detection Block

If the ADDET pin was detected to have 3.6 V (Typ) or more, ADGATE will output LOW and turn ON the PMOS switch of the adapter line. When priority is given to an adapter, (cable), wireless power supply will be stopped (EPT/EOC output), and then the OUT output will be stopped. After that, the voltage at OUT will be checked and if it is 0.7 V or less and the adapter line of PMOS switch will be turned ON (ADGATE: H to L).
The sequence of operation during adapter detection is as follows.

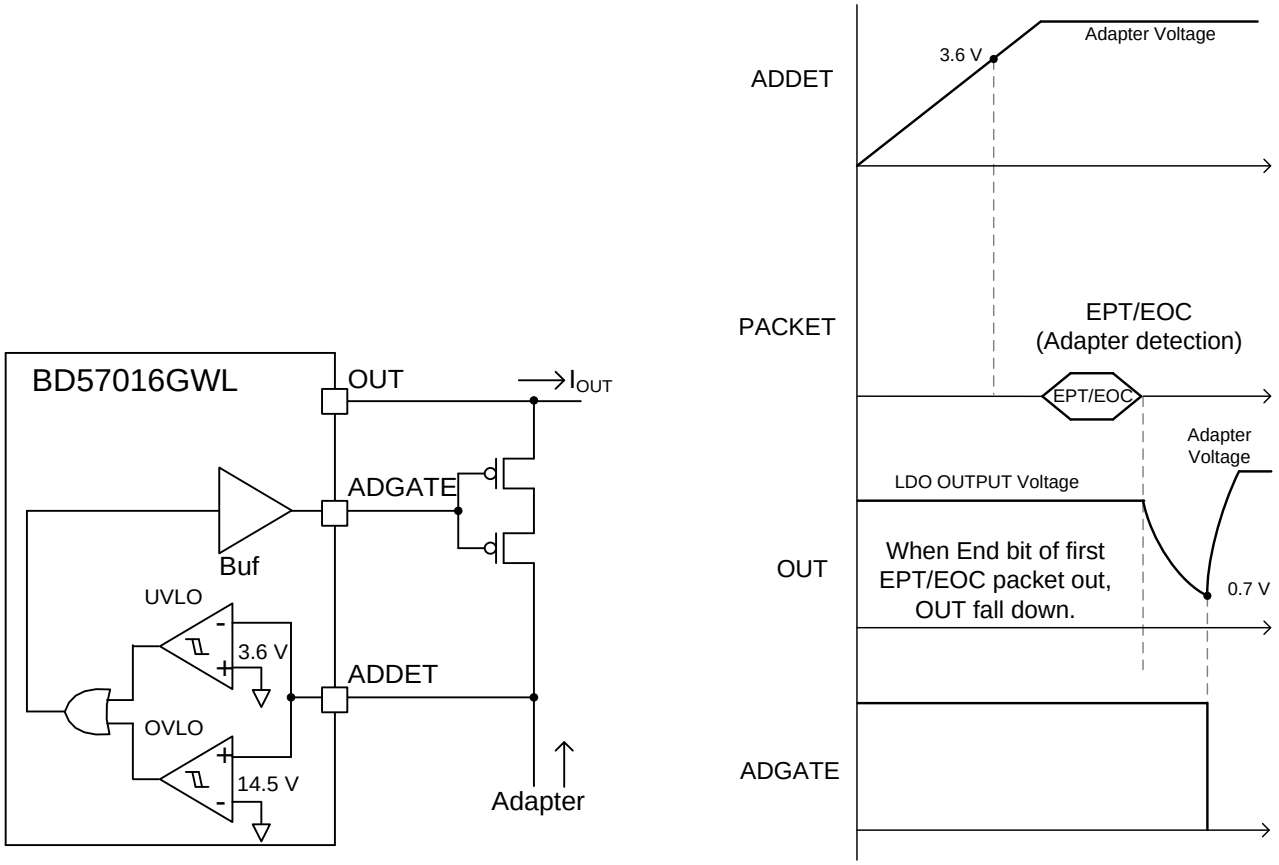


Figure 2. Adapter Detection

If the ADDET voltage is more than the threshold of OVP, it will be in a detection state and the power path of PMOS will instantly stop regardless of the wireless power supply.

Description of Blocks - continued

9. ILIM Setting

The current limit value of the OUT pin can be set by the resistance connected to the ILIMSET1, ILIMSET2 pin or the register shown below. The following formula shows the relation between setting resistance and limit current (I_{LIM}).

Current Limit I_{LIM} [mA]	$R_{ILIMSET}$ [kΩ]
ILIMSET register setting	OPEN
500	120
700	75
900	56
1000	43
1200	36
1400	30
1500	24
1600	20

The used resistance should have accuracy of ±1 %.

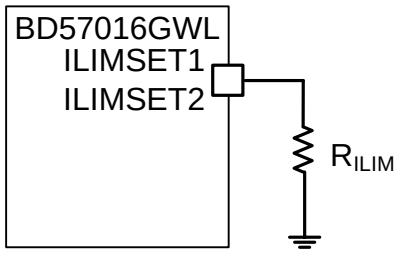


Figure 3. ILIMSET1, ILIMSET2 Setting

If the ILIMSET1, ILIMSET2 pin is shorted to GND, it will be a setting error and will produce the EPT (internal fault) or it will output EOC.

When the ILIMSET1, ILIMSET2 pin is OPEN or the bit [7] of the following register is set to “1”, the Output Current Limit value (of ILIM) can be set depending on the following register (0x07,0x09). If the bit [7] of this register is set to “1”, the setting of register has priority regardless of the resistance connected to the ILIMSET1, ILIMSET2 pin. Furthermore, the state related to the ILIMSET1, ILIMSET2 pin can be confirmed depending on the next register (0x06,0x08).

ILIMSET setting register (For Qi BPP and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
ILIM1_SET	0x06	[7] ILIM1_REG_EN 0x0: Normal mode (ILIM1 is decided by ADC value) 0x1: Test mode (ILIM1 is decided by [5:0] of this register) [6] Reserved [5:0] ILIM1_SET_VAL OUT Pin Current Limit Level setting 0x5: 500 mA / 0x10: 1050 mA 0x6: 550 mA / 0x11: 1100 mA 0x7: 600 mA / 0x12: 1150 mA 0x8: 650 mA / 0x13: 1200 mA 0x9: 700 mA / 0x14: 1250 mA 0xA: 750 mA / 0x15: 1300 mA 0xB: 800 mA / 0x16: 1350 mA 0xC: 850 mA / 0x17: 1400 mA 0xD: 900 mA / 0x18: 1450 mA 0xE: 950 mA / 0x19: 1500 mA 0xF: 1000 mA / Other: Reserved	0x11	R/W
ILIM1_STATE	0x07	[7] ILIM1_SHORT_DET Short detection of the ILIMSET1 pin. 0x0: not short 0x1: short (sending EPT in Qi mode, EOC in PMA mode) [6:4] ILIM1_ADC_VAL Current limit value set based on the read value in A/D. If the read value in A/D is outside the setting range, it is 0x0. 0x0: 500 mA / 0x4: 1100 mA 0x1: 700 mA / 0x5: 1200 mA 0x2: 900 mA / 0x6: 1300 mA 0x3: 1000 mA / 0x7: 1500 mA [3] ILIM1_OPEN_DET Enable/Disable of the register setting. 0x0: Disable 0x1: Enable (make the ILIMSET1 pin OPEN to enable this) [2:0]: Reserved	0x00	R

Please set an initial value into Reserved bits.

9. ILIM Setting - continued

ILIMSET setting register (For Qi EPP)

Register Name	Address	Bit [7:0]	Initial Value	R/W
ILIM2_SET	0x08	[7] ILIM2_REG_EN 0x0: Normal mode (ILIM2 is decided by ADC value) 0x1: Test mode (ILIM2 is decided by [5:0] of this register) [6] Reserved [5:0] ILIM2_SET_VAL OUT Pin Current Limit Level setting 0x5: 500 mA / 0x10: 1050 mA 0x6: 550 mA / 0x11: 1100 mA 0x7: 600 mA / 0x12: 1150 mA 0x8: 650 mA / 0x13: 1200 mA 0x9: 700 mA / 0x14: 1250 mA 0xA: 750 mA / 0x15: 1300 mA 0xB: 800 mA / 0x16: 1350 mA 0xC: 850 mA / 0x17: 1400 mA 0xD: 900 mA / 0x18: 1450 mA 0xE: 950 mA / 0x19: 1500 mA 0xF: 1000 mA / Other: Reserved	0x11	R/W
ILIM2_STATE	0x09	[7] ILIM2_SHORT_DET Short detection of the ILIMSET2 pin. 0x0: not short 0x1: short (sending EPT in Qi mode or EOC in PMA mode) [6:4] ILIM2_ADC_VAL Current limit value set based on the read value in A/D. If the read value in A/D is outside the setting range, it is 0x0. 0x0: 500 mA / 0x4: 1100 mA 0x1: 700 mA / 0x5: 1200 mA 0x2: 900 mA / 0x6: 1300 mA 0x3: 1000 mA / 0x7: 1500 mA [3] ILIM2_OPEN_DET Enable/Disable of the register setting. 0x0: Disable 0x1: Enable (make the ILIMSET2 pin OPEN to enable this) [2:0]: Reserved	0x00	R

Please set an initial value into Reserved bits.

Description of Blocks - continued

10. FOD Setting

In Qi mode, in order to implement FOD (Foreign Object Detection) function, it is required to strictly compute the received power and to compare it with the transmitted power from the TX side. The FOD1B, FOD1E, FOD2B and FOD2E pin is used for power fine adjustment and to adjust other power losses (e.g. LC loss) inside the IC. Adjustment is performed by using the resistance connected to the FOD1B, FOD1E, FOD2B and FOD2E pin or the register shown below. The relation of the received power (PRP) supply and each parameter is shown on the formula below.

The FOD1B, FOD2B pin: FOD1, FOD2 setting for Qi BPP

The FOD1E, FOD2E pin: FOD1, FOD2 setting for Qi EPP

$$P_{PR} = \alpha \times f(V_{RECT}, I_{OUT}) + \beta \quad [\mathrm{W}]$$

$$\alpha = FOD2\_Value$$

$$\beta = FOD1\_Value \quad [\mathrm{W}]$$

FOD1_Value [mW]	R_{FOD1} [kΩ]
FOD1_SET resister setting	OPEN or 820
-64(-96)	300
-32(-32)	180
32(32)	130
64(96)	100
96(160)	82
128(224)	68
160(288)	56
192(352)	47
224(416)	39
256(480)	33
288(544)	27
320(608)	24
352(672)	22
384(736)	20

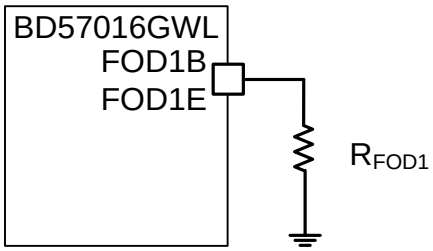


Figure 4. FOD1 Setting

( ): Setting in FOD1E=EPP MODE.

The used resistance should have accuracy of ±1 %.

When the FOD1B, FOD1E pin is shorted to GND, it will be a setting error and will produce an EPT.

FOD2_Value [-]	R_{FOD2} [kΩ]
FOD2_SET resister setting	OPEN or 820
1.054	300
1.070	180
1.086	130
1.102	100
1.118	82
1.134	68
1.150	56
1.166	47
1.182	39
1.198	33
1.214	27
1.230	24
1.246	22
1.262	20

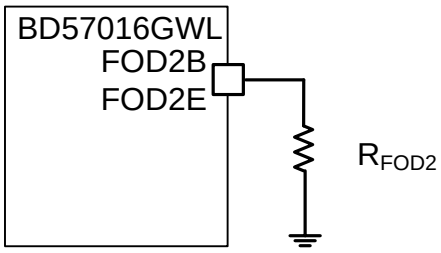


Figure 5. FOD2 Setting

The used resistance should have accuracy of ±1 %.

When the FOD2B, FOD2E pin is shorted to GND, it will be a setting error and will produce an EPT.

10. FOD Setting - continued

On the previous page, α is the inclination adjustment. β is the offset adjustment.

Function f (V_{RECT}, I_{OUT}) is almost proportional to output power with the value calculated in the internal IC.

In addition, the setting mentioned above is a reference value. The materials, the shape of the coil, an external factors including the distance to the environment (metal presence to absorb the magnetic flux including the battery) TX coil around the coil is considered and the adjustment is necessary.

It is possible to set the FOD1 and FOD2 value in the registers (0x20, 0x22, 0x24, 0x26) by leaving the FOD1B, FOD1E, FOD2B and FOD2E pins OPEN or setting the bit [7] of these registers (0x21, 0x023, 0x25, 0x27) to "1". If the bit [7] of these registers is set to "1", the setting of register has priority regardless of the resistance connected to the FOD1B, FOD1E, FOD2B and FOD2E pin.

In addition, the related states in FOD1 and FOD2 value can be confirmed on the next registers (0x21, 0x023, 0x25, 0x27).

FOD1 register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
FOD1_BPP_STATE	0x21	[7] FOD1B_SHORT_DET Short detection of the FOD1B pin. 0x0: not short 0x1: short (sending EPT) [6:3] FOD1B_ADC_VAL The set value based on the read value in A/D. 0xF when the read value in A/D was detected short. 0x0 when the read value in A/D was detected open. 0x1: -64 mW 0x8: +192 mW 0x2: -32 mW 0x9: +224 mW 0x3: +32 mW 0xA: +256 mW 0x4: +64 mW 0xB: +288 mW 0x5: +96 mW 0xC: +320 mW 0x6: +128 mW 0xD: +352 mW 0x7: +160 mW 0xE: +384 mW [2] FOD1B_OPEN_DET Enable/ Disable of the register setting. 0x0: Disable 0x1: Enable (make FOD1B pin OPEN to enable this) [1:0] Reserved	0x00	R
FOD1_EPP_STATE	0x23	[7] FOD1E_SHORT_DET Short detection of the FOD1E pin. 0x0: not short 0x1: short (sending EPT) [6:3] FOD1E_ADC_VAL The set value based on the read value in A/D. 0xF when the read value in A/D was detected short. 0x0 when the read value in A/D was detected open. 0x1: -96 mW 0x8: +352 mW 0x2: -32 mW 0x9: +416 mW 0x3: +32 mW 0xA: +480 mW 0x4: +96 mW 0xB: +544 mW 0x5: +160 mW 0xC: +608 mW 0x6: +224 mW 0xD: +672 mW 0x7: +288 mW 0xE: +736 mW [2] FOD1E_OPEN_DET Enable/ Disable of the register setting. 0x0: Disable 0x1: Enable (make the FOD1E pin OPEN to enable this) [1:0] Reserved	0x00	R

Please set an initial value into Reserved bits.

10. FOD Setting - continued

FOD2 register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
FOD2_BPP_STATE	0x25	[7] FOD2B_SHORT_DET Short detection of the FOD2B pin. 0x0: not short 0x1: short (sending EPT) [6:3] FOD2B_ADC_VAL The set value based on the read value in A/D. 0xF when the read value in A/D was detected short. 0x0 when the read value in A/D was detected open. 0x01: 1.054 times 0x08: 1.166 times 0x02: 1.070 times 0x09: 1.182 times 0x03: 1.086 times 0x0A: 1.198 times 0x04: 1.102 times 0x0B: 1.214 times 0x05: 1.118 times 0x0C: 1.230 times 0x06: 1.134 times 0x0D: 1.246 times 0x07: 1.150 times 0x0E: 1.262 times [2] FOD2B_OPEN_DET Enable/ Disable of the register setting. 0x0: Disable 0x1: Enable (make the FOD2B pin OPEN to enable this) [1:0] Reserved	0x00	R
FOD2_EPP_STATE	0x27	[7] FOD2E_SHORT_DET Short detection of the FOD2E pin. 0x0: not short 0x1: short (sending EPT) [6:3] FOD2E_ADC_VAL The set value based on the read value in A/D. 0xF when the read value in A/D was detected short. 0x0 when the read value in A/D was detected open. 0x01: 1.054 times 0x08: 1.166 times 0x02: 1.070 times 0x09: 1.182 times 0x03: 1.086 times 0x0A: 1.198 times 0x04: 1.102 times 0x0B: 1.214 times 0x05: 1.118 times 0x0C: 1.230 times 0x06: 1.134 times 0x0D: 1.246 times 0x07: 1.150 times 0x0E: 1.262 times [2] FOD2E_OPEN_DET Enable/ Disable of the register setting. 0x0: Disable 0x1: Enable (make the FOD2E pin OPEN to enable this) [1:0] Reserved	0x00	R

Please set an initial value into Reserved bits.

10. FOD Setting - continued

FOD1 register setting (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
FOD1_BPP_SET	0x20	[7] FOD1B_REG_EN 0x0: If the FOD1B pin is not OPEN, the setting of this register (bit [4:0]) is invalid. 0x1: The setting of this register (bit [4:0]) is valid forcibly. [6] FOD1B_POLARITY Set the polarity 0x0: Plus mode (Add the setting value) 0x1: Minus mode (Subtract the setting value) [5] Reserved [4:0] FOD1B Setting of the FOD1B value. 0x00: 0 mW / 0x08: 256 mW 0x01: 32 mW / 0x09: 288 mW 0x02: 64 mW / 0x0A: 320 mW 0x03: 96 mW / 0x0B: 352 mW 0x04: 128 mW / 0x0C: 384 mW 0x05: 160 mW / 0x0D: 416 mW 0x06: 192 mW / 0x0E: 448 mW 0x07: 224 mW / Other: Reserved	0x00	R/W
FOD1_EPP_SET	0x22	[7] FOD1E_REG_EN 0x0: If the FOD1E pin is not OPEN, the setting of this register (bit [4:0]) is invalid. 0x1: The setting of this register (bit [4:0]) is valid forcibly. [6] FOD1E_POLARITY Set the polarity 0x0: Plus mode (Add the setting value) 0x1: Minus mode (Subtract the setting value) [5] Reserved [4:0] FOD1E Setting of the FOD1E value. 0x00: 0 mW / 0x08: 256 mW 0x01: 32 mW / 0x09: 288 mW 0x02: 64 mW / 0x0A: 320 mW 0x03: 96 mW / 0x0B: 352 mW 0x04: 128 mW / 0x0C: 384 mW 0x05: 160 mW / 0x0D: 416 mW 0x06: 192 mW / 0x0E: 448 mW 0x07: 224 mW / Other: Reserved	0x00	R/W

10. FOD Setting - continued

FOD2 register setting (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
FOD2_BPP_SET	0x24	[7] FOD2B_REG_EN 0x0: If the FOD2B pin is not OPEN, the setting of this register (bit [5:0]) is invalid. 0x1: The setting of this register (bit [5:0]) is valid forcibly. [6] Reserved [5:0] FOD2B Setting of the FOD2B value. 0x01: 1.054 times 0x02: 1.062 times 0x03: 1.070 times 0x04: 1.078 times 0x05: 1.086 times 0x06: 1.094 times 0x07: 1.102 times 0x08: 1.110 times 0x09: 1.118 times 0x0A: 1.126 times 0x0B: 1.134 times 0x0C: 1.142 times 0x0D: 1.150 times 0x0E: 1.158 times Other: Reserved	0x07	R/W
FOD2_EPP_SET	0x26	[7] FOD2E_REG_EN 0x0: If the FOD2E pin is not OPEN, the setting of this register (bit [5:0]) is invalid. 0x1: The setting of this register (bit [5:0]) is valid forcibly. [6] Reserved [5:0] FOD2E Setting of the FOD2E value. 0x01: 1.054 times 0x02: 1.062 times 0x03: 1.070 times 0x04: 1.078 times 0x05: 1.086 times 0x06: 1.094 times 0x07: 1.102 times 0x08: 1.110 times 0x09: 1.118 times 0x0A: 1.126 times 0x0B: 1.134 times 0x0C: 1.142 times 0x0D: 1.150 times 0x0E: 1.158 times Other: Reserved	0x07	R/W

Description of Blocks - continued

11. Q Value Setting

It is necessary to send FOD Status packet with the information of the Q value from RX to perform foreign object detection (Foreign Object Detection) in the Qi standard (more than 5W). The Q value shown here is a Q value of the coil of the TX when RX is put on Test TX#MP1 defined in Qi standard. The setting of the Q factor connects resistance to the QSET1, QSET2 pin or setting a register (0x2C, 0x2E).
(When operating BD57016GWL in EPP mode)

For example, in the case of Q=100, set 0x64, R_{QSET1}=27 kΩ, R_{QSET2}=39 kΩ

Q Value bit [3:0] 0x3A	R_{QSET1} [kΩ]	Q Value bit [7:4] 0x3A	R_{QSET2} [kΩ]
F	820	F	820
E	300	E	300
D	180	D	180
C	130	C	130
B	100	B	100
A	82	A	82
9	68	9	68
8	56	8	56
7	47	7	47
6	39	6	39
5	33	5	33
4	27	4	27
3	24	3	24
2	22	2	22
1	20	1	20
0	18	0	18

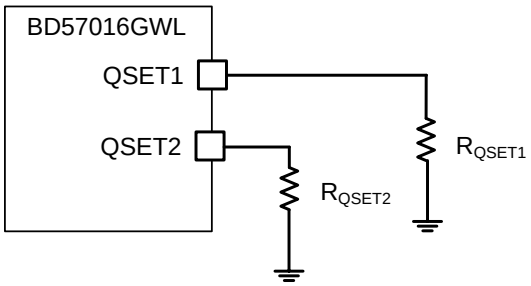


Figure 6. Q Value Setting

The used resistance should have accuracy of ±1 %.

Q value setting register (Only for Qi)
Please set an initial value into Reserved bits

Register Name	Address	Bit [7:0]	Initial Value	R/W
FOD_S_PCKT_EN	0x2C	[7:1] Reserved [0] SEL_QFOD_DATA 0: The QSET1, QSET2 pin setting 1: Register setting	0x00	R/W
FOD_S_PCKT_0	0x2E	[7:0] FOD_PCKT_B1 Q value sent as FOD Status packet. A Q level does not have a unit. For example, in the case of Q=125, set 0x7D. This register is available by setting the FOD_S_PCKT_EN [0] register to 1.	0x00	R/W

Description of Blocks - continued

12. Position Gap Detection Function During Start Up

The RECT voltage at start up is monitored, and it will detect the position gap of the RX coil in reference to the XY position on the TX coil. The threshold value (V_{THPOS}) used for position gap detection can also be set through the POSSET setting register (0x6A).
When the RECT voltage is lower than V_{THPOS}, the interrupt signal could be generated by the INTB pin. In the default setting, this function is disabled. The Position Gap Detection setting register need to be changed to enable this function in the situation that impressed the external power supply on the VCC pin. Detection of the position gap is performed about 30 ms after the RX was put on the TX, RECT waked up, and VRECTUV was released. At that timing, the interrupt signal was generated at the INTB pin.

The initial value of V_{THPOS} is the LDO Output Voltage setting value x 40 %.

V_{THPOS} is determined using the formula below.
V_{THPOS} = LDO output voltage setting value x set ratio in the register
(Refer to section "*13. OUTSET setting"* for LDO Output Voltage setting.)

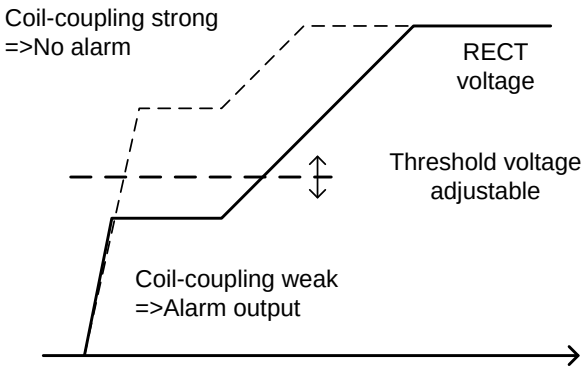


Figure 7. Detection of Position Gap

POSSET setting register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
POS_GAP_LV_SET	0x6A	[7:4] Reserved [3:0] POS_GAP_LV_SET Set the V_{THPOS} voltage. 0x0: OUTSET*(Note 1)* x40 % 0x1: OUTSET*(Note 1)* x45 % 0x2: OUTSET*(Note 1)* x50 % 0x3: OUTSET*(Note 1)* x55 % 0x4: OUTSET*(Note 1)* x60 % 0x5: OUTSET*(Note 1)* x65 % 0x6: OUTSET*(Note 1)* x70 % 0x7: OUTSET*(Note 1)* x75 % 0x8: OUTSET*(Note 1)* x80 % 0x9: OUTSET*(Note 1)* x85 % 0xA: OUTSET*(Note 1)* x90 % 0xB: OUTSET*(Note 1)* x95 % 0xC: OUTSET*(Note 1)* x100 % 0xD: OUTSET*(Note 1)* x105 % 0xE: OUTSET*(Note 1)* x110 % 0xF: OUTSET*(Note 1)* x115 %	0x00	R/W

(Note 1) LDO Output Voltage Setting.
Please set an initial value into Reserved bits.

Position Gap Detection setting register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
ALIGN_DET_EN	0x67	[7:1] Reserved [0] ALIGN_DET_EN_WAKEUP Position Gap Detection Function Enable (during start up) 0x0: disable 0x1: enable	0x00	R/W

Please set an initial value into Reserved bits.

Description of Blocks - continued

13. OUTPUT Voltage Setting

The Output voltage of the OUT pin could be set by the resistance connected to the OUTSET pin or the register shown below. (The OUTSET pin = BPPSET, EPPSET, PMASET)

OUT Pin Output Voltage [V]	R_{OUTSET} [kΩ]
OUTSET_SET register setting	OPEN or 470
12	120
11	75
10	56
9	43
7	36
6	30
5.3	24
5	20

The used resistance should have accuracy of ±1 %.

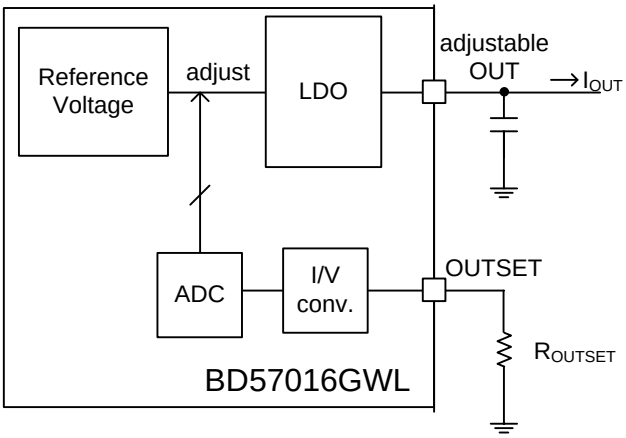


Figure 8. OUTSET Setting

When the OUTSET pin is set to OPEN or the bit [7] of the following register is set to "1", the output voltage of the OUT pin can be set through the following register (0x00,0x02,0x04). If the bit [7] of this register is set to "1", the setting of register has priority regardless of the resistance connected to the OUTSET pin. Additionally, the related states on the OUTSET pin can be confirmed depending on the next register (0x01, 0x03, 0x05).

OUTSET setting register (For Qi BPP)

Register Name	Address	Bit [7:0]	Initial Value	R/W
BPPSET_SET	0x00	[7] BPPSET_REG_EN 0x0: If the OUTSET pin is not OPEN, the setting of this register (bit [2:0]) is invalid. 0x1: The setting of this register (bit [2:0]) is valid forcibly. [6:3] Reserved [2:0] BPPSET Set the LDO output voltage. 0x0: 5.0 V 0x4: 9.0 V 0x1: 5.3 V 0x5: 10.0 V 0x2: 6.0 V 0x6: 11.0 V 0x3: 7.0 V 0x7: 12.0 V	0x00	R/W
BPPSET_STATE	0x01	OUTSET status [7] BPPSET_SHORT_DET Short detection of the OUTSET pin. 0x0: not short 0x1: short (Send the EPT In the case of Qi) [6:4] BPPSET_ADC_VAL Set LDO output voltage on the read value of A/D 0x0 when the read value in A/D is outside the setting range. 0x0: 5.0 V 0x4: 9.0 V 0x1: 5.3 V 0x5: 10.0 V 0x2: 6.0 V 0x6: 11.0 V 0x3: 7.0 V 0x7: 12.0 V [3] BPPSET_OPEN_DET Enable / Disable of the register setting 0x0: disable 0x1: enable (make the OUTSET pin OPEN to enable this) [2:0] BPPSET_OUTPUT Actual LDO output voltage to be used 0x0: 5.0 V 0x4: 9.0 V 0x1: 5.3 V 0x5: 10.0 V 0x2: 6.0 V 0x6: 11.0 V 0x3: 7.0 V 0x7: 12.0 V	0x00	R

Please set an initial value into Reserved bits.

13. OUTPUT Voltage Setting - continued

OUTSET setting register (For Qi EPP)

Register Name	Address	Bit [7:0]	Initial Value	R/W
EPPSET_SET	0x02	[7] EPPSET_REG_EN 0x0: If the OUTSET pin is not OPEN, the setting of this register (bit [2:0]) is invalid. 0x1: The setting of this register (bit [2:0]) is valid forcibly. [6:3] Reserved [2:0] EPPSET Set the LDO output voltage. 0x0: 5.0 V 0x4: 9.0 V 0x1: 5.3 V 0x5: 10.0 V 0x2: 6.0 V 0x6: 11.0 V 0x3: 7.0 V 0x7: 12.0 V	0x04	R/W
EPPSET_STATE	0x03	OUTSET status [7] EPPSET_SHORT_DET Short detection of the OUTSET pin. 0x0: not short 0x1: short (EPP mode off) [6:4] EPPSET_ADC_VAL Set LDO output voltage on the read value of A/D 0x0 when the read value in A/D is outside the setting range. 0x0: 5.0 V 0x4: 9.0 V 0x1: 5.3 V 0x5: 10.0 V 0x2: 6.0 V 0x6: 11.0 V 0x3: 7.0 V 0x7: 12.0 V [3] EPPSET_OPEN_DET Enable / Disable of the register setting 0x0: disable 0x1: enable (make the OUTSET pin OPEN to enable this) [2:0] EPPSET_OUTPUT Actual LDO output voltage to be used 0x0: 5.0 V 0x4: 9.0 V 0x1: 5.3 V 0x5: 10.0 V 0x2: 6.0 V 0x6: 11.0 V 0x3: 7.0 V 0x7: 12.0 V	0x00	R

Please set an initial value into Reserved bits.

13. OUTPUT Voltage Setting - continued

OUTSET setting register (For PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
PMASET_SET	0x04	[7] PMASET_REG_EN 0x0: If the OUTSET pin is not OPEN, the setting of this register (bit [2:0]) is invalid. 0x1: The setting of this register (bit [2:0]) is valid forcibly. [6:3] Reserved [2:0] PMASET Set the LDO output voltage. 0x0: 5.0 V 0x4: 9.0 V 0x1: 5.3 V 0x5: 10.0 V 0x2: 6.0 V 0x6: 11.0 V 0x3: 7.0 V 0x7: 12.0 V	0x00	R/W
PMASET_STATE	0x05	OUTSET status [7] PMASET_SHORT_DET Short detection of the OUTSET pin. 0x0: not short 0x1: short (Send the EOC In the case of PMA) [6:4] PMASET_ADC_VAL Set LDO output voltage on the read value of A/D 0x0 when the read value in A/D is outside the setting range. 0x0: 5.0 V 0x4: 9.0 V 0x1: 5.3 V 0x5: 10.0 V 0x2: 6.0 V 0x6: 11.0 V 0x3: 7.0 V 0x7: 12.0 V [3] PMASET_OPEN_DET Enable / Disable of the register setting 0x0: disable 0x1: enable (make the OUTSET pin OPEN to enable this) [2:0] PMASET_OUTPUT Actual LDO output voltage to be used 0x0: 5.0 V 0x4: 9.0 V 0x1: 5.3 V 0x5: 10.0 V 0x2: 6.0 V 0x6: 11.0 V 0x3: 7.0 V 0x7: 12.0 V	0x00	R

Please set an initial value into Reserved bits.

Description of Blocks - continued

14. NTC Setting

Connect the recommended NTC thermistor to the NTC pin when detecting abnormal temperature as described by the PMA standard. An EOC signal will be sent to the Transmitter in the PMA mode when voltage in the NTC pin is higher than the threshold V_{NTC0} set in NTC setting register (0x0A). The abnormal temperature detection in NTC is not available in Qi mode.

In addition to using the NTC thermistor, the EOC signal can also be sent by using the CTRL pin when temperature is monitored. Refer to section "*7. External Control Input (EN1, EN2, and CTRL)*" for the details. (Common to both PMA and Qi modes.)

The V_{NTC0} threshold can be defined in the following expressions.

$$V_{NTC0} = \frac{V_{REF\_NTC}}{R_{NTC}} \times R_{NTC0}$$
$$= \frac{25000^{(Note\ 2)}}{R_{NTC}} \text{ [V]}$$

(Note 2) Precision includes variation of 21250 to 28750.

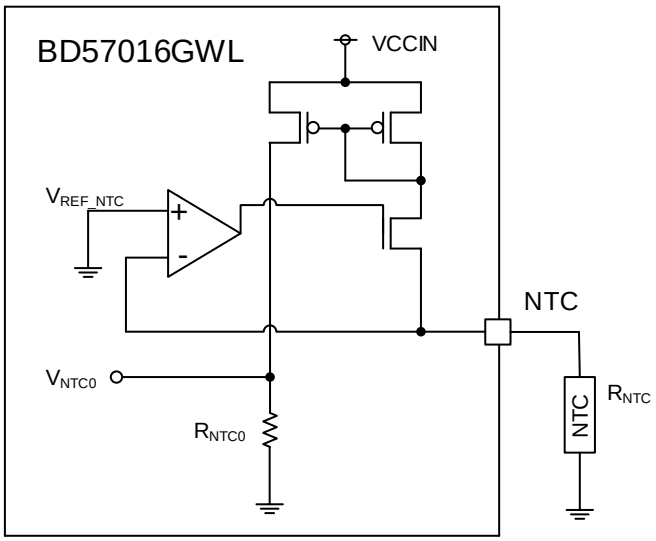


Figure 9. NTC Setting

14. NTC Setting - continued

NTC setting register

Register Name	Address	Bit [7:0]	Initial Value	R/W
NTC_SET	0x0A	[7] NTC_EN_QI (Qi mode) with/without the NTC temperature detection function 0x0: disabled 0x1: enabled [6] NTC_EN_PMA (PMA mode) with/without the NTC temperature detection function 0x0: disabled 0x1: enabled [5:4] Reserved [3:0] NTC_TH V_{NTC0} threshold setting for the abnormal temperature detection (Judge as abnormal if more than V_{NTC0} is detected) 0x0: more than 0.5 V 0x8: more than 1.3 V 0x1: more than 0.6 V 0x9: more than 1.4 V 0x2: more than 0.7 V 0xA: more than 1.5 V 0x3: more than 0.8 V 0xB: more than 1.6 V 0x4: more than 0.9 V 0xC: more than 1.7 V 0x5: more than 1.0 V 0xD: more than 1.8 V 0x6: more than 1.1 V 0xE: more than 1.9 V 0x7: more than 1.2 V 0xF: more than 2.0 V	0xC4	R/W
NTC_STATE	0X0B	[7:1] Reserved [0] NTC_DET Abnormal temperature detection for NTC. 0x0: Abnormal temperature undetected 0x1: Abnormal temperature detected	0x00	R

Please set an initial value into Reserved bits.

The recommended NTC thermistor is NCP15WF104F03RC (MURATA Co., Ltd.).

Resistance value (25 °C)	100 kΩ
Resistance value (25 °C) tolerance	±1 %
B constant (25 °C /50 °C)	4250 K
B constant (25 °C /50 °C) tolerance	±1 %
B constant (25 °C /85 °C) (Typ)	4311 K

Description of Blocks - continued

15. PAD_DETECTION

Regarding the PAD_DETECTION function, it can send a signal to the host when Receiver is removed from the Transmitter after the charging was completed. To use this function, connect the external power supply to the VCCPD, put a pull-up resistance in PD then connect to the VCC.
The host can detect when the PD signal changes from L to H to monitor if it was removed from the charger.

The flow to the detection

1. After stopping the charging, RX receives Digital Ping or Analog Ping signal from TX. (AC2 of figure below)
2. RX accumulates an electric charge to a capacitor connected to the PD_TIME pin using that pulse. (It's judged that RX is still put on TX during this pulse exist.)
3. If RX is removed from TX the pulse to AC2 is not generated, so the signal of the PD pin reverse after period of CR time constant.

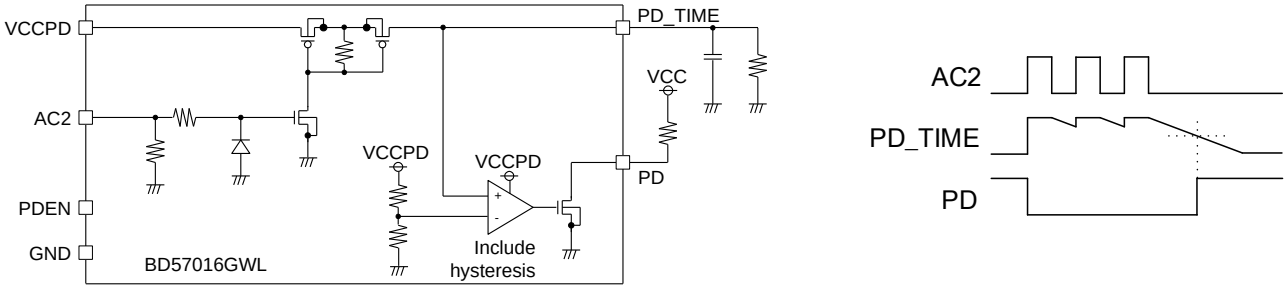


Figure 10. PAD_DETECTION

Description of Blocks - continued

16. Interrupt Control Block

The circuit for Interruption Generation is shown below.
This circuit detects the edge of the interrupt signal. An interrupt is sent on the INTB pin depending on the events triggering the interrupt as set by the Interrupt Mask register. INTB is active L.

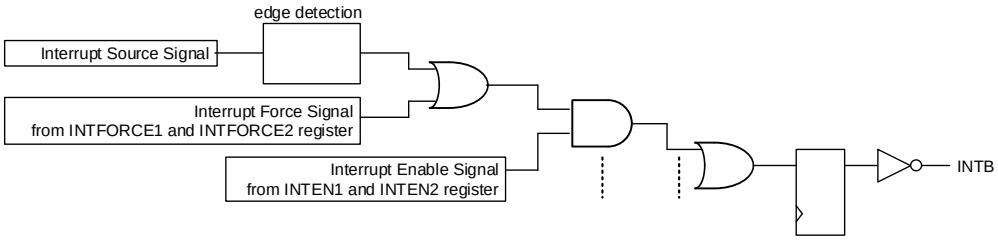


Figure 11. Interrupt Circuit Generation

16.1 Interrupt Control Register

The generation of interruption for each can be controlled by this register. If a bit is set to 1, the corresponding interrupt event will be enabled, if it is set to 0, it will be disabled. The interrupt is disabled by default.

Interrupt Control register 1 (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
INTEN1	0x10	[7:6] Reserved [5] INT_EN_PMA_EOC_QI_EPT PMA EOC/QI_EPT interrupt detection activation setting [4:1] Reserved [0] INT_EN_CHG_START_DET Charging start interrupt detection activation setting	0x00	R/W

Please set an initial value into Reserved bits.

Interrupt Control register 2 (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
INTEN2	0x11	[7:2] Reserved [1] INT_EN_ERR_POSSET_CLR Clear POSSET Error interrupt detection activation setting (During start up) [0] INT_EN_ERR_POSSET POSSET Error interrupt detection activation setting (During start up)	0x00	R/W

Please set an initial value into Reserved bits.

16.2 Interrupt Status Register

It can be checked what kind of event caused an interrupt by checking this register. In order to clear the interrupt event, refer to section "*16.3 Clear Interrupt Register*".

Interrupt Status register 1 (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
INTSTAT1	0x12	[7:6] Reserved [5] INT_PMA_EOC_QI_EPT PMA EOC/QI_EPT interrupt detection [4:1] Reserved [0] INT_CHG_START_DET Charging start interrupt detection	0x00	R

Reserved bits read "0"

Interrupt Status register 2 (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
INTSTAT2	0x13	[7:2] Reserved [1] INT_ERR_POSSET_CLR Clear POSSET Error interrupt detection (During start up) [0] INT_ERR_POSSET POSSET Error interrupt detection (During start up)	0x00	R

Reserved bits read "0"

16. Interrupt Control Block - continued

16.3 Clear Interrupt Register

The interrupt status register is used to clear the interrupt. It can clear every interrupt.
Each interrupt will be cleared by entering “1” to each bit and wait for the detection of the next interrupt.
Please re-enter “0” after resetting with “1”, so the device can detect the next events for interrupt.

Clear Interrupt register 1 (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
INTCLR1	0x14	[7:6] Reserved [5] INT_CLR_PMA_EOC_QI_EPT PMA EOC/QI_EPT interrupt detection cleared [4:1] Reserved [0] INT_CLR_CHG_START_DET Charging start interrupt detection cleared	0x00	R/W

Please set an initial value into Reserved bits.

Clear Interrupt register 2 (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
INTCLR2	0x15	[7:2] Reserved [1] INT_CLR_ERR_POSSET_CLR Clear POSSET Error interrupt detection cleared (During start up) [0] INT_CLR_ERR_POSSET POSSET Error interrupt detection cleared (During start up)	0x00	R/W

Please set an initial value into Reserved bits.

16.4 Forced Interrupt Generation Register.

This register can force generation of an interrupt caused by any of the events. Interrupt is generated by writing 1 in each bit. After writing 1, please always write 0.

Forced Interrupt Generation register 1 (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
INTFORCE1	0x16	[7:6] Reserved [5] INT_FORCE15 [4:1] Reserved [0] INT_FORCE10	0x00	R/W

Please set an initial value into Reserved bits.

Forced Interrupt Generation register 2 (For Qi and PMA)

INTFORCE2	0x17	[7:2] Reserved [1] INT_FORCE21 [0] INT_FORCE20	0x00	R/W

Please set an initial value into Reserved bits.

Description of Blocks - continued

17. Received Power Monitor Register

The Received Power value that BD57016GWL received from TX can be monitor with this register. This value is the value of Received Power Packet to TX or the value of the Received Power calculated regularly internally to the BD57016GWL.

Received power monitor register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
RP16VAL_B0	0x53	[7:0] RP_VAL[15:8] Received Power Value (Upper 8 bits)	0x00	R
RP16VAL_B1	0x54	[7:0] RP_VAL[7:0] Received Power Value (Lower 8 bits)	0x00	R

During the Qi BPP mode, 8bit of 0x53 is used as Received Power Packet.

18. Charge Frequency Monitor Register

It can monitor the Carrier Frequency from TX. However, it may not be able to monitor correctly the Carrier Frequency when the rectified voltage waveform is disturbed.

Calculation Method:
RP_FREQ = 8192 ÷ ((Received Frequency value) ÷ 64) [kHz]
(Calculate Received Frequency Value using Decimal number.)

Charge Frequency Monitor register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
RPFREQ_B0	0x57	[7:5] Reserved [4:0] RP_FREQ[12:8] Received Frequency Value (Upper 5 bits)	0x00	R
RPFREQ_B1	0x58	[7:0] RP_FREQ[7:0] Received Frequency Value (Lower 8 bits)	0x00	R

Reserved reads “0”

19. Control Error Packet Monitor Register

In Qi mode, the received power can be controlled by sending the Control Error Packet (CE) form RX to TX. The value of CE sent by RX can be monitored.

CE Monitor register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
CE_VAL	0x50	[7:0] CE_VAL[7:0] Control Error Packet Value	0x00	R

20. Signal Strength Packet Monitor Register

In Qi mode, it sends the Signal Strength value that shows in the strength of connection to TX side during the start up. This register can monitor the sent SS value by RX.

SS Monitor register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
SS_VAL	0x4F	[7:0] SS_VAL[7:0] Signal Strength Packet Value	0x00	R

Description of Blocks - continued

21. GPIO

BD57016GWL is equipped with the GPIO1, GPIO2 and GPIO3 pins. Because they can be used as input or output, they can be used either to monitor the input or to output data.

21.1 GPIO Input register

It can check the input condition of the GPIO1, GPIO2 and GPIO3 pins. If the read value is 1, the input condition of each pin is high. If it is 0, the input condition is Low.

GPIO Input register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
GPODIN	0x90	[7:3] Reserved [2] GPIO3_DAT_IN GPIO3 pin input condition [1] GPIO2_DAT_IN GPIO2 pin input condition [0] GPIO1_DAT_IN GPIO1 pin input condition	XX	R

Initial value is undefined value.

21.2 GPIO Output Register

It can check the output condition of the GPIO1, GPIO2 and GPIO3 pins. When setting 1, the output of GPIO is 1. And when setting 0, the output is 0. It is necessary to set the output mode in the GPIO I/O switching register.

GPIO Output register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
GPODOUT	0x91	[7:3] Reserved [2] GPIO3_DAT_OUT GPIO3 pin Output value setting 0x0: output “0” 0x1: output “1” [1] GPIO2_DAT_OUT GPIO2 pin Output value setting 0x0: output “0” 0x1: output “1” [0] GPIO1_DAT_OUT GPIO1 pin Output value setting 0x0: output “0” 0x1: output “1”	0x00	R/W

Please set an initial value into Reserved bits.

21.3 GPIO I/O switching register

It can set the pin I/O direction of the GPIO1, GPIO2 and GPIO3 pins. When setting 1, it will be in output mode, and when setting 0, it will be in the input mode.

GPIO I/O switching register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
GPODIR	0x92	[7:3] Reserved [2] GPIO3_DIR GPIO3 pin Input / Output setting 0x0: input mode 0x1: output mode [1] GPIO2_DIR GPIO2 pin Input / Output setting 0x0: input mode 0x1: output mode [0] GPIO1_DIR GPIO1 pin Input / Output setting 0x0: input mode 0x1: output mode	0x07	R/W

Please set an initial value into Reserved bits.

21. GPIO - continued

21.4 GPIO Pull Up/Down Resistance Control Register

In GPIO, pull up resistance/ Pull down resistance can be added internally. This register controls whether these resistances are connected or disconnected internally. When setting 1, it will connect the pull up or pull down resistance and when setting 0, it will disconnect pull up or pull down resistance.

GPIO Pull Up/Down Resistance Control register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
GPOPUL	0x93	[7] Reserved [6] GPIO3_PD GPIO3 Pull down resistance setting 0x0: OFF 0x1: ON [5] GPIO2_PD GPIO2 Pull down resistance setting 0x0: OFF 0x1: ON [4] GPIO1_PD GPIO1 Pull down resistance setting 0x0: OFF 0x1: ON [3] Reserved [2] GPIO3_PU GPIO3 Pull up resistance setting 0x0: OFF 0x1: ON [1] GPIO2_PU GPIO2 Pull up resistance setting 0x0: OFF 0x1: ON [0] GPIO1_PU GPIO1 Pull up resistance setting 0x0: OFF 0x1: ON	0x00	R/W

Please set an initial value into Reserved bits.

21.5 GPIO Function Selection register

It can set the function of the GPIO. Always set 0 for normal use.

GPIO Function Selection register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
GPOFUNC	0x94	[7:3] Reserved [2] GPIO3_FUNC_SEL GPIO3 pin function setting 0x0: output the value set with GPIO Output register(0x91) 0x1: output the internal monitor signal set with GPIO3 Internal Signal Monitor Selection register(0x97) [1] GPIO2_FUNC_SEL GPIO2 pin function setting 0x0: output the value set with GPIO Output register(0x91) 0x1: output the internal monitor signal set with GPIO2 Internal Signal Monitor Selection register(0x96) [0] GPIO1_FUNC_SEL GPIO1 pin function setting 0x0: output the value set with GPIO Output register(0x91) 0x1: output the internal monitor signal set with GPIO1 Internal Signal Monitor Selection register(0x95)	0x07	R/W

Please set an initial value into Reserved bits.

21. GPIO - continued

21.6 GPIO Internal Signal Monitor Selection Register

Always set to 0 for normal use.

GPIO1 Internal Signal Monitor Selection register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
GPOSEL1	0x95	[7:6] Reserved [5:0] GPIO1_DAT_SEL GPIO1 Internal monitor selection	0x00	R/W

Please set an initial value into Reserved bits.

GPIO2 Internal Signal Monitor Selection register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
GPOSEL2	0x96	[7:6] Reserved [5:0] GPIO2_DAT_SEL GPIO2 Internal monitor selection	0x00	R/W

Please set an initial value into Reserved bits.

GPIO3 Internal Signal Monitor Selection register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
GPOSEL3	0x97	[7:6] Reserved [5:0] GPIO3_DAT_SEL GPIO3 Internal monitor selection	0x00	R/W

Please set an initial value into Reserved bits.

22. REVISION Register

It contains the chip revision and the vendor ID of LSI.

REVISION register (For Qi and PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
CHIP_ID	0xDF	[7:4] CHIP_NO [3:0] Vendor ID [3:0] REV [3:0] Chip Revision	0x13	R

Description of Blocks - continued

23. Qi ID Register

It contains the Manufacture Code and compliant version / device ID used in the Qi mode.

Qi Major version & Minor Version register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
RX_ID_B0	0x79	[7:4] MAJOR_VER [3:0] Based on the Major Version of the Qi standard [3:0] MINOR_VER [3:0] Based on the Minor Version of the Qi standard	0x12	R

Qi Manufacture Code Register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
RX_ID_B1	0x7A	[7:0] MNFCT_CODE [15:8] Manufacture Code (Identification packet B1)	0x00	R/W
RX_ID_B2	0x7B	[7:0] MNFCT_CODE [7:0] Manufacture Code (Identification packet B2)	0x27	R/W
RX_ID_B3	0x7C	[7] EXT [6:0] DEVICE_ID [30:24] Device ID (Identification packet B3)	0x16	R/W

The code of 0x27 is the Manufacture Code assigned to ROHM by WPC.
Please do not set the code other than 0x27.

24. PMA ID Register

It contains the OUI and RX Serial Number specified by IEEE and used in PMA standard. The PMA Manufacture Code register and the PMA RX Model Number register will be enabled by setting bit0 of PMA ID Write Enable setting register to 1. In that case, the written value will be used as PMA ID.

PMA Manufacture Code register (Only for PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
MAC_ID_3	0x19	[7:0] MAC_EXT_ID [23:16]	XX	R/W
MAC_ID_2	0x1A	[7:0] MAC_EXT_ID [15:8]	XX	R/W
MAC_ID_1	0x1B	[7:0] MAC_EXT_ID [7:0]	XX	R/W

Initial value is undefined value.

PMA RX Model Number register (Only for PMA)

Register Name	Address	Bit [7:0]	Initial Value	R/W
MAC_OUI_3	0x1C	[7:0] MAC_OUI [23:16]	XX	R/W
MAC_OUI_2	0x1D	[7:0] MAC_OUI [15:8]	XX	R/W
MAC_OUI_1	0x1E	[7:0] MAC_OUI [7:0]	XX	R/W

Initial value is undefined value.

PMA ID Write Enable setting register (Only for PMA)

Register Name	Address	Bit[7:0]	Initial Value	R/W
MAC_OUI_ID_EN	0x1F	[7:1] Reserved [0] MAC_OUI_EN Enable the register value of 0x19 to 0x1E 0x0: Disable 0x01: Enable	0x08	R/W

Please set an initial value into Reserved bits.

Description of Blocks - continued

25. QI CONFIG Register

The parameter of FSK defined in Qi spec can be changed or confirmed with the register below.

Qi CONFIG register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
RX_CONF_B4	0x7F	[7:5] Reserved [4] NEG Request for proceeding to the Negotiation phase 0x0: Not request 0x1: Request [3] FSK_POL Polarity of FSK of TX 0x0: positive (frequency modulation to higher frequency) 0x1: negative (frequency modulation to lower frequency) [2] Reserved [1:0] FSK_DEPTH Modulation depth of FSK of TX 0x0: Minimum depth 0x3: Maximum depth	0x03	R/W

Please set an initial value into Reserved bits.

26. QI TXID Register

TXID can be read from following register.

Qi TXID register (Only for Qi)

Register Name	Address	Bit [7:0]	Initial Value	R/W
TXID_B0	0x5F	[7:4] TX_MAJOR_VERSION Indicate TX's major version [3:0] TX_MINOR_VERSION Indicate TX's minor version	0x00	R
TXID_B1	0x60	[7:0] TX_MNFCT_CODE[15:8] Indication of TX's Manufacturer Code (Upper 8 bits)	0x00	R
TXDI_B2	0x61	[7:0] TX_MNFCT_CODE[7:0] Indication of TX's Manufacturer Code (Lower 8 bits)	0x00	R

Description of Blocks - continued

27. Command Interface

27.1 Command Interface

The BD57016GWL uses I²C bus method to communicate with host CPU. Most registers of the BD57016GWL can be written in or read out. BD57016GWL has Slave Address of 0x44(7 bit). A Select Address is necessary after a Slave Address for read or write action. The format of the I²C bus method slave mode is shown below.

S	Slave Address	A	Select Address	A	Data	A	Data	A	P

S: Start Condition
Slave Address: Send a total of 8bit data, put bit of the read mode (H") or write mode (L") after the slave address (7 bit) that was set in the ADDR. (MSB first)
A: Add acknowledge bit in each byte in the acknowledged data sent/received.
If the data was sent/received correctly, this acknowledge bit will be "L".
If "H" was sent/received, it means that it didn't acknowledge the data.
Select Address: Use 1 byte to select the register address in BD57016GWL (MSB first)
Data: Byte data, Data sent/received (MSB first)
P: Stop Condition

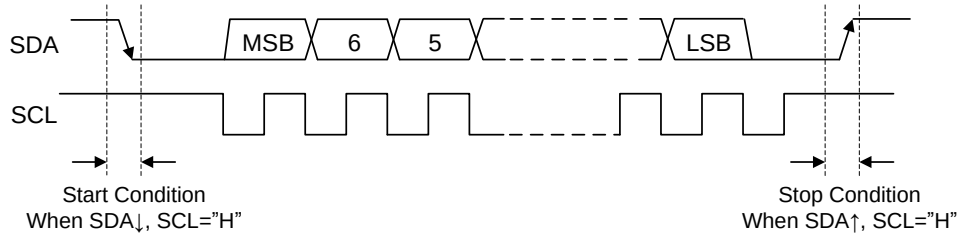


Figure 12. Command Interface

Following is the repeated start condition. By using the condition, new sequence can be started without slave address. Do not use the repeated start condition in an irregular timing during the communication.

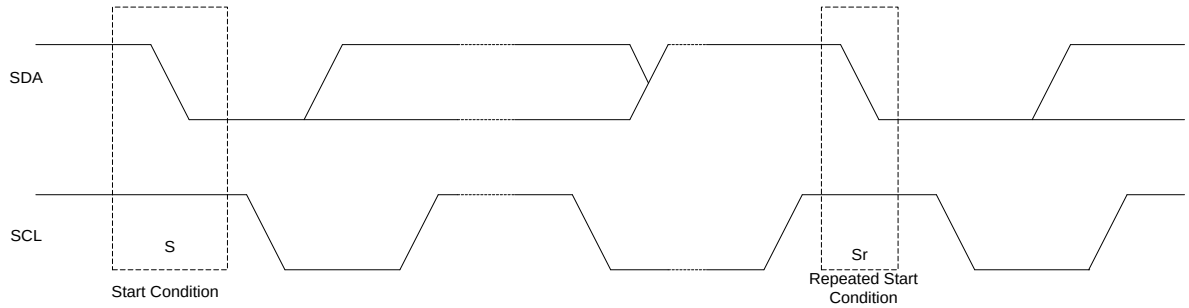


Figure 13. Repeated Start Condition

27. Command Interface - continued

27.2 Data Format

Write format

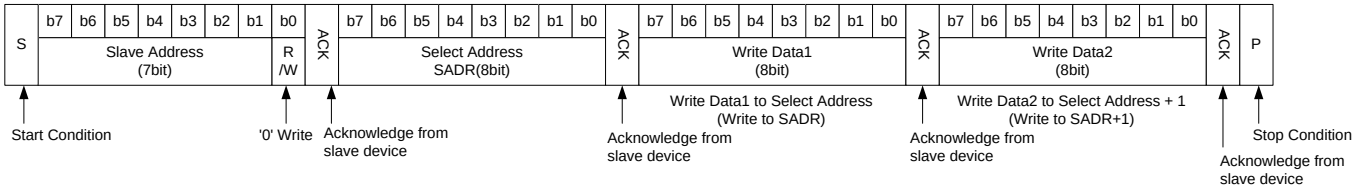


Figure 14. Write Data Format

Read format (In case of reading from the Select Address for 0x00)

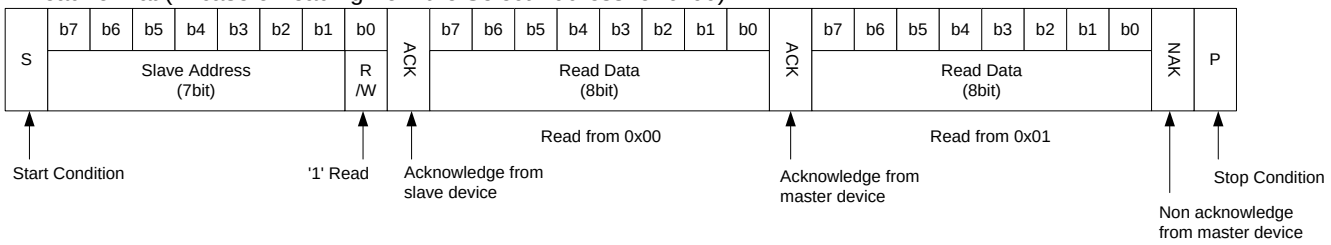


Figure 15. Read Data Format

Read Data from specified Select Address

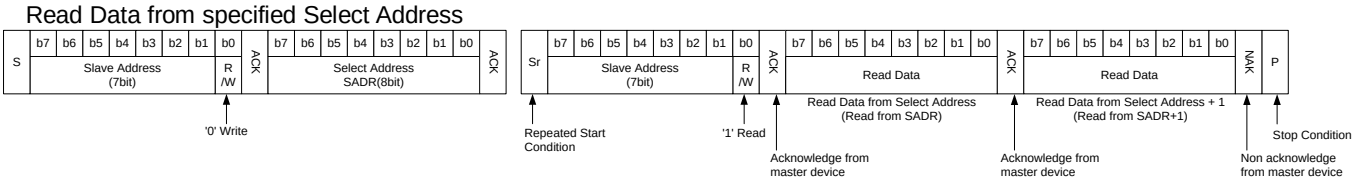


Figure 16. Read Data from Specified Select Address (1)

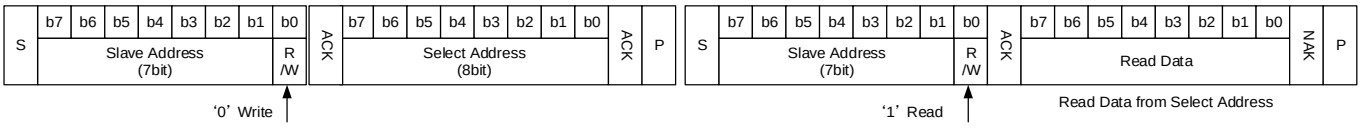


Figure 17. Read Data from Specified Select Address (2)

27. Command Interface - continued

27.3 Control Signal Specification

Electric Specification/ Timing of bus line or I/O stage

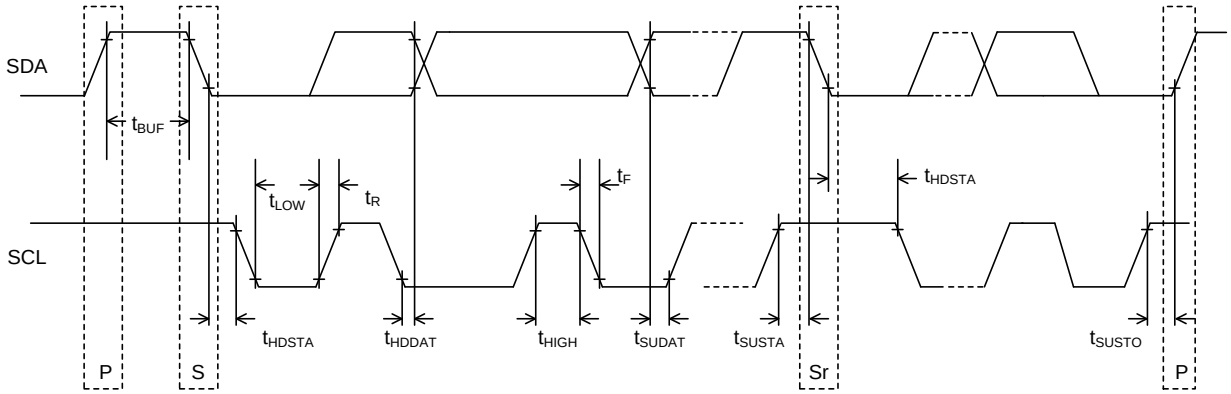


Figure 18 Timing Chart

Table 1. SDA/SCL Bus Line Feature (unless otherwise specified Ta=25 °C, VCC=3.0 V)

Parameter		Symbol	High Speed Mode		Unit
			Min	Max	
1	SCL Clock Frequency	f_{SCL}	0	400	kHz
2	Bus Free Time between “Stop” Condition and “Start” Condition	t_{BUF}	1.3	-	µs
3	Hold Time (Re-transmit) “Start” Condition. After This Period, The First Clock Pulse is Being Generated.	t_{HDSTA}	0.6	-	µs
4	LOW Condition Holding Time of SCL Clock	t_{LOW}	1.3	-	µs
5	HIGH Condition Holding Time of SCL Clock	t_{HIGH}	0.6	-	µs
6	Set-up Time of Re-transmit “Start” Condition	t_{SUSTA}	0.6	-	µs
7	Data Hold Time	t_{HDDAT}	0	-	µs
8	Data Set-up Time	t_{SUDAT}	100	-	ns
9	Start up Time of SDA/SCL Signal	t_R	$20+0.1C_B$	300	ns
10	Fall Time of SDA/SCL Signal	t_F	$20+0.1C_B$	300	ns
11	Set-up Time of “stop” Condition	t_{SUSTO}	0.6	-	µs
12	Load Capacity of Each Bus Line	C_B	-	400	pF

The values written above depend on the values V_{IHSDA}, V_{ILSDA}, V_{IHSCL} and V_{ILSCL}.

Description of Blocks - continued

28. Register Map

Register Name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial Value	R/W
BPPSET_SET	00	BPPSET_REG_EN	Reserved					BPPSET[2:0]		00	R/W
BPPSET_STATE	01	BPPSET_SHORT_DET	BPPSET_ADC_VAL[2:0]			BPPSET_OPEN_DET	BPPSET_OUTPUT[2:0]			00	R
EPPSET_SET	02	EPPSET_REG_EN	Reserved					EPPSET[2:0]		04	R/W
EPPSET_STATE	03	EPPSET_SHORT_DET	EPPSET_ADC_VAL[2:0]			EPPSET_OPEN_DET	EPPSET_OUTPUT[2:0]			00	R
PMASET_SET	04	PMASET_REG_EN	Reserved					PMASET[2:0]		00	R/W
PMASET_STATE	05	PMASET_SHORT_DET	PMASET_ADC_VAL[2:0]			PMASET_OPEN_DET	PMASET_OUTPUT[2:0]			00	R
ILIM1_SET	06	ILIM1_REG_EN	Reserved	ILIM1_SET_VAL[5:0]						11	R/W
ILIM1_STATE	07	ILIM1_SHORT_DET	ILIM1_ADC_VAL[2:0]			ILIM1_OPEN_DET	Reserved			00	R
ILIM2_SET	08	ILIM2_REG_EN	Reserved	ILIM2_SET_VAL[5:0]						11	R/W
ILIM2_STATE	09	ILIM2_SHORT_DET	ILIM2_ADC_VAL[2:0]			ILIM2_OPEN_DET	Reserved			00	R
NTC_SET	0A	NTC_EN_QI	NTC_EN_PMA	Reserved		NTC_TH[3:0]				C4	R/W
NTC_STATE	0B	Reserved							NTC_DET	00	R
-	0C	Reserved								00	-
-	0D	Reserved								00	-
EPT_CODE	0E	EPT_CODE[7:0]								FF	R
EOC_WR	0F	EOC_TEMP	EOC_NO_LOAD	EOC_FULL_CHARGE	OUT_UVLO	EOC_CTRL	EOC_TSD	EOC_EN1	EOC_ADP_DET	00	R
INTEN1	10	Reserved		INT_EN_PMA_EOC_QI_EPT	Reserved				INT_EN_CHG_START_DET	00	R/W
INTEN2	11	Reserved						INT_EN_ERR_POSSET_CLR	INT_EN_ERR_POSSET	00	R/W
INTSTAT1	12	Reserved		INT_PMA_EOC_QI_EPT	Reserved				INT_CHG_START_DET	00	R
INTSTAT2	13	Reserved						INT_ERR_POSSET_CLR	INT_ERR_POSSET	00	R
INTCLR1	14	Reserved		INT_CLR_PMA_EOC_QI_EPT	Reserved				INT_CLR_CHG_START_DET	00	R/W
INTCLR2	15	Reserved						INT_CLR_ERR_POSSET_CLR	INT_CLR_ERR_POSSET	00	R/W
INTFORCE1	16	Reserved		INT_FORCE15	Reserved				INT_FORCE10	00	R/W
INTFORCE2	17	Reserved						INT_FORCE21	INT_FORCE20	00	R/W
-	18	Reserved								00	-
MAC_ID_3	19	MAC_EXT_ID[23:16]								XX	R/W
MAC_ID_2	1A	MAC_EXT_ID[15:8]								XX	R/W
MAC_ID_1	1B	MAC_EXT_ID[7:0]								XX	R/W
MAC_OUI_3	1C	MAC_OUI[23:16]								XX	R/W
MAC_OUI_2	1D	MAC_OUI[15:8]								XX	R/W
MAC_OUI_1	1E	MAC_OUI[7:0]								XX	R/W
MAC_OUI_ID_EN	1F	Reserved							MAC_OUI_EN	08	R/W
FOD1_BPP_SET	20	FOD1B_REG_EN	FOD1B_POLARITY	Reserved	FOD1B[4:0]					00	R/W
FOD1_BPP_STATE	21	FOD1B_SHORT_DET	FOD1B_ADC_VAL[3:0]				FOD1B_OPEN_DET	Reserved		00	R
FOD1_EPP_SET	22	FOD1E_REG_EN	FOD1E_POLARITY	Reserved	FOD1E[4:0]					00	R/W
FOD1_EPP_STATE	23	FOD1E_SHORT_DET	FOD1E_ADC_VAL[3:0]				FOD1E_OPEN_DET	Reserved		00	R
FOD2_BPP_SET	24	FOD2B_REG_EN	Reserved	FOD2B[5:0]						07	R/W
FOD2_BPP_STATE	25	FOD2B_SHORT_DET	FOD2B_ADC_VAL[3:0]				FOD2B_OPEN_DET	Reserved		00	R
FOD2_EPP_SET	26	FOD2E_REG_EN	Reserved	FOD2E[5:0]						07	R/W
FOD2_EPP_STATE	27	FOD2E_SHORT_DET	FOD2E_ADC_VAL[3:0]				FOD2E_OPEN_DET	Reserved		00	R
-	28	Reserved								41	-
-	29	Reserved								41	-
-	2A	Reserved								00	-
-	2B	Reserved								05	-
FOD_S_PCKT_EN	2C	Reserved							SEL_QFOD_DATA	00	R/W
-	2D	Reserved								22	-
FOD_S_PCKT_0	2E	FOD_PCKT_B1[7:0]								00	R/W
-	2F	Reserved								00	-
-	30	Reserved								00	-
-	31	Reserved								00	-
-	32	Reserved								80	-
-	33	Reserved								00	-
-	34	Reserved								00	-
-	35	Reserved								00	-
-	36	Reserved								00	-
-	37	Reserved								00	-
-	38	Reserved								00	-
-	39	Reserved								00	-
-	3A	Reserved								00	-
-	3B	Reserved								00	-
-	3C	Reserved								00	-
-	3D	Reserved								00	-
-	3E	Reserved								00	-
-	3F	Reserved								00	-
-	40	Reserved								00	-
-	41	Reserved								00	-
-	42	Reserved								00	-
-	43	Reserved								00	-
-	44	Reserved								00	-
-	45	Reserved								00	-
-	46	Reserved								00	-
-	47	Reserved								00	-
-	48	Reserved								00	-
-	49	Reserved								00	-
-	4A	Reserved								00	-
-	4B	Reserved								00	-
-	4C	Reserved								00	-
-	4D	Reserved								00	-
-	4E	Reserved								00	-
SS_VAL	4F	SS_VAL[7:0]								00	R

Do not use “Reserved”. When it is necessary to access Reserved bits, please write in an initial value by all means.

28. Register Map – continued

Register Name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial Value	R/W
CE_VAL	50	CE_VAL[7:0]								00	R
-	51	Reserved								24	-
MONI_MODE	52	Reserved							POWER_MODE	00	R
RP16VAL_B0	53	RP_VAL[15:8]								00	R
RP16VAL_B1	54	RP_VAL[7:0]								00	R
-	55	Reserved								00	-
-	56	Reserved								00	-
RPFREQ_B0	57	Reserved			RP_FREQ[12:8]					00	R
RPFREQ_B1	58	RP_FREQ[7:0]								00	R
-	59	Reserved								00	-
-	5A	Reserved								00	-
-	5B	Reserved								00	-
-	5C	Reserved								00	-
-	5D	Reserved								00	-
-	5E	Reserved								00	-
TXID_B0	5F	TX_MAJOR_VERSION[3:0]				TX_MINOR_VERSION[3:0]				00	R
TXID_B1	60	TX_MNFCT_CODE[15:8]								00	R
TXID_B2	61	TX_MNFCT_CODE[7:0]								00	R
-	62	Reserved								0A	-
-	63	Reserved								00	-
-	64	Reserved								00	-
-	65	Reserved								00	-
-	66	Reserved								00	-
ALIGN_DET_EN	67	Reserved							ALIGN_DET_EN_WAKEUP	00	R/W
-	68	Reserved								00	-
-	69	Reserved								70	-
POS_GAP_LV_SET	6A	Reserved				POS_GAP_LV_SET[3:0]				00	R/W
-	6B	Reserved								00	-
-	6C	Reserved								00	-
-	6D	Reserved								00	-
-	6E	Reserved								00	-
-	6F	Reserved								00	-
-	70	Reserved								00	-
-	71	Reserved								00	-
-	72	Reserved								0A	-
-	73	Reserved								02	-
-	74	Reserved								0A	-
-	75	Reserved								0A	-
-	76	Reserved								0A	-
-	77	Reserved								0A	-
-	78	Reserved								04	-
RX_ID_B0	79	MAJOR_VER[3:0]				MINOR_VER[3:0]				12	R
RX_ID_B1	7A	MNFCT_CODE[15:8]								00	R/W
RX_ID_B2	7B	MNFCT_CODE[7:0]								27	R/W
RX_ID_B3	7C	EXT	DEVICE_ID[30:24]							16	R/W
-	7D	Reserved								0A	-
-	7E	Reserved								00	-
RX_CONF_B4	7F	Reserved			NEG	FSK_POL	Reserved	FSK_DEPTH[1:0]		03	R/W
EOC_MASK	80	Reserved				MASK_NO_LOAD	MASK_FULL	Reserved		0C	R/W
-	81	Reserved								21	-
-	82	Reserved								6C	-
MODE STATUS	83	Reserved	PMA_MODE	QI_MODE	MODE_DETECTION _ERROR	Reserved				00	R
-	84	Reserved								20	-
-	85	Reserved								EE	-
-	86	Reserved								00	-
-	87	Reserved								00	-
-	88	Reserved								00	-
-	89	Reserved								00	-
-	8A	Reserved								00	-
-	8B	Reserved								00	-
-	8C	Reserved								00	-
-	8D	Reserved								00	-
-	8E	Reserved								00	-
-	8F	Reserved								00	-

Do not use “Reserved”. When it is necessary to access Reserved bits, please write in an initial value by all means.

28. Register Map - continued

Register Name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial Value	R/W
GPODIN	90	Reserved					GPIO3_DAT_IN	GPIO2_DAT_IN	GPIO1_DAT_IN	XX	R
GPODOUT	91	Reserved					GPIO3_DAT_OUT	GPIO2_DAT_OUT	GPIO1_DAT_OUT	00	R/W
GPODIR	92	Reserved					GPIO3_DIR	GPIO2_DIR	GPIO1_DIR	07	R/W
GPOPUL	93	Reserved	GPIO3_PD	GPIO2_PD	GPIO1_PD	Reserved	GPIO3_PU	GPIO2_PU	GPIO1_PU	00	R/W
GPOFUNC	94	Reserved					GPIO3_FUNC_SEL	GPIO2_FUNC_SEL	GPIO1_FUNC_SEL	07	R/W
GPOSEL1	95	Reserved		GPIO1_DAT_SEL[5:0]						00	R/W
GPOSEL2	96	Reserved		GPIO2_DAT_SEL[5:0]						00	R/W
GPOSEL3	97	Reserved		GPIO3_DAT_SEL[5:0]						00	R/W
-	98	Reserved								00	-
-	99	Reserved								00	-
-	9A	Reserved								a9	-
-	9B	Reserved								05	-
-	9C	Reserved								05	-
-	9D	Reserved								00	-
-	9E	Reserved								00	-
-	9F	Reserved								00	-
-	A0	Reserved								19	-
-	A1	Reserved								C0	-
-	A2	Reserved								80	-
-	A3	Reserved								00	-
-	A4	Reserved								00	-
-	A5	Reserved								01	-
-	A6	Reserved								0F	-
-	A7	Reserved								03	-
-	A8	Reserved								01	-
-	A9	Reserved								00	-
-	AA	Reserved								00	-
-	AB	Reserved								00	-
-	AC	Reserved								00	-
-	AD	Reserved								00	-
-	AE	Reserved								00	-
-	AF	Reserved								00	-
-	B0	Reserved								00	-
-	B1	Reserved								00	-
-	B2	Reserved								00	-
-	B3	Reserved								07	-
-	B4	Reserved								00	-
-	B5	Reserved								00	-
-	B6	Reserved								00	-
-	B7	Reserved								00	-
-	B8	Reserved								00	-
-	B9	Reserved								00	-
-	BA	Reserved								00	-
-	BB	Reserved								00	-
-	BC	Reserved								00	-
-	BD	Reserved								00	-
-	BE	Reserved								00	-
-	BF	Reserved								00	-
-	C0	Reserved								00	-
-	C1	Reserved								00	-
-	C2	Reserved								00	-
-	C3	Reserved								00	-
-	C4	Reserved								00	-
-	C5	Reserved								00	-
-	C6	Reserved								00	-
-	C7	Reserved								00	-
-	C8	Reserved								00	-
-	C9	Reserved								00	-
-	CA	Reserved								00	-
-	CB	Reserved								00	-
-	CC	Reserved								00	-
-	CD	Reserved								00	-
-	CE	Reserved								00	-
-	CF	Reserved								00	-
-	D0	Reserved								00	-
-	D1	Reserved								00	-
-	D2	Reserved								00	-
-	D3	Reserved								00	-
-	D4	Reserved								00	-
-	D5	Reserved								00	-
-	D6	Reserved								00	-
-	D7	Reserved								00	-
-	D8	Reserved								00	-
-	D9	Reserved								00	-
-	DA	Reserved								00	-
-	DB	Reserved								00	-
-	DC	Reserved								00	-
-	DD	Reserved								00	-
-	DE	Reserved								00	-
CHIP_ID	DF	CHIP_NO[3:0]					REV[3:0]			13	R

Do not use “Reserved”. When it is necessary to access Reserved bits, please write in an initial value by all means.

Description of Blocks - continued

29. Application Circuit Example

29.1 Recommended Circuit Diagram

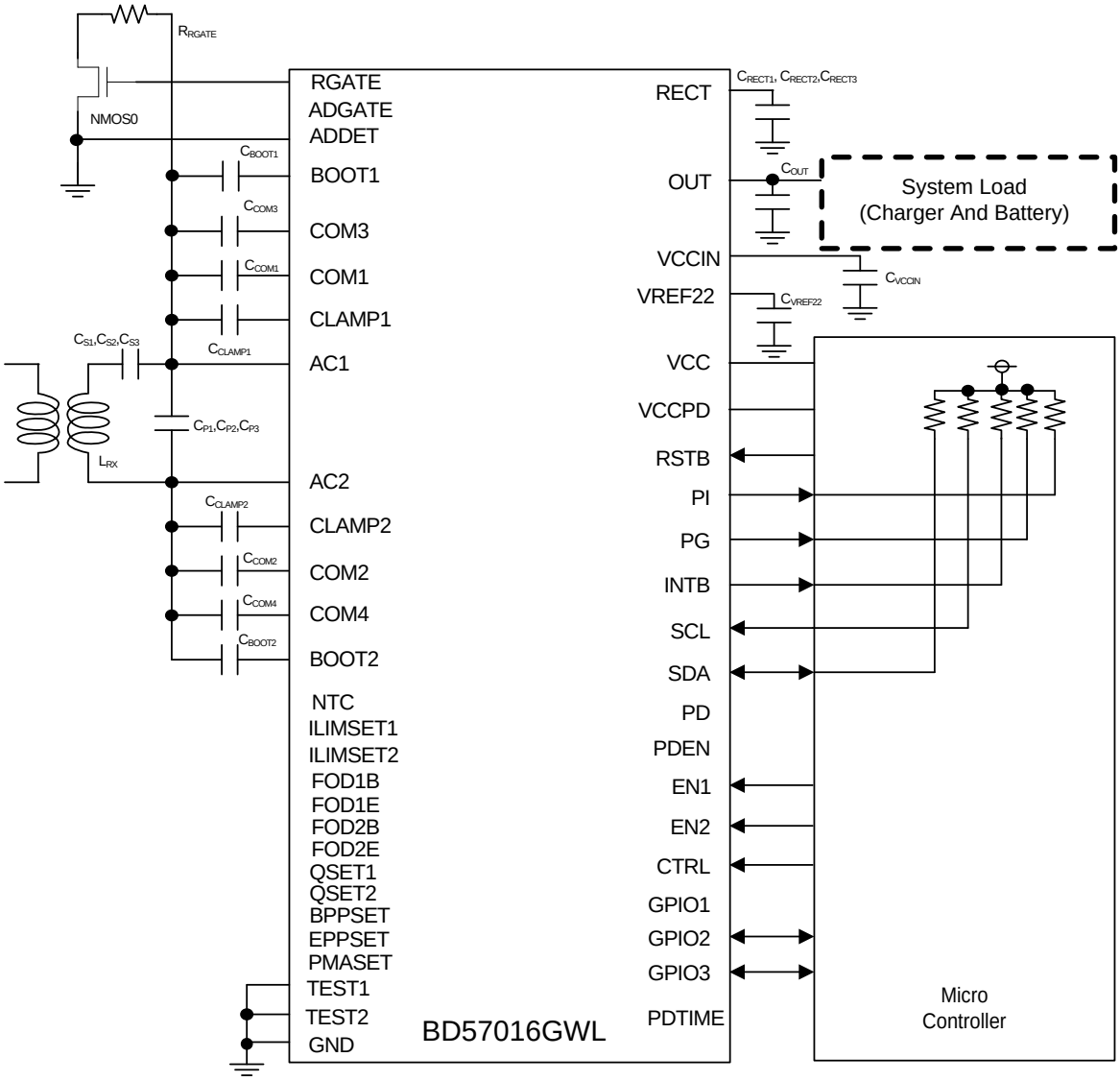


Figure 19. Representative Application Circuit Diagram

29.2 Parts List

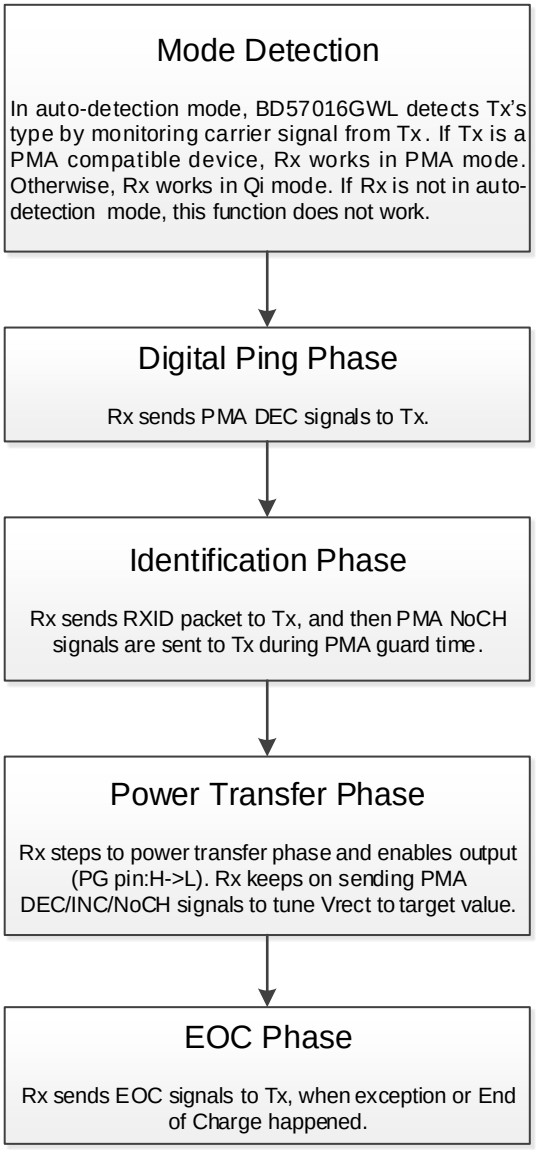
Part Name	Informative Value	Unit	Informative Part	Maker
L_{RX}	8.0	µH	760 308 102 207	WURTH ELEKTRONIK Co.,Ltd
C_{S1}	0.1	µF	GRM Series	MURATA Co.,Ltd.
C_{S2}	0.082	µF	GRM Series	MURATA Co.,Ltd.
C_{S3}	0.082	µF	GRM Series	MURATA Co.,Ltd.
C_{P1}	2200	pF	GRM Series	MURATA Co.,Ltd.
C_{P2}	820	pF	GRM Series	MURATA Co.,Ltd.
C_{P3}	-	pF	GRM Series	MURATA Co.,Ltd.
C_{BOOT1}, C_{BOOT2}	0.01	µF	GRM Series	MURATA Co.,Ltd.
C_{COM1}, C_{COM2}	0.047	µF	GRM Series	MURATA Co.,Ltd.
C_{COM3}, C_{COM4}	0.01	µF	GRM Series	MURATA Co.,Ltd.
C_{CLAMP1}, C_{CLAMP2}	0.1	µF	GRM Series	MURATA Co.,Ltd.
C_{RECT1}	10	µF	GRM Series	MURATA Co.,Ltd.
C_{RECT2}	10	µF	GRM Series	MURATA Co.,Ltd.
C_{RECT3}	10	µF	GRM Series	MURATA Co.,Ltd.
C_{OUT}	2.2	µF	GRM Series	MURATA Co.,Ltd.
R_{RGATE}	3.9	Ω	MCR10 Series	ROHM Co.,Ltd.
NMOS0	-	-	RTF025N03	ROHM Co.,Ltd.

Description of Blocks - continued

30. Operation Sequence

30.1 PMA Operation Sequence

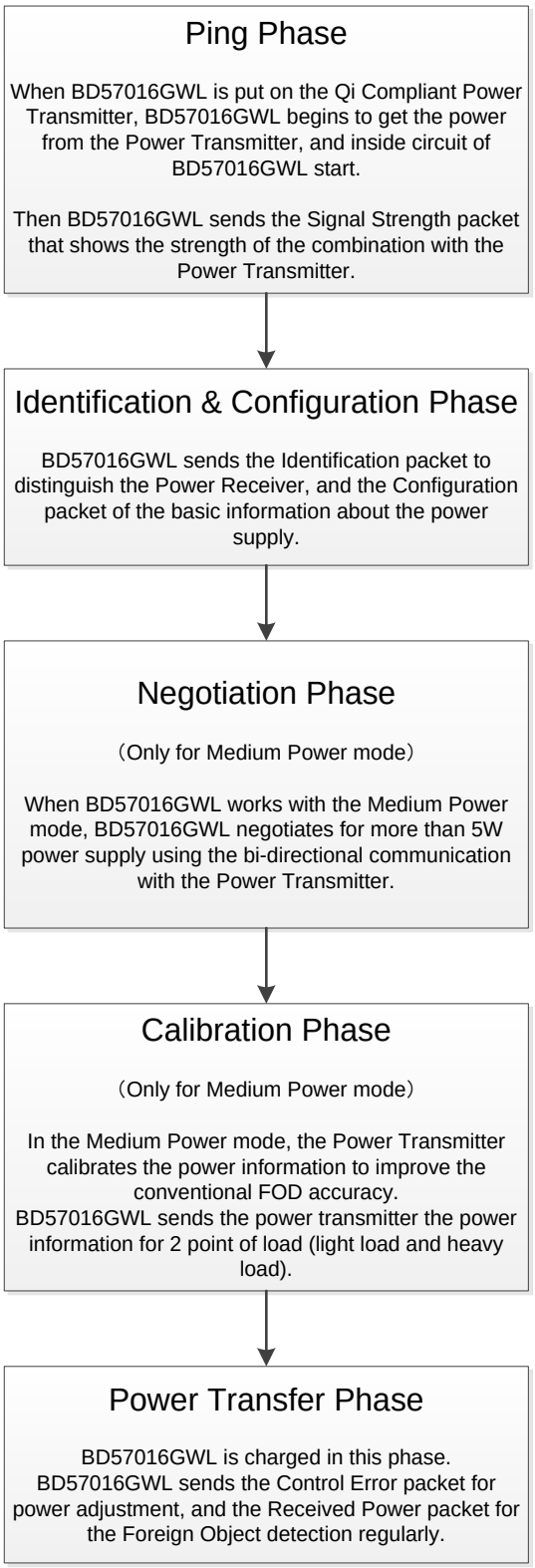
The Operation Sequence in the PMA Mode is shown below.



30. Operation Sequence - continued

30.2 Qi Operation Sequence

The Operation Sequence in the Qi Mode is shown below.



Description of Blocks - continued

31. Instructions in The Wireless Power Supply System

When developed a product of the Qi / PMA certification, the compliance test of each standard should be taken. It is necessary to take a compliance test to every product even if used this IC. Besides, the compatibility for all acceptable transmission device cannot be guaranteed when a compliance test does PASS.

Typical Performance Curves

Start up waveform

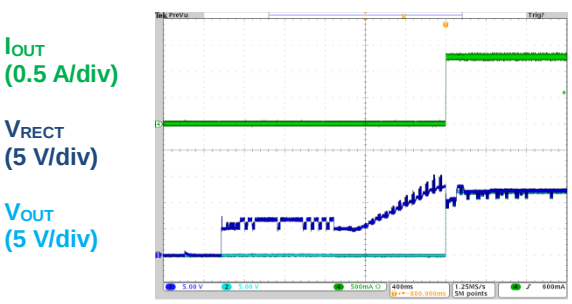


Figure 20. Qi EPP Mode: OUT=12 V
TX=BD57020MWV (MP A11)

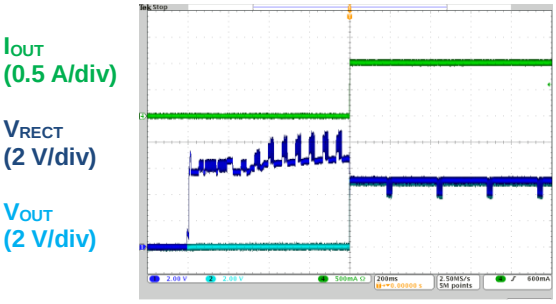


Figure 21. Qi BPP Mode: OUT=5 V
TX=BD57021MWV (LP A11)

Load step

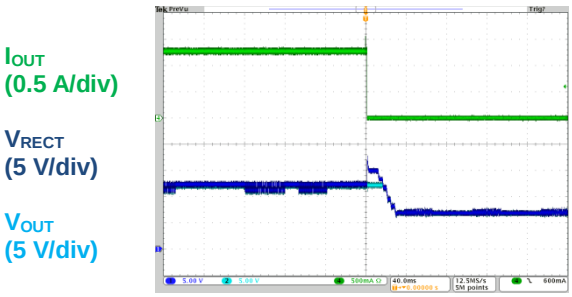


Figure 22. Qi EPP Mode: OUT=12 V
0 A to 1.25 A TX=BD57020MWV (MP A11)

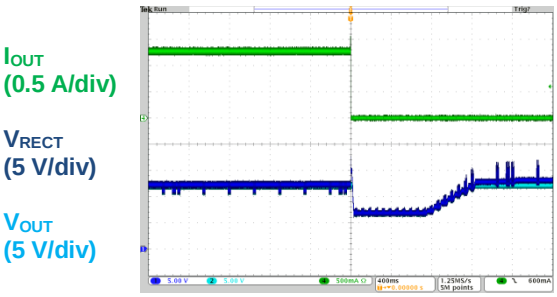


Figure 23. Qi EPP Mode: OUT=12 V
1.25 A to 0 A TX=BD57020MWV (MP A11)

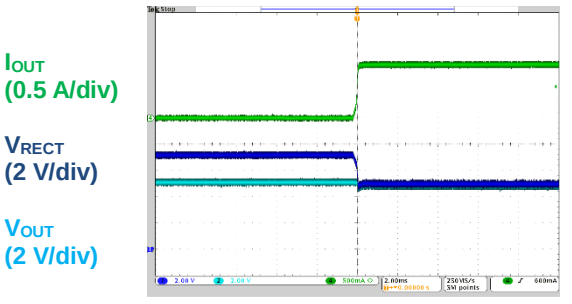


Figure 24. Qi BPP Mode: OUT=12 V
0 A to 1.0 A TX=BD57021MWV (LP A11)

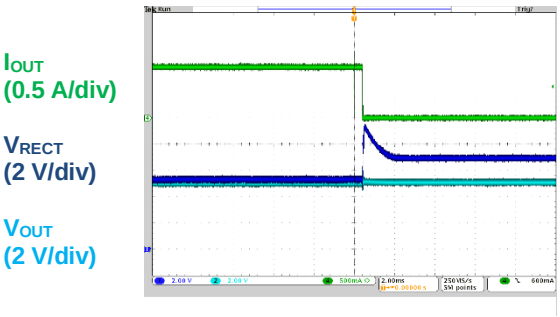


Figure 25. Qi BPP Mode: OUT=5 V
1.0 A to 0 A TX=BD57021MWV (LP A11)

Typical Performance Curves – continued

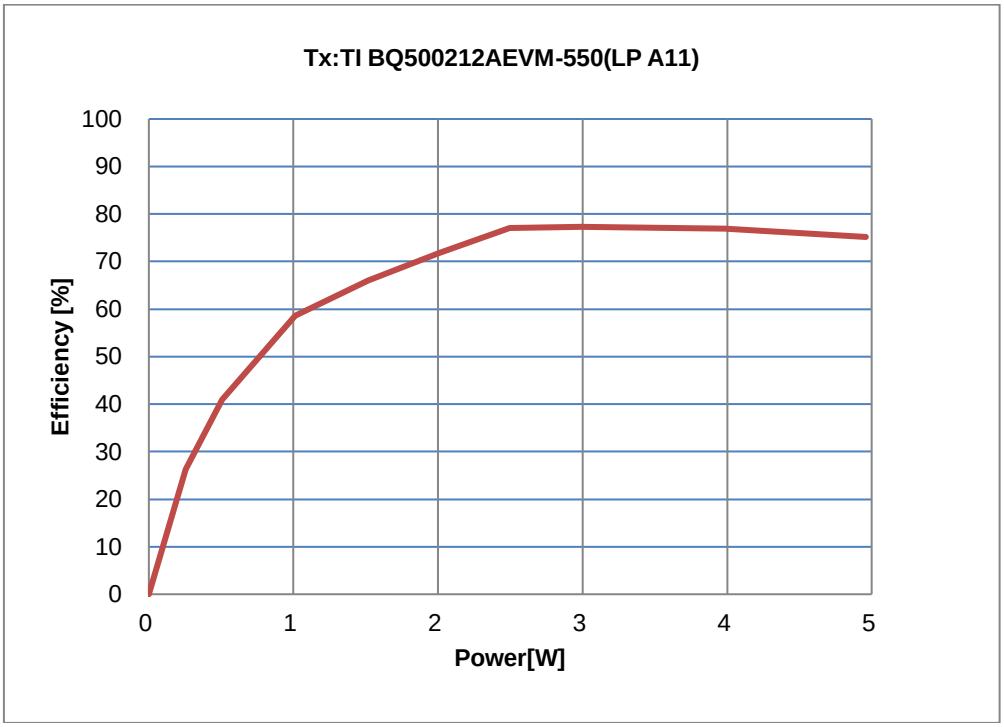


Figure 26. System Efficiency (BPP: V_{OUT}=5 V)

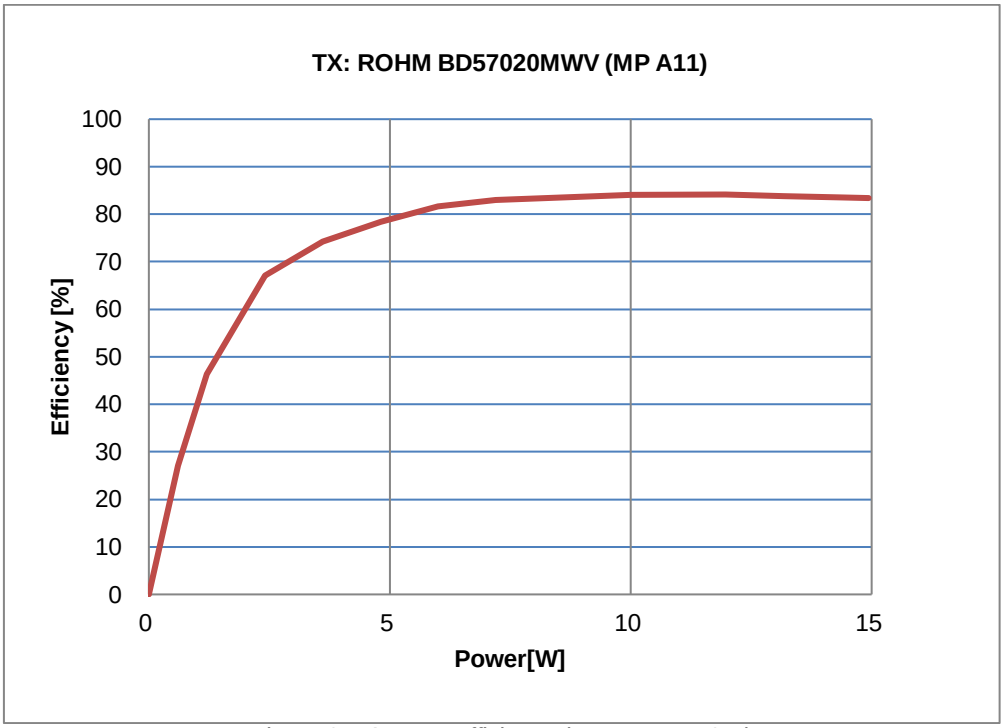


Figure 27. System Efficiency (EPP: V_{OUT}=12 V)

(Measurement condition)
Rx side thickness = 1.0 mm (Acrylic board)
Coil position = Center
Battery on Rx = None

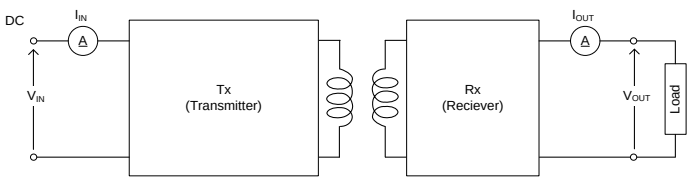
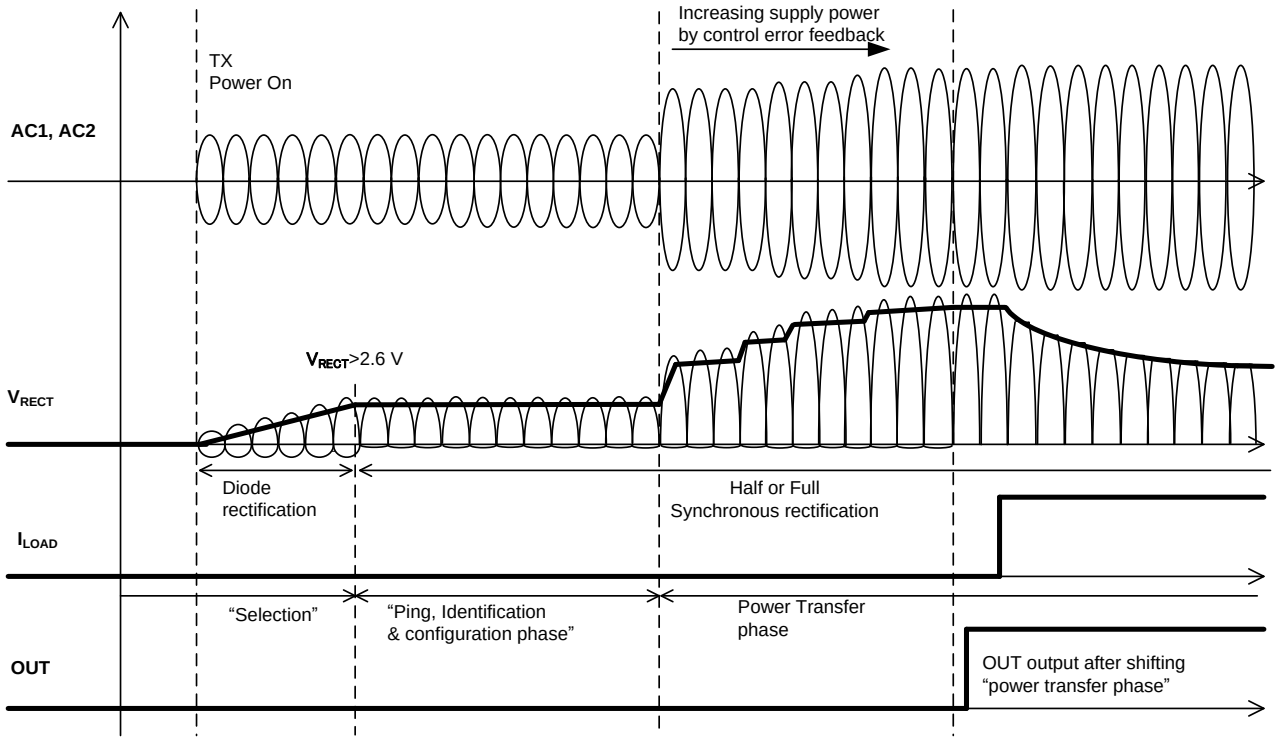


Figure 28. Measurement Circuit

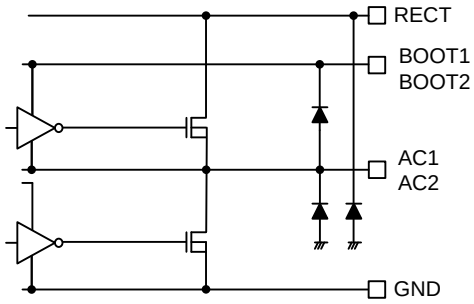
Timing Chart

Start up sequence

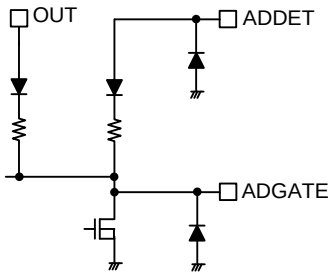


I/O Equivalence Circuits

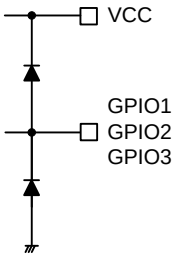
RECT, AC1(AC2), BOOT1(BOOT2), GND pin



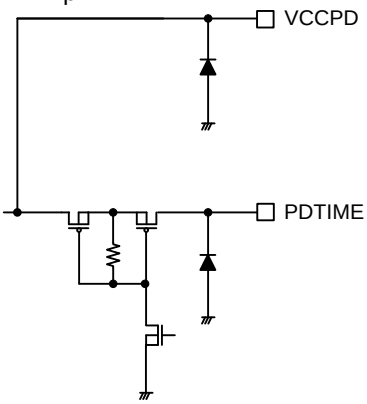
ADDET, ADGATE pin



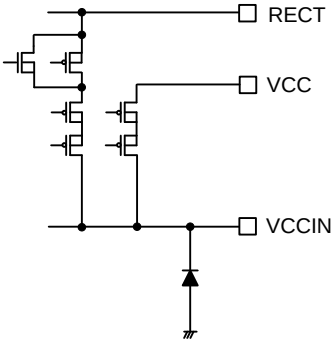
VCC, GPIO1(GPIO 2, GPIO 3) pin



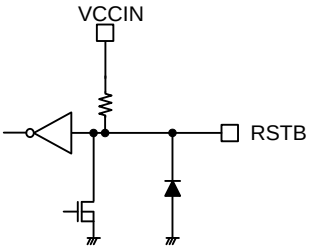
VCCPD, PDTIME pin



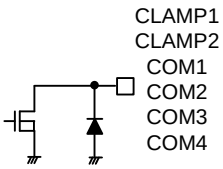
VCCIN pin



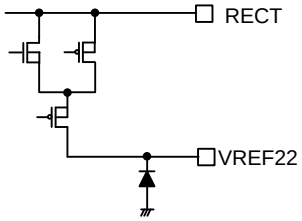
RSTB pin



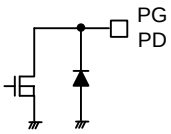
COM1, COM2, COM3, COM4, CLAMP1, CLAMP2 pin



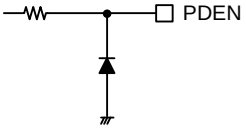
VREF22 pin



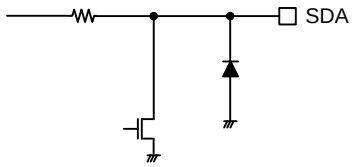
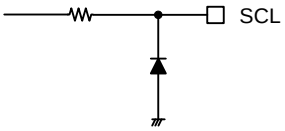
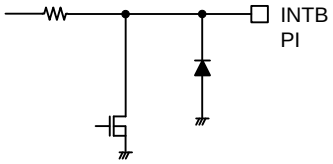
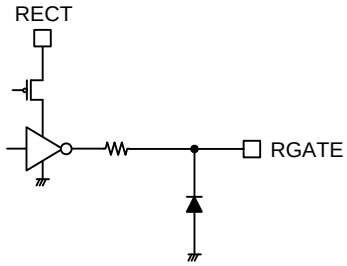
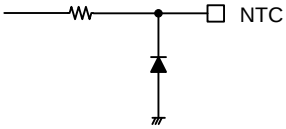
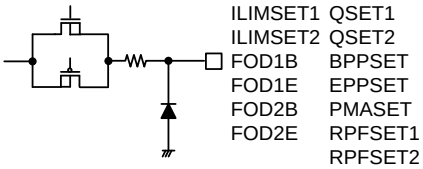
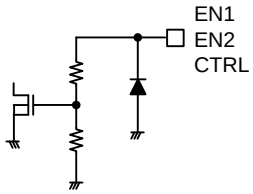
PG, PD pin



PDEN pin



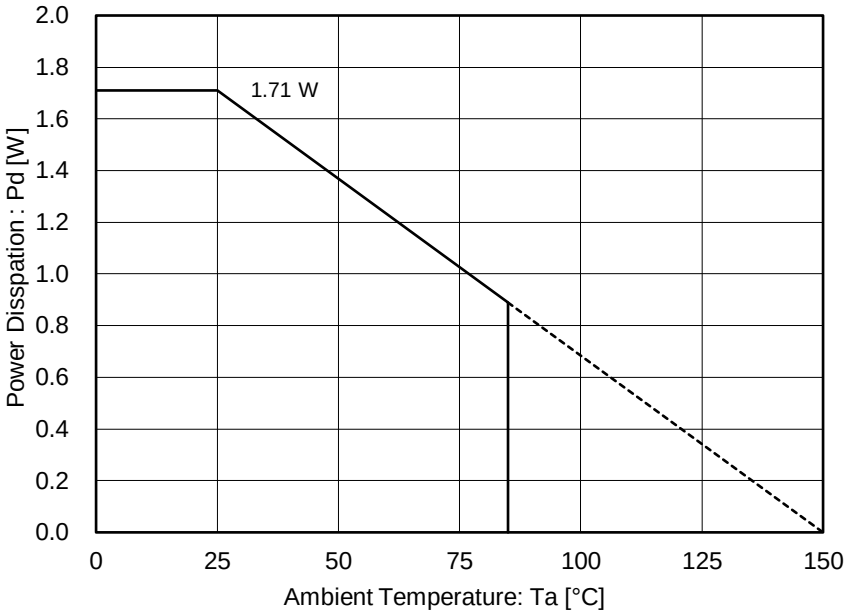
I/O Equivalence Circuits – continued

SDA pin 	SCL pin 	INTB, PI pin 
RGATE pin 	NTC pin 	BPPSET, EPPSET, PMASET, QSET1, QSET2, ILIMSET1, ILIMSET2 FOD1B, FOD1E, FOD2B, FOD2E RPFSET1, RPFSET2, pin 
EN1, EN2, CTRL pin 		

Thermal/Heat Loss

(UCSP50L4C Package)

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.



* 54 mm x 62 mm x 1.6 mm Glass Epoxy Board

Figure 29. Power Dissipation Curve (Pd-Ta Curve)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

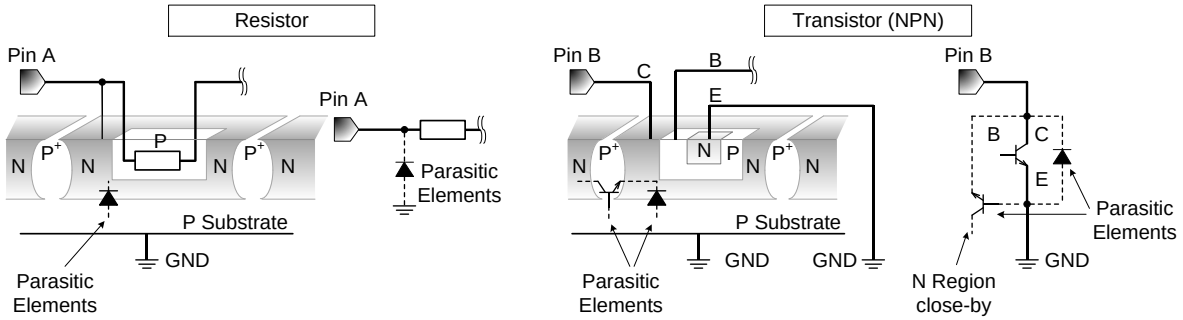


Figure 30. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the Tj falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Disturbance Light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information

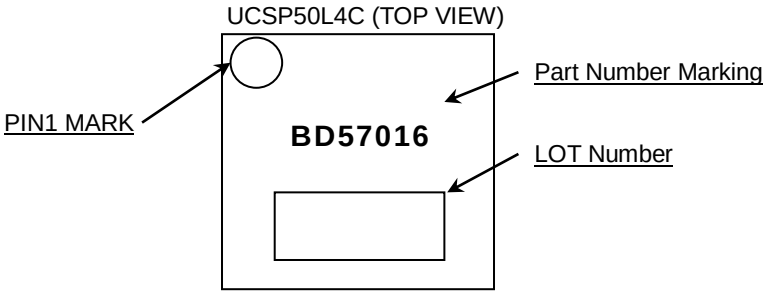
B D 5 7 0 1 6 G W L	-	E 2

Part Number

Package
GWL: UCSP50L4C

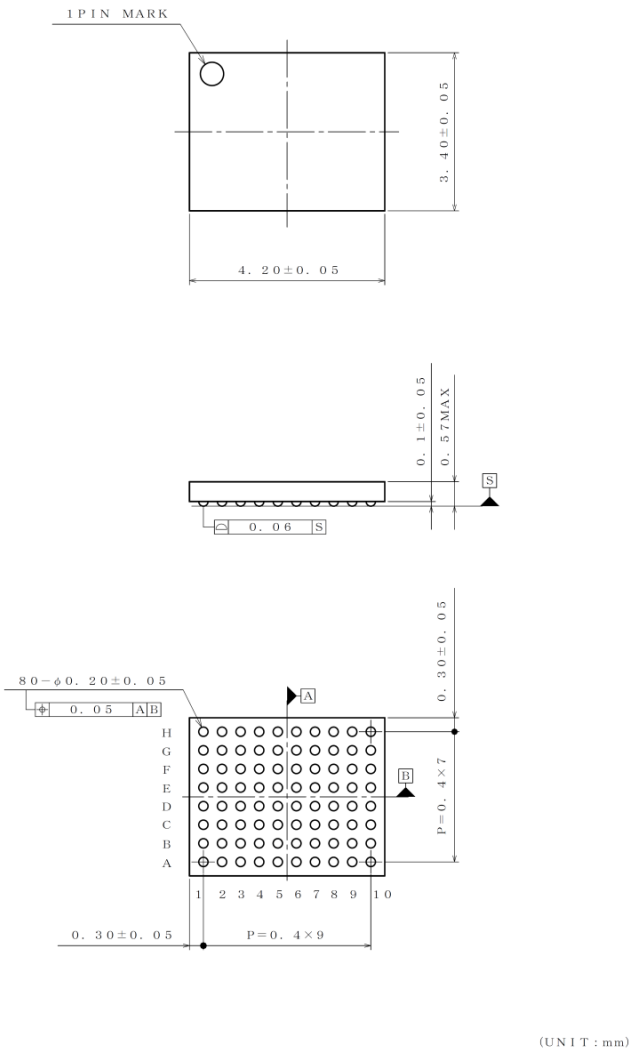
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



Physical Dimension and Packing Information

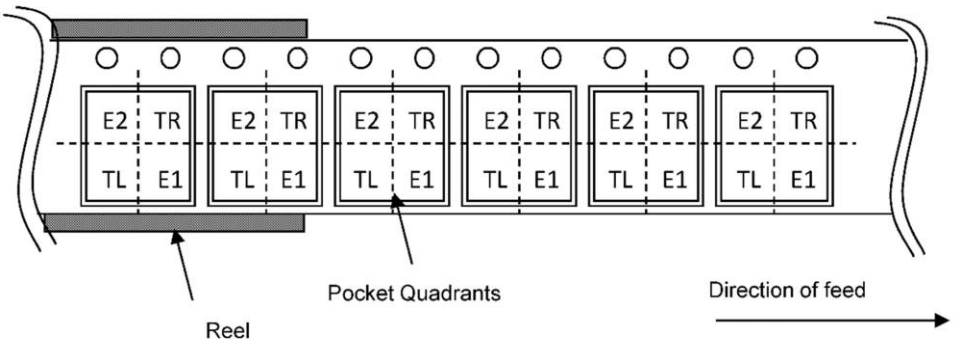
Package Name	UCSP50L4C(BD57016GWL)



(UNIT : mm)

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2,500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
22.Nov.2018	001	New release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.

BD57016GWL - Web Page

Buy

Distribution Inventory

Part Number	BD57016GWL
Package	UCSP50L4C
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes