

3-Axis Digital Accelerometer

General Description

The RT3020 is a low power three-axis motion acceleration sensor with digital output. This device has user selectable full scale ranges of $\pm 2g$, $\pm 4g$, $\pm 8g$, and $\pm 16g$, and it is capable of measuring acceleration with output data rates (ODR) from 6.25Hz to 400Hz.

The RT3020's low power design yields a nominal operating current rating of less than $5.8\mu A$ at 25Hz ODR and the device can automatically switch to an even lower power in Wakeup Mode with $1.4\mu A$ current at 6.25Hz ODR when no motion is detected for a given period of time. Once in this low power mode, it can be triggered by a motion to return to the normal operation mode of higher ODR automatically. In Normal Mode, the low pass filter can be enabled to limit the bandwidth according to the ODR setting. High resolution measurement data therefore can be obtained due to lower noise power bandwidth.

In order to further reduce the system power, a deep FIFO is provided to store data locally, therefore allows host processor stay in low power sleep mode longer. Upon the FIFO buffer full, an interrupt is issued to inform the host processor to fetch the entire block of data.

On-chip hardware is employed to detect most frequently used motion events and issues interrupts to the host processor, such as tapping, free fall, etc. As a result, it enables the system to respond to critical events with minimum delay time.

The RT3020 can operate over a wide 1.8V to 3.3V supply range and the operating temperature range covers from -40 to $+85$ degree centigrade. The RT3020 is available in LGA-12L 2x2mm package, ideal for health band, smart watch and other battery powered products.

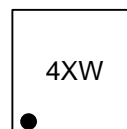
Features

- **Low Power Consumption**
 - ▶ **9.1 μA @ 50Hz ODR Normal Mode**
 - ▶ **5.8 μA @ 25Hz ODR Normal Mode**
 - ▶ **1.4 μA @ 6.25Hz ODR Wakeup Mode**
 - ▶ **0.11 μA @ Power Down Mode**
- **System Level Power Saving Features**
 - ▶ **Automatic Wakeup to Normal Mode Switching**
 - ▶ **Deep FIFO :**
 - ◆ **120 frames for 8-bit Data**
 - ◆ **80 frames for 12-bit Data**
- **Embedded Motion Detection Features**
 - ▶ **Single / Double Tap Sensing**
 - ▶ **Flat Detection**
 - ▶ **Orientation Recognition**
 - ▶ **Shock and Free-Fall Detection**
 - ▶ **Static Gesture Recognition**
- **Programmable Full Scale Range: $\pm 2g/\pm 4g/\pm 8g/\pm 16g$**
- **Wide Supply and I/O Voltage Range: 1.8V to 3.3V**
- **Operation Temperature: $-40^{\circ}C$ to $85^{\circ}C$**
- **Digital I/O Interface**
 - ▶ **I²C Interface Supporting Standard Mode, Fast Mode and Fast Mode Plus**

Applications

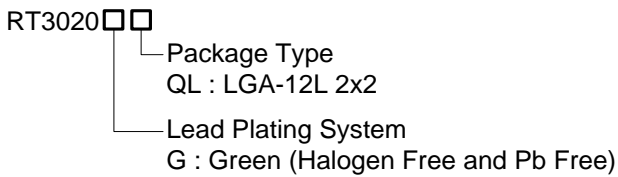
- IoT Devices
- Mobile Phones
- Tablets
- Wearables

Marking Information



4X : Product Code
W : Date Code

Ordering Information



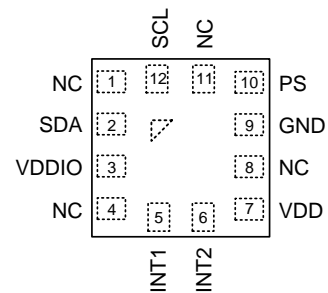
Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)

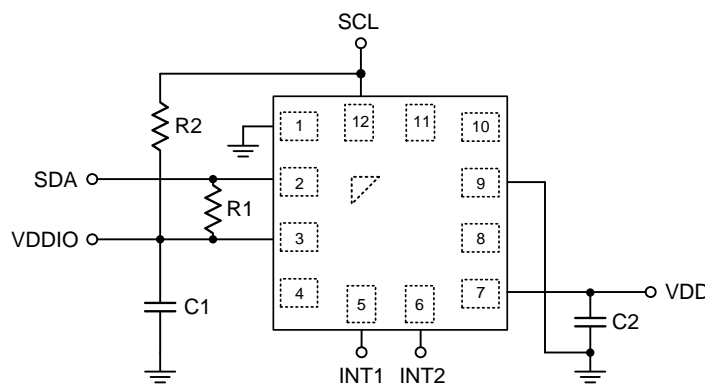


LGA-12L 2x2

Functional Pin Description

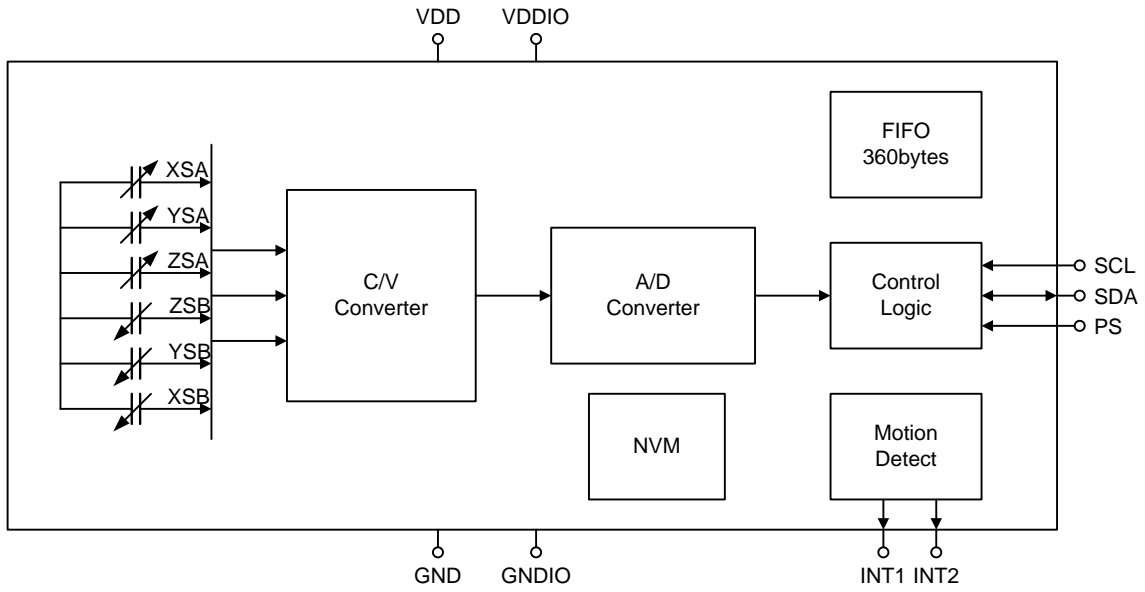
| Pin No. | Pin Name | I/O Type | Description |
|-------------|----------|-------------|--|
| 2 | SDA | Digital I/O | I ² C serial data. |
| 3 | VDDIO | Supply | Power supply for I/O pins. |
| 1, 4, 8, 11 | NC | NC | No internal connection. |
| 5 | INT1 | Digital Out | Interrupt 1 output. |
| 6 | INT2 | Digital Out | Interrupt 2 output. |
| 7 | VDD | Supply | Power supply for analog and digital domain. |
| 9 | GND | Ground | Ground. |
| 10 | PS | Digital In | Must be high or no connect for I ² C communication. |
| 12 | SCL | Digital In | I ² C serial clock. |

Typical Application Circuit



Note : The recommended value for C1 and C2 is 0.1μF.

Functional Block Diagram



Absolute Maximum Ratings (Note1)

- VDD Supply Voltage----- -0.2V to 4V
- VDDIO Supply Voltage----- -0.2V to 4V
- Logic Pin Voltage----- -0.2V to (VDDIO + 0.3V)
- Storage Temperature Range ----- -40°C to 125°C
- ESD Susceptibility (Note 2)
 - HBM (Human Body Model) ----- 2kV
 - CDM (Charged Device Model)----- 500V
- Mechanical Shock----- 10000g for 0.2ms

Electrical Characteristics

(VDD = 2.5V, TA = 25°C, unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|--------|------------------|-------------|-----|-------------|------|
| Supply Voltage – Core (Note 3) | VDD | | 1.8 | 2.5 | 3.3 | V |
| Supply Voltage – I/O | VDDIO | VDDIO ≤ VDD | 1.8 | -- | VDD | V |
| Input Voltage Low | VIL | I ² C | -- | -- | 0.3 x VDDIO | V |
| Input Voltage High | VIH | I ² C | 0.7 x VDDIO | -- | -- | V |
| Output Voltage Low | VOL | IOL = 4mA | -- | -- | 0.2 x VDDIO | V |
| Output Voltage High | VOH | IOH = 4mA | 0.8 x VDDIO | -- | -- | V |
| Operating Ambient Temperature Range | TA | | -40 | -- | 85 | °C |

Specification

(VDD = 2.5V, TA = 25°C, Resolution = 12bits, unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------|--------|------------|-----|-----|-----|------|
| Acceleration Range | FS2g | | -- | ±2 | -- | g |
| | FS4g | | -- | ±4 | -- | |
| | FS8g | | -- | ±8 | -- | |
| | FS16g | | -- | ±16 | -- | |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|---------------------------------------|--------------------|--|------------|-------|-----|--------|----|
| Sensitivity | RBITS | Output resolution | -- | 12 | -- | bits | |
| | S _{2g} | Sensitivity of FS _{2g} | -- | 1 | -- | mg/LSB | |
| | S _{4g} | Sensitivity of FS _{4g} | -- | 2 | -- | mg/LSB | |
| | S _{8g} | Sensitivity of FS _{8g} | -- | 4 | -- | mg/LSB | |
| | S _{16g} | Sensitivity of FS _{16g} | -- | 8 | -- | mg/LSB | |
| | C _{2g} | Counts of FS _{2g} | -- | 1024 | -- | LSB/g | |
| | C _{4g} | Counts of FS _{4g} | -- | 512 | -- | LSB/g | |
| | C _{8g} | Counts of FS _{8g} | -- | 256 | -- | LSB/g | |
| | C _{16g} | Counts of FS _{16g} | -- | 128 | -- | LSB/g | |
| Sensitivity Temperature Coefficient | TCS _{2g} | FS _{2g} | -- | ±0.05 | -- | %/°C | |
| Zero-g Offset | OFS _{new} | FS _{2g} , before soldering | -- | ±25 | -- | mg | |
| | OFS | FS _{2g} , over life-time | -- | TBD | -- | mg | |
| Zero-g Offset Temperature Coefficient | TCO _{2g} | FS _{2g} , | -- | ±0.8 | -- | mg/°C | |
| Non-Linearity | NL | Percentage of full scale, Best fit straight line, FS _{2g} | -- | ±0.5 | -- | % | |
| Cross Axis Sensitivity | CAS | Coupling between two axis | -- | ±1.25 | -- | % | |
| RMS Noise | N _{rms} | 25Hz ODR with Lowpass Filter Corner at ODR/3 | -- | 0.65 | -- | mg | |
| Current Consumption | IDD _{ME} | Measurement mode | ODR = 50Hz | -- | 9.1 | -- | μA |
| | | | ODR = 25Hz | -- | 5.8 | -- | |
| | IDD _{WU} | Wakeup mode, ODR = 6.25Hz | -- | 1.4 | -- | | |
| | IDD _{PD} | Power-Down mode | -- | 0.11 | -- | | |
| Self-Test Output Change | V _{ST} | X/Y axis | -- | 120 | -- | mg | |
| | | Z axis | -- | 300 | -- | | |
| Wake Time | t _{WU} | From Wakeup mode to Normal mode | -- | -- | 1.3 | ms | |
| Start-Up Time | tsu | Power up to Power-Down mode | -- | 60 | -- | ms | |

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution is recommended.

Note 3. Maximum supply voltage must be controlled within +5% of its rating.

Operation

Operating Modes

The RT3020 provides four different operating modes for users to select in order to meet specific application requirements with minimum power consumption. As the RT3020 is intended to be an “Always-ON” sensor, by setting the operation in Wake-up mode, a low ODR and a subset of function is configured to only detect the occurrence of an event and wake up the measurement function for detailed acceleration data. In Normal Mode the full measurement functionality is available as well as a higher ODR is usually chosen, therefore higher power consumption is observed. When no activity is detected for a period of time, the Normal Mode will return to Wakeup mode to save power. Noted that switching between Wakeup and Normal mode is carried out seamlessly without host processor’s intervention.

The power down and high resolution mode can be set through the host processor and stays in the same mode until a different mode setting is issued by the host. When high accuracy data is required, the High Resolution mode can be selected where internal filtering is added to limit the noise bandwidth to ODR/3. A state diagram of the operating mode is shown in Figure 1.

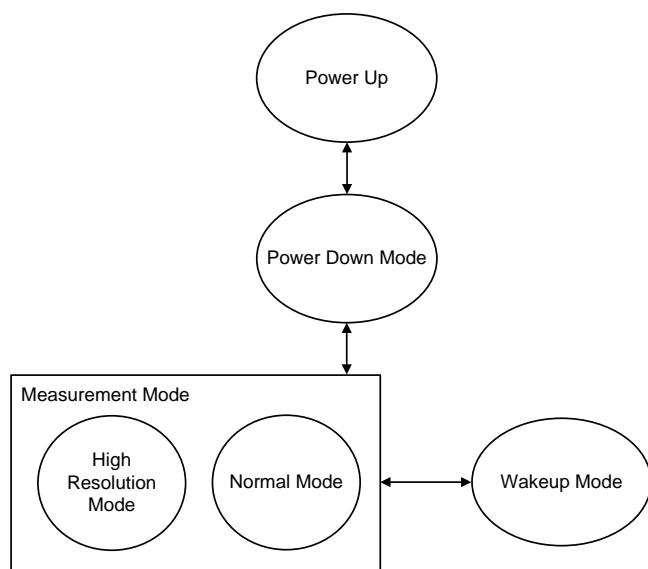


Figure 1 Operating Mode State Diagram

Power-Down Mode

In power down mode, almost all internal blocks are switched off, and only the digital interface is kept alive to allow communication to the host. All previous states before entering power down mode are not preserved. When switching from power down mode to other operation modes, a wait time of 60msec is required before writing or reading the RT3020 registers via I²C.

Wakeup Mode

Wakeup mode is used to activate the sensing on an as-needed basis when a motion event arises. The power consumption is extremely low, about 1.4µA at 6.25Hz ODR and can go down to 0.7µA at 1.5Hz ODR. The wakeup mode can be used to implement a motion activated ON/OFF switch in a system to replace the mechanical switch.

The acceleration event that is larger than a pre-set threshold will automatically switch the device to normal measurement mode with higher sampling frequency.

The RT3020 can enter into the wakeup mode either by a time based manner when no motion is detected in a predefined time window or by forcing the register control bit in 0x08 at any time. The default ODR in this mode is 6.25Hz and can be set from 1.5Hz to 50Hz.

Normal Measurement Mode

All salient features are supported in normal measurement mode, they are : motion detection, FIFO buffer, data filtering and wide ODR range from 6.25Hz to 400Hz. Due to its full functionality and higher ODR, the power consumption is higher than wakeup or power down mode.

High Resolution Measurement Mode

High resolution measurement is obtained by using higher internal sampling frequency and through a decimation lowpass filter to remove the out of band noise. The lowpass corner frequency is fixed at ODR/3 to insure no noise is aliased into data band. Noted that lower ODR setting implies lower noise bandwidth and therefore higher resolution. The power consumption in

this mode is the highest and it is used when high resolution is required. The ODR supported is from 6.25Hz to 400Hz.

Programmable Measurement Range

The RT3020 has measurement ranges of $\pm 2g$, $\pm 4g$, $\pm 8g$, and $\pm 16g$. Acceleration samples are always converted by a 12bits ADC. When the acceleration exceeds the measurement range, data is clipped at the full scale value 0x7FF of maximum positive value or 0x800 of minimum negative value. Users can access three axis data from register, which 0x10 to 0x15 provide full 12bits data for accessing.

Programmable Output Data Rate

The RT3020 reports acceleration data at various data rates ranging from 6.25Hz to 400Hz in measurement mode. In wakeup mode, ODR can be configured from 1.5Hz to 50Hz.

FIFO Operation

The RT3020 includes a 360 bytes first in, first out (FIFO) buffer. The FIFO can be configured to a maximum of 120 frames (3 bytes for x/y/z axis data) with 8 bits data resolution or 80 frames (4.5 bytes for x/y/z axis data) with 12 bits data resolution. While the FIFO is enabled, the accelerometer data is written into the FIFO. Host processor only needs to move the data to the host memory upon FIFO full status flag assertion. There are four FIFO operating modes that can be selected for different application scenarios.

Stream Mode

Once the buffer is full in stream mode, the new data will overwrite the oldest data that was recorded in the FIFO. It is different from the FIFO Mode which always holds the oldest data. In Stream Mode, on the other hand, the FIFO always keeps the latest data while the oldest is dropped to gives space for the new arriving data.

FIFO Mode

When the FIFO function is enabled, the three axis data are stored in the FIFO and the data collection is stopped when FIFO is full. Once the buffer is full, new data are ignored and the captured data are locked in the FIFO

permanently.

To reset the “FIFO Full” state, it is necessary to force the FIFO into Bypass Mode first before restarting the FIFO Mode operation.

Bypass Mode

Bypass mode is used to bypass the FIFO buffer and at the same time clears or reset its contents. It is recommended to enter Bypass Mode first before using other FIFO modes.

Trigger Mode

Trigger Mode is also called Stream-to-FIFO mode. As the name indicates, the Trigger Mode combines the characteristics of the Stream Mode and the FIFO Mode. When it is first enabled, it operates under the Stream Mode until a trigger condition is met, then it switches to the FIFO Mode where the data from trigger event are captured and locked in the FIFO for further analysis. The trigger event is programmable and can be from one of many detected motion sources.

Same as in FIFO Mode, the locked data and state can be reset and cleared by forcing it into the Bypass Mode.

Motion Detect

Tap Sensing

Tapping or clicking is an action that is manifested by a narrow acceleration pulse, it is defined by a window within which the pulse is confined. When this condition is met, an interrupt is issued. The pre- or post-window cursor shall not be detected in order to qualify a tapping motion. Two consecutive tapping separated within a given duration is defined as a double-tapping or double-clicking action and an interrupt is issued for this motion. Single and double tapping is often used to control a device (e.g true wireless earpods) where mechanical switch or touch sensing switch is not practical.

Shock Detect

Shock is defined as a motion driven by a long sustaining force in which acceleration is above a predefined threshold for a specified duration. Events meeting the shock criteria, interrupts are issued to signify such motion. For example, it can be used to detect the impact force in car accident in EDR (Event Data Recorder) devices. The recording will be stopped upon large impact detection to protect the data being overwritten.

Free Fall Detect

The free fall is the state of weightlessness. It means all three axis are zero acceleration or gravity. Once free fall is detected it can alert the system to take precautionary action to protect sensitive parts. For example a hard drive may incorporate the free fall sensor to detect the drop of the device and prevent the drive head from crashing on the magnetic disk, therefore causes data loss.

Display Profile Switch

Display profile switch is mainly intended for smart phone or tablet devices where either landscape or portrait display mode is automatically switched depending on the detected gravity with respect to the three axis (x/y/z). Using this built-in function, it allows efficient display rotation without host processor having to read the three axis data and calculate display's angle position.

Gesture Recognition

A gesture is a static position defined by the three accelerometer axis. The RT3020 can set the threshold and its region of tolerance on each individual axis to define a certain gesture. It is particularly useful in applications such as detecting a smart band's position for reading or glancing the display, therefore power on the screen, when the device is not at "glance position" the screen is off to save power.

Additional Features

Latch Interrupt

The RT3020 provides programmable interrupt active duration for microcontroller. Latch mode, non-latch mode, and programmable latch mode are implemented in the RT3020. The INT1 and INT2 have different settings for different requirements. While it is set to non-latch mode, the pulse width with 25usec will be signaled when specific interrupt occurs. The latch mode is selected to prevent missing any interrupt event. The interrupt flag will be hold till the interrupt status has been read. The programmable latch mode holds the active duration from 2.5msec to maximum 20.5sec no matter host has read interrupt status or not.

Self-Test

The RT3020 has the self-test feature for the sensor functionality check by applying electrostatic force to the sensor element. A static offset of the acceleration data can be observed when the self-test is activated. The acceleration measurement range should be set to 2g before self-test is enabled. When the self-test bit is set, an actuation force is applied to the sensor, simulating a definite input acceleration. The typical offset differences of self-test for XY axis are about 120mg and Z axis is about 300mg.

Power

Power Supply Requirements

It's recommended to power up the RT3020 always from 0V. When the RT3020 is in operation, any time supply power falls below the operating voltage range, all the supplies must be discharged to 0V before re-applying the power.

It is recommended to use a voltage regulator with a shutdown discharge function, such as RT9078.

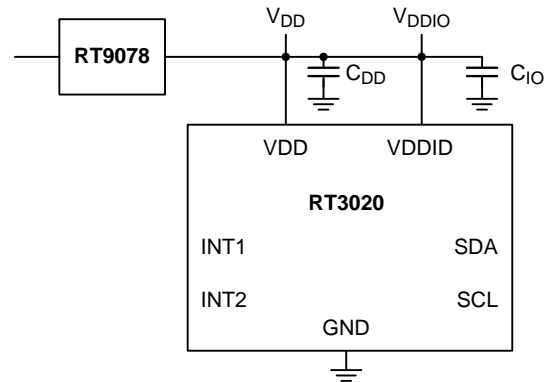


Figure 2 Single Power Supply Design Using the RT9078

Communications

I²C : Inter-Integrated Circuit

There are two signals associated with the I²C bus : the serial clock line (SCx) and the serial data line (SDx). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to VDDIO through external pull-up resistor. When the bus is free, both lines are high.

Electrical Characteristics : I²C Interface

| Parameter | Symbol | Standard-Mode | | Fast-Mode | | Fast-Mode Plus | | Unit |
|---|--------------------|---------------|------|-----------|-----|----------------|------|------|
| | | Min | Max | Min | Max | Min | Max | |
| SCL Clock Frequency | f _{SCLK} | 10 | 100 | 10 | 400 | 10 | 1000 | kHz |
| Hold Time After (Repeated) Start Condition. After This Period, the First Clock is Generated | t _{HDSTA} | 4 | -- | 0.6 | -- | 0.26 | -- | μs |
| LOW Period of The SCL Clock | t _{LOW} | 4.7 | -- | 1.3 | -- | 0.5 | -- | μs |
| HIGH Period of The SCL Clock | t _{HIGH} | 4.0 | -- | 0.6 | -- | 0.26 | -- | μs |
| Set-Up Time for a Repeated START Condition | t _{SUSTA} | 4.7 | -- | 0.6 | -- | 0.26 | -- | μs |
| Data Hold Time | t _{HDDAT} | 0 | 2490 | 0 | 610 | 0 | 200 | ns |
| t _{SUDAT} Data Set-Up Time | t _{SUDAT} | 250 | -- | 100 | -- | 50 | -- | ns |
| Set-Up Time for STOP Condition | t _{SUSTO} | 4.0 | -- | 0.6 | -- | 0.26 | -- | μs |
| Bus Free Time between a STOP and START Condition | t _{BUF} | 4.7 | -- | 1.3 | -- | 0.5 | -- | μs |

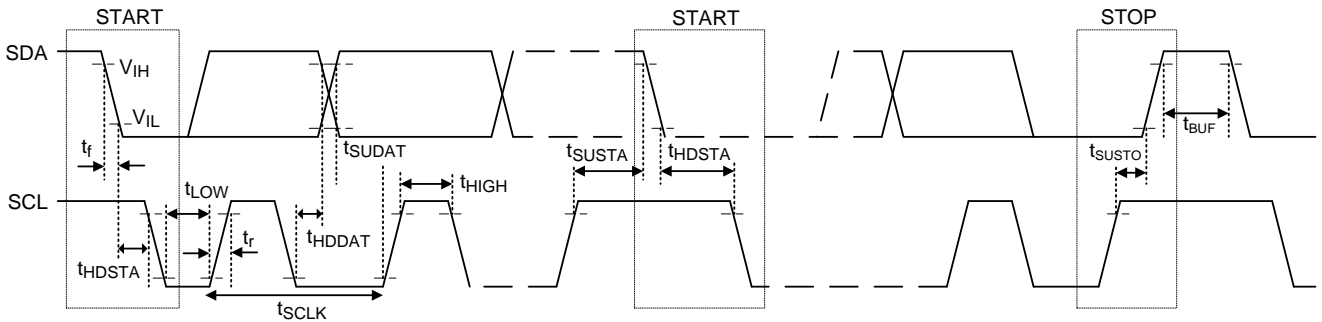


Figure 3. Timing Chart of the I²C

I²C Protocol

The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master wants to do a write or a read command. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

| Command | SDO Connection | WR bits | Slave Address |
|---------|-------------------|---------|---------------|
| Read | VDDIO or floating | 1 | 8'h33 |
| Write | VDDIO or floating | 0 | 8'h32 |

The I²C burst read or write is supported in the RT3020. The RT3020 continuously writes/reads the data to/from the following address till it receives STOP condition.

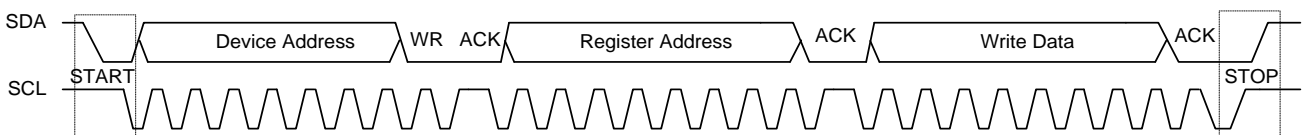


Figure 4. Write Command

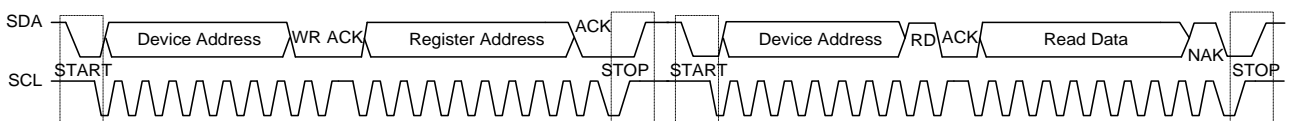


Figure 5. Read Data

Register Mapping

| Addr | Typ | Name | Def | Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 | | |
|------|-----|-----------|------|----------------------------------|------------------|----------------|-----------|--------------------------------|----------|-----------------|----------|--|--|
| 0x00 | R | WHOAMI | 0x33 | WHO AM I | | | | | | | | | |
| 0x01 | R | IRQ_STS | 0x00 | -- | STS_SIGM | STS_TAP | STS_AOI | STS_OVN | STS_WTM | STS_DRDY | -- | | |
| 0x02 | R | MODE_STS | 0x00 | -- | -- | -- | PO_DRDY | -- | STS_MES | -- | STS_STBY | | |
| 0x07 | RW | CTRL_CFG0 | 0x02 | -- | -- | -- | SELF_TEST | -- | -- | | | | |
| 0x08 | RW | MODE_CFG | 0x00 | -- | -- | -- | SW_RST | -- | -- | MEASURE[1:0] | | | |
| 0x09 | RW | CTRL_CFG1 | 0x07 | -- | ODR[2:0] | | | HR | ZEN | YEN | XEN | | |
| 0x0A | RW | CTRL_CFG2 | 0x00 | I2_ACT | I2_SLP | I1_ACT | I1_SLP | IRQ2_POL | IRQ1_POL | FULL_SCALE[1:0] | | | |
| 0x0B | RW | CTRL_CFG3 | 0x00 | ILATCH2_SEL[3:0] | | | | ILATCH1_SEL[3:0] | | | | | |
| 0x10 | R | XDATA_L | 0x00 | XDATA[3:0] | | | | 4'b0000 | | | | | |
| 0x11 | R | XDATA_H | 0x00 | XDATA[11:4] | | | | | | | | | |
| 0x12 | R | YDATA_L | 0x00 | YDATA[3:0] | | | | 4'b0000 | | | | | |
| 0x13 | R | YDATA_H | 0x00 | YDATA[11:4] | | | | | | | | | |
| 0x14 | R | ZDATA_L | 0x00 | ZDATA[3:0] | | | | 4'b0000 | | | | | |
| 0x15 | R | ZDATA_H | 0x00 | ZDATA[11:4] | | | | | | | | | |
| 0x16 | R | FIFO_UNRD | 0x00 | UNREAD[7:0] | | | | | | | | | |
| 0x17 | R | FIFO_STS | 0x00 | -- | -- | -- | -- | -- | OVN | WTM | EMPTY | | |
| 0x18 | R | AOI_STS1 | 0x00 | PO_AOI | -- | ZH1 | ZL1 | YH1 | YL1 | XH1 | XL1 | | |
| 0x19 | R | AOI_STS2 | 0x00 | -- | -- | -- | -- | -- | SIGN_Z | SIGN_Y | SIGN_X | | |
| 0x1A | R | TAP_STS | 0x00 | PO_TAP | -- | DCLICK | SCCLICK | SIGN | ZTAP | YTAP | XTAP | | |
| 0x20 | RW | IRQ1_MAP | 0x00 | -- | I1_SIGM | I1_TIA | I1_AOI | I1_OVN | I1_WTM | I1_DRDY | -- | | |
| 0x21 | RW | IRQ2_MAP | 0x00 | -- | I2_SIGM | I2_TIA | I2_AOI | I2_OVN | I2_WTM | I2_DRDY | -- | | |
| 0x22 | RW | FIFO_CFG | 0x00 | FIFO_EN | FIFO_HR | FIFO_MODE[1:0] | | FIFO_SKIP[1:0] | | TRIG_SRC[1:0] | | | |
| 0x23 | RW | FIFO_THS | 0x00 | FIFO_THRES[7:0] | | | | | | | | | |
| 0x24 | RW | FILTER | 0x00 | -- | -- | UNSIGN | -- | -- | -- | HP_AOI | HP_DATA | | |
| 0x30 | RW | AOI_CFG | 0x00 | -- | AOI | COMP_Z[1:0] | | COMP_Y[1:0] | | COMP_X[1:0] | | | |
| 0x31 | RW | AOI_TIME | 0x00 | AOI_ACTIVE_TIME[7:0] (2.5ms/LSB) | | | | | | | | | |
| 0x32 | RW | AOI_THSX | 0x00 | AOI_ACTIVE_THRESH_X[7:0] | | | | (2's complement w/ signed bit) | | | | | |
| 0x33 | RW | AOI_THSY | 0x00 | AOI_ACTIVE_THRESH_Y[7:0] | | | | (2's complement w/ signed bit) | | | | | |
| 0x34 | RW | AOI_THSZ | 0x00 | AOI_ACTIVE_THRESH_Z[7:0] | | | | (2's complement w/ signed bit) | | | | | |
| 0x35 | RW | AOI_HYSX | 0x00 | HYS_X[3:0] | | | | - | ZCMP | YCMP | XCMP | | |
| 0x36 | RW | AOI_HYSZY | 0x00 | HYS_Z[3:0] | | | | HYS_Y[3:0] | | | | | |
| 0x37 | RW | TAP_CFG | 0x00 | -- | -- | ZDEN | ZSEN | YDEN | YSEN | XDEN | XSEN | | |
| 0x38 | RW | TAP_THS | 0x00 | -- | TAP_THRESH[6:0] | | | | | | | | |
| 0x39 | RW | TAP_LIMIT | 0x00 | TAP_LIMIT[7:0] (10ms/LSB) | | | | | | | | | |
| 0x3A | RW | TAP_LAT | 0x00 | TAP_LATENCY[7:0] (10ms/LSB) | | | | | | | | | |
| 0x3B | RW | TAP_WIN | 0x00 | TAP_WINDOW[7:0] (10ms/LSB) | | | | | | | | | |
| 0x3C | RW | SIGM_THS | 0x00 | -- | SIGM_THRESH[6:0] | | | | | | | | |
| 0x3D | RW | SIGM_TIME | 0x00 | -- | -- | -- | -- | PROOF_TIME[1:0] | | SKIP_TIME[1:0] | | | |

Register Table

Register 0x00 (WHOAMI)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|----------|-------|-------|-------|-------|-------|-------|-------|
| WHO AM I | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|--------|---------|-------------|
| [7:0] | R | WHOAMI | 0x33 | Chip ID. |

Register 0x01 (IRQ_STS)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|----------|---------|---------|---------|---------|----------|-------|
| -- | STS_SIGM | STS_TAP | STS_AOI | STS_OVN | STS_WTM | STS_DRDY | -- |

| Bit | Type | Name | Default | Description |
|-----|------|----------|---------|---|
| 6 | R | STS_SIGM | 0 | Significant motion. 1 : Significant motion is detected. |
| 5 | R | STS_TAP | 0 | Tap Sensing. 1 : Single or double tapping is detected. |
| 4 | R | STS_AOI | 0 | AND/OR interrupt (Shock/Freefall/Profile/Gesture) 1 : Configured AOI motion is detected. |
| 3 | R | STS_OVN | 0 | FIFO overrun. 1 : FIFO is full. |
| 2 | R | STS_WTM | 0 | FIFO water mark. 1 : FIFO is filled up to watermark threshold. |
| 1 | R | STS_DRDY | 0 | Data ready. 1 : Axis sample ready. |

Register 0x02 (MODE_STS)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-------|-------|---------|-------|----------|-------|----------|
| -- | -- | -- | PO_DRDY | -- | STS_MEAS | -- | STS_STBY |

| Bit | Type | Name | Default | Description |
|-----|------|----------|---------|--|
| 4 | R | PO_DRDY | 0 | Data ready. 1 : Axis sample ready. The difference between STS_DRDY and DRDY is that reading IRQ_STATUS will clear all interrupt source but reading MODE_STATUS only clear data ready flag. If user captures data by interrupt, it is suggested to read IRQ_STATUS. If user captures data by polling, it is suggested to poll MODE_STATUS. |
| 2 | R | STS_MEAS | 0 | Measurement mode status. 1 : Operation mode is in the measurement mode |
| 0 | R | STS_STBY | 0 | Power down mode status 1 : Operation mode is in the power down mode |

Register 0x07 (CTRL_CFG0)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-------|-------|-----------|-------|-------|-------|-------|
| -- | -- | -- | SELF_TEST | -- | -- | | |

| Bit | Type | Name | Default | Description |
|-----|------|-----------|---------|-------------------------|
| 4 | RW | SELF_TEST | 0 | Self-Test 1 : Enable |

Register 0x08 (MODE_CFG)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-------|-------|--------|-------|-------|--------------|-------|
| -- | -- | -- | SW_RST | -- | -- | MEASURE[1:0] | |

| Bit | Type | Name | Default | Description |
|-------|------|---------|---------|---|
| 4 | RW | SW_RST | 0 | Soft reset 1 : Enable |
| [1:0] | RW | MEASURE | 00 | Operation mode selection. 2 : Enter normal measurement mode. 1 : Enter wakeup mode. 0 : Enter power down mode. |

Register 0x09 (CTRL_CFG1)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|----------|-------|-------|-------|-------|-------|-------|
| -- | ODR[2:0] | | | HR | ZEN | YEN | XEN |

| Bit | Type | Name | Default | Description |
|-------|------|------|---------|---|
| [6:4] | RW | ODR | 000 | Output data rate (Operation mode is in the measure mode) 6 : 400Hz 5 : 200Hz 4 : 100Hz 3 : 50Hz 2 : 25Hz 1 : 12.5Hz 0 : 6.25Hz |
| 3 | RW | HR | 0 | Low pass filter enable 1 : Enable low pass filter |
| 2 | RW | ZEN | 1 | Z Axis enable 1 : Enable Z Axis capturing. |
| 1 | RW | YEN | 1 | Y Axis enable 1 : Enable Y Axis capturing. |
| 0 | RW | XEN | 1 | X Axis enable 1 : Enable X Axis capturing. |

Register 0x0A (CTRL_CFG2)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|--------|--------|--------|--------|----------|----------|-----------------|-------|
| I2_ACT | I2_SLP | I1_ACT | I1_SLP | IRQ2_POL | IRQ1_POL | FULL_SCALE[1:0] | |

| Bit | Type | Name | Default | Description |
|-------|------|----------|---------|---|
| 7 | RW | I2_ACT | 0 | Active status map to INT2 1 : Enable the active status map to INT2. Active is defined as the operation mode in wakeup mode switches to measurement mode. |
| 6 | RW | I2_SLP | 0 | Inactive status map to INT2 1 : Enable the inactive status map to INT2. Inactive is defined as the operation mode in measurement mode switches to wakeup mode. |
| 5 | RW | I1_ACT | 0 | Active status map to INT1 1 : Enable the active status map to INT1. |
| 4 | RW | I1_SLP | 0 | Inactive status map to INT1 1 : Enable the inactive status map to INT1. |
| 3 | RW | IRQ2_POL | 0 | INT2 polarity. 1 : Interrupt flag is Low active. 0 : Interrupt flag is High active. |
| 2 | RW | IRQ1_POL | 0 | INT1 polarity. 1 : Interrupt flag is Low active. 0 : Interrupt flag is High active. |
| [1:0] | RW | FSCALE | 00 | Measurement full scale range. 3 : ±16g 2 : ±8g 1 : ±4g 0 : ±2g |

Register 0x0B (CTRL_CFG3)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-----------------|-------|-------|-------|-----------------|-------|-------|-------|
| LATCH2_SEL[3:0] | | | | LATCH1_SEL[3:0] | | | |

| Bit | Type | Name | Default | Description |
|-------|------|----------|---------|--|
| [7:4] | RW | LAT2_SEL | 0000 | INT2 latch duration selection. 15 : 20.5sec 14 : 10.25sec 13 : 5.1sec 12 : 2.5sec 11 : 1.3sec 10 : 640msec 9 : 320msec 8 : 160msec 7 : 80msec 6 : 40msec 5 : 20msec 4 : 10msec 3 : 5msec 2 : 2.5msec 1 : Latched (Interrupt is cleared after IRQ_STATUS is read) 0 : Non-Latched (Interrupt pulse width is about 25μsec) |
| [3:0] | RW | LAT1_SEL | 0000 | INT1 latch duration selection. 15 to 0 : Same as INT2 latch duration selection. |

Register 0x10 (XDATA_L)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|------------|-------|-------|-------|-------|-------|-------|-------|
| XDATA[3:0] | | | | 0000 | | | |

| Bit | Type | Name | Default | Description |
|-------|------|---------|---------|---------------------------|
| [7:4] | R | XDATA_L | 0000 | LSB 4bits data of X axis. |

Register 0x11 (XDATA_H)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| XDATA[11:4] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|---------|-----------|---------------------------|
| [7:0] | R | XDATA_H | 0000 0000 | MSB 8bits data of X axis. |

Register 0x12 (YDATA_L)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|------------|-------|-------|-------|-------|-------|-------|-------|
| YDATA[3:0] | | | | 0000 | | | |

| Bit | Type | Name | Default | Description |
|-------|------|---------|---------|---------------------------|
| [7:4] | R | YDATA_L | 0000 | LSB 4bits data of Y axis. |

Register 0x13 (YDATA_H)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| YDATA[11:4] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|---------|-----------|---------------------------|
| [7:0] | R | YDATA_H | 0000 0000 | MSB 8bits data of Y axis. |

Register 0x14 (ZDATA_L)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|------------|-------|-------|-------|-------|-------|-------|-------|
| ZDATA[3:0] | | | | 0000 | | | |

| Bit | Type | Name | Default | Description |
|-------|------|---------|---------|---------------------------|
| [7:4] | R | ZDATA_L | 0000 | LSB 4bits data of Z axis. |

Register 0x15 (ZDATA_H)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| ZDATA[11:4] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|---------|-----------|---------------------------|
| [7:0] | R | ZDATA_H | 0000 0000 | MSB 8bits data of Z axis. |

Register 0x16 (FIFO_UNRD)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|------------------|-------|-------|-------|-------|-------|-------|-------|
| FIFO_UNREAD[7:0] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|-----------|-----------|--|
| [7:0] | R | FIFO_UNRD | 0000 0000 | FIFO unread number. Number of frames are still in the FIFO and haven't been read out. |

Register 0x17 (FIFO_STS)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| -- | -- | -- | -- | -- | OVN | WTM | EMPTY |

| Bit | Type | Name | Default | Description |
|-----|------|-------|---------|--|
| 2 | R | OVN | 0 | FIFO overrun. 1 : FIFO is full. The difference between STS_OVN and OVN is that reading IRQ_STATUS will clear all interrupt source but reading FIFO_STATUS only check the status of FIFO. |
| 1 | R | WTM | 0 | FIFO water mark. 1 : FIFO is filled up to water mark threshold. The difference between STS_WTM and WTM is that reading IRQ_STATUS will clear all interrupt source but reading FIFO_STATUS only check the status of FIFO. |
| 0 | R | EMPTY | 0 | FIFO empty. 1 : FIFO is empty. |

Register 0x18 (AOI_STS1)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|--------|-------|-------|-------|-------|-------|-------|-------|
| PO_AOI | -- | ZH | ZL | YH | YL | XH | XL |

| Bit | Type | Name | Default | Description |
|-----|------|--------|---------|---|
| 7 | R | PO_AOI | 0 | Polling AOI status. 1 : AOI is valid. 0 : AOI is invalid. |
| 5 | R | ZH | 0 | Z high 1 : Z axis is higher than THSZ if COMP_Z[1] = 0 1 : Z axis is located in positive THSZ ± HYSZ range if COMP_Z[1] = 1 |
| 4 | R | ZL | 0 | Z low 1 : Z axis is lower than THSZ if COMP_Z[1] = 0 1 : Z axis is located in negative THSZ ± HYSZ range if COMP_Z[1] = 1 |
| 3 | R | YH | 0 | Y high 1 : Y axis is higher than THSY if COMP_Y[1] = 0 1 : Y axis is located in positive THSY ± HYSY range if COMP_Y[1] = 1 |
| 2 | R | YL | 0 | Y low 1 : Y axis is lower than THSY if COMP_Y[1] = 0 1 : Y axis is located in negative THSY ± HYSY range if COMP_Y[1] = 1 |
| 1 | R | XH | 0 | X high 1 : X axis is higher than THSX if COMP_X[1] = 0 1 : X axis is located in positive THSX ± HYSX range if COMP_X[1] = 1 |
| 0 | R | XL | 0 | X low 1 : X axis is lower than THSX if COMP_X[1] = 0 1 : X axis is located in negative THSX ± HYSX range if COMP_X[1] = 1 |

Register 0x19 (AOI_STS2)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-------|-------|-------|-------|--------|--------|--------|
| -- | -- | -- | -- | -- | SIGN_Z | SIGN_Y | SIGN_X |

| Bit | Type | Name | Default | Description |
|-----|------|--------|---------|--|
| 2 | R | SIGN_Z | 0 | Signed bit of Z axis. 1 : Z axis is higher than THSZ and is a positive value. 0 : Z axis is higher than THSZ and is a negative value. This bit is valid when COMP_Z is set to 00. |
| 1 | R | SIGN_Y | 0 | Signed bit of Y axis. 1 : Y axis is higher than THSY and is a positive value. 0 : Y axis is higher than THSY and is a negative value. This bit is valid when COMP_Y is set to 00. |
| 0 | R | SIGN_X | 0 | Signed bit of X axis. 1 : X axis is higher than THSX and is a positive value. 0 : X axis is higher than THSX and is a negative value. This bit is valid when COMP_X is set to 00. |

Register 0x1A (TAP_STS)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|--------|-------|--------|--------|-------|-------|-------|-------|
| PO_TAP | - | DCLICK | SCLICK | SIGN | ZTAP | YTAP | XTAP |

| Bit | Type | Name | Default | Description |
|-----|------|--------|---------|--|
| 7 | R | PO_TAP | 0 | Polling TAP status. 1 : TAP is valid. 0 : TAP is invalid. |
| 5 | R | DCLICK | 0 | Double click status. 1 : Double tapping is detected. |
| 4 | R | SCLICK | 0 | Single click status. 1 : Single tapping is detected. |
| 3 | R | SIGN | 0 | Signed bit of the click. 1 : Positive tapping. 0 : Negative tapping. |
| 2 | R | ZTAP | 0 | Z Click status. 1 : Z axis tapping is detected. |
| 1 | R | YTAP | 0 | Y Click status. 1 : Y axis tapping is detected. |
| 0 | R | XTAP | 0 | X Click status. 1 : X axis tapping is detected. |

Register 0x20 (IRQ1_MAP)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|---------|--------|--------|--------|--------|---------|-------|
| -- | I1_SIGM | I1_TIA | I1_AOI | I1_OVN | I1_WTM | I1_DRDY | -- |

| Bit | Type | Name | Default | Description |
|-----|------|---------|---------|---|
| 6 | RW | I1_SIGM | 0 | Significant motion. 1 : Maps significant motion status to INT1 pin. |
| 5 | RW | I1_TIA | 0 | Tap sensing. 1 : Maps tapping status to INT1 pin. |
| 4 | RW | I1_AOI | 0 | AND/OR interrupt (Shock/Freefall/Display Profile/Gesture) 1 : Maps AOI status to INT1 pin. |
| 3 | RW | I1_OVN | 0 | FIFO overrun. 1 : Maps FIFO full flag to INT1 pin. |
| 2 | RW | I1_WTM | 0 | FIFO water mark. 1 : Maps FIFO WTM flag to INT1 pin. |
| 1 | RW | I1_DRDY | 0 | Data ready. 1 : Maps data ready flag to INT1 pin. |

Register 0x21 (IRQ2_MAP)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|---------|--------|--------|--------|--------|---------|-------|
| -- | I2_SIGM | I2_TIA | I2_AOI | I2_OVN | I2_WTM | I2_DRDY | -- |

| Bit | Type | Name | Default | Description |
|-----|------|---------|---------|---|
| 6 | RW | I2_SIGM | 0 | Significant motion. 1 : Maps significant motion status to INT2 pin. |
| 5 | RW | I2_TIA | 0 | Tap sensing. 1 : Maps tapping status to INT2 pin. |
| 4 | RW | I2_AOI | 0 | AND/OR interrupt (Shock/Freefall/Display Profile/Gesture) 1 : Maps AOI status to INT2 pin. |
| 3 | RW | I2_OVN | 0 | FIFO overrun. 1 : Maps FIFO full flag to INT2 pin. |
| 2 | RW | I2_WTM | 0 | FIFO water mark. 1 : Maps FIFO WTM flag to INT2 pin. |
| 1 | RW | I2_DRDY | 0 | Data ready. 1 : Maps data ready flag to INT2 pin. |

Register 0x22 (FIFO_CFG)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|---------|---------|----------------|-------|----------------|-------|---------------|-------|
| FIFO_EN | FIFO_HR | FIFO_MODE[1:0] | | FIFO_SKIP[1:0] | | TRIG_SRC[1:0] | |

| Bit | Type | Name | Default | Description |
|-------|------|-----------|---------|--|
| 7 | RW | FIFO_EN | 0 | FIFO function enable. 1 : Start record data frames into FIFO. |
| 6 | RW | FIFO_HR | 0 | FIFO resolution mode. 1 : 12bits data content is recorded in FIFO. 0 : MSB 8bits data content is recorded in FIFO. |
| [5:4] | RW | FIFO_MODE | 00 | FIFO mode selection. 3 : Trigger mode (Stream-to-FIFO mode) 2 : Stream mode 1 : FIFO mode 0 : Bypass mode |
| [3:2] | RW | FIFO_SKIP | 00 | FIFO skip frames selection. 3 : Only record one sample per 8 samples, the others are dropped. 2 : Only record one sample per 4 samples, the others are dropped. 1 : Only record one sample per 2 samples, the others are dropped. 0 : Disable skip function. |
| [1:0] | RW | TRIG_SRC | 00 | Trigger mode source selection. 2 : Trigger source is significant motion. 1 : Trigger source is tapping sensing. 0 : Trigger source is AOI detection. |

Register 0x23 (FIFO_THS)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|
| FIFO_THRES[7:0] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|----------|-----------|---------------------------|
| [7:0] | RW | FIFO_THS | 0000 0000 | FIFO water mark threshold |

Register 0x24 (FILTER)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-------|--------|-------|-------|-------|--------|---------|
| -- | -- | UNSIGN | -- | -- | -- | HP_AOI | HP_DATA |

| Bit | Type | Name | Default | Description |
|-----|------|---------|---------|--|
| 5 | RW | UNSIGN | 0 | Unsigned format. 1 : Change data format from 2's complement to unsigned. |
| 1 | RW | HP_AOI | 0 | AOI HPF enable. 1 : AOI source is pass through high pass filter. |
| 0 | RW | HP_DATA | 0 | Data register HPF enable. 1 : Axis data is pass through high pass filter. |

Register 0x30 (AOI_CFG)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-------|-------------|-------|-------------|-------|-------------|-------|
| -- | AOI | COMP_Z[1:0] | | COMP_Y[1:0] | | COMP_X[1:0] | |

| Bit | Type | Name | Default | Description |
|-------|------|--------|---------|---|
| 6 | RW | AOI | 0 | Interrupt AND/OR selection. 1 : AND all three axis conditions. 0 : OR all three axis conditions. |
| [5:4] | RW | COMP_Z | 00 | Z axis comparator selection 3 : Absolute match. Axis is located in any positive or negative range (THSZ ± HYSZ). Ignore signed bit. 2 : Relative match. Axis is located in specific range (THSZ ± HYSZ). Should compare the signed bit. 1 : Lower than. Axis is lower than THSZ. Ignore signed bit. 0 : Higher than. Axis is higher than THSZ. Ignore signed bit. |
| [3:2] | RW | COMP_Y | 00 | Y axis comparator selection. |
| [1:0] | RW | COMP_X | 00 | Z axis comparator selection. |

Register 0x31 (AOI_TIME)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|----------------------|-------|-------|-------|-------|-------|-------|-------|
| AOI_ACTIVE_TIME[7:0] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|----------|-----------|--|
| [7:0] | RW | AOI_TIME | 0000 0000 | AOI active duration. (2.5msec per LSB) |

Register 0x32 (AOI_THSX)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|--------------------------|-------|-------|-------|-------|-------|-------|-------|
| AOI_ACTIVE_THRESH_X[7:0] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|----------|-----------|--|
| [7:0] | RW | AOI_THSX | 0000 0000 | X axis AOI threshold. (2's complement w/ signed bit) |

Register 0x33 (AOI_THSY)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|--------------------------|-------|-------|-------|-------|-------|-------|-------|
| AOI_ACTIVE_THRESH_Y[7:0] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|----------|-----------|--|
| [7:0] | RW | AOI_THSY | 0000 0000 | Y axis AOI threshold. (2's complement w/ signed bit) |

Register 0x34 (AOI_THSZ)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|--------------------------|-------|-------|-------|-------|-------|-------|-------|
| AOI_ACTIVE_THRESH_Z[7:0] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|----------|-----------|--|
| [7:0] | RW | AOI_THSZ | 0000 0000 | Z axis AOI threshold. (2's complement w/ signed bit) |

Register 0x35 (AOI_HYSX)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| AOI_HYS_X[3:0] | | | | -- | ZCMP | YCMP | XCMP |

| Bit | Type | Name | Default | Description |
|-------|------|----------|---------|---|
| [7:4] | RW | AOI_HYSX | 0000 | X axis hysteresis selection. 15 to 8 : 128 to 1008mg, 128mg per step for tolerance range. 7 to 0 : 0 to 112mg, 16mg per step for hysteresis |
| 2 | RW | ZCMP | 0 | Z Axis AOI Comparison enable. 1 : Enable 0 : Disable |
| 1 | RW | YCMP | 0 | Y axis AOI comparison enable. 1 : Enable 0 : Disable |
| 0 | RW | XCMP | 0 | X axis AOI comparison enable. 1 : Enable 0 : Disable |

Register 0x36 (AOI_HYSZY)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|----------------|-------|-------|-------|----------------|-------|-------|-------|
| AOI_HYS_Z[3:0] | | | | AOI_HYS_Y[3:0] | | | |

| Bit | Type | Name | Default | Description |
|-------|------|----------|---------|---|
| [7:4] | RW | AOI_HYSZ | 0000 | Z axis hysteresis selection. 15 to 8 : 128 to 1008mg, 128mg per step for tolerance range. 7 to 0 : 0 to 112mg, 16mg per step for hysteresis |
| [3:0] | RW | AOI_HYSY | 0000 | Y axis hysteresis selection. 15 to 8 : 128 to 1008mg, 128mg per step for tolerance range. 7 to 0 : 0 to 112mg, 16mg per step for hysteresis |

Register 0x37 (TAP_CFG)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| -- | -- | ZDEN | ZSEN | YDEN | YSEN | XDEN | XSEN |

| Bit | Type | Name | Default | Description |
|-----|------|------|---------|--|
| 5 | RW | ZDEN | 0 | Z axis double tapping enable. 1 : Enable 0 : Disable |
| 4 | RW | ZSEN | 0 | Z axis single tapping enable. 1 : Enable 0 : Disable |
| 3 | RW | YDEN | 0 | Y axis double tapping enable. 1 : Enable 0 : Disable |
| 2 | RW | YSEN | 0 | Y axis single tapping enable. 1 : Enable 0 : Disable |
| 1 | RW | XDEN | 0 | X axis double tapping enable. 1 : Enable 0 : Disable |
| 0 | RW | XSEN | 0 | X axis single tapping enable. 1 : Enable 0 : Disable |

Register 0x38 (TAP_THS)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-----------------|-------|-------|-------|-------|-------|-------|
| -- | TAP_THRESH[6:0] | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|---------|----------|-----------------------------|
| [6:0] | RW | TAP_THS | 000 0000 | Tapping detected threshold. |

Register 0x39 (TAP_LIMIT)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| TAP_LIMIT[7:0] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|-----------|-----------|---------------------------------------|
| [7:0] | RW | TAP_LIMIT | 0000 0000 | Tapping pulse window (10msec per LSB) |

Register 0x3A (TAP_LAT)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|------------------|-------|-------|-------|-------|-------|-------|-------|
| TAP_LATENCY[7:0] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|---------|-----------|---|
| [7:0] | RW | TAP_LAT | 0000 0000 | Tapping quiet window that wrap around the event. (10msec per LSB) |

Register 0x3B (TAP_WIN)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-----------------|-------|-------|-------|-------|-------|-------|-------|
| TAP_WINDOW[7:0] | | | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|---------|-----------|---|
| [7:0] | RW | TAP_WIN | 0000 0000 | Tapping interval window between two successive events. (10msec per LSB) |

Register 0x3C (SIGM_THS)

| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-------|------------------|-------|-------|-------|-------|-------|
| -- | | SIGM_THRESH[6:0] | | | | | |

| Bit | Type | Name | Default | Description |
|-------|------|----------|----------|---|
| [6:0] | RW | SIGM_THS | 000 0000 | Significant motion detected threshold. The significant motion detection is enabled when the SIGM_THS is set to non-zero value. |

Register 0x3D (SIGM_TIME)

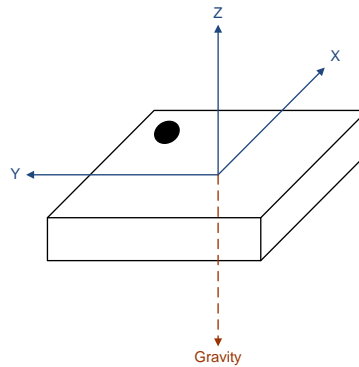
| Bit-7 | Bit-6 | Bit-5 | Bit-4 | Bit-3 | Bit-2 | Bit-1 | Bit-0 |
|-------|-------|-------|-------|-----------------|-------|----------------|-------|
| -- | -- | -- | -- | PROOF_TIME[1:0] | | SKIP_TIME[1:0] | |

| Bit | Type | Name | Default | Description |
|-------|------|-------|---------|--|
| [3:2] | RW | PROOF | 00 | Significant motion proof time. 3 : 1.92sec 2 : 0.96sec 1 : 0.48sec 0 : 0.24sec |
| [1:0] | RW | SKIP | 00 | Significant motion skip time. 3 : 10.24sec 2 : 5.12sec 1 : 2.56sec 0 : 1.28sec |

Sensing Axes Orientation

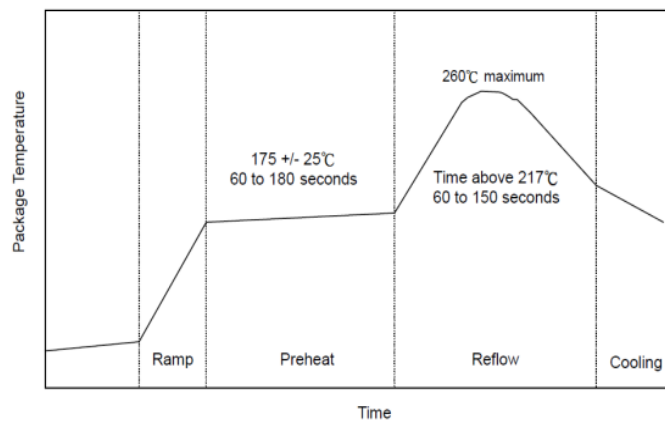
The sensor is at rest in gravity field according to the following figure, and the output signals are :

- 0g for the X-axis
- 0g for the Y-axis
- +1g for the Z-axis



Soldering Guidelines

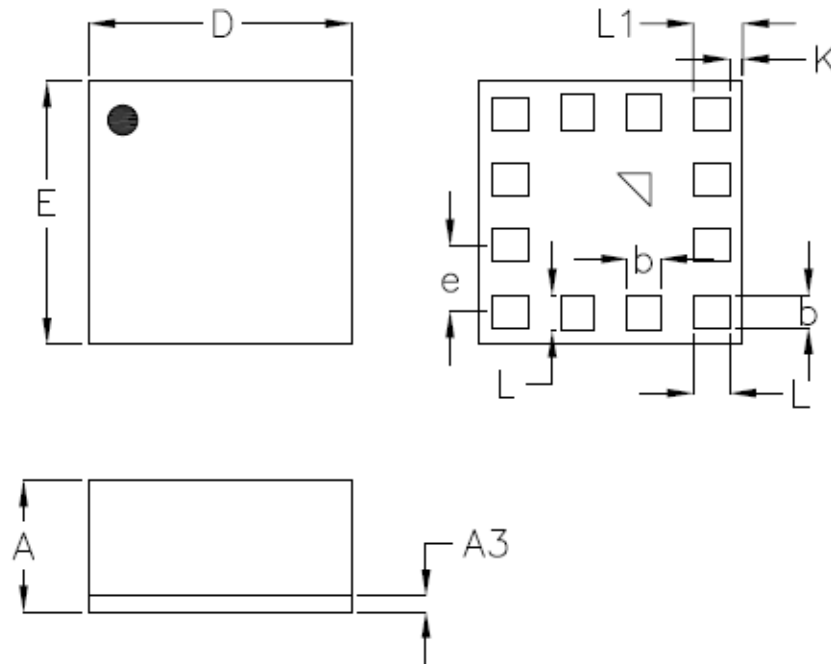
| Condition | Contents |
|--|-------------------|
| Preheat temperature 175 (±25)°C | 60 to 180 seconds |
| Temperature maintained above 217°C | 60 to 150 seconds |
| Time within 5°C of actual peak temperature | 20 to 40 seconds |
| Peak temperature | 260°C |
| Ramp-down rate | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |



Layout Considerations

- ▶ No extra traces and components under the device.
- ▶ Do not place any components or vias at a distance less than 2mm from the device.
- ▶ The solder mask opening must be larger than the land pad.
- ▶ Use a pick and place machine and the solder paste thickness must be as uniform as possible to avoid uneven stress.

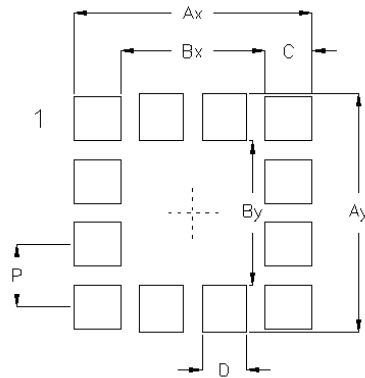
Outline Dimensions



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.855 | 0.995 | 0.034 | 0.039 |
| A3 | 0.100 | 0.150 | 0.004 | 0.006 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| D | 1.900 | 2.100 | 0.075 | 0.083 |
| E | 1.900 | 2.100 | 0.075 | 0.083 |
| e | 0.500 | | 0.020 | |
| L | 0.225 | 0.325 | 0.009 | 0.013 |
| L1 | 0.325 | 0.425 | 0.013 | 0.017 |
| K | 0.100 | | 0.004 | |

12L LGA 2x2 Package

Footprint Information



| Package | Number of Pin | Footprint Dimension (mm) | | | | | | | Tolerance |
|-----------|---------------|--------------------------|------|------|------|------|------|------|-----------|
| | | P | Ax | Ay | Bx | By | C | D | |
| LGA2x2-12 | 12 | 0.50 | 1.90 | 1.90 | 1.15 | 1.15 | 0.40 | 0.35 | ±0.05 |

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