MAX20067

Automotive 3-Channel Display Bias IC with VCOM Buffer, Level Shifter, and I2C Interface

General Description

The MAX20067 IC is a complete TFT bias solution for automotive applications. It includes a current-mode boost converter and two push-pull charge-pump drivers.

The IC also includes a gate-shading push-pull level shifter that can be used to improve display uniformity (when needed), and a DAC and VCOM buffer. All blocks on the IC can be used in stand-alone mode or through the I2C interface.

Comprehensive control functions are included using the built-in I2C interface, as well as diagnostics and monitoring.

The IC is intended to operate with 2.7V to 5.5V supplies.

The MAX20067 is available in a 32-pin TQFN package and operates in the -40°C to +105°C temperature range.

Applications

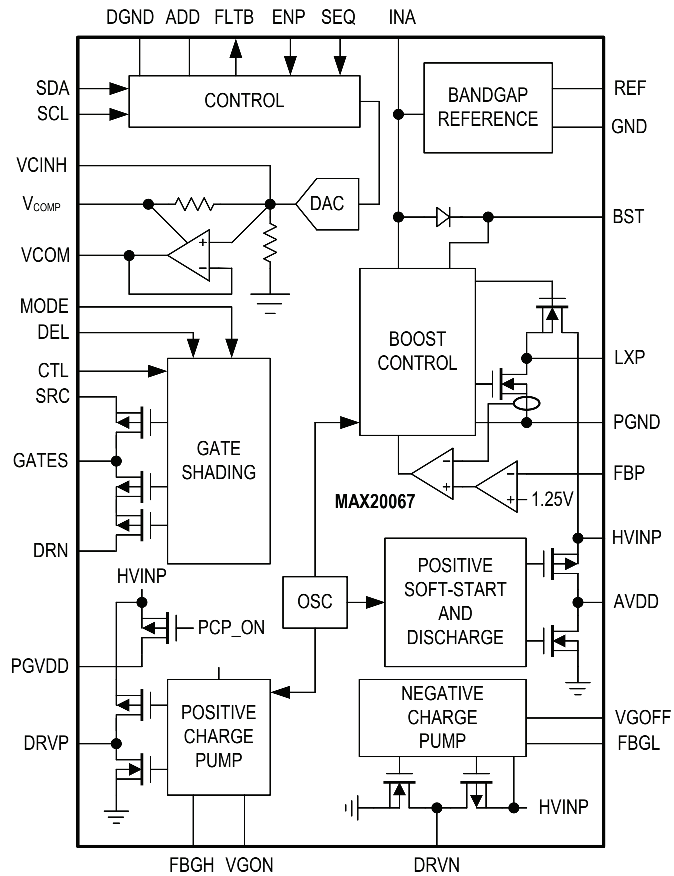
- Infotainment Displays
- Central Information Displays
- Instrument Clusters

Ordering Information appears at end of data sheet.

Benefits and Features

- Versatile TFT Display Power Section
  - Integrated Synchronous Boost Converter with Output Voltages Up to 18V
  - Integrated Charge-Pump Drivers for the VGON (+36V, max) and VGOFF (-24V, min) Outputs
- Low EMI Operation
  - Programmable Switching Frequencies of 440kHz or 2.2MHz
  - Programmable Spread Spectrum
- Full Sequencing Flexibility Through I2C, Along with Preset Sequences Using SEQ Pin
- Extended Diagnostics Using I2C Interface
  - Undervoltage/Overvoltage on HVINP, VGON, and VGOFF
  - Overcurrent on AVDD
  - Temperature Warning
- Built-In Gate-Shading Circuit Controlled by CTL Input
- 8-Bit DAC-Controlled VCOM Buffer
- Robust
  - -40°C to +105°C Operating Temperature Range
  - Internal Temperature Shutdown
  - AEC-Q100 Qualified
- Compact 32-Pin (5mm x 5mm) TQFN Package

Simplified Block Diagram



Absolute Maximum Ratings

INA, SDA, SCL, ENP, FLTB, CTL to GND ....-0.3V to +6V
DEL, REF, FBP, FBGH, FBGL, SEQ,
MODE, ADD to GND ....- 0.3V to INA + 0.3V
LXP, BST to GND ....-0.3V to +26V
BST to LXP...-0.3V to +6V
HVINP, V_{COMP} to GND..-0.3V to +26V
VCINH, VCOM to GND ....-0.3V to V_{COMP} + 0.3V
VCINH to VCOM ....+1V
AVDD, PGVDD to HVINP........................-0.3V to HVINP + 0.3V
VGON, SRC, DRN to GND ....-0.3V to +38V
DRN to GATES...-38V to +38V
GATES to GND ....-0.3V to SRC + 0.3V
VGOFF to GND ....-26V to +0.3V
DRVP, DRVN to PGND ....-0.3V to HVINP + 0.3V
GND to PGND ....-0.3V to +0.3V
GND to DGND...-0.3V to +0.3V
LXP Continuous Current 2.4A
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C)
W to 2.758W
Package Thermal Resistance ....1.7°C/W
ESDHB .... -2kV to +2kV
ESDMM ....-200V to +200V
Operating Temperature ....-40°C to 105°C
Junction Temperature..................................... -40°C to +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature Range...+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

32-Pin TQFN

PACKAGE CODE	T3255+4C
Outline Number	**21-0140**
Land Pattern Number	**90-0012**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	47
Junction to Case (θ_{JC})	1.7
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	29
Junction to Case (θ_{JC})	1.7

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{INA} = 3.6V, limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INA POWER INPUT						
INA Supply Voltage Range	V_{INA}		2.7		5.5	V
INA Undervoltage-Lockout Threshold, Rising	$UVLO_R$		2.45	2.55	2.65	V
INA Undervoltage-Lockout Threshold, Falling	$UVLO_F$			2.45		V
Supply Current	I_{INA}	ENP = 1 or ENP bit = 1, no switching		1.8	3	mA
Shutdown Current	I_{SD}	ENP = 0 and ENP bit = 0, total current INA + HVINP		7	15	µA
OSCILLATOR						
Boost Converter Switching Frequency	f_{SW0}	SWFREQ bit = 0	1.98	2.2	2.42	MHz
Boost Converter Switching Frequency, Low Setting	f_{SW1}	SWFREQ bit = 1	390	440	490	kHz
Frequency Dither		SSOFF bit = 1	-4		+4	%
REFERENCE						
REF Output Voltage	V_{REF}		1.238	1.25	1.262	V
REF Load Regulation		I_{REF} from 0µA to 100µA		10	20	mV
REF Line Regulation		2.7V < V_{INA} < 5.5V, no load			5	mV
BOOST CONVERTER						
AVDD Output Voltage Range	V_{AVDD}		V_{INA} + 1		18	V
LXP Current Limit			2.1	2.5	2.9	A
Low-Side Switch On-Resistance	R_{LXP}			0.2	0.4	Ω
LXP Leakage Current	I_{LXP}	V_{LXP} = 18V, T_A = +25°C			5	µA
Synchronous Rectifier On-Resistance	R_{SYNC}			0.25	0.5	Ω
Synchronous Rectifier Zero-Crossing Threshold	I_{SYNCZ}	2.2MHz		140		mA
Maximum Duty Cycle	DC_{MAX}		90	94	98	%
Current-Limit Ramp Time at Startup	t_{RAMP}			12.5		ms
FBP Regulation Voltage	V_{FPB}		1.225	1.25	1.275	V
FBP Load Regulation		1mA < I_{AVDD} < 200mA		-1		%
FBP Line Regulation		V_{INA} = 2.7V to 5.5V	-0.4		+0.4	%

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FBP Undervoltage-Fault Threshold	V_{FBPUV}		75	80	85	%
FBP Overvoltage-Fault Threshold	V_{FBPOV}		110	115	120	%
FBP Input Bias Current	I_{FBP}				200	nA
HVINP-AVDD Switch On-Resistance	R_{HA}			0.5	1	Ω
AVDD Discharge Resistance	R_{AVDD}		1	1.5	2	kΩ
HVINP-AVDD Switch Current Limit	I_{LIMHA}	After soft-start	240			mA
		During soft-start	120			
POSITIVE CHARGE-PUMP REGULATOR						
PGVDD Operating Voltage Range	V_{PGVDD}		6		18	V
VGON Output Voltage Range	V_{VGON}				36	V
DRVP Current Limit	I_{LIM_P}		40			mA
Positive Charge-Pump Switching Frequency				440		kHz
FBGH Regulation Voltage	V_{FBGH}		1.225	1.25	1.275	V
FBGH Undervoltage-Fault Threshold	V_{FBGHUV}		75	80	85	%
FBGH Overvoltage-Fault Threshold	V_{FBGHOV}		110	115	120	%
DRVP On-Resistance High	R_{ONH_DRVP}				60	Ω
DRVP On-Resistance Low	R_{ONL_DRVP}				30	Ω
HVINP-PGVDD Switch On-Resistance	R_{HP}			30	60	Ω
HVINP-PGVDD Current Limit			40			mA
VGON Discharge Resistance			8	12	16	kΩ
NEGATIVE CHARGE-PUMP REGULATOR						
VGOFF Output Voltage Range			-24		-6	V
DRVN Current Limit	I_{LIMN}		15			mA
Negative Charge-Pump Switching Frequency				440		kHz
FBGL Regulation Voltage	V_{FBGL}	V_{REF} - V_{FBGL}	0.98	1	1.02	V
FBGL Undervoltage-Fault Threshold	V_{FBGLUV}	Rising	400	450	500	mV

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FBGL Overvoltage-Fault Threshold	V_{FBGLOV}	Falling	20	50	100	mV
DRVN On-Resistance High	R_{ONH_DRVN}				60	Ω
DRVN On-Resistance Low					30	Ω
VGOFF Discharge Resistance			8	12	16	kΩ
GATE-SHADING CIRCUIT						
SRC Input Voltage Range	V_{SRC}				36	V
SRC-to-GATES Switch On-Resistance	R_{SRC_GATES}			10	20	Ω
DRN-to-GATES Switch On-Resistance	R_{DRN_GATES}			10	20	Ω
DEL Pullup Current			4	5	6	µA
DEL Enable Threshold				1.25		V
CTL-to-GATES Delay		C_{GATES} = 1nF		150		ns
MODE Switch On-Resistance				1250		Ω
MODE Voltage Threshold		MODE rising	2			V
MODE Pullup Current			80	100	120	µA
MODE Current-Source Stop Threshold				1.7		V
VCOM BUFFER						
V_{COMP} Voltage Range			5		18	V
V_{COMP} Quiescent Supply Current		I_{VCOMP} = 0mA, V_{COMP} = 12V		1.8		mA
VCINH Input Impedance				500		kΩ
VCINH/V_{COMP} Division Ratio				0.5		V/V
VCOM Output Current Limit			130			mA
VCOM Offset Voltage			-8		+8	mV
VCOM Output Voltage Range			1.5		V_{COMP} - 1.5V	V
VCOM DAC Step Size				19.5		mV
VCOM DAC Voltage Range				V_{COMP}/2 +2.5V		V
VCOM Undervoltage-Detection Threshold		VCINH - VCOM, falling	-0.55	-0.35	-0.15	V
VCOM Overvoltage-Detection Threshold		VCINH - VCOM, rising	0.04	0.25	0.41	V

Electrical Characteristics (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCOM Fault Detection Filter Time		tfault[1:0] = 01		60		ms
VCOM Discharge Resistance			6	13	20	kΩ
TFT FAULT PROTECTION						
Fault Timeout		tfault[1:0] = 01		60		ms
Fault Retry Time				2.4		s
FLTB Output Frequency		Stand-alone mode only	0.88	1	1.12	kHz
FLTB Output Duty Cycle, VGON or VGOFF Fault				75		%
FLTB Output Duty Cycle, HVINP Fault				50		%
FLTB Output Duty Cycle, AVDD Fault				25		%
AVDD Undervoltage-Fault Threshold		Relative measurement between HVINP and AVDD	70	75	80	%
FBP Short-Circuit Fault Threshold			30	40	50	%
FBGH Short-Circuit Fault Threshold			30	40	50	%
FBGL Short-Circuit Fault Threshold			0.8	0.85	0.9	V
Short-Circuit and Overload Fault Delay				10		µs
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			165		°C
Thermal-Shutdown Hysteresis	T_{SHDN_HYS}			15		°C
LOGIC INPUT AND OUTPUTS						
FLTB, DEL Low Output Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
FLTB, DEL, SDA Leakage Current	I_{ILEAK}		-1		+1	µA
SDA Output Voltage Low	V_{OLSDA}				0.8	V
ENP Pulldown Resistor Value	R_{ENPPD}		50	75		kΩ
ENP Glitch Filter Time	t_{ENP}			10		µs
ENP, CTL, SCL, SDA, ADD Input Voltage Low	V_{IL}				0.8	V
ENP, CTL, SCL, SDA, ADD Input Voltage High	V_{IH}		2			V

Electrical Characteristics (continued)

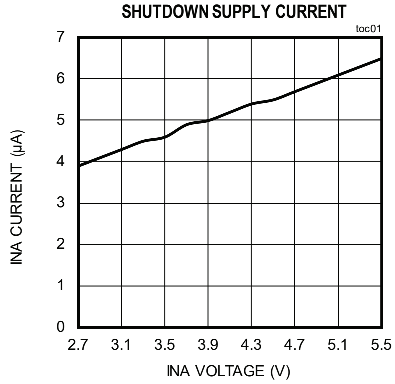
(V_{INA} = 3.6V, limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. T_A = T_J = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I2C INTERFACE						
Clock Frequency	f_{SCL}				400	kHz
Setup Time (Repeated) START	$t_{SU:STA}$		260			ns
Hold Time (Repeated) START	$t_{HD:STA}$		260			ns
SCL Low Time	t_{LOW}		350			ns
SCL High Time	t_{HIGH}		260			ns
Data Setup Time	$t_{SU:DAT}$		50			ns
Data Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU:STO}$		260			ns
Spike Suppression				50		ns

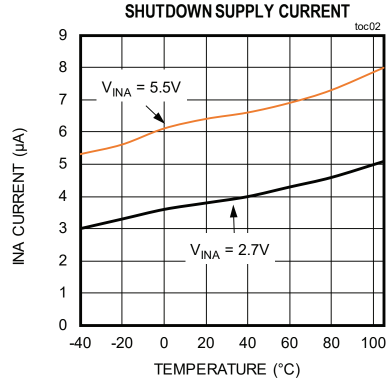
Typical Operating Characteristics

(V_{INA} = 3.3V, f_{SW} = 2.2MHz, C_{VCOM} = 1µF, T_A = +25°C, unless otherwise noted.)

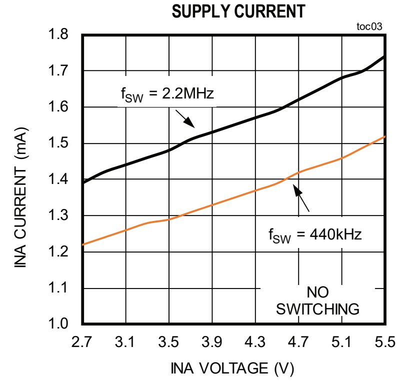
SHUTDOWN SUPPLY CURRENT



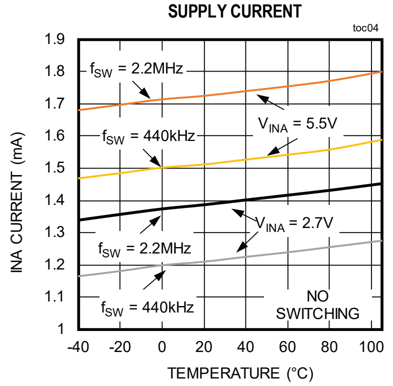
SHUTDOWN SUPPLY CURRENT



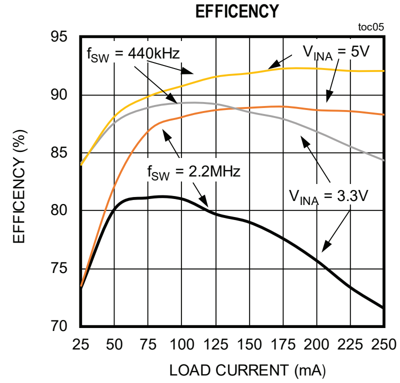
SUPPLY CURRENT



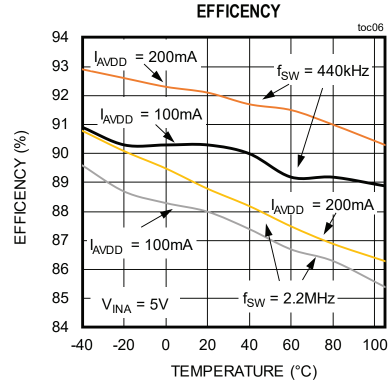
SUPPLY CURRENT



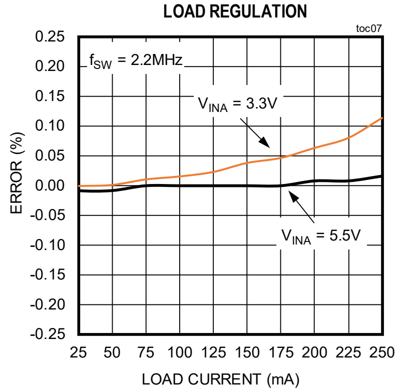
BOOST REGULATOR EFFICENCY



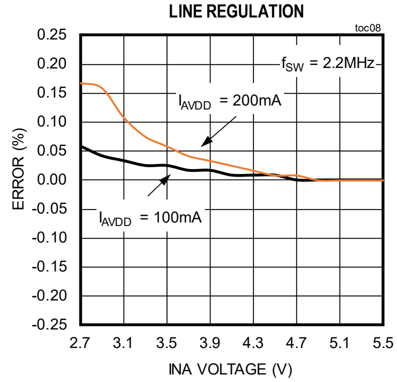
BOOST REGULATOR EFFICENCY



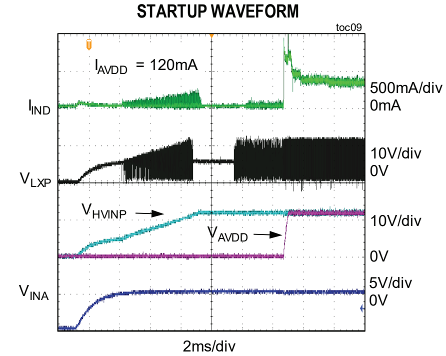
BOOST REGULATOR LOAD REGULATION



BOOST REGULATOR LINE REGULATION

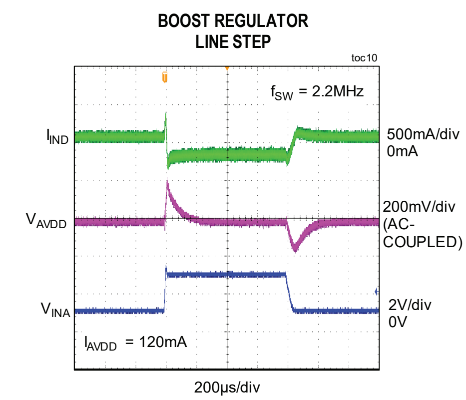


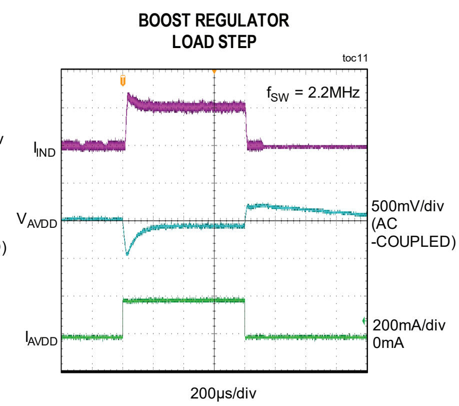
BOOST REGULATOR STARTUP WAVEFORM

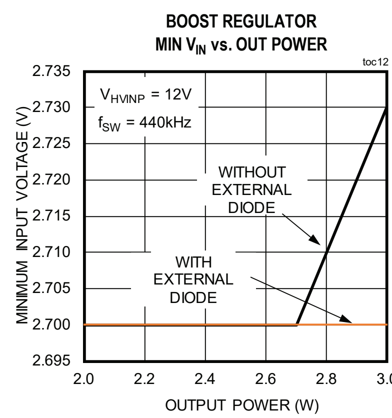


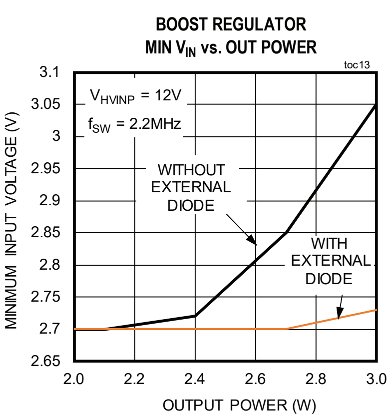
Typical Operating Characteristics (continued)

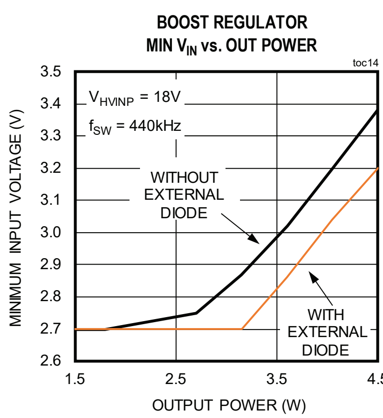
(V_{INA} = 3.3V, f_{SW} = 2.2MHz, C_{VCOM} = 1μF, T_A = +25°C, unless otherwise noted.)

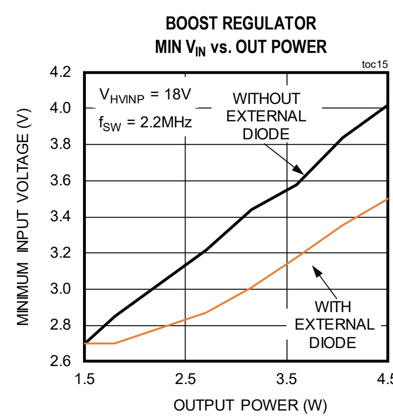


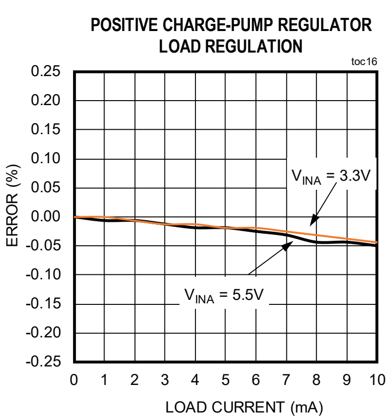


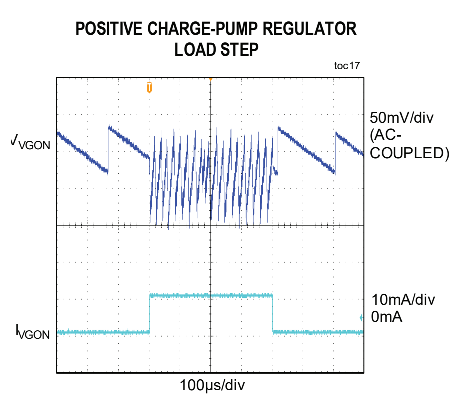


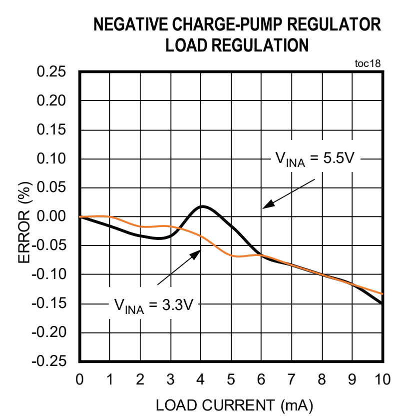








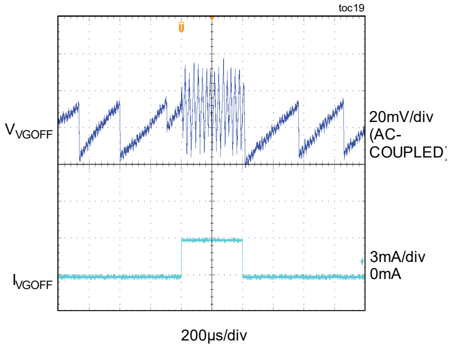




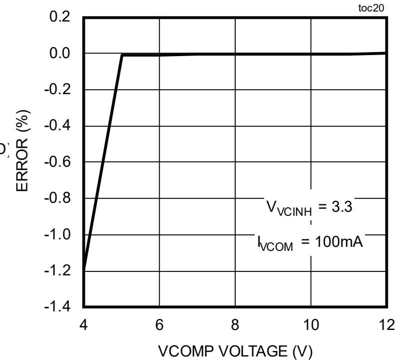
Typical Operating Characteristics (continued)

(V_{INA} = 3.3V, f_{SW} = 2.2MHz, C_{VCOM} = 1µF, T_A = +25°C, unless otherwise noted.)

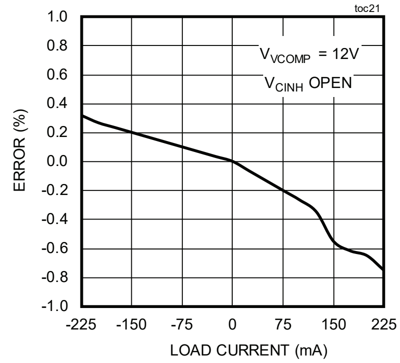
NEGATIVE CHARGE-PUMP REGULATOR LOAD STEP



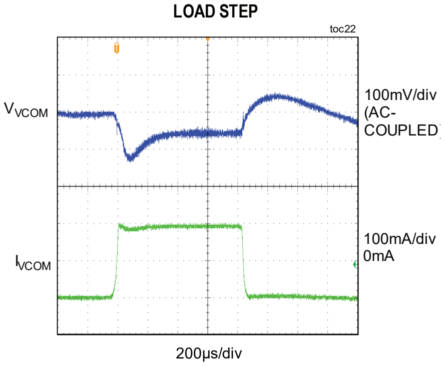
VCOM BUFFER LINE REGULATION



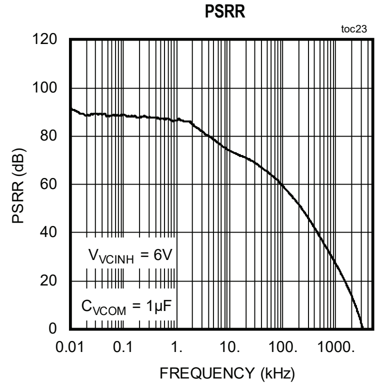
VCOM BUFFER LOAD REGULATION



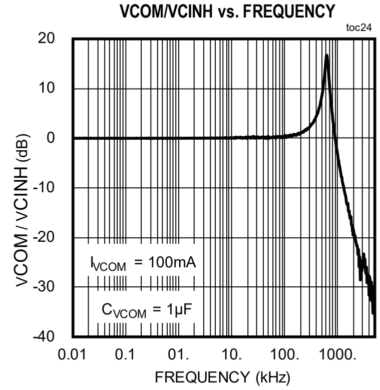
VCOM BUFFER LOAD STEP



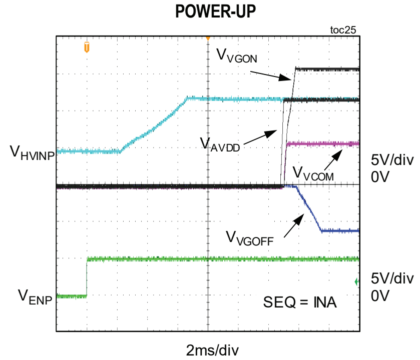
VCOM BUFFER PSRR



VCOM BUFFER VCOM/VCINH vs. FREQUENCY



SUPPLY SEQUENCING WAVEFORMS POWER-UP



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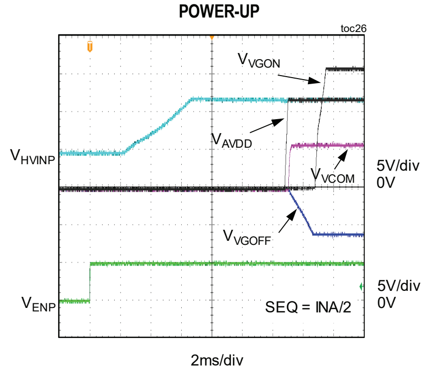
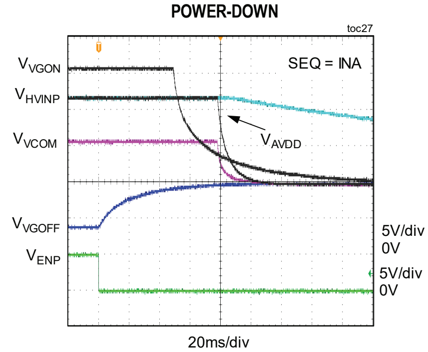


SUPPLY SEQUENCING WAVEFORMS POWER-DOWN



Typical Operating Characteristics (continued)

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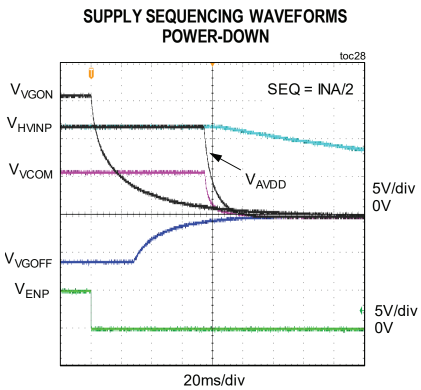
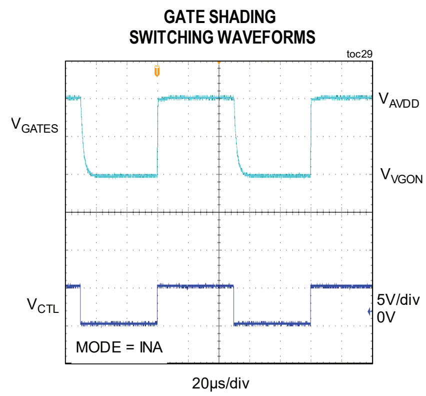
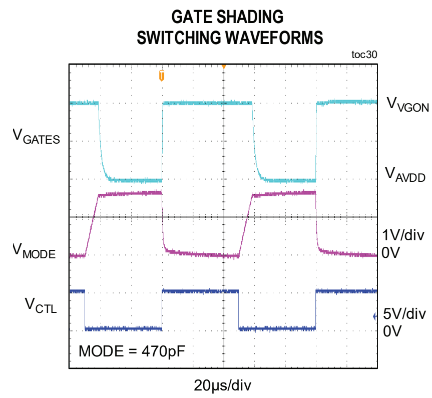
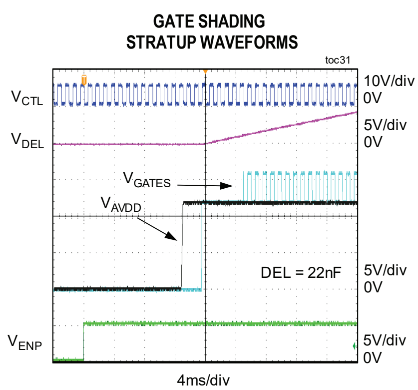
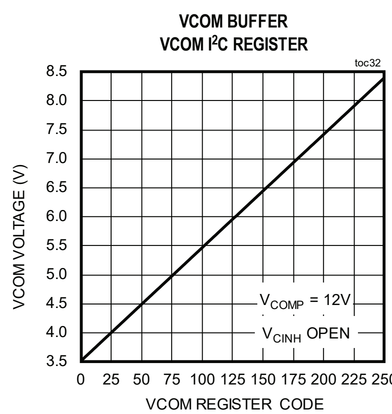


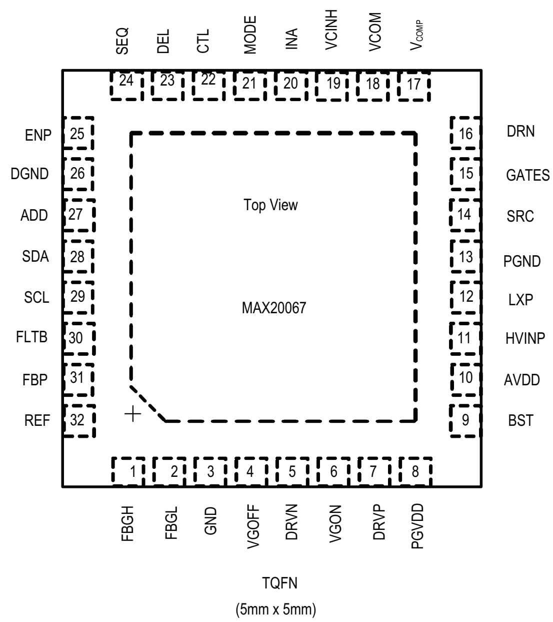








Pin Configuration



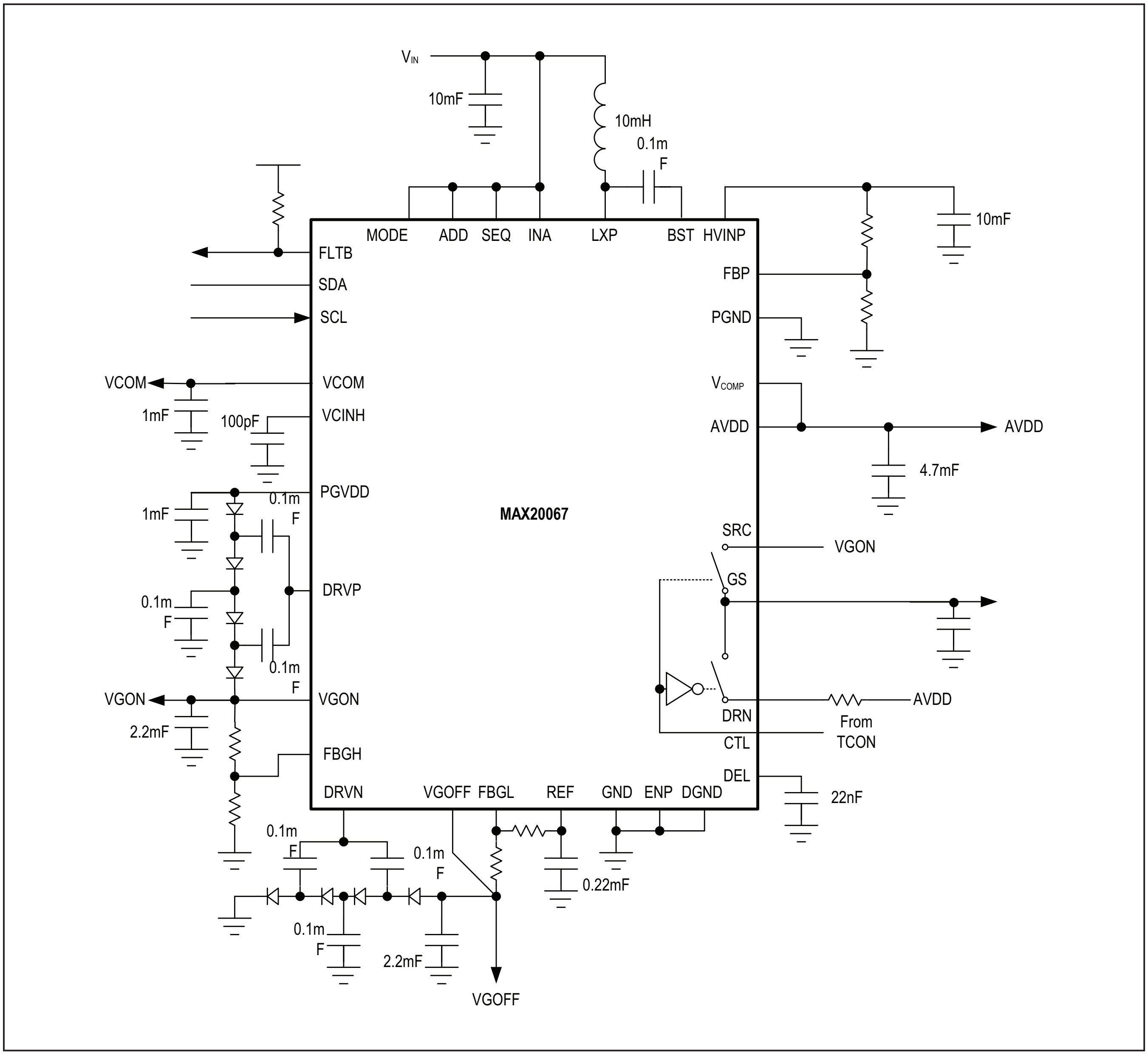
Pin Description

PIN	NAME	FUNCTION
1	FBGH	Positive Charge-Pump Feedback Connection. FBGH is regulated to 1.25V. Connect a resistor-divider from VGON to GND with its midpoint connected to FBGH.
2	FBGL	Negative Charge-Pump Feedback Connection. FBGL is regulated to 0.25V. Connect a resistor-divider from REF to VGOFF with its midpoint connected to FBGL.
3	GND	Ground Connection
4	VGOFF	Output of Negative Charge-Pump Block.
5	DRVN	Negative Charge-Pump Push-Pull Drive Output
6	VGON	Output of Positive Charge-Pump Block
7	DRVP	Positive Charge-Pump Push-Pull Drive Output
8	PGVDD	Supply voltage for positive charge-pump. PGVDD is connected to HVINP by means of an internal switch when the positive charge-pump is enabled. Bypass PGVDD with a ceramic capacitor of at least 1μF to GND.
9	BST	Bootstrap Capacitor Connection for Synchronous Rectifier Driver. Connect a 0.1μF ceramic capacitor between BST and LXP.
10	AVDD	Switched Output of Boost Converter. Connect a bypass capacitor of at least 4.7μF from AVDD to PGND.
11	HVINP	Boost Output and Input to Positive and Negative Charge Pumps. Bypass HVINP with the boost-converter output capacitor placed close to the pin.
12	LXP	Switching Node of Boost Converter. Connect the boost inductor between LXP and INA.
13	PGND	Ground Connection for Boost Switching Device and VCOM Buffer. Connect to GND using a low-impedance trace.

Pin Description (continued)

PIN	NAME	FUNCTION
14	SRC	Source of Internal High-Side Switch in Gate-Shading Circuit. SRC is usually connected to VGON. Bypass SRC with a 0.1μF capacitor placed close to the pin.
15	GATES	Switched Output of Gate-Shading Circuit
16	DRN	Lower Input of Gate-Shading Circuit. Connect to an external source or GND through a discharge resistor.
17	V_{COMP}	Supply Voltage for VCOM Buffer. Normally connected to AVDD. Bypass V_{COMP} with a 0.1μF ceramic capacitor placed close to the pin.
18	VCOM	Output of VCOM Amplifier. Bypass VCOM to GND with a 1μF ceramic capacitor.
19	VCINH	Noninverting Input of VCOM Amplifier. In stand-alone mode, drive VCINH to set the VCOM output voltage. VCINH is prebiased to 50% of V_{COMP} with an internal resistor-divider comprising two 1MΩ resistors.
20	INA	Supply Connection for Display Bias Circuitry. Bypass INA with a local 0.1μF capacitor.
21	MODE	Mode Configuration Pin for Gate-Shading Level Shifter. MODE is used to adjust the timing of the gate-shading output. MODE is high impedance when connected to INA, and internally pulled down during UVLO or in shutdown.
22	CTL	Control Input for Gate-Shading Circuit. When CTL is high, the switch between GATES and SRC is on and the switch between GATES and DRN is off. When CTL is low, the switch between GATES and DRN is on and the switch between GATES and SRC is off. CTL is inhibited by V_{CC} UVLO and when DEL is less than 1.25V.
23	DEL	Gate-Shading Circuit Delay Input. Connect a capacitor from DEL to GND to set the turn-on delay.
24	SEQ	Logic-Level Sequencing Input Pin. The voltage level on SEQ determines whether the IC is serially controlled, or one of the predetermined sequences is used. Connect SEQ to INA or a resistive divider between INA and GND to set one of the preset stand-alone sequences (see Table 3). For serial control, connect SEQ to GND.
25	ENP	Active-High Enable Input for Boost Converter. ENP also enables the VGON and VGOFF regulators in the set sequence. ENP has an internal pulldown resistor. When serial control is used, connect ENP low.
26	DGND	Digital Ground. Connect directly to the exposed pad of the package.
27	ADD	I2C Address-Selection Pin. Connect to GND for a base address of 0x20, or to INA for a base address of 0x28.
28	SDA	Bidirectional I2C Data Pin
29	SCL	Serial-Clock Input
30	FLTB	Open-Drain, Active-Low Fault Output. Connect a pullup resistor from FLTB to a logic supply ≤ 5V. In stand-alone mode, the duty cycle of the FLTB pin indicates an error condition, if present (see Table 4). When the serial interface is used, FLTB is either a 0 (indicating data to be read from the internal registers) or a 1. It does not output a PWM signal.
31	FBP	Boost Feedback Connection. FBP is regulated to 1.25V. Connect a resistor-divider from HVINP to GND with its midpoint connected to FBP.
32	REF	Internal 1.25V Reference Output. Connect a 0.22μF capacitor from REF to GND.
—	EP	Exposed Pad. Connect EP to GND.

Typical Application Circuit



Detailed Description

The MAX20067 is a highly integrated power-supply IC for automotive TFT-LCD applications. The IC integrates one boost converter, two gate-driver supplies, a high-voltage "gate-shading" level shifter, and a high-current VCOM buffer.

The main power-supply section, comprising the boost converter and gate-driver supplies, operates from a 2.7V to 5.5V supply. The boost converter operates at 440kHz or 2.2MHz and has built-in spread spectrum that can be disabled using the serial interface for reducing EMI.

The boost converter provides an output voltage adjustable up to 18V, with up to 200mA output current and has two internal MOSFET switching elements.

The IC provides gate-driver supplies using positive and negative charge-pump regulators, with a current capability of 10mA for the positive charge pump (using a doubler charge pump) and 3mA for the negative charge pump (assuming a 2-stage charge pump). Output voltage is adjustable with a +36V (max) output on the positive charge pump and -22V on the negative charge pump.

The startup and shutdown sequences for all power domains, controlled using one of the preset modes, are selected using the SEQ pin. Sequencing can also be controlled through the serial interface when the SEQ pin is grounded.

TFT Power Section

Source-Driver Power Supplies

The source-driver power supply consists of a boost converter that generates +18V (max) and can deliver up to +200mA. The source-driver power supply's regulation voltage (HVINP) is set by a resistor-divider on FBP. The source driver uses constant-frequency peak-current-mode control, with internal fixed-slope compensation. Internal compensation stabilizes the control loop. At low output power, the converter enters skip mode.

The TFT boost converter has an internal error amplifier with a g_m of 13μS that has FBP and REF = 1.25V as inputs. There is an internal compensation network at the output of the error amplifier as follows:

$$C_C = 140\text{pF}, R_C = 500\text{k}\Omega$$

For the current loop, there is internal current sensing using a transresistance of R_T = 0.21V/A. The current-sense voltage (V_{CS} = I_inductor x R_T) is added to the slope compensation. The slope-compensation signal has a slope of 1250mV per microsecond.The resulting V_{SUM} = V_{CS} + V_{SLOPE} is compared to V_{COMP} (output of the error amplifier) at the input of the PWM comparator to regulate the LXP duty cycle.

Gate-Driver Power Supplies

The positive gate-driver charge pump (VGON) generates +36V (max) and the negative gate-driver charge pump (VGOFF) generates -24V (max). The gate-driver supplies have a current capability of 10mA for the positive charge pump (using a doubler charge pump) and 3mA for the negative charge pump (assuming a 2-stage charge pump). The VGON and VGOFF regulation voltages are both set using the external resistor networks, as shown in the *Typical Application Circuit*. Both charge-pump regulators use a 440kHz switching frequency. The charge pumps regulate the output voltages by controlling the current that flows into the flying capacitors.

Operation of the Positive Charge Pump

The positive charge-pump regulator is typically used to generate the positive supply rail for the TFT-LCD gate-driver ICs.

The output voltage is set with an external resistive voltage-divider from its output to GND, with the midpoint connected to FBGH. The number of charge-pump stages and the setting of the feedback-divider determine the output voltage of the positive charge-pump regulator. The charge pump push-pull output consists of a high-side p-channel MOSFET (P1) and a low-side n-channel MOSFET (N1) to control the power transfer.

The positive charge pump uses a simple skipping control scheme. The feedback signal (FBGH) is compared with a 1.25V internal reference. The result of this comparison is sampled on every clock cycle. If the feedback signal is below 1.25V, a DRVP cycle is initiated. In the first half period, the rising edge of the clock turns on N1 and turns off P1, allowing the flying capacitors to charge, while during the second half period, the falling edge of the clock turns off N1 allowing charge transfer to the output. During both phases, N1 and P1 act as current-limited switches with a current limit of at least 40mA.

Alternatively, if the feedback signal is above 1.25V at the clock rising edge, the regulator ignores the clock period and N1 and P1 remain off.

The charge-pump regulator also includes a discharge switch from VGON to ground, turned off to discharge the output capacitors during the sequential turn-off of the output voltages, as programmed by the SEQ pin or through I^2C. The PGVDD node is internally connected through a switch to the HVINP voltage. See Table 3 for stand-alone sequencing options.

Operation of the Negative Charge Pump

The negative charge-pump regulator is typically used to generate the negative supply rail for the TFT-LCD gate-driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF, with the midpoint connected to FBGL. The number of charge-pump stages and the setting of the feedback-divider determine the output of the negative charge-pump regulator. The charge-pump controller includes a high-side p-channel MOSFET (P1) and a low-side n-channel MOSFET (N1) to control the power transfer.

The feedback signal (FBGL) is compared with a 0.25V internal reference obtained by partitioning the main 1.25V reference. The result of this comparison is sampled on every clock cycle. If (REF - FBGL) is less than 1.25V - 0.25V or 1V, a DRVN cycle is initiated. In the first half period, the rising edge of the clock turns on P1 and turns off N1, allowing the flying capacitors to charge, while during the second half period, the falling edge of the clock turns on N1 and turns off P1 allowing charge transfer to the output. During both phases, N1 and P1 act as current-limited switches with a current limit of at least 15mA.

Alternatively, if (REF - FBGL) is less than 1V at the clock rising edge, the regulator ignores the clock period and N1 and P1 remain off.

For sequencing of the output voltages at turn-off, a discharge switch is connected from VGOFF to ground. The desired sequence is programmable using the SEQ pin or through I2C. See Table 3 for the stand-alone sequencing options.

Fault Protection on the TFT Section

The IC has robust fault and overload protection. If any of the source-driver or gate-driver supplies fall below 80% (typ) or above 115% of the programmed regulation voltage for more than 60ms (typ, default), all the outputs turn off and a fault condition is set. If a short condition occurs on any of the source-driver supplies for more than 10μs, all the outputs turn off and a fault condition is set. A short condition is detected when the output voltage falls below 40% of the intended regulation voltage. The output with the fault turns off immediately, while the other outputs follow the turn-off sequence programmed by the SEQ pin or through I2C. The fault condition is cleared when the ENP pin or INA supply is cycled or after the retry timer (2.4s typ, default) times out, if enabled. If needed, the retry time can be adjusted or this function disabled using the serial interface. In the case of a thermal fault, the IC turns off immediately and remains off until the chip temperature drops by 15°C (typ).

Output Control

The sequencing of the IC's source-driver and gate-driver outputs (AVDD, VGON, and VGOFF) is determined by the setting of the SEQ pin or through I2C. All outputs are brought up with soft-start control to limit the inrush current. Table 3 lists the sequencing options using the SEQ pin.

The outputs are also turned off in sequence, with the boost converter the last block to be disabled. Active pulldowns are provided on all outputs to facilitate a controlled discharge. The pulldowns remain active for 512ms after the boost has been disabled, at which point the IC enters shutdown mode, if applicable.

Power-Up/Power-Down Sequencing and Timing

The IC allows for flexible power-up/power-down sequencing and timing of the source-driver and gate-driver power supplies (AVDD, VGON, and VGOFF). Toggling the ENP pin from low to high initiates an adjustable preset power-up sequence. Alternatively, power-up sequencing can be controlled through I2C. Toggling the ENP pin from high to low initiates the power-down sequence. The ENP pin has an internal deglitching filter of 10μs (typ). **Note:** A glitch in the ENP signal with a period less than 10μs is ignored by the internal enable circuitry.

Gate-Shading Level Shifter

The gate-shading level shifter is enabled when the soft-start of all regulators is completed and the DEL pin exceeds its enable threshold. A capacitor on the DEL pin can be used to adjust the startup-delay time together with the internal 5µA current source. The delay can be calculated using the following equation:

$$DELAY = \frac{(1.25V \times C_{DEL})}{5\mu A}$$

When the IC is disabled, GATES is discharged to GND. After the IC is enabled, the GATES switches are off and GATES is high impedance until the complete power sequence is finished (without a fault occurring) and DEL exceeds 1.25V. When DEL exceeds 1.25V, the level shifter is activated and its state controlled by the CTL and MODE inputs according to Table 1. An external resistor and capacitor are used to produce the desired waveform where the rise of the output signal is fast, but the fall is an exponential decay controlled by the external values of the resistor and capacitor. In addition, a capacitor on the MODE pin can be used to delay the fall of the GATES output.

Connect MODE to INA when the V_{GGS} delay is not needed. Connect a capacitor from MODE to GND to set the delay according to the following equation:

$$C_{MODE} = \frac{(100\mu A \times t_{DMODE})}{1.75V}$$

where t_{DMODE} is the desired delay if the level shifter is not used to connect CTL to GND.

VCOM Buffer

The VCOM buffer is enabled when AVDD crosses its power-good threshold. The VCOM positive supply is V_{COMP}, which is normally externally connected to the AVDD output, while its negative supply is ground. The output voltage is set by default to half of V_{COMP} through two 1000kΩ internal resistors. The VCOM buffer can be controlled either by driving the VCINH pin or using the internal DAC that is written to through the serial interface. When driving the VCINH pin, the source impedance or the resistance of the external resistor-divider should be much lower than 500kΩ. In DAC mode, an 8-bit value is written through I2C, which sets the VCOM output voltage in a nominal range of ±2.5V around AVDD/2. Table 2 shows the correspondence between the DAC value written and the VCOM output voltage. The VCOM output can source or sink a current up to a peak of 130mA. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the buffer. In a short-circuit condition, the power dissipation of the VCOM buffer can lead to complete thermal shutdown of the IC.

The VCOM buffer should be used with an external 1µF ceramic capacitor connected from its output to GND.

A VCOM buffer fault is detected if the voltage difference between VCINH and the VCOM output pin is greater than 250mV. The VCOM fault detection is filtered internally and a VCOM buffer fault is latched. To clear a fault, write a 0 to the corresponding fault bit. In stand-alone mode, toggle the ENP pin or power down the device and then power it on again.

Table 1. Gate-Shading Operating Modes

CTL	MODE	GATES OUTPUT	CMODE DISCHARGE
Low	High	GATES shorted to DRN using internal device	—
High	High	GATES shorted to SRC using internal device	—
Low	Low	GATES shorted to DRN using internal device	Off
High	Low	GATES shorted to SRC using internal device	On

Table 2. VCOM DAC Values

DAC VALUE	NOMINAL VCOM OUTPUT VOLTAGE WITH V_{AVDD} = 12V
0xFF	8.5V
0xFE	8.5V
...	...
0x80	6.02V
0x7F	6V
0x7E	5.98V
...	...
0x01	3.52V
0x00	3.5V

FLTB Output

The FLTB output pin is an active-low, open-drain output that can be used to signal various device faults (for operation in stand-alone mode, see the *Stand-Alone Mode* section). When the I2C interface is used, the FLTB output can flag any or all of the following conditions:

- Overtemperature fault
- Overcurrent on AVDD
- Undervoltage on HVINP, VGON, or VGOFF
- Overvoltage on HVINP, VGON, or VGOFF
- VCOM overvoltage or undervoltage

Some of the above conditions can be masked from causing FLTB to go low by using the corresponding mask bit in the Fault Mask 1 (0x08) and Fault Mask 2 (0x09) registers.

Stand-Alone Mode

The IC can be used either in stand-alone mode (when there is no local microcontroller), or in I2C mode. In stand-alone mode, the SEQ pin sets the sequence according to Table 3.

The ENP pin (active high) is used to turn on or off the complete device. In stand-alone mode, the open-drain FLTB output is high when there is no detected fault. When a fault is detected, the FLTB pin outputs a signal with a duty cycle that indicates what type of fault has been detected. This is summarized in Table 4.

I2C Serial Interface

The IC contains an I2C serial interface and acts as a slave device. The basic unit of data transfer is 8 bits. To select I2C mode, connect the SEQ pin to GND. The state of the SEQ pin is sampled when the INA voltage exceeds approximately 2V and the status is latched.

Control of the power-up sequence through I2C can be performed in two ways, manual or automatic. In manual mode, the I2C host enables the outputs individually using the bits in the Regulator Control register (0x02). If a fault is detected in manual mode, the faulty output is disabled after the corresponding deglitch time and no other action is performed. Retry is disabled in manual mode.

The bits in Fault registers 0x0A and 0x0B can be cleared by writing a 0 to the corresponding position in the register. If the values of the other bits are retained, a 1 should be written to them. (e.g., if the vgon_ov bit is cleared in register 0x0A, 0x77 should be written to the register). In this manner, only bit 3 is cleared, and the other bits are left unchanged.

In automatic mode, the sequence is preset using the autoseq_row1–autoseq_row3 and textd_dly1, textd_dly2 bits, and executed using the autoseq_ctrl bit. See the *Autosequencing Mode* section for further details.

Table 3. Output Sequencing

NOMINAL SEQ PIN VOLTAGE	POWER-ON SEQUENCING			POWER-OFF SEQUENCING		
	1st	2nd	3rd	1st	2nd	3rd
GND	I2C CONTROL					
INA/2	AVDD	VGOFF	VGON	VGON	VGOFF	AVDD
INA	AVDD	VGON	VGOFF	VGOFF	VGON	AVDD

Table 4. FLTB Output Duty Cycle

FLTB DUTY CYCLE	ERROR CONDITION
Continuously high	No error
75%	VGON or VGOFF fault
50%	HVINP fault
25%	AVDD fault
1.5%	Thermal shutdown

I2C Protocol

The IC's Slave ID is chosen by connecting the ADD pin to either GND or INA (see Table 5). A master device communicates with the IC by transmitting the correct Slave ID followed by the register address and data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The IC's SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus, or the resistor has to be selected as a function of bus capacitance, such that the rise time on the bus is not greater than 120ns per the I2C bus specification. The IC's SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. In general, for the SCL line resistor selection, the same recommendations as the SDA line apply. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to ensure proper device operation even on a noisy bus.

Individual Output Control Through I2C

Using the bits in the Regulator Control register (0x02), all outputs can be controlled individually by the local host microcontroller. When using this mode of operation, a fault on any output is signaled by the FLTB output pin (if not masked) and the fault bits. The output with the fault remains active until the microcontroller intervenes.

When using the individual control bits, the boost converter must always be enabled first and disabled last in the sequence.

Autosequencing Mode

In autosequencing mode, a complete sequence is configured using the autoseq_row1-3[2:0] and textd_dly1-2 bits and then executed by setting the autoseq_ctrl bit.

To use autosequencing, set the en_autoseq bit in the Configurations register (0x01) to 1 and then configure the desired sequence using the autoseq_row1–autoseq_row3 bits in the Auto Sequencing ctrl1 (0x04) and Auto Sequencing ctrl2 (0x05) registers. The 3 bits of autoseq_row1 correspond to the AVDD output and each bit represents one of three time slots. To enable AVDD during the first time slot, set autoseq_row1 to 100. To enable AVDD during the second time slot, set autoseq_row1 to 010, etc. In an analogous fashion, autoseq_row2 sets the VGON time slot and autoseq_row3 sets the VGOFF time slot.

The delays between each of the time slots are configured using the textd_dly1 and textd_dly2 settings.

When the complete configuration is set, the sequence is executed automatically by setting autoseq_ctrl in the Regulator Control register (0x02) to 1. The corresponding power-off uence can be performed by setting autoseq_ctrl to 0. If a fault occurs in automatic mode, the faulty output is turned off and the other outputs are turned off in the set order. If retry is enabled, a retry is attempted after the appropriate delay.

Note: If the manual control bits have been used to enable one or more of the outputs, automatic sequencing behaves differently: it starts immediately when the en_autoseq bit is set.

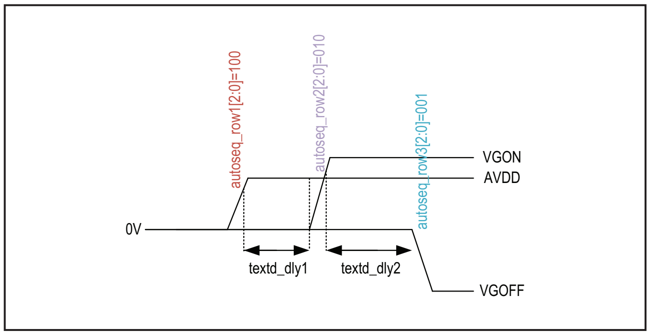


Figure 1. Sample Sequence

Table 5. I2C Slave Addresses

ADD PIN CONNECTION	DEVICE ADDRESS							WRITE ADDRESS	READ ADDRESS
	A6	A5	A4	A3	A2	A1	A0		
GND	0	1	0	0	0	0	0	0x40	0x41
INA	0	1	0	1	0	0	0	0x50	0x51

Register Map

ADDRESS	NAME	MSB (7)	6	5	4	3	2	1	LSB (0)
bank 0									
0x00	Device Id[7:0]	rev_id[7:4]				dev_id[3:0]			
0x01	Configurations[7:0]	fault_ latch_dis	en_auto- seq	tretry[5:4]		tfault[3:2]		dis_ss	swfrq
0x02	Regulator control[7:0]	—	auto- seq_ctrl	dis_vcom	dis_gs	en_vgoff	en_vgon	en_avdd	en_bst
0x03	Regulator power status[7:0]	—	—	vcom_on	gs_on	vgoff_on	vgon_on	avdd_on	bst_on
0x04	Auto sequencing ctrl1[7:0]	—	—	autoseq_row2[5:3]			autoseq_row1[2:0]		
0x05	Auto sequencing ctrl2[7:0]	—	textd_dly2[6:5]		textd_dly1[4:3]		autoseq_row3[2:0]		
0x06	VCOM voltage[7:0]	vcom_dac[7:0]							
0x07	UNUSED - do not write to this register[7:0]	—	—	—	—	—	—	—	—
0x08	Fault mask 1[7:0]	—	vgoff_uv_ mask	vgoff_ ov_mask	vgon_ uv_mask	vgon_ ov_mask	avdd_ ovld_ mask	hvinp_ uv_mask	hvinp_ ov_mask
0x09	Fault mask 2[7:0]	—	—	—	vcom_ uv_mask	vcom_ ov_mask	—	—	—
0x0A	Fault register 1[7:0]	—	vgoff_uv	vgoff_ov	vgon_uv	vgon_ov	avdd_ ovld	hvinp_uv	hvinp_ov
0x0B	Fault register 2[7:0]	—	—	—	vcom_uv	vcom_ov	—	th_shdn	hw_rst

Device Id (0x00)

Register to identify the device type and the revision number.

BIT	7	6	5	4	3	2	1	0
Field	rev_id[7:4]				dev_id[3:0]			
Reset	0x0				0x9			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
rev_id	7:4	Revision ID. 0 = revision 1, etc.
dev_id	3:0	Device ID. Reads 0x9.

Configurations (0x01)

Miscellaneous configurations needed for part operations.

BIT	7	6	5	4	3	2	1	0
Field	fault_latch_dis	en_autoseq	tretry[5:4]		tfault[3:2]		dis_ss	swfrq
Reset	0x0	0x0	0x2		0x1		0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
fault_latch_dis	7	Fault register control. When set to 0, the fault register bits are latched.	0x0: Fault register bits are latched fault flags 0x1: Fault register bits are fault status bits (no latching)
en_autoseq	6	When set to 1, this bit enables the automatic sequencing feature.	0x0: Automatic sequencing is disabled 0x1: Automatic sequencing is enabled
tretry	5:4	If retry is enabled (set to any value other than 0x0), then this is the time that elapses before a new power-on is attempted after turn-off due to a regulator fault.	0x0: Retry is disabled 0x1: Retry to power on regulator after 0.95s 0x2: Retry to power on regulator after 1.9s 0x3: Retry to power on regulator after 3.8s
tfault	3:2	Fault-deglitch duration. This is the time that a regulator fault must be continuously present before the fault is considered valid.	0x0: 30ms 0x1: 60ms 0x2: 120ms 0x3: 250ms
dis_ss	1	Boost spread-spectrum-disable control bit.	0x0: Boost spread spectrum enabled 0x1: Boost spread spectrum disabled
swfrq	0	Boost converter switching-frequency selection.	0x0: 2.2MHz boost switching frequency 0x1: 440kHz boost switching frequency

Regulator control (0x02)

Direct control of regulators enable. This register can be used on I²C variant when "en_autoseq = 0" to control the manual sequencing of regulators (i.e. regulators' sequencing is completely controlled by host software). Note that some controls are implemented in this register. As an example, the enable of any regulator is not allowed unless "en_bst" has been enabled and ready (bst_on = 1).

BIT	7	6	5	4	3	2	1	0
Field	—	autoseq_ctrl	dis_vcom	dis_gs	en_vgoff	en_vgon	en_avdd	en_bst
Reset	—	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	—	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
autoseq_ctrl	6	Controls the automatic sequencer. If the automatic sequencer is enabled, setting this bit to 1 starts the power-on sequence as programmed. Deasserting this bit to 0 starts the power-down sequence. Note that the sequence programming cannot be altered while the sequence is ongoing. Once the current sequence is completed, sequence programming is again enabled. If the en_autoseq bit is set to 0, this bit has no effect.	0x0: If regulators are off, keep them as they are. If regulators are on, start the power off sequence and keep them off 0x1: If regulators are off start the power on sequence and keep them on. Else keep them as they are.
dis_vcom	5	VCOM buffer disable. By default, the VCOM buffer is enabled when the AVDD crosses its power-good threshold.	0x0: VCOM buffer is enabled 0x1: VCOM buffer has been disabled
dis_gs	4	Gate-shading disable. By default, the gate-shading block is enabled when soft-start for all regulators is completed and when the DEL pin exceeds its enable threshold.	0x0: Gate shading is enabled 0x1: Gate shading has been disabled
en_vgoff	3	Negative charge-pump enable.	0x0: Negative charge pump is disabled 0x1: Negative charge pump has been enabled
en_vgon	2	Positive charge-pump enable.	0x0: Positive charge pump is disabled 0x1: Positive charge pump has been enabled
en_avdd	1	Control bit for the switch between HVINP and AVDD. Note that any attempt to set this bit to 1 fails if the field "bst_ok" is 0.	0x0: Switch beween HVINP and AVDD is open 0x1: Switch beween HVINP and AVDD is closed
en_bst	0	Boost converter enable.	0x0: Buck is disabled 0x1: Buck is enabled

Regulator power status (0x03)

Status of the regulators. Each bit set to 1 means that related regulator is powered on (i.e. it has been enabled, the transient has completed and it's active ready).

BIT	7	6	5	4	3	2	1	0
Field	—	—	vcom_on	gs_on	vgoff_on	vgon_on	avdd_on	bst_on
Reset	—	—	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	—	—	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
vcom_on	5	This bit shows the status of the VCOM buffer.	0x0: The VCOM buffer is off 0x1: The VCOM buffer is on
gs_on	4	This bit shows the status of the gate-shading block.	0x0: The gate shading is off 0x1: The gate shading is on
vgoff_on	3	This bit shows the status of the negative charge pump.	0x0: The charge pump is off 0x1: The charge pump is on
vgon_on	2	This bit shows the status of the positive charge pump.	0x0: The charge pump is off 0x1: The charge pump is on
avdd_on	1	This bit shows the status of the switch between HVINP and AVDD.	0x0: The switch is open 0x1: The switch is closed
bst_on	0	When this bit is set to 1, the boost converter has been activated and its output voltage is in range.	0x0: Boost has not been activated 0x1: Boost has been activated and power on transient completed

Auto sequencing ctrl1 (0x04)

Programming for the control of the automatic sequencing.

BIT	7	6	5	4	3	2	1	0
Field	—	—	autoseq_row2[5:3]			autoseq_row1[2:0]		
Reset	—	—	0x0			0x0		
Access Type	—	—	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
autoseq_row2	5:3	Autosequencing matrix row 2, corresponding to VGON. A 1 in this bit corresponds to start the regulator in slot 1, 2, or 3 depending on the position of the 1. If more than a 1 is present in the field, only the first one is considered valid.
autoseq_row1	2:0	Autosequencing matrix row 1, corresponding to AVDD. A 1 in this bit corresponds to start the regulator in slot 1, 2, or 3 depending on the position of the 1. If more than a 1 is present in the field, only the first one is considered valid.

Auto sequencing ctrl2 (0x05)

Programming for the control of the automatic sequencing.

BIT	7	6	5	4	3	2	1	0
Field	—	textd_dly2[1:0]		textd_dly1[1:0]		autoseq_row3[2:0]		
Reset	—	0x0		0x0		0x0		
Access Type	—	Write, Read		Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
textd_dly2	6:5	Delay extension as a percentage of the time that elapses between the power-on command for regulators in slot 2 and the assertion of the feedback signal that notifies they completed ramp up. If we name Tok such time the delay between slot 2 and slot 3 will be Tok x (1 + textd_dly2).	0x0: No delay after power OK of preceeding regulators 0x1: Additional 10% delay after power OK of preceeding regulators 0x2: Additional 20% delay after power OK of preceeding regulators 0x3: Additional 30% delay after power OK of preceeding regulators
textd_dly1	4:3	Delay extension as a percentage of the time that elapses between the power-on command for regulators in slot 1 and the assertion of the feedback signal that notifies they completed ramp up. If we name Tok such time the delay between slot 1 and slot 2 will be Tok x (1 + textd_dly1).	0x0: No delay after power OK of preceeding regulators 0x1: Additional 10% delay after power OK of preceeding regulators 0x2: Additional 20% delay after power OK of preceeding regulators 0x3: Additional 30% delay after power OK of preceeding regulators
autoseq_ row3	2:0	Autosequencing matrix row 3, corresponding to VGOFF. A 1 in this bit corresponds to start the regulator in slot 1, 2, or 3 depending on the position of the 1. If more than a 1 is present in the field, only the first one is considered valid.	

VCOM voltage (0x06)

This byte controls the setting of the DAC controlling the VCOM output voltage.

BIT	7	6	5	4	3	2	1	0
Field	vcom_dac[7:0]							
Reset	0x7F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
vcom_dac	7:0	This byte controls the DAC that sets the VCOM output voltage. The output step is 20mV/LSB. The mid-point is 0x7F = AVDD/2.	

Fault mask 1 (0x08)

Fault mask register. Each bit in this register is able to mask the fault of the related bit. A 1 in a position enables the contribution of the fault flag to the FLTB assertion.

BIT	7	6	5	4	3	2	1	0
Field	—	vgoff_uv_mask	vgoff_ov_mask	vgon_uv_mask	vgon_ov_mask	avdd_ovld_mask	hvinp_uv_mask	hvinp_ov_mask
Reset	—	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	—	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
vgoff_uv_mask	6	Mask for VGOFF undervoltage fault. If this bit is set to 1, an undervoltage fault on VGOFF does not cause FLTB to go low.
vgoff_ov_mask	5	Mask for VGOFF overvoltage fault. If this bit is set to 1, an overvoltage fault on VGOFF does not cause FLTB to go low.
vgon_uv_mask	4	Mask for VGON undervoltage fault. If this bit is set to 1, an undervoltage fault on VGON does not cause FLTB to go low.
vgon_ov_mask	3	Mask for VGON overvoltage fault. If this bit is set to 1, an overvoltage fault on VGON does not cause FLTB to go low.
avdd_ovld_mask	2	Mask for AVDD overcurrent fault. If this bit is set to 1, an overcurrent fault on AVDD does not cause FLTB to go low.
hvinp_uv_mask	1	Mask for HVINP underervoltage fault. If this bit is set to 1, an undervoltage fault on HVINP does not cause FLTB to go low.
hvinp_ov_mask	0	Mask for HVINP overvoltage fault. If this bit is set to 1, an overvoltage fault on HVINP does not cause FLTB to go low.

Fault mask 2 (0x09)

Fault mask register. Each bit in this register is able to mask the fault of the related bit. A 1 in a position enables the contribution of the fault flag to the FLTB assertion.

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	vcom_uv_mask	vcom_ov_mask	—	—	—
Reset	—	—	—	0x0	0x0	—	—	—
Access Type	—	—	—	Write, Read	Write, Read	—	—	—

BITFIELD	BITS	DESCRIPTION
vcom_uv_mask	4	Mask for VCOM undervoltage fault. If this bit is set to 1, an undervoltage fault on VCOM does not cause FLTB to go low.
vcom_ov_mask	3	Mask for VCOM overvoltage fault. If this bit is set to 1, an overvoltage fault on VCOM does not cause FLTB to go low.

Fault register 1 (0x0A)

Fault register 1. Each bit of this register can be a status bit (reflecting current status of the fault) or a flag bit (latched version of a status bit).

BIT	7	6	5	4	3	2	1	0
Field	—	vgoff_uv	vgoff_ov	vgon_uv	vgon_ov	avdd_ovld	hvinp_uv	hvinp_ov
Reset	—	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	—	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read	Write 0 to Clear, Read

BITFIELD	BITS	DESCRIPTION	DECODE
vgoff_uv	6	VGOFF undervoltage fault. Depending on programing of "fault_latch_dis," this is a status bit or a clear-on-read flag bit.	0x0: No fault is present or has happened 0x1: If "fault_latch_dis" = 0 then a fault has happened or is still present. In this case the bit is CoR but reasserts if fault is still present. If "fault_latch_dis" = 1 then a fault is currently present else this bit is 0.
vgoff_ov	5	VGOFF overvoltage fault. Depending on programing of "fault_latch_dis," this is a status bit or a clear-on-read flag bit.	0x0: No fault is present or has happened 0x1: If "fault_latch_dis" = 0 then a fault has happened or is still present. In this case the bit is CoR, but reasserts if fault is still present. If "fault_latch_dis" = 1 then a fault is currently present, else this bit is 0.
vgon_uv	4	VGON undervoltage fault. Depending on programing of "fault_latch_dis," this is a status bit or a clear-on-read flag bit.	0x0: No fault is present or has happened 0x1: If "fault_latch_dis" = 0 then a fault has happened or is still present. In this case the bit is CoR, but reasserts if fault is still present. If "fault_latch_dis" = 1 then a fault is currently present, else this bit is 0.
vgon_ov	3	VGON overvoltage fault. Depending on programing of "fault_latch_dis," this is a status bit or a clear-on-read flag bit.	0x0: No fault is present or has happened 0x1: If "fault_latch_dis" = 0 then a fault has happened or is still present. In this case the bit is CoR, but reasserts if fault is still present. If "fault_latch_dis" = 1 then a fault is currently present, else this bit is 0.
avdd_ovld	2	AVDD overcurrent fault. Depending on programing of "fault_latch_dis," this is a status bit or a clear-on-read flag bit.	0x0: No fault is present or has happened 0x1: If "fault_latch_dis" = 0 then a fault has happened or is still present. In this case the bit is CoR, but reasserts if fault is still present. If "fault_latch_dis" = 1 then a fault is currently present, else this bit is 0.
hvinp_uv	1	HVINP undervoltage fault. Depending on programing of "fault_latch_dis," this is a status bit or a clear-on-read flag bit.	0x0: No fault is present or has happened 0x1: If "fault_latch_dis" = 0 then a fault has happened or is still present. In this case the bit is CoR, but reasserts if fault is still present. If "fault_latch_dis" = 1 then a fault is currently present, else this bit is 0.
hvinp_ov	0	HVINP overvoltage fault. Depending on programing of "fault_latch_dis," this is a status bit or a clear-on-read flag bit.	0x0: No fault is present or has happened 0x1: If "fault_latch_dis" = 0 then a fault has happened or is still present. In this case the bit is CoR, but reasserts if fault is still present. If "fault_latch_dis" = 1 then a fault is currently present, else this bit is 0.

Fault register 2 (0x0B)

Fault register 2. Each bit of this register is a flag bit (latched fault).

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	vcom_uv	vcom_ov	—	th_shdn	hw_rst
Reset	—	—	—	0x0	0x0	—	0x0	0x1
Access Type	—	—	—	Write 0 to Clear, Read	Write 0 to Clear, Read	—	Write 0 to Clear, Read	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
vcom_uv	4	VCOM buffer undervoltage fault. Depending on programing of "fault_latch_dis," this is a status bit or a clear-on-read flag bit.	0x0: No fault is present or has happened 0x1: If "fault_latch_dis" = 0 then a fault has happened or is still present. In this case the bit is CoR, but reasserts if fault is still present. If "fault_latch_dis" = 1 then a fault is currently present, else this bit is 0.
vcom_ov	3	VCOM buffer overvoltage fault. Depending on programing of "fault_latch_dis," this is a status bit or a clear-on-read flag bit.	0x0: No fault is present or has happened 0x1: If "fault_latch_dis" = 0 then a fault has happened or is still present. In this case the bit is CoR, but reasserts if fault is still present. If "fault_latch_dis" = 1 then a fault is currently present, else this bit is 0.
th_shdn	1	Thermal-shutdown event was detected. If the event is still on, the flag reasserts upon CoR.	0x0: no thermal shutdown since last read 0x1: Device is in thermal shutdown
hw_rst	0	Hardware reset event was detected	0x0: no POR since last read 0x1: this is the first read from the device after a POR

Applications Information

Boost Converter

Inductor Selection

The value of the boost inductor is determined as follows:

$$L = \frac{(V_{INA} \times D)}{(LIR \times I_{INA} \times f_{SW})}$$

where V_{INA} is the boost input voltage, D is the duty cycle, LIR is the current ripple factor in the inductor (choose a value between 0.5 and 1), I_{INA} is the boost converter input current, and f_{SW} is either 2.2MHz or 440kHz.

Calculate the duty-cycle using:

$$D = \frac{(1 - \eta \times V_{INA})}{V_{OUT}}$$

where η is the converter efficiency (assume 0.85) and V_{OUT} is the boost output voltage.

I_{INA}, the average input current, can be estimated as follows:

$$I_{INA} = \frac{(V_{OUT} \times I_{OUT})}{(\eta \times V_{INA})}$$

where I_{OUT} is the boost output current.

Capacitor Selection

The input and output filter capacitors should be a low-ESR type (e.g., tantalum, ceramic, or low-ESR electrolytic) and should have RMS current ratings greater than:

$$I_{RMS} = \frac{(LIR \times I_{INA})}{\sqrt{12}}$$

for the input capacitor, and:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{\left(D + \frac{LIR^2}{12}\right)}{(1 - D)}}$$

for the output capacitor. The output voltage contains a ripple component whose peak-to-peak value depends on the value of the ESR and capacitance of the output capacitor and is approximately the sum of two contributions:

$$\Delta V_{RIPPLE} = \Delta V_{ESR} + \Delta V_{CAP}$$

where:

$$\Delta V_{ESR} = I_{INA} \times \left(1 + \frac{LIR}{2}\right) \times R_{ESR}$$

and

$$\Delta V_{CAP} = \frac{(I_{OUT} \times D)}{(C_{OUT} \times f_{SW})}$$

where R_{ESR} is the ESR of the chosen output capacitor.

Output-Voltage Selection

The output voltage of the boost converter can be adjusted using a resistive voltage-divider formed by R_{TOP} and R_{BOTTOM}. Connect R_{TOP} between HVINP and FBP, and connect R_{BOTTOM} between FBP and GND. Select R_{BOTTOM} in the 10kΩ to 50kΩ range. Calculate R_{TOP} with the following equation:

$$R_{TOP} = R_{BOTTOM} \times \left(\left(\frac{V_{OUT}}{1.25}\right) - 1\right)$$

Place the resistors close to the device and connect R_{BOTTOM} to the analog ground plane.

Boost Converter Operation at Low INA and High Output Power

At high boost output power and low input voltages, the input current becomes high and the boost converter's efficiency is lower. Under these conditions, it may be preferable to use the 440kHz low-frequency setting. A further boost in efficiency at low input voltages can be obtained by adding a Schottky diode from LXP to HVINP. See all the relevant curve in the *Typical Operating Characteristics* section

Charge-Pump Regulators

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output voltage requirement. The number of positive charge-pump stages is given by:

$$nPOS = \frac{VGON + V_{DROPOUT} - V_{AVDD}}{V_{SUP} - 2 \times V_D}$$

where nPOS is the number of positive charge-pump stages, VGON is the output of the positive charge-pump regulator, V_{SUP} is the supply voltage of the charge-pump regulators (HVINP), V_D is the forward voltage drop of the charge-pump diodes, and $V_{DROPOUT}$ is the dropout margin for the regulator. Use $V_{DROPOUT}$ = 600mV.

The number of negative charge-pump stages is given by:

$$nNEG = \frac{-VGOFF + V_{DROPOUT}}{V_{SUP} - 2 \times V_D}$$

where nNEG is the number of negative charge-pump stages and VGOFF is the output of the negative charge-pump regulator.

Flying Capacitors

Increasing the flying capacitor (connected to DRVN and DRVP) value lowers the effective source impedance and increases the output current capability. Increasing the capacitance indefinitely, however, has a negligible effect on output-current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1μF ceramic capacitor works well in most applications. The flying capacitor's voltage rating must exceed the following:

$$VCX > n \times V_{HVINP}$$

where n is the stage number in which the flying capacitor appears.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output-voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT\_CP} > \frac{I_{LOAD\_CP}}{2 \times f_{SW} \times V_{RIPPLE\_CP}}$$

where C_{OUT_CP} is the output capacitor of the charge pump, I_{LOAD_CP} is the load current of the charge pump, V_{RIPPLE_CP} is the desired peak-to-peak value of the output ripple, and f_{SW} is the switching frequency, which is 440kHz.

Power Dissipation

Total power dissipation of the IC comprises five terms:

1) Boost converter power dissipation
2) Positive charge-pump dissipation
3) Negative charge-pump dissipation
4) Gate-shading power dissipation
5) VCOM buffer power dissipation

Items 2–4 are negligible, while the other terms can be estimated using:

$$P_{BOOST} = I^2_{INA} \times R_L \times D + I^2_{INA} \times R_H \times (1 - D) + 0.5 \times I_{INA} \times V_{HVINP} \times t_{RF} \times f_{SW}$$

where R_L is the low-side LXP switch resistance, R_H is the high-side LX switch resistance, and t_{RF} is the LXP rise/fall time that can be approximated by 5ns:

$$P_{VCOM} = (V_{AVDD} - V_{VCOM}) \times I_{VCOM}$$

where I_{VCOM} is the RMS VCOM buffer output current.

PCB Layout Example

Figure 2 shows an example for the layout of the power components around the MAX20067. This layout minimizes the area of the LXP node and the area of the switching current loop. Follow these guidelines for the rest of the layout:

- Separate power and analog grounds on the board and connect them together at a single point.
- Connect all feedback resistor-dividers to the analog or "quiet" ground, along with the REF and INA capacitors. Feedback resistors should be placed close to their associated pins to avoid noise pickup.
- Place decoupling capacitors as close as possible to their respective pins.
- Keep high-current paths as short and wide as possible.
- Route high-speed switching nodes (i.e., LXP, DRVN, and DRVP) away from sensitive analog nodes (i.e., FBP, FBGH, FBGL, and REF).

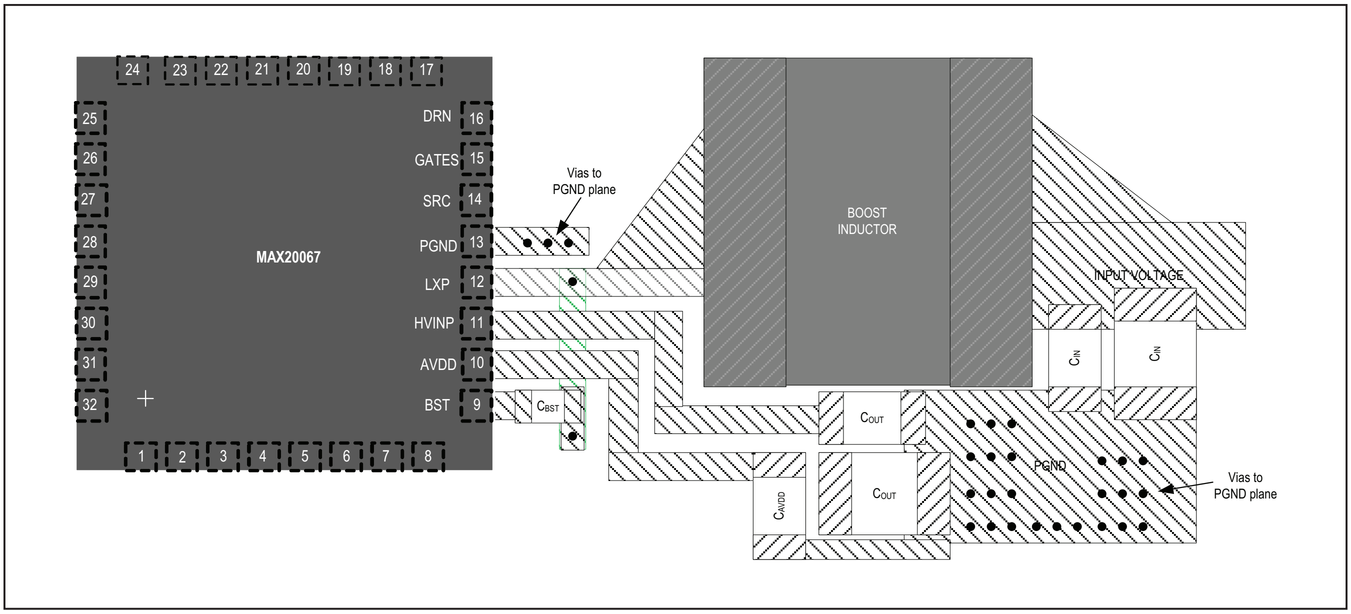


Figure 2. Layout Example

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX20067GTJ/V+	-40°C to +105°C	32 TQFN-EP*	T3255+4C

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/17	Initial release	—

