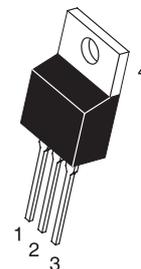
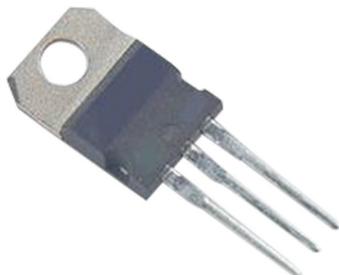


Complementary Silicon Plastic Power Transistor

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Pin Configuration

1. Base
2. Collector
3. Emitter
4. Collector

Description:

These devices are designed for use in general-purpose amplifier and switching applications.

Features:

- DC Current Gain Specified to 7A
 $h_{FE} = 30-150 @ I_C$
- Collector-Emitter Sustaining Voltage - $V_{CEO(sus)} = 50 \text{ V DC (Min)}$
- High Current Gain - Bandwidth Product - $f_T = 10\text{MHz (Min)} @ I_C = 500\text{mA DC}$
- TO-220AB Compact Package

Maximum Ratings

Characteristic	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	V DC
Collector-Base Voltage	V_{CBO}	60	
Emitter-Base Voltage	V_{EBO}	5	
Collector Current-Continuous -Peak	I_C	7 10	A DC
Base Current	I_B	3	
Total Power Dissipation at $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40 0.32	W W/ $^\circ\text{C}$
Operation and Storage Junction Temperature Range	T_J, T_{STG}	-65 to +150	$^\circ\text{C}$

Thermal Characteristics

Characteristic	Symbol	Max.	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	3.125	$^\circ\text{C/W}$

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Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
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Off Characteristics

Collector-Emitter Sustaining Voltage (1*) $I_C = 100\text{mA DC}, I_B = 0$	$V_{CEO(sus)}$	50	-	V DC
Collector Cut off Current $V_{CE} = 40\text{V DC}, I_B = 0$	I_{CEO}	-	1	mA DC
Collector Cut off Current $V_{CE} = 60\text{V DC}, V_{EB(off)} = 1.5\text{V DC}$ ($V_{CE} = 50\text{V DC}, V_{EB(off)} = 1.5\text{V DC}, T_C = 150^\circ\text{C}$)	I_{CEX}	-	100 2	$\mu\text{A DC}$ mA DC
Emitter Cut off Current $V_{EB} = 5\text{V DC}, I_C = 0$	I_{EBO}	-	1	mA DC

On Characteristics (1*)

DC Current Gain $I_C = 2.5\text{A DC}, V_{CE} = 4\text{V DC}$ $I_C = 7\text{A DC}, V_{CE} = 4\text{V DC}$	h_{FE}	30 2.3	150 -	-
Collector-Emitter Saturation Voltage $I_C = 7\text{A DC}, I_B = 3\text{A DC}$	$V_{CE(sat)}$	-	3.5	V DC
Base-Emitter On Voltage $I_C = 7\text{A DC}, V_{CE} = 4\text{V DC}$	$V_{BE(on)}$	-	3	

Dynamic Characteristics

Current Gain - Bandwidth Product (2*) $I_C = 500\text{mA DC}, V_{CE} = 4\text{V DC}, f_{test} = 1\text{MHz}$	f_T	10	-	MHz
Output Capacitance ($V_{CB} = 10\text{V DC}, I_E = 0, f = 1\text{MHz}$)	C_{ob}	-	250	pF
Small-Signal Current Gain ($I_C = 0.5\text{A DC}, V_{CE} = 4\text{V DC}, f = 50\text{kHz}$)	h_{fe}	20	-	-

1* = Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

2* = $f_T = |h_{fe}| \cdot f_{test}$

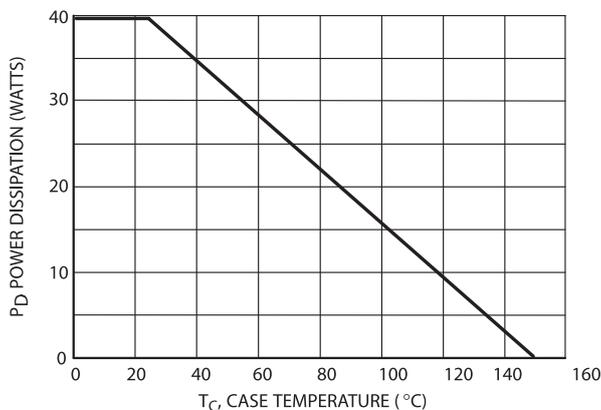


Figure 1. Power Derating

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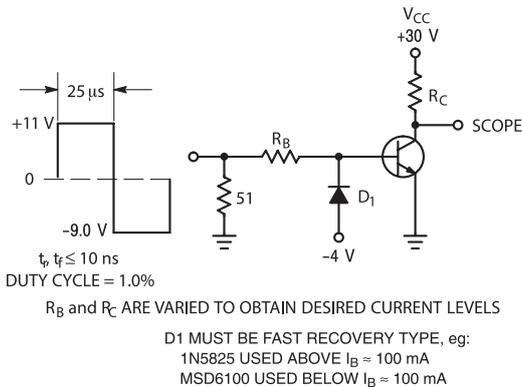


Figure 2. Switching Time Test Circuit

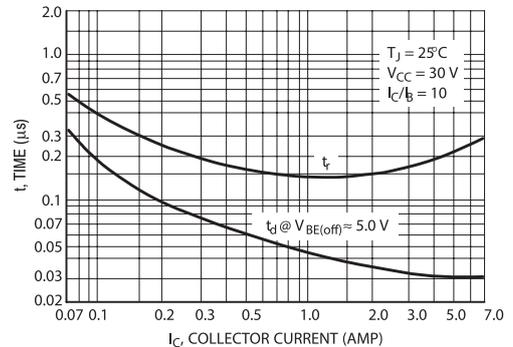


Figure 3. Turn-On Time

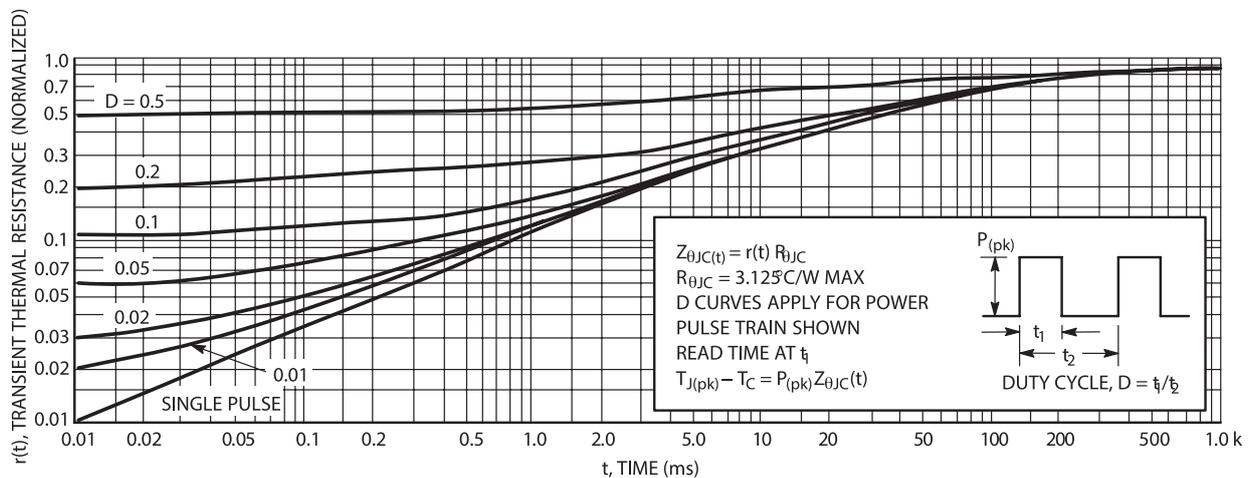


Figure 4. Thermal Response

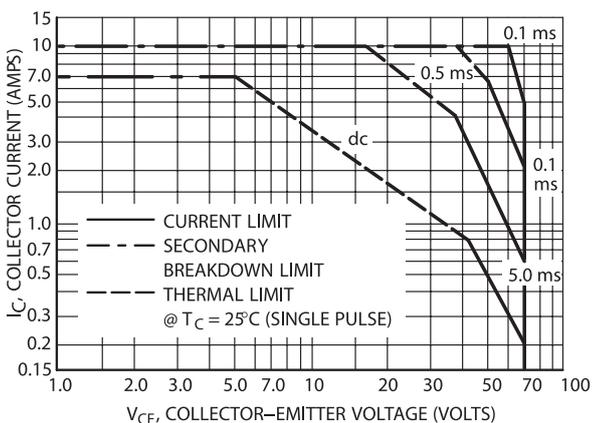


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

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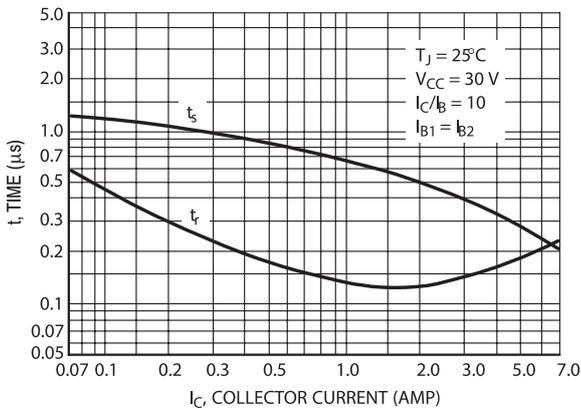


Figure 6. Turn-Off Time

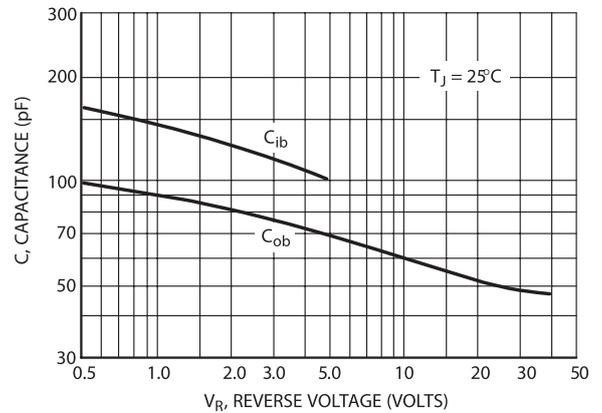
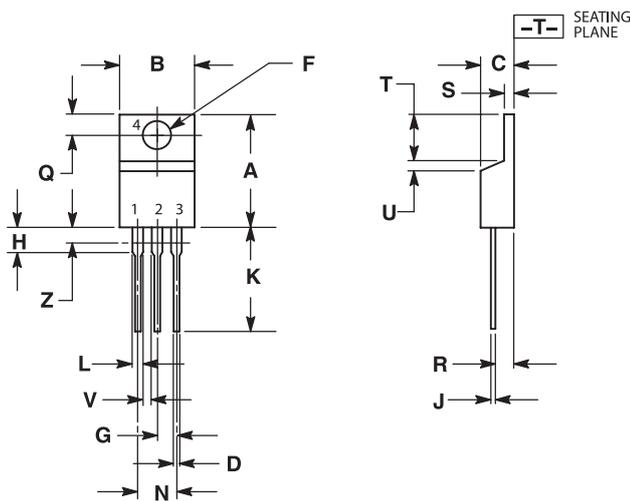


Figure 7. Capacitance



Pin Configuration

1. Base
2. Collector
3. Emitter
4. Collector

Dimensions	Min.	Max.
A	14.48	15.75
B	9.66	10.28
C	4.07	4.82
D	0.64	0.88
F	3.61	3.73
G	2.42	2.66
H	2.8	3.93
J	0.46	0.64
K	12.7	14.27
L	1.15	1.52
N	4.83	5.33
Q	2.54	3.04
R	2.04	2.79
S	1.15	1.39
T	5.97	6.47
U	0	1.27
V	1.15	-
Z	-	2.04

Part Number Table

Description	Part Number
Transistor, PNP, TO-220	2N6109

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