Description

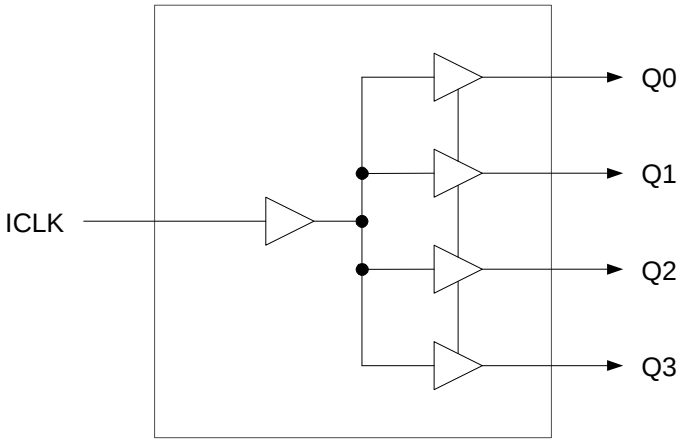
The 524S is a low skew, single input to four output, clock buffer. The 524S has best in class additive phase Jitter of sub 50 fsec.

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

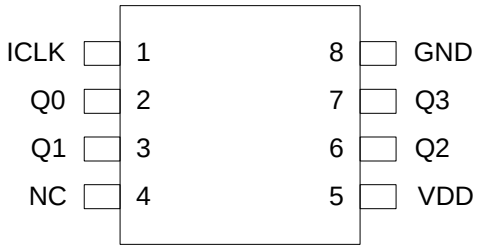
Features

- Low additive phase jitter RMS: 50fs
- Extremely low skew outputs (50ps)
- Low cost clock buffer
- Packaged in 8-pin SOIC and 8-pin DFN, Pb-free
- Input/Output clock frequency up to 200 MHz
- Non-inverting output clock
- Ideal for networking clocks
- Operating Voltages: 1.8V to 3.3V
- Advanced, low power CMOS process
- Extended temperature range (-40°C to +105°C)

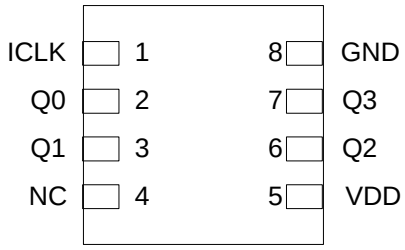
Block Diagram



Pin Assignments



8-pin SOIC



8-pin DFN

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	Input	Clock input.
2	Q0	Output	Clock output 0.
3	Q1	Output	Clock output 1.
4	NC	–	No connect.
5	VDD	Power	Connect to +1.8V, +2.5 V, or +3.3 V.
6	Q2	Output	Clock Output 2.
7	Q3	Output	Clock Output 3.
8	GND	Power	Connect to ground.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD on pin 5 and GND on pin 8, as close to the device as possible. A 33Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the 524S is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15 ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 524S. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Outputs	-0.5 V to VDD+0.5 V
ICLK	3.465V
Ambient Operating Temperature (extended)	-40° to +105°C
Storage Temperature	-65° to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -10 mA	1.3			V
Output Low Voltage	V_{OL}	I_{OL} = 10 mA			0.35	V
Operating Supply Current	IDD	No load, 135 MHz		16		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -16 mA	1.8			V
Output Low Voltage	V_{OL}	I_{OL} = 16 mA			0.5	V
Operating Supply Current	IDD	No load, 135 MHz		18		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

VDD=3.3 V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Input High Voltage, ICLK	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, ICLK	V_{IL}	Note 1			0.3xVDD	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.2			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.7	V
Operating Supply Current	IDD	No load, 135 MHz		22		mA
Nominal Output Impedance	Z_O			17		Ω
Input Capacitance	C_{IN}	ICLK		5		pF

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.36 to 1.44 V, C_L=5 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	1.44 to 0.36 V, C_L=5 pF		0.6	1.0	ns
Propagation Delay		Note 1	1.5	2	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2			65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.5 to 2.0 V, C_L=5 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.0 to 0.5 V, C_L=5 pF		0.6	1.0	ns
Propagation Delay		Note 1	1.8	2.5	4.5	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2			65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms

VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.66 to 2.64 V, C_L=5 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.64 to 0.66 V, C_L=5 pF		0.6	1.0	ns
Propagation Delay		Note 1	1.5	2	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew		Rising edges at VDD/2, Note 2			65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			2	ms

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

Phase Noise Plots

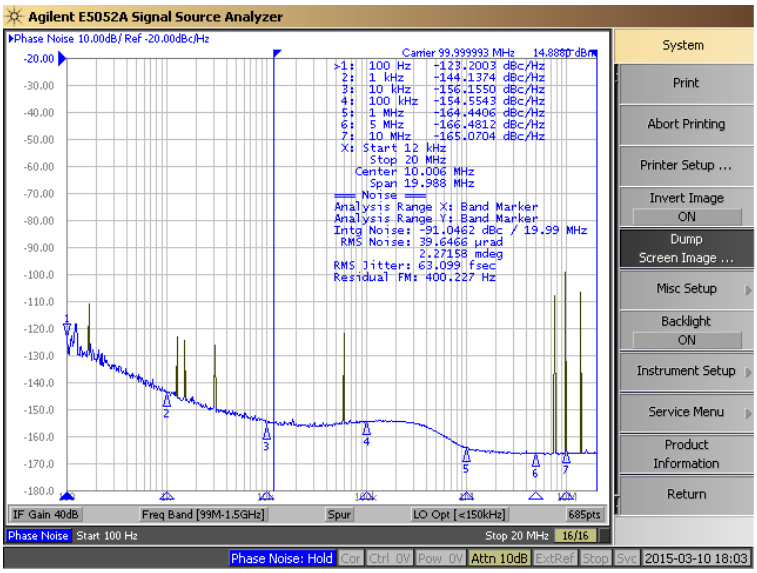


Figure 1. 524S Reference Phase Noise 63fs (12kHz to 20MHz)

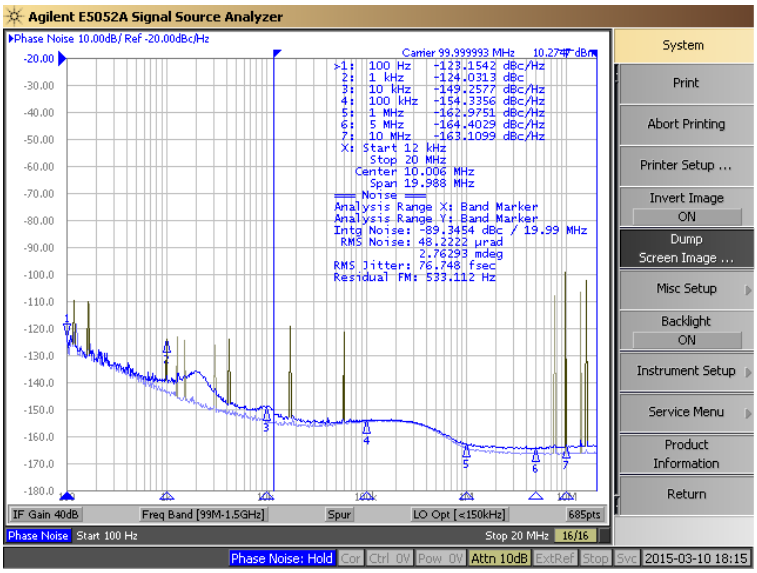
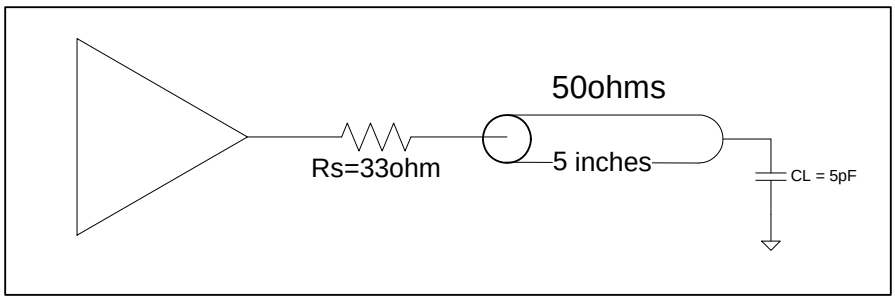


Figure 2. 524S Output Phase Noise 76fs (12kHz to 20MHz)

The phase noise plots above show the low Additive Jitter of the 524S high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 63fs of RMS phase jitter while the output of 524S has about 76fs of RMS phase jitter. This results in a low Additive Phase Jitter of only 42fs.

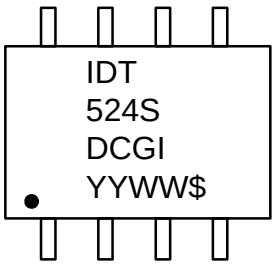
Test Load and Circuit



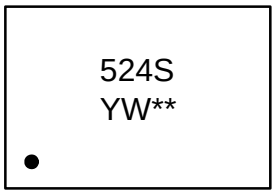
Thermal Characteristics (8SOIC)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagrams



8-pin SOIC

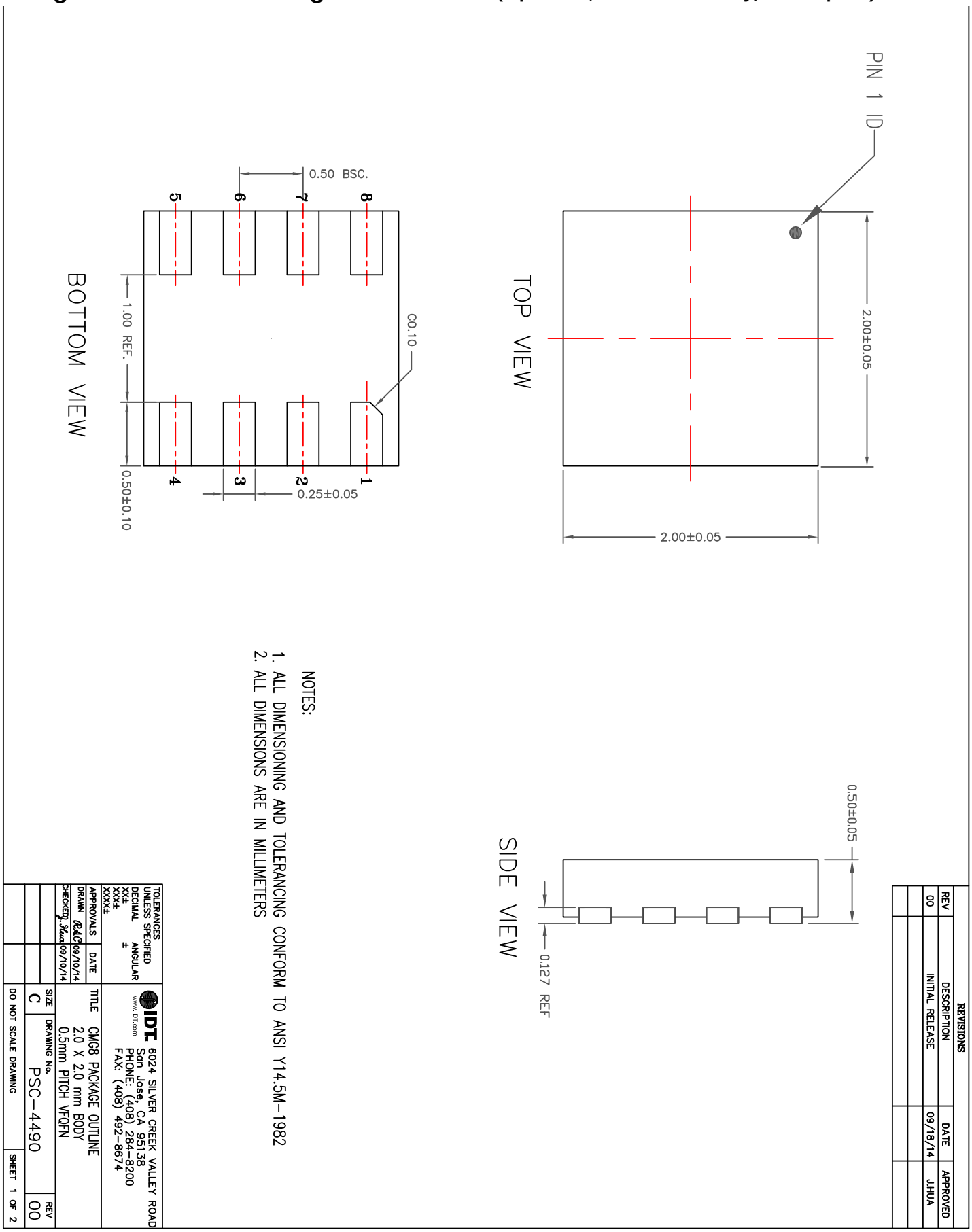


8-pin DFN

Notes:

1. "**" is the lot number.
2. "YYWW" or "YW" are the last digits of the year and week that the part was assembled.
3 "G" denotes RoHS compliant package.
4. "$" denotes the mark code.
5. "I" denotes extended temperature range device.

Package Outline and Package Dimensions (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)



NOTES:

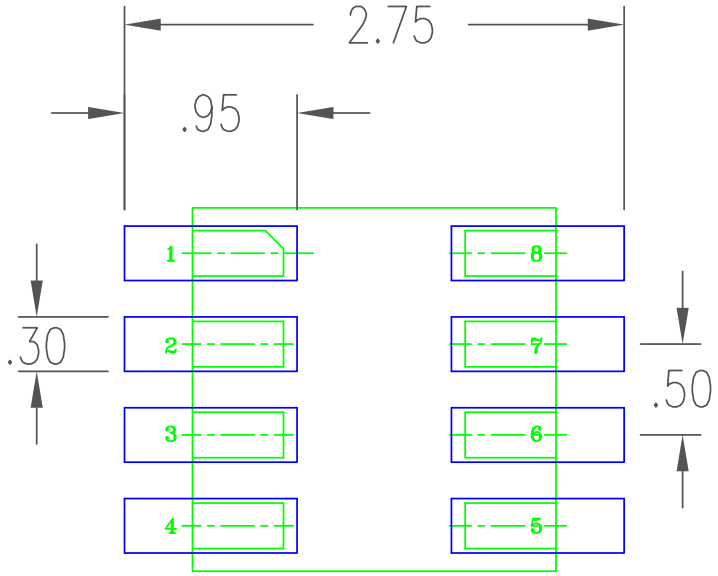
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	09/18/14	J.HUA

TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±	IDT. www.IDT.com	6024 SILVER CREEK VALLEY ROAD San Jose, CA 95138 PHONE: (408) 284–8200 FAX: (408) 492–8674
APPROVALS DRAWN DATE 09/10/14 CHECKED DATE 09/10/14	TITLE	CMG8 PACKAGE OUTLINE 2.0 X 2.0 mm BODY 0.5mm PITCH VFQFN
	SIZE C	DRAWING No. PSC–4490 REV 00
DO NOT SCALE DRAWING		SHEET 1 OF 2

Package Outline and Package Dimensions, cont. (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	09/18/14	J.HUA

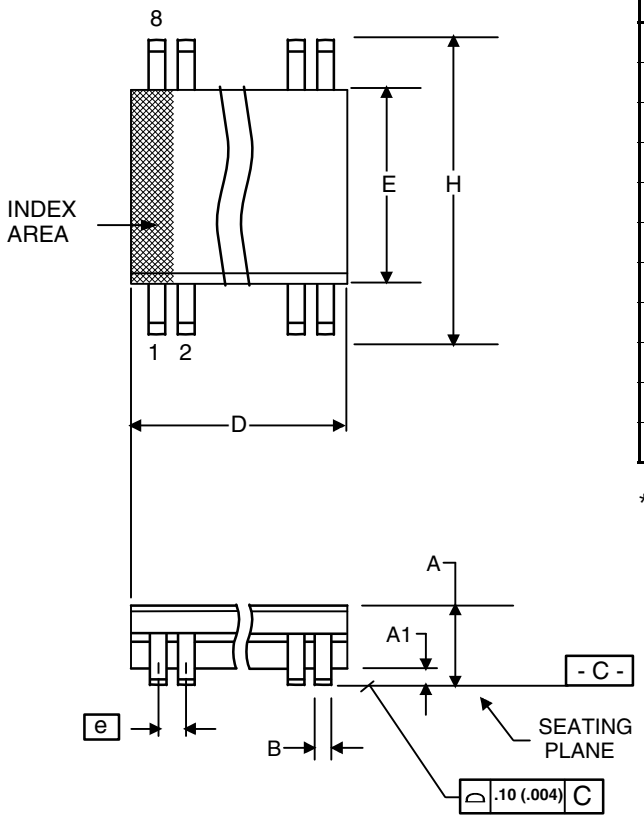


RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT. www.IDT.com	6024 SILVER CREEK VALLEY ROAD San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 492-8674
APPROVALS	DATE	TITLE	CMG8 PACKAGE OUTLINE 2.0 X 2.0 mm BODY 0.5 mm PITCH VFQFN
DRAWN RAC	09/10/14		
CHECKED			
		SIZE C	DRAWING No. PSC-4490 REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
a	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
524SDCGI	see page 7	Tubes	8-pin SOIC	-40° to +105°C
524SDCGI8		Tape and Reel	8-pin SOIC	-40° to +105°C
524SCMGI		Cut Tape	8-pin DFN	-40° to +105°C
524SCMGI8		Tape and Reel	8-pin DFN	-40° to +105°C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	03/18/15	B. Chandhoke	Initial release.

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