

1 to 4-Cell Li-Ion Battery Manager

For Application Processors

BD99958GW

General Description

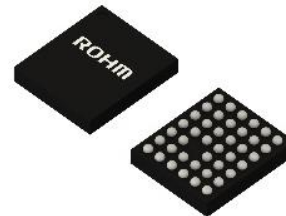
BD99958GW is a Battery Management LSI for 1 to 4-Cell Lithium-Ion battery, and available in a small 41-ball 0.4 mm pitch 2.6 mm x 3.0 mm Wafer-level CSP package which is designed to meet high degree demands for space-constraint equipment such as Low Profile Notebook PC, Tablets and other applications.

BD99958GW provides a Dual-source Battery Charger, two port BCS1.2 detectors and a Battery Monitor with several alarm (INT#, PROCHOT#) outputs.

Package

UCSP55M3C 41pin
(BD99958GW)

W(Typ) x D(Typ) x H(Max)
2.60 mm x 3.00 mm x 0.62 mm



UCSP55M3C (BD99958GW)

Features

- Dual-source Battery Charger
 - High Efficiency Step-up/down Switching Charger for 1 to 4-Cell Li-Ion/Li-poly Battery
 - Two Separate Input Sources for USB-VBUS and DC Adapter.
 - Two Port BCS1.2 Detectors.
 - JEITA Compliant Charging Profile
 - Programmable Parameters for Preconditioning, Pre-charge Current, and Fast-charge Current
 - Programmable Charging Voltage
 - Programmable Charge Current
 - Programmable Switching Frequency: 600 kHz to 1.2 MHz
 - Support USB BCS1.2, OTG
 - USB-VBUS Over Voltage Protection
 - Over Voltage Battery Protection
 - Battery Short Circuit Detection
 - Power Path Management with Charge Pump Gate Driver
 - Flexibility Power Path Control
 - Reverse Buck/Boost Option for USB/USB-PD
 - Bias Voltage Output for the External Thermistor
 - PMON Output
 - PROCHOT# Output
 - Support Inhibit/Autonomous Charging
 - Battery Learn Function
 - Input Operating Range: 3.8 V to 25.0 V
- Voltage Measurement for Thermistor.
 - Bias Voltage Output for the External Thermistor.
- SMBus Interface (Clock Up Friendly I2C) for Host Communication
- Embedded OTPROM for Initial Settings

Applications

- Ultrabook
- Notebook PC
- Ultra-Mobile PC
- Tablet PC

Contents

General Description	1
Features.....	1
Package.....	1
Applications	1
Notation.....	3
Reference.....	3
1. Introduction	4
1.1. Typical Application Circuits	4
2. Pin Configuration.....	5
3. Pin Description	6
4. Absolute Maximum Ratings	7
5. Power Dissipation	7
6. Recommended Operating Conditions	7
7. Function Descriptions.....	8
7.1. Block Diagram	8
7.2. Electrical Characteristics for Battery Charger	9
7.3. DC Input & Over Voltage Protection (OVP)	11
7.4. USB Detection	12
7.5. DC/DC Converter	13
7.6. Charger	16
7.7. Reverse DC/DC Converter	18
7.8. 12-bit ADC	19
7.9. Power On	20
8. Control Specification	22
8.1. SMBus Communication	22
8.2. SMBus Protocols	22
8.3. Command Code	24
8.4. Resister Default Value	28
8.5. Battery Charger Commands Description	31
8.6. Extended Commands Description	34
9. I/O Equivalence Circuit.....	118
10. Ordering Information	121
11. Marking Diagram.....	121
12. Physical Dimension and Packing Information	122
13. Operational Notes	123
14. Revision History	126

Notation

Category	Notation	Description
Unit	V	Volt (Unit of voltage)
	A	Ampere (Unit of current)
	Ω , Ohm	Ohm (Unit of resistance)
	F	Farad (Unit of capacitance)
	deg., degree	degree Celsius (Unit of Temperature)
	Hz	Hertz (Unit of frequency)
	s (lower case)	second (Unit of time)
	Min	minute (Unit of time)
	b, bit	bit (Unit of digital data)
	B, byte	1 byte = 8 bits
Unit Prefix	M, mega-, mebi-	$2^{20} = 1,048,576$ (used with "bit" or "byte")
	M, mega-, million-	$10^6 = 1,000,000$ (used with " Ω " or "Hz")
	K, kilo-, kibi-	$2^{10} = 1,024$ (used with "bit" or "byte")
	k, kilo-	$10^3 = 1,000$ (used with " Ω " or "Hz")
	m, milli-	10^{-3}
	μ , micro-	10^{-6}
	n, nano-	10^{-9}
	p, pico-	10^{-12}
Numeric Value	xxh, xxH	Hexadecimal number. "x": any alphanumeric of 0 to 9 or A to F.
	Xxb	Binary number; "b" may be omitted. "x": a number, 0 or 1 " " is used as a nibble (4-bit) delimiter. (e.g. "0011_0101b" = "35h")
Address	#xxh	Address in a hexadecimal number. "x": any alphanumeric of 0 to 9 or A to F.
Data	bit[n]	n-th single bit in the multi-bit data.
	bit[n:m]	Bit range from bit[n] to bit[m].
Signal Level	"H", High	High level (over V_{IH} or V_{OH}) of logic signal.
	"L", Low	Low level (under V_{IL} or V_{OL}) of logic signal.
	"Z", "Hi-Z"	High impedance state of 3-state signal.

Reference

Name	Reference Document	Release Date	Publisher
I2C-bus	"UM10204: I ² C-bus specification and user manual Rev. 4"	Feb. 13, 2012	NXP Semiconductors
SMBus	System Management Bus (SMBus) Specification 3.0	Dec. 20, 2014	SBS-IF
JEITA Profile	"A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook-type Personal Computers"	Apr. 10, 2007	JEITA
USB BCS	"Battery Charging Specification Revision 1.2"	Dec. 07, 2010	USB.org
Smart Battery Charger	Smart Battery Charger Specification Revision 1.1	Dec. 11, 1998	SBS-IF
USB 2.0	Universal Serial Bus Specification Revision 2.0	Jul. 26, 2013	USB.org
USB 3.1	Universal Serial Bus Revision 3.1 Specification Rev. 1.0	Aug. 11, 2014	USB.org
USB PD	USB Power Delivery Specification Rev. 2.0 V1.0	Apr. 27, 2000	USB.org

1. Introduction

BD99958GW is a Battery Manager IC for 1 to 4-Cell Lithium-Ion/Lithium-Ion polymer battery pack used in portable equipment such as Tablets, Ultrabooks or others.

BD99958GW includes a Battery Charger, two port BCS1.2 detection, a Battery Monitor for voltage, current, temperature and alarm (INT#, PROCHOT#) Controller.

1.1. Typical Application Circuits

Figure 1 shows the Typical Application Circuit.

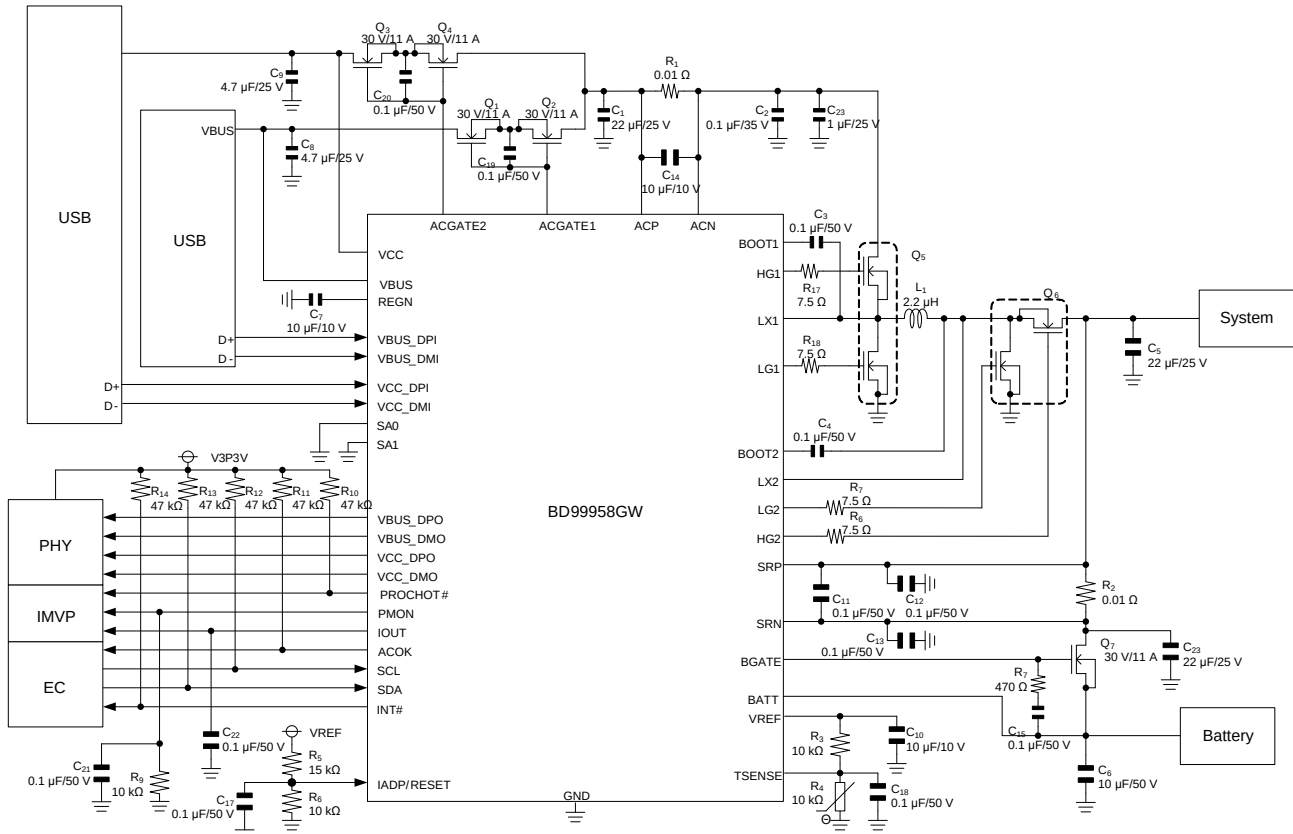


Figure 1. Typical Application Circuit

2. Pin Configuration

G	SA1	PMON	VREF	BATT	SRN	SRP
F	VCC_DPO	SDA	IOUT	BGATE	GND	HG2
E	VCC_DMO	SCL	N/C	TSENSE	LX2	BOOT2
D	VCC_DMI	SA0	VCC_DPI	ACOK	LG2	LG1
C	VBUS_DPO	VBUS_DMO	VBUS_DPI		LX1	BOOT1
B	VBUS_DMI	ACGATE2	ACGATE1	PROCHOT#	VBUS	HG1
A	IADP/RESET	ACP	ACN	INT#	VCC	REGN
	6	5	4	3	2	1

Figure 2. Pin Configuration in WL-CSP (TOP VIEW)

3. Pin Description

Table 1. Pin Description

#	Ball No. [CSP]	Pin Name	Function
1	A1	REGN	LDO output
2	A2	VCC	DC power supply
3	A3	INT#	Interrupt for I2C
4	A4	ACN	Input current sense resistor negative input
5	A5	ACP	Input current sense resistor positive input
6	A6	IADP/RESET	Default input current limit setting pin and system register reset pin
7	B1	HG1	DC/DC buck side high side gate driver
8	B2	VBUS	USB power supply
9	B3	PROCHOT#	Active low open drain output of "processor hot" indicator. The charger IC monitors events like adapter current, battery discharge current. Once any event in PROCHOT# profile is triggered, a minimum 10 ms pulse is asserted.
10	B4	ACGATE1	Charge pump output to drive adapter input n-channel MOSFETs The ACGATE1 voltage is 5 V above VBUS during AC adapter insertion
11	B5	ACGATE2	Charge pump output to drive adapter input n-channel MOSFETs The ACGATE2 voltage is 5 V above VCC during AC adapter insertion.
12	B6	VBUS_DMI	VBUS side USB D- input/output
13	C1	BOOT1	DC/DC buck side driver voltage output
14	C2	LX1	DC/DC buck side inductor connection
15	C3	-	-
16	C4	VBUS_DPI	VBUS side USB D+ input/output
17	C5	VBUS_DMO	VBUS side USB D- output/input
18	C6	VBUS_DPO	VBUS side USB D+ output/input
19	D1	LG1	DC/DC buck side low side gate driver
20	D2	LG2	DC/DC boost side low side gate driver
21	D3	ACOK	AC adapter voltage detection open drain output
22	D4	VCC_DPI	VCC side USB D+ input/output
23	D5	SA0	Slave address decide bit 1 pin input Need to connect the REGN pin or the GND pin
24	D6	VCC_DMI	VCC side USB D- input/output
25	E1	BOOT2	DC/DC boost side driver voltage output
26	E2	LX2	DC/DC boost side inductor connection
27	E3	TSENSE	Battery temperature monitor pin Active low battery present input signal. LOW indicates battery is present, and HIGH indicates the battery is absent and the charging stop.
28	E4	N/C	Non connection pin Please connect PCB GND or open.
29	E5	SCL	SMBus clock input
30	E6	VCC_DMO	VCC side USB D- output/input
31	F1	HG2	DC/DC boost side high side gate driver
32	F2	GND	Ground
33	F3	BGATE	Gate control output
34	F4	IOOUT	Buffered adapter or charge current output selectable with SMBus command
35	F5	SDA	SMBus data input/output
36	F6	VCC_DPO	VCC side USB D+ output/input
37	G1	SRP	Charge current sense resistor positive input
38	G2	SRN	Charge current sense resistor negative input
39	G3	BATT	Battery voltage input
40	G4	VREF	1.5 V LDO output
41	G5	PMON	Buffered total system power current output. Place a resistor between the PMON pin and the GND pin
42	G6	SA1	Slave address decide bit 2 pin input Need to connect the REGN pin or the GND pin

4. Absolute Maximum Ratings (Ta=25°C)

	Parameter	Rating	Unit
Voltage Range (With Respect to GND)	VBUS, VCC, SRN, SRP, ACN, ACP, BATT	-0.3 to +28.0	V
	LX1, LX2	-2 to +28	V
	ACGATE1, ACGATE2, BGATE, BOOT1, BOOT2, HG1, HG2	-0.3 to +32	V
	LX1-BOOT1, LX2-BOOT2	-0.3 to +6.0	V
	ACP-ACN, SRP-SRN	-0.3 to +0.3	V
	VBUS_DPI, VBUS_DMI, SA0, VBUS_DPO, VBUS_DMO, VCC_DPI, VCC_DMI, SA1, VCC_DPO, VCC_DMO, ACOK, REGN, INT#, PROCHOT#, IOUT, PMON, SCL, SDA, LG1, LG2	-0.3 to +7.0	V
	TSENSE, IADP/RESET, VREF	-0.3 to +2.1	V
Maximum Junction Temperature		150	°C
Storage Temperature Range		-50 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

5. Power Dissipation^(Note 1)

Parameter	Symbol	Typ	Unit
UCSP55M3C(BD99958GW)			
Power Dissipation ^(Note 2)	Pd	0.97	W

Layer Number of Measurement Board	Material	Board Size
9 Layers ^(Note 3)	FR-4	63 mm x 55 mm x 1.6 mmt

(Note 1) Based on JESD51-2A (Still-Air) only BD99958GW

(Note 2) Derate by 78.1 mW/°C when operating above Ta=25 °C (when mounted in ROHM's standard board)

(Note 3) Using a 4s5p PCB board

6. Recommended Operating Conditions

Parameter	Min	Max	Unit
VBUS	3.8	25.0	V
VCC	3.8	25.0	V
BATT	0	19.2	V
IIN	-	16	A
ISYS	-	16	A
ICHARGE	-	16	A
Operating Temperature	-30	+85	°C

7. Function Descriptions

7.1. Block Diagram

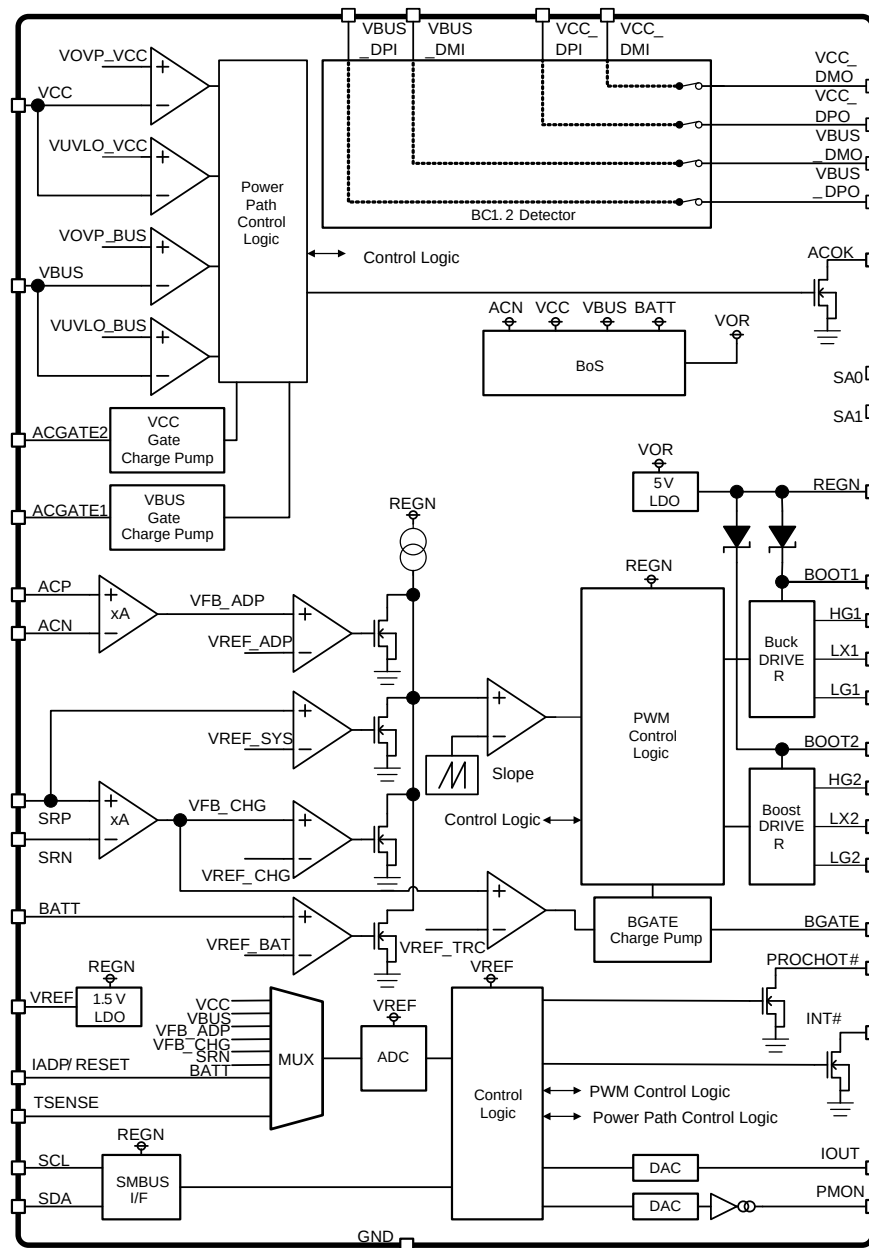


Figure 3. Block Diagram

7.2. Electrical Characteristics for Battery Charger

Adapter=18.0 V, Battery=7.4 V, LX1=LX2=0.0 V, GND=0 V, Ta=25 °C (unless otherwise noted.)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
<General>						
Adapter Standby Current 1	I _{ADP1}	-	1.0	1.5	mA	Charge Pump ON
Adapter Operating Current 2	I _{ADP2}	-	4.0	8.0	mA	Charge Pump ON Not Switching
Battery Standby Current (VBUS=VCC=0.0V)	I _{BATT1}	-	50.0	100.0	μA	BGATE Charge Pump ON REG0x7Ch[2:0]=5h ^(Note 1)
Battery Standby Current (VBUS=VCC=0.0V)	I _{BATT2}	-	25.0	50.0	μA	BGATE Charge Pump OFF Deep Sleep mode REG0x7Ch[2:0]=6h ^(Note 1) SDA=SCL=0 V
Battery Standby Current (VBUS=VCC=0.0V)	I _{BATT3}	-	125	200	μA	BGATE Charge Pump ON PROCHOT# only VSYS [1 ms/S] REG0x7Ch[2:0]=2h ^(Note 1)
Battery Standby Current (VBUS=VCC=0.0V)	I _{BATT4}	-	150	290	μA	BGATE Charge Pump ON PROCHOT# only VSYS [250 μs/S] REG0x7Ch[2:0]=1h ^(Note 1)
Battery Current (VBUS=VCC=0.0V)	I _{BATT5}	-	700	900	μA	BGATE Charge Pump ON with PROCHOT# Monitored System voltage and Battery current REG0x7Ch[2:0]=0h ^(Note 1)
SMBus Operation Frequency	f _{SMB}	10	-	400	kHz	-
REGN Output Voltage	V _{REGN}	5.0	5.2	5.4	V	-
REGN External Output Current Capability	I _{REGN_LD}	-	-	10	mA	-
REGN UVLO Voltage	V _{REGN_UVLO}	2.375	2.500	2.625	V	Detecting REGN falling edge
REGN UVLO Hysteresis Range	V _{REGN_UVLO_HYS RANGE}	50	100	200	mV	Detecting REGN rising edge
LDO Output Voltage	V _{REF}	1.45	1.50	1.55	V	I _{VREF} =1 mA
VREF UVLO Release Voltage	V _{REF_UVLO}	1.35	1.40	1.45	V	Detecting VREF rising edge
VREF UVLO Hysteresis Range	V _{REF_UVLO_HYS_ RANGE}	25	50	100	mV	Detecting VREF falling edge
<External Pin>						
ACOK Low Voltage	V _{ACOKL}	-	-	0.3	V	I _{ACOK} =1 mA
ACOK Leakage Current	I _{L_ACOK}	-	-	1	μA	V _{ACOK} =5.0 V
INT# Low Voltage	V _{INTL}	-	-	0.3	V	I _{ACOK} =1 mA
INT# Leakage Current	I _{L_INT}	-	-	1	μA	V _{INT} =5.0 V
PROCHOT# Low Voltage	V _{PROCHOTL}	-	-	0.3	V	I _{ACOK} =1 mA
PROCHOT# Leakage Current	I _{L_PROCHOT}	-	-	1	μA	V _{PROCHOT#} =5.0 V
TSENSE Pin Input Current	I _{TSENSE}	-	-	1	μA	V _{TSENSE} =1.5 V
IADP Pin Input Current	I _{IADP}	-	-	1	μA	V _{IADP} =5.0 V
SA0 Pin Input Current H	I _{SA0H}	-	-	1	μA	V _{SA0} =5.0 V
SA0 Pin Input Current L	I _{SA0L}	-	-	1	μA	V _{SA0} =0.0 V
SA0 High Threshold Voltage	V _{THH_SA0}	REGN x 0.8	-	-	V	-
SA0 Low Threshold Voltage	V _{THL_SA0}	-	-	REGN x 0.2	V	-
SA1 Pin Input Current H	I _{SA1H}	-	-	1	μA	V _{SA1} =5.0 V
SA1 Pin Input Current L	I _{SA1L}	-	-	1	μA	V _{SA1} =0.0 V
SA1 High Threshold Voltage	V _{THH_SA1}	REGN x 0.8	-	-	V	-
SA1 Low Threshold Voltage	V _{THL_SA1}	-	-	REGN x 0.2	V	-

(Note 1) Resister address refer to extended commands

7.2. Electrical Characteristics for Battery Charger - continued

Adapter=18.0 V, Battery=7.4 V, LX1=LX2=0.0 V, GND=0 V, Ta=25 °C (unless otherwise noted.)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
<PMON>						
Power Monitor Amplifier Gain (I _{PMON})/(V _{ACP} X I _{ACP} + V _{BATT} X I _{BATT})	G _{PMON}	-	16	-	μA/W	REG0x25h[2:0] =6h ^(Note 1) 6.25 W Setting
		-	8	-	μA/W	REG0x25h[2:0] =5h ^(Note 1) 12.5 W Setting
		-	4	-	μA/W	REG0x25h[2:0] =4h ^(Note 1) 25 W Setting
		-	2	-	μA/W	REG0x25h[2:0] =3h ^(Note 1) 50 W Setting
		-	1	-	μA/W	REG0x25h[2:0] =2h ^(Note 1) 100 W Setting
		-	0.5	-	μA/W	REG0x25h[2:0] =1h ^(Note 1) 200 W Setting
		-	0.25	-	μA/W	REG0x25h[2:0] =0h ^(Note 1) 400 W Setting
		ACC _{PMON}	-5	-	+5	%
PMON Maximum Current	I _{PMONMAX}	-	-	200	μA	-
<IOUT>						
IADP Voltage Accuracy	G _{IADP}	-	20	-	V/V	(V _{IADP})/(V _{ACP} - V _{ACN})
	V _{IOUT1}	802.8	819.2	835.6	mV	(V _{ACP} - V _{ACN})=40.96 mV
	V _{IOUT2}	393.2	409.6	426	mV	(V _{ACP} - V _{ACN})=20.48 mV
	V _{IOUT3}	174.1	204.8	235.5	mV	(V _{ACP} - V _{ACN})=10.24 mV
	V _{IOUT4}	81.92	102.4	122.9	mV	(V _{ACP} - V _{ACN})=5.12 mV
	V _{IOUT5}	-	51.2	-	mV	(V _{ACP} - V _{ACN})=2.56 mV
	V _{IOUT6}	-	25.6	-	mV	(V _{ACP} - V _{ACN})=1.28 mV
IDCHG Voltage Accuracy	G _{IDCHG}	-	16	-	V/V	(V _{IDCHG})/(V _{SRN} - V _{SRP})
	V _{IDCHG1}	622.6	655.4	688.2	mV	(V _{SRN} - V _{SRP})=40.96 mV
	V _{IDCHG2}	298.2	327.7	357.2	mV	(V _{SRN} - V _{SRP})=20.48 mV
	V _{IDCHG3}	122.9	163.8	204.8	mV	(V _{SRN} - V _{SRP})=10.24 mV
	V _{IDCHG4}	41	81.9	122.9	mV	(V _{SRN} - V _{SRP})=5.12 mV

(Note 1) Resister address refer to extended commands

7.3. DC Input & Over Voltage Protection (OVP)

7.3.1. Outline

- Dual-input for the battery charger source: USB VBUS and VCC
- 25 V over voltage protection.
- One of two DC input selection (exclusive)
- Effective input is selected by the control registers, VCC as default.

7.3.2. Electrical Characteristics

Adapter=18.0 V, Battery=7.4 V, LX1=LX2=0.0 V, GND=0 V, Ta=25 °C (unless otherwise noted.)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
VCC Input Operating Range	V _{CCRNG}	3.8	-	25	V	-
VCC UVLO Release Voltage	V _{CC_UVLO}	3.7	3.8	3.9	V	VCC rising
VCC UVLO Hysteresis Range	V _{CC_UVLO_HYS_RANGE}	80	130	180	mV	VCC falling
VCC OVP Detection Voltage	V _{CC_OVP}	25.0	25.5	26.0	V	VCC rising
VCC OVP Hysteresis Range	V _{CC_OVP_HYS_RANGE}	100	150	200	mV	VCC falling
USB Input Operating Range	V _{USBRNG}	3.8	-	25	V	-
VBUS UVLO Release Voltage	V _{BUS_UVLO}	3.7	3.8	3.9	V	VBUS rising
VBUS UVLO Hysteresis Range	V _{BUS_UVLO_HYS_RANGE}	80	130	180	mV	VBUS falling
VBUS OVP Detection Voltage	V _{BUS_OVP}	25.0	25.5	26	V	VBUS rising
VBUS OVP Hysteresis Range	V _{BUS_OVP_HYS_RANGE}	100	150	200	mV	VBUS falling
VACOK Output "L" Voltage	V _{OK_ON}	-	-	1.0	V	I(V _{ACOK}) =1 mA
VACOK Leakage Current	I _{OKL}	-	-	1	μA	V _{ACOK} =5 V
VBUS Reverse Output Turn-on Time	t _{VBUS_ON}	-	5	10	ms	-
Voltage Output Turn-off Time	t _{VBUS_OFF}	-	1	5	μs	-

7.4. USB Detection

7.4.1. Outline

- USB Charger port detection
- Supports USB BCS1.2, USB ACA, USB OTG, and PD plug detection.
- Integrated analog switch supports USB HS (480 Mbps).

7.4.2. Electrical Characteristics

(Ta=25 °C, BATT=3.6 V, VBUS=5.0 V)

Parameter	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
<USB Charger Detection>						
VDP_SRC Voltage (output voltage for D+)	V _{DP_SRC}	0.5	0.6	0.7	V	I _o =0 μA to 200 μA
VDM_SRC Voltage (output voltage for D-)	V _{DM_SRC}	0.5	0.6	0.7	V	I _o =0 μA to 200 μA
RCD Resistance (D+ pull up resistance)	R _{CD}	75	100	125	kΩ	-
USB Port Un-detection Resistance (Host D+ pull down resistance)	R _{HDP}	100	-	-	kΩ	-
V _{DAT_REF} Voltage (D+/D- detection voltage)	V _{DAT_REF}	0.3	0.35	0.4	V	HDPR/HDML voltage rising
V _{LGC} Voltage (D+/D- detection voltage)	V _{LGC}	1.2	1.4	1.6	V	HDPR/HDML voltage rising
D+ Sink Current	I _{DP_SINK}	50	85	150	μA	V(HDPR)=0.6 V
D- Sink Current	I _{DM_SINK}	50	85	150	μA	V(HDML)=0.6 V
<USB Switch (DP, DM)>						
Switch On-state resistance	R _{ON_USBSW}	-	5	10	Ω	VIN=0 V or 3.3 V
Switch Off-state leakage Current	I _{IOFF_USB}	-3	-	+3	μA	VIN=0 V or 3.3 V, VBUS=OPEN
Switch Capacitance	C _{SW}	-	6	-	pF	USBSW ON
USB SwitchStart-up Time	t _{UPUSB}	-	-	1	ms	USBSW OFF→ON

7.5. DC/DC Converter

7.5.1. Outline

- Input Current Limit value setting: 96 mA to 16352 mA for VBUS and VCC
- Charger supply voltage anti-collapse control.
- Low power mode support
- Include thermal protection and shutdown

7.5.2. Electrical Characteristics

Adapter=18.0 V, Battery=7.4 V, LX1=LX2=0.0 V, GND=0 V, Ta=25 °C (unless otherwise noted.)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
<INPUT CURRENT>						
USB 500 mA Current Accuracy	I _{USB500}	398	448	500	mA	REG0x07h/08h=01C0h ^(Note 1)
USB 900 mA Current Accuracy	I _{USB900}	764	832	900	mA	REG0x07h/08h=0340h ^(Note 1)
BCS1.2 1500 mA Current Accuracy	I _{USB1500}	1380	1440	1500	mA	REG0x07h/08h=05A0h ^(Note 1)
USB-PD 3A Current Accuracy	I _{USB3000}	2824	2912	3000	mA	REG0x07h/08h=0B60h ^(Note 1)
USB-PD 5A Current Accuracy	I _{USB5000}	4792	4896	5000	mA	REG0x07h/08h=1320h ^(Note 1)
Input Current Setting Range	I _{ADPRNG}	96	-	16352	mA	REG0x07h or REG0x08h ^(Note 1)
Charge Current Setting LSB	I _{ADPLSB}	-	32	-	mA	
Input Current Accuracy (10 mΩ current sense resistor)	I _{INLIM1}	-2 %	4096	+2 %	mA	-
	I _{INLIM2}	-3 %	2048	+3 %	mA	-
	I _{INLIM3}	-5 %	1024	+5 %	mA	-
	I _{INLIM4}	-10 %	512	+10 %	mA	-
IADP/RESET Pin Input Voltage Range	V _{ADPTRNG}	0.1	-	1.4	V	-
IADP/RESET Pin Current Setting Range	I _{ADPTRNG}	128	-	5120	mA	-
IADP/RESET Pin Current Setting Step	I _{ADPSTEP}	-	512	-	mA	-
RESET Detection Voltage	V _{RESET_DET}	-	-	0.22	V	IADP/RESET voltage falling
RESET Release Voltage	V _{RESET_REL}	0.44	-	-	V	IADP/RESET voltage rising
RESET Detection Duration Time	t _{RESET}	100	-	-	μs	-
<SYSTEM VOLTAGE>						
Minimum System Voltage Setting Range	V _{MSVRNG}	2.560	-	19.2	V	VSYSREG_SET=2,560 mV to 19,200 mV, 64 mV steps.
Minimum System Voltage Setting LSB	V _{MSVLSB}	-	64	-	mV	
Minimum System Voltage Accuracy	V _{MSV1}	-2.0 %	3.072	+2.0 %	V	REG0x11h=0C00h ^(Note 1)
	V _{MSV2}	-1.0 %	6.144	+1.0 %	V	REG0x11h=1800h ^(Note 1)
	V _{MSV3}	-2.0 %	9.216	+2.0 %	V	REG0x11h=2400h ^(Note 1)
	V _{MSV4}	-2.0 %	12.288	+2.0 %	V	REG0x11h=3000h ^(Note 1)
VSYS Output Voltage Ratio	V _{SYSR}	VBATT x 1.10	VBATT x 1.15	VBATT x 1.20	V	VSYSREG_SET < V _{SYSR}
VSYS OVP Voltage	V _{SYS_OVP}	-	V _{SYSSSET} x 1.1	-	V	-
VSYS OVP Detection Hysteresis Range	V _{ROVP_HYS_RANGE}	-	V _{ROUT} X 1.05	-	V	-
<Anti-Collapse Voltage>						
VBUS Anti-Collapse Threshold Voltage Range	V _{ANTI_VBUS}	3.84	-	25.0	V	REG0x0Dh ^(Note 1)
Anti-Collapse Threshold Voltage Accuracy	V _{ANTI_VBUS_ACC}	-100	-	+100	mV	-
VCC Anti-Collapse Threshold Voltage Range	V _{ANTI_VCC}	3.84	-	25.0	V	REG0x0Eh ^(Note 1)
Anti-Collapse Threshold Voltage Accuracy	V _{ANTI_VCC_ACC}	-100	-	+100	mV	-

(Note 1) Resister address refer to extended commands

7.5.2. Electrical Characteristics - continued

Adapter=18.0 V, Battery=7.4 V, LX1=LX2=0.0 V, GND=0 V, Ta=25 °C (unless otherwise noted.)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
<Switching Frequency>						
Switching Frequency 1	f _{OSC1}	510	600	690	kHz	REG0x0Ch[3:2]=00b ^(Note 1)
Switching Frequency 2	f _{OSC2}	770	860	950	kHz	REG0x0Ch[3:2]=01b ^(Note 1)
Switching Frequency 3	f _{OSC3}	850	1000	1150	kHz	REG0x0Ch[3:2]=10b ^(Note 1)
Switching Frequency 4	f _{OSC4}	1020	1200	1380	kHz	REG0x0Ch[3:2]=11b ^(Note 1)
<DRIVER>						
HRDV1 PMOS RON	R _{HDRV1P}	-	6.0	10.0	Ω	-
HRDV1 NMOS RON	R _{HDRV1N}	-	0.7	1.3	Ω	-
LRDV1 PMOS RON	R _{LDRV1P}	-	7.5	12.0	Ω	-
LRDV1 NMOS RON	R _{LDRV1N}	-	0.9	1.4	Ω	-
HRDV2 PMOS RON	R _{HDRV2P}	-	6.0	10.0	Ω	-
HRDV2 NMOS RON	R _{HDRV2N}	-	0.7	1.3	Ω	-
LRDV2 PMOS RON	R _{LDRV2P}	-	7.5	12.0	Ω	-
LRDV2 NMOS RON	R _{LDRV2N}	-	0.9	1.4	Ω	-

(Note 1) Resister address refer to extended commands

7.5.3. Detailed IADP Input Current Limit Settings

- Input Current limit is set by the external IADP/RESET pin.
- This function is enabled by VM_CTRL_SET.EXTIADPEN bit =1.
- Once the charger reset is released when this function is enabled, the corresponding input current value which depends on the IADP/RESET voltage will be stored to the SEL_ILIM_VAL register. And this is used as the input current limit. It can be overwritten through SMBus.

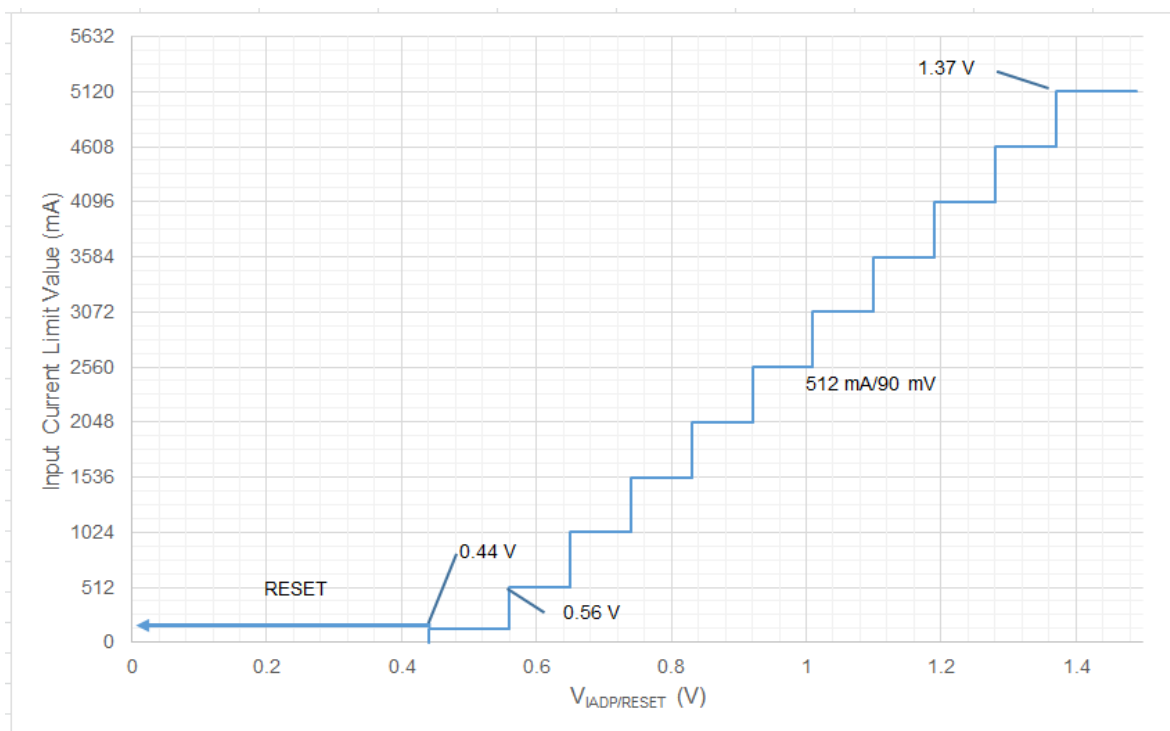


Figure 4. IADP Pin Input Current Limit Settings

7.6. Charger

7.6.1. Outline

- Supports battery insertion and removal detection.
- Controls the VSYS output voltage with a deeply discharged battery.
- JEITA compliant Battery Charging Profile with thermal control of the charging current and voltage settings by measuring the temperature from the external thermistor
- Supports battery supplement mode
- Automatic or manual control of the Watchdog Timer (via software) while Pre-charging and Fast-charging

7.6.2. Electrical Characteristics

Adapter=18.0 V, Battery=7.4 V, LX1=LX2=0.0 V, GND=0 V, Ta=25 °C (unless otherwise noted.)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Battery Input Operating Range	V _{BATRNG}	0.0	-	19.2	V	With Adapter Input
		2.5	-	19.2	V	Without Adapter Input
<CHARGE VOLTAGE>						
Charge Voltage Setting Range	V _{CVRNG}	2.560	-	19.200	V	REG0x1Ah, REG0x1Bh or REG0x1Ch (Note 1)
Charge Voltage Setting LSB	V _{CVLSB}	-	16	-	mV	
Charge Voltage Accuracy	V _{CV1S}	-0.5 %	4.192	+0.5 %	V	REG0x1Ah/0x1Bh/0x1Ch=1060h (Note 1)
	V _{CV2S}	-0.5 %	8.400	+0.5 %	V	REG0x1Ah/0x1Bh/0x1Ch=20D0h (Note 1)
	V _{CV3S}	-0.5 %	12.592	+0.5 %	V	REG0x1Ah/0x1Bh/0x1Ch=3130h (Note 1)
	V _{CV4S}	-0.5 %	16.800	+0.5 %	V	REG0x1Ah/0x1Bh/0x1Ch=41A0h (Note 1)
VBATT OVP Detection Range	V _{OVPNG}	2.56	-	19.2	V	REG0x1Eh (Note 1)
<CHARGE CURRENT>						
Charge Current Setting Range	I _{CHGRNG}	0	-	16384	mA	REG0x16h (Note 1)
Charge Current Setting LSB	I _{CHGLSB}	-	64	-	mA	
Charge Current Accuracy (10mΩ current sense resistor, BATT > Minimum System Voltage)	I _{CHG1}	-2 %	4096	+2 %	mA	REG0x16h=1000h (Note 1)
	I _{CHG2}	-3 %	2048	+3 %	mA	REG0x16h=0800h (Note 1)
	I _{CHG3}	-5 %	1024	+5 %	mA	REG0x16h=0400h (Note 1)
	I _{CHG4}	-20 %	256	+20 %	mA	REG0x16h=0100h (Note 1)
	I _{CHG5}	-40 %	128	+40 %	mA	REG0x16h=0080h (Note 1)
Trickle Charge Current Setting Range	I _{TRCCHGRNG}	0	256	1024	mA	REG0x14h or REG0x15h (Note 1)
Trickle Charge Current Setting LSB	I _{TRCCHGLSB}	-	64	-	mA	
Maximum Trickle Charge Current (10mΩ current sense resistor, BATT < Minimum System Voltage)	I _{CHG6}	-	1024	-	mA	REG0x14h or REG0x15h (Note 1)
<Thermal Control>						
Battery Temperature Threshold HOT1	V _{TH_HOT1}	-	45	-	°C	OTP Programmable REG0x45h (Note 1)
Battery Temperature Threshold HOT2	V _{TH_HOT2}	-	50	-	°C	OTP Programmable REG0x44h (Note 1)
Battery Temperature Threshold HOT3	V _{TH_HOT3}	-	58	-	°C	OTP Programmable REG0x43h (Note 1)
Battery Temperature Threshold COLD1	V _{TH_COLD1}	-	10	-	°C	OTP Programmable REG0x42h (Note 1)
Battery Temperature Threshold COLD2	V _{TH_COLD2}	-	2	-	°C	OTP Programmable REG0x41h (Note 1)
Battery Temperature Measurement Accuracy	T _{BAT}	-2	-	+2	°C	-
Battery Open Detection Voltage	V _{TH_OPN}	-	V _{REF} x0.95	-	V	-
<Battery Short Current Detection>						
Battery Short Current Detection	I _{BATSHORT}	0	-	25,000	mA	REG0x1Fh (Note 1)
Battery Short Current Duration Time	t _{BATSHORT}	4	-	1020	ms	REG0x10h[15:8] (Note 1)
<Watchdog Timer>						
Pre Charging Time	t _{PRE}	13.0	14.5	16	min	-
Fast Charging Time	t _{FAST}	196	218	240	min	-
High Temperature Protection Time	t _{HTPRO}	108	120	132	min	Over 58 °C
Charging Termination Delay Time	t _{TOPOFF}	13	15	17	s	-

(Note 1) Resister address refer to extended commands

7.6.3. Battery Charging Profile

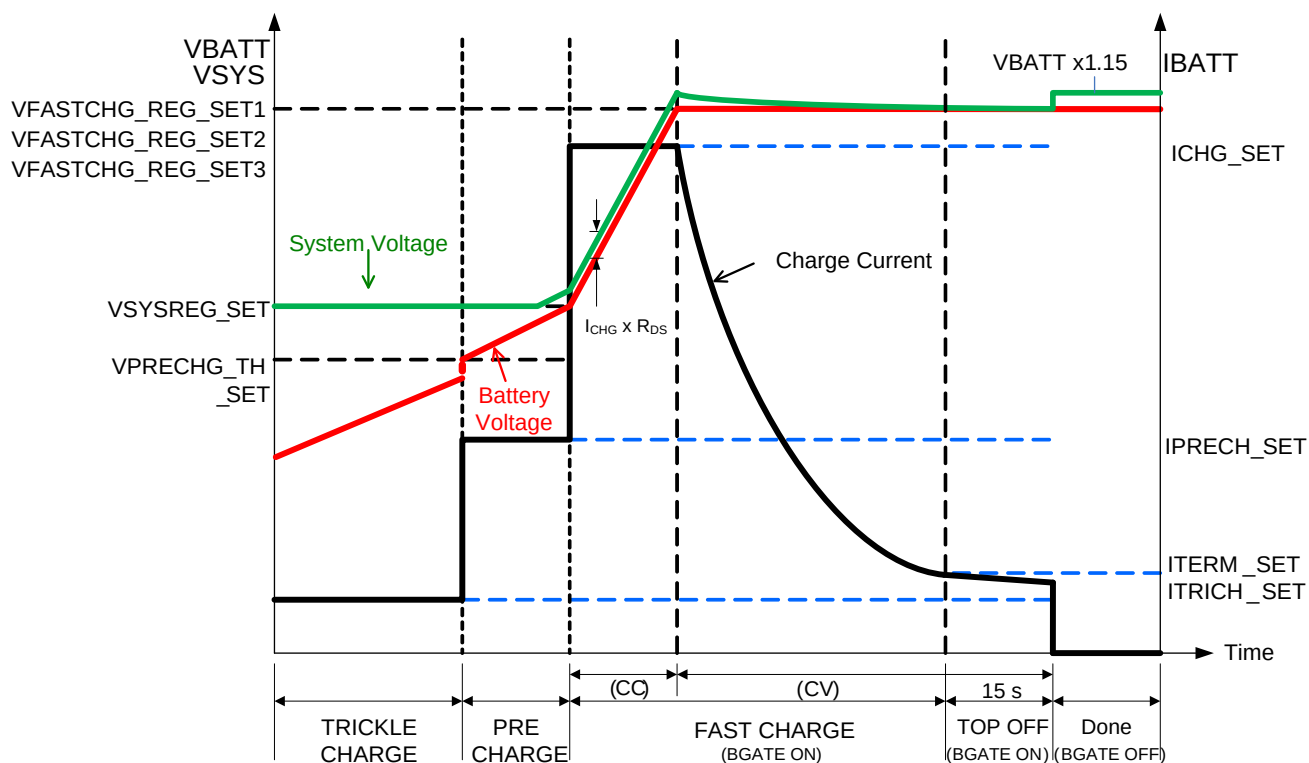
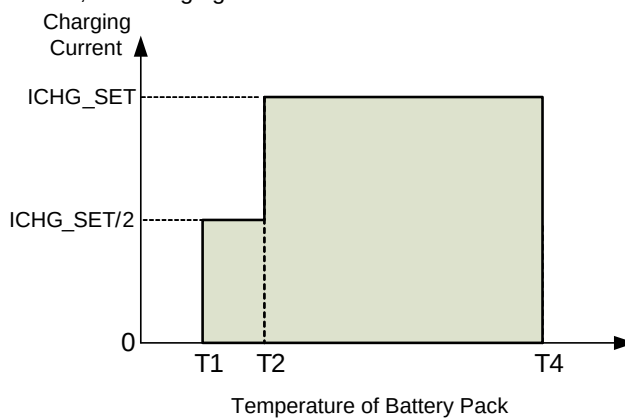
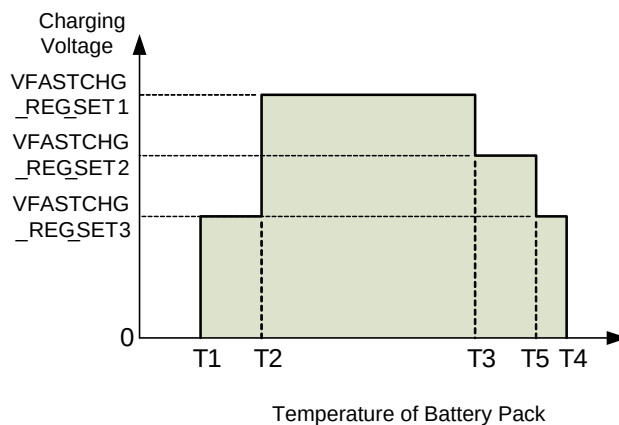


Figure 5. Battery Charging Profile

The charging current is controlled by the battery temperature measured from the external thermistor. In the low-temperature condition, the charging current is reduced to a half of the setting value (ICHG_SET).



The charging voltage is also reduced by the temperature as set by the control registers, VFASTCHG_REG_SET1, VFASTCHG_REG_SET 2, and VFASTCHG_REG_SET 3.



7.7. Reverse DC/DC Converter

7.7.1. Outline

- Charger provides a voltage output (Reverse Buck/Boost) via VBUS or/and VCC when an USB OTG device is connected.

7.7.2. Electrical Characteristics

Adapter=18.0 V, Battery=7.4 V, LX1=LX2=0.0 V, GND=0 V, Ta=25 °C (unless otherwise noted.)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
<OUTPUT CURRENT Limit>						
Output Current Limit Setting Range	I _{RADPRNG}	0	4096	8128	mA	REG0x09h ^(Note 1)
Output Current Limit Setting LSB	I _{RADPLSB}	-	32	-	mA	
Output Current Limit Accuracy (10 mΩ current sense resistor)	I _{RADP1}	-2 %	4096	+2 %	mA	REG0x09h =1000h ^(Note 1)
	I _{RADP2}	-3 %	2048	+3 %	mA	REG0x09h =0800h ^(Note 1)
	I _{RADP3}	-5 %	1024	+5 %	mA	REG0x09h =0400h ^(Note 1)
	I _{RADP4}	-10 %	512	+10 %	mA	REG0x09h =0200h ^(Note 1)
<Output VOLTAGE>						
Output Voltage Setting 1	V _{ROUT1}	4.95	5.0	5.05	V	REG0x19h =1380h ^(Note 1)
Output Voltage Setting 2	V _{ROUT2}	5.15	5.2	5.25	V	REG0x19h =1440h ^(Note 1)
Output Voltage Setting 3	V _{ROUT3}	8.91	9.0	9.09	V	REG0x19h =2340h ^(Note 1)
Output Voltage Setting 4	V _{ROUT4}	11.88	12.0	12.12	V	REG0x19h =2F00h ^(Note 1)
Output Voltage Setting 5	V _{ROUT5}	19.8	20.0	20.2	V	REG0x19h =4E40h ^(Note 1)
Output Voltage Setting Range	V _{ROUTRNG}	4.032	-	22.016	V	REG0x19h ^(Note 1)
Output Voltage Setting LSB	V _{ROUTLSB}	-	64	-	mV	
VBUS Buck/Boost Output Short Circuit Protection	V _{RSCP}	-	V _{BUS_UVLO} V _{CC_UVLO}	-	V	-
VBUS Buck/Boost OVP Voltage	V _{ROVP}	-	V _{ROUT} X 1.1	-	V	-
VBUS Buck/Boost OVP Detection Hysteresis Range	V _{ROVP_HYS_RANGE}	-	V _{ROUT} X 1.05	-	V	-

(Note 1) Register address refer to extended commands

7.8. 12-bit ADC

7.8.1. Outline

- 12-bit Successive Approximation Register A/D Converter
- Input Voltage range: 2.0 V to 19.2 V (VBATT)
- Input Voltage range: 2.0 V to 25.0 V (VBUS, VCC, ACP, SRP)
- Input Voltage range: 0.1 V to 1.4 V (TSENSE)
- Input Voltage range: 0.1 V to 1.4 V (IADP/RESET)
- Current monitor range: 0 A to 16.384 A (IACP)
- Current monitor range: 0 A to 25 A (IBATT)

7.8.2. Electrical Characteristics

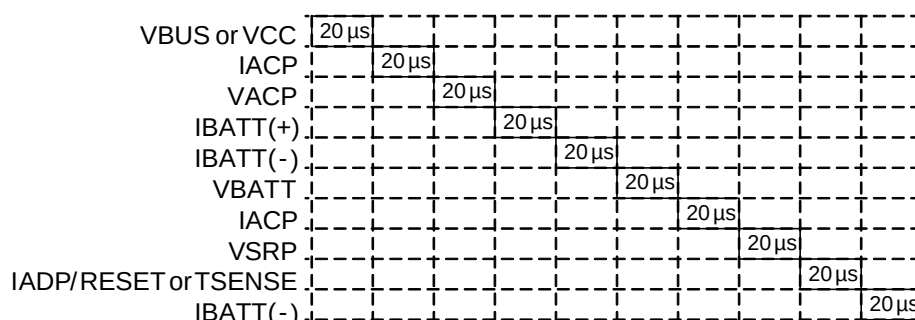
(Unless otherwise specified, Ta=25 °C, VREF=1.5 V)

Unless otherwise specified, $T_A = 25^{\circ}\text{C}$, $V_{REF} = 1.5\text{ V}$						
Parameter	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
<12-bit SAR ADC>						
Resolution	RES	-	-	12	bit	-
Conversion Period	t _{CONV}	-	20	-	μs	-
Gain Error	Gerr	-1.1	-	+1.1	%	BATT, VBUS, VCC, ACP, SRP=5 V and 15 V
Gain Error	Gerr	-1.1	-	+1.1	%	TSENSE, IADP/RESET = 0.5 V and 1.0 V
Gain Error	Gerr	-1.1	-	+1.1	%	IACP, IBATT = 1.5 A and 8 A
Voltage Offset Error	V _{OFFSET}	-110	0	+110	mV	-
Current Offset Error	I _{OFFSET}	-110	0	+110	mA	-

7.8.3. Functions

SAR-ADC measures the 10 following factors by time sharing. These factors can be disabled by SMBus command.
The actual value and the 2-sample moving average value are read by SMBus command.

#	Factor	Conversion Period	Conversion Interval
1	VBUS or VCC	20 μs	VBUS 400 μs VCC 400 μs
2	IACP	20 μs	200 μs
3	VACP	20 μs	200 μs
4	IBATT(+)	20 μs	200 μs
5	IBATT(-)	20 μs	200 μs
6	VBATT	20 μs	200 μs
7	IACP	20 μs	200 μs
8	VSRP	20 μs	200 μs
9	IADP/RESET or TSENSE	20 μs	IADP/RESET 200 μs TSENSE 1 s
10	IBATT(-)	20 μs	200 μs



The power calculation of PMON is carried out from IACP, VACP, IBATT, VBATT.

$$PACP = IACP \times VACP$$

$$PBAT = IBATT \times VBATT$$

$$PMON = PACP + PBAT$$

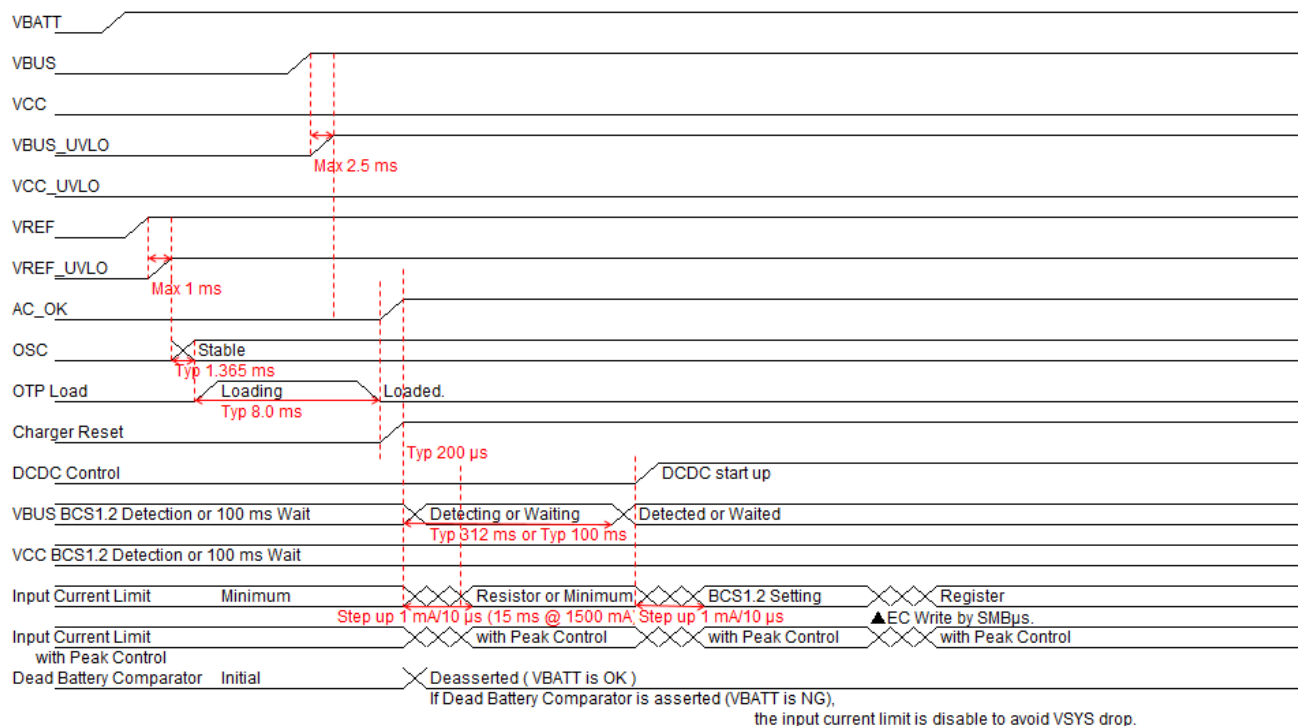
PMON power change can be observed when the value is stable longer than the "Conversion Interval", 200 μs.

7.9. Power On

Whenever BD99958GW receives power from the adapter or battery, BD99958GW wakes up and starts loading data from the OTP. After OTP loading is completed, BD99958GW is in standby position.

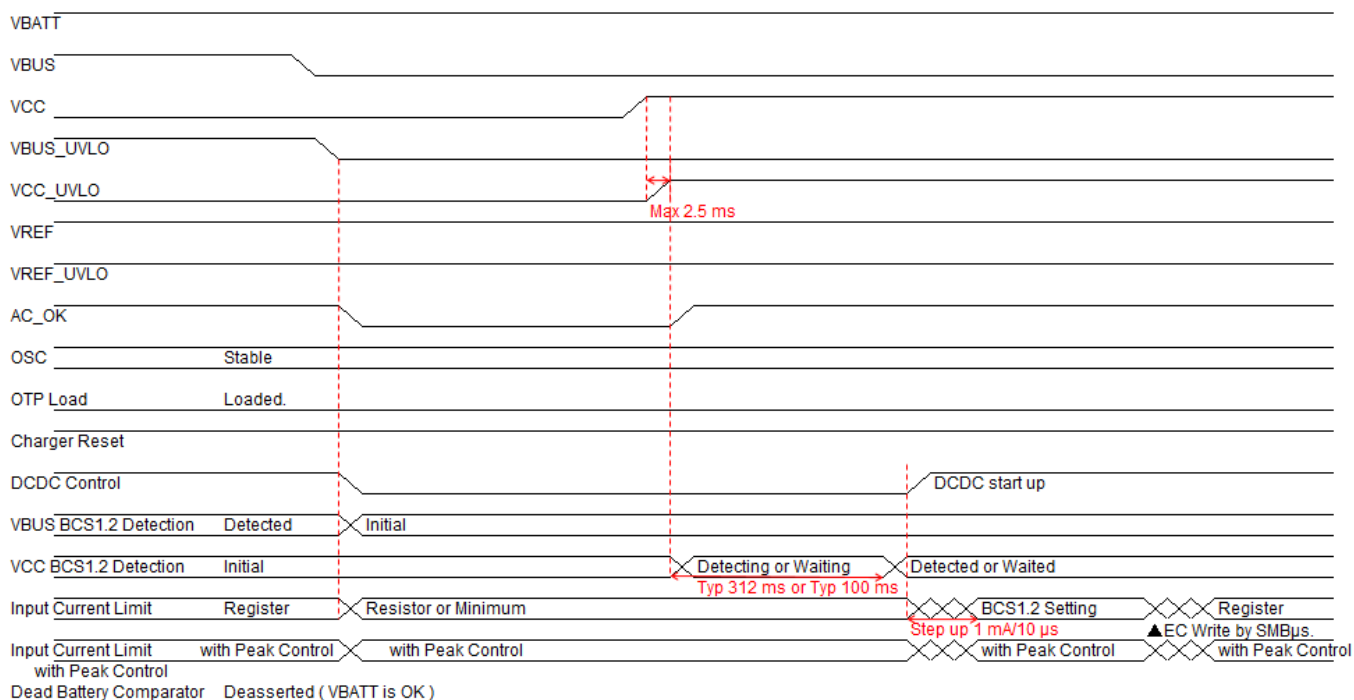
7.9.1. VBATT Power On and VBUS/VCC Plugged-in

At the first VBATT power on, BD99958GW starts OTP loading. And when VBUS or VCC is eventually plugged in, BD99958GW asserts ACOK and starts the BCS1.2 Detection sequence. After the BCS1.2 Detection is completed, BD99958GW limits the input current, reflects the BCS1.2 setting and starts charging.



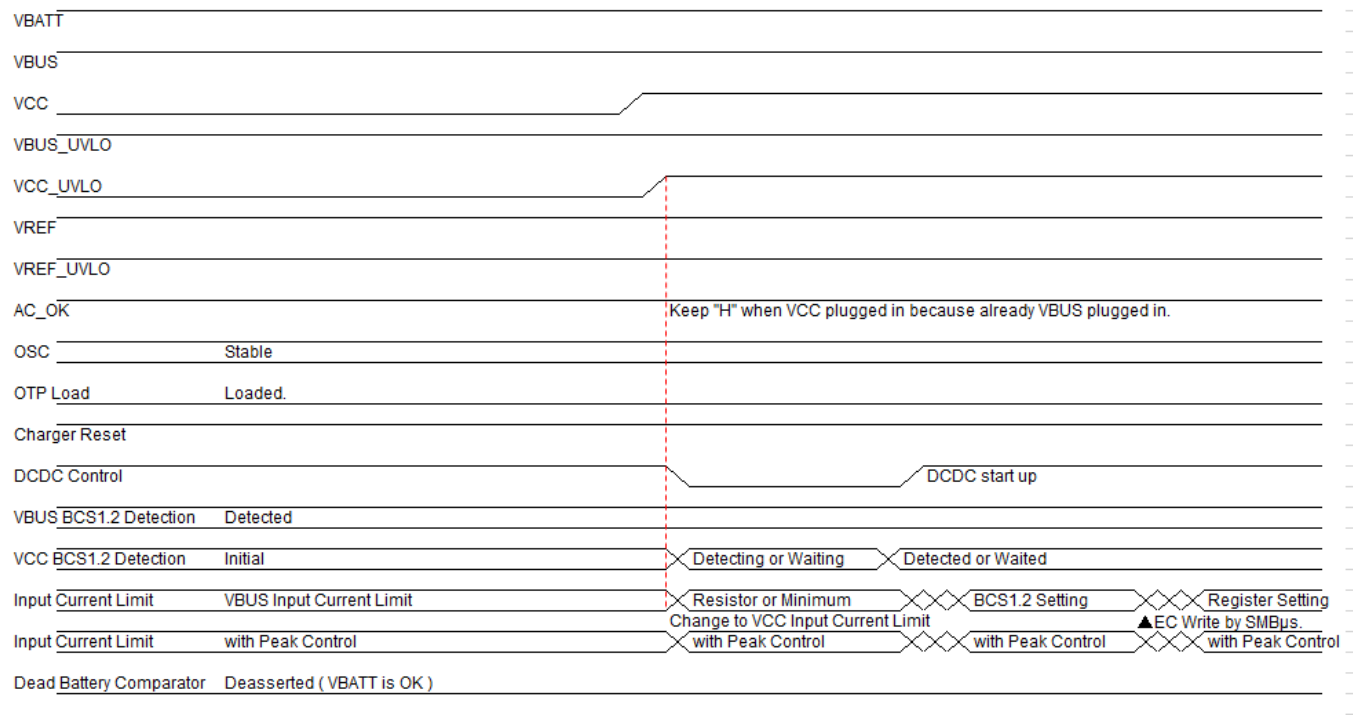
7.9.2. VBUS/VCC Plugged-off

When VBUS plugged off, BD99958GW deasserts AC_OK and limits input current as IADP external pin or minimum setting (it is programmable). And then VBUS or VCC plugged in again, BD99958GW asserts AC_OK and starts BCS1.2 detection.



7.9.3. VBUS and VCC Plugged-in

When VBUS plugged in and then VCC plugged in, BD99958GW selects VBUS or VCC with priority setting. If VCC is 1st priority (programmable), BD99958GW changes power source from VBUS to VCC. If VBUS is 1st priority BD99958GW keeps power source VBUS. Each case AC_OK keeps “H”.



8. Control Specification

BD99958GW has several control registers to set configurations or to sense the hardware status for the internal function operations. Host is able to write to or read from the control registers via SMBus (friendly I2C).

8.1. SMBus Communication

BD99958GW operates in slave mode on the SMBus and supports Layer 2 communication protocol.

8.1.1. SMBus Slave Address

Slave Address for the BD99958GW is 0001_ xx1.

The register address is set by "Slave Address". The "Slave Address" is also used as the start address of contiguous addressing for multiple write or read access.

The slave address can be set external pin assigned the SA0 pin and the SA1 pin. The SA0 pin assign slave address bit "1" and the SA1 pin assign slave address bit "2".

For SMBus communication, the SA0 pin and the SA1 pin need to connect the REGN pin or the GND pin.

Table 2. Description of Slave Address

SA1	SA0	Slave Address(Bit)	Slave Address(DEC)
0	0	0001_ <u>00</u> 1	9
0	1	0001_ <u>01</u> 1	11
1	0	0001_ <u>10</u> 1	13
1	1	0001_ <u>11</u> 1	15

8.2. SMBus Protocols

The following is a description of the various SMBus protocols. BD99958GW supports the protocols defined in this section. BD99958GW does not support all the protocols defined in the SMBus Specification. The results returned by such a device to a protocol it does not support is undefined.

Below is a key to the protocol diagrams in this section. Not all protocol elements will be presented in every command. For instance, not all packets are required to include the packet error code.

- S Start Condition
- Sr Repeated Start Condition
- Rd Read (bit value of 1)
- Wr Write (bit value of 0)
- x Shown under a field indicates that that field is required to have the value of 'x'
- A Acknowledge (this bit position may be '0' for an ACK)
- N Acknowledge (this bit position may be '1' for a NACK)
- P Stop Condition
- PEC Packet Error Code
-  Master (SMBus Host) to Slave
-  Slave (SMBus Device) to Master

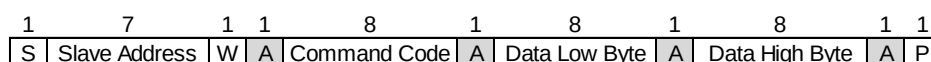
BD99958GW supports following protocols.

- ✧ Write Word
- ✧ Read Word

8.2.1. Write Word

The first byte of a Write Word access is the command code. The next are the high data byte and low data byte to be written. In this example the master asserts the slave device address followed by the write bit. The device acknowledges and the master delivers the command code. The slave again acknowledges before the master sends the data bytes. The slave acknowledges each byte, and the entire transaction is finished with a STOP condition.

BD99958GW does not support PEC.

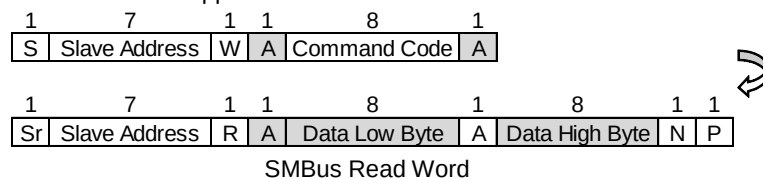


SMBus Write Word

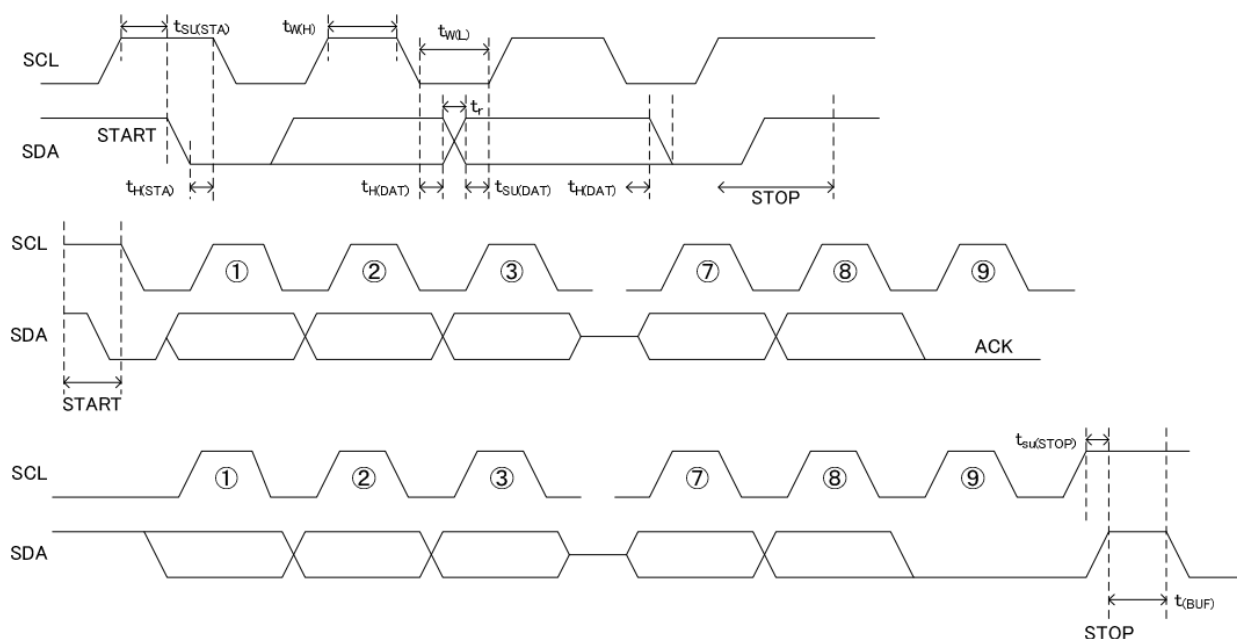
8.2.2. Read Word

Reading data is slightly more complicated than writing data. First the host must write a command to the slave device. Then it must follow that command with a repeated START condition to denote a read from that device's address. The slave then returns one high and low byte of data.

Note that there is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer. BD99958GW does not support PEC.



8.2.3. SMBus Communication Timing Waveforms and Timing Specification



(Unless otherwise specified, $T_a=25\text{ }^{\circ}\text{C}$, $V_{REF}=1.5\text{ V}$)

Unless otherwise specified, TA=25 °C, VREF=1.5 V						
Parameter	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
<SMBus>						
SMBus Frequency	fSMBUS	10	-	400	kHz	
SDA/SCL Input Low Voltage	VINL	0.0	-	0.8	V	
SDA/SCL Input High Voltage	VINH	2.1	-	5.5	V	
SDA Hold Time from SCL	tH(DAT)	250	-	-	ns	
SDA Setup Time from SCL	tSU(DAT)	300	-	-	ns	
Start Condition Hold Time from SCL	tH(STA)	4	-	-	µs	
Start Condition Setup Time from SCL	tSU(STA)	4.7	-	-	µs	
Stop Condition Setup Time from SCL	tSU(STOP)	4	-	-	µs	
Bus Free Time	tBUF	4.7	-	-	µs	

8.3. Command Code

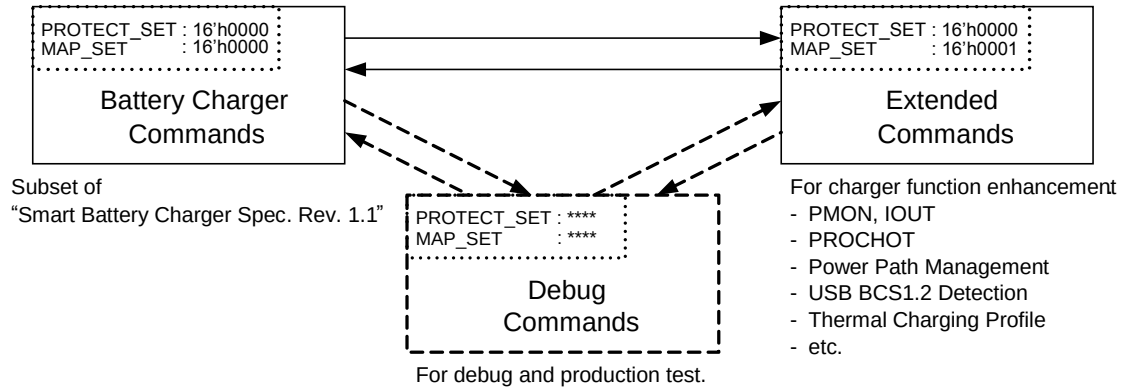
BD99958GW has 3 command maps, "Battery Charger Commands", "Extended Commands" and "Debug Commands". All commands are addressed within 00h to 7Fh address area. And 80h to FFh address is a mirror of 00h to 7Fh.

"Battery Charger Commands" is a subset of "Smart Battery Charger Specification Revision 1.1."

"Extended Commands" is for charger function enhancement.

"Debug Commands" are used for debug purpose or in production test.

These are selectable by MAP_SET command. Default MAP_SET value is set 16h'0000.



8.3.1. Battery Charger Commands

Following is a table of "Battery Charger Commands" which BD99958GW supports. "Battery Charger Commands" is subset of "Smart Battery Charger Specification Revision 1.1."

Reserved command should not be accessed. If accessed, operation is not guaranteed.

Code	Command	Protocols	Byte Size	Description
14h	ChargingCurrent	Read/Write Word	2	The Battery, System Host or other master device sends the desired charging rate (mA). This command is a mirror of ICHG_SET command of the extended command.
15h	ChargingVoltage	Read/Write Word	2	The Battery, System Host or other master device sends the desired charging voltage to the Smart Battery Charger (mV). This command is a mirror of VFASTCHG_REG_SET1 command of the extended command.
3Ch	IBUS_LIM_SET	Read/Write Word	2	VBUS Input Current Limit Setting. This command is a mirror of IBUS_LIM_SET command of the extended command.
3Dh	ICC_LIM_SET	Read/Write Word	2	VCC Input Current Limit Setting. This command is a mirror of ICC_LIM_SET command of the extended command.
3Eh	PROTECT_SET	Read/Write Word	2	Access Un-protect Setting for the "debug command map" (debug and production test only). This command is a mirror of PROTECT_SET command of the extended command.
3Fh	MAP_SET	Read/Write Word	2	Change Command Code Map. This command is a mirror of MAP_SET command of the extended command.

8.3.2. Extended Commands

Following is a table of "Extended Commands" which BD99958GW supports. "Extended Commands" is for charger function enhancement.

Reserved command should not be accessed. If accessed, operation is not guaranteed.

Code	Command	Protocols	Byte Size	Description
00h	CHGSTM_STATUS	Read Word	2	Charger State Machine Status
01h	VBAT/VSYS_STATUS	Read Word	2	VBATT and VSYS Status
02h	VBUS/VCC_STATUS	Read Word	2	VBUS and VCC Status
03h	CHGOP_STATUS	Read Word	2	Charger Operation Status
04h	WDT_STATUS	Read Word	2	Charger WDT and Temperature WDT Status
05h	CUR_ILIM_VAL	Read Word	2	Actual Input Current Limit
06h	SEL_ILIM_VAL	Read Word	2	Selected Input Current Limit
07h	IBUS_LIM_SET	Read/Write Word	2	VBUS Input Current Limit Setting
08h	ICC_LIM_SET	Read/Write Word	2	VCC/VACP Input Current Limit Setting
09h	IOTG_LIM_SET	Read/Write Word	2	OTG Output Current Limit Setting
0Ah	VIN_CTRL_SET	Read/Write Word	2	VBUS and VCC Control Setting
0Bh	CHGOP_SET1	Read/Write Word	2	Charger Operation Control Setting 1
0Ch	CHGOP_SET2	Read/Write Word	2	Charger Operation Control Setting 2
0Dh	VBUSCLPS_TH_SET	Read/Write Word	2	VBUS Collapse Detect Threshold Voltage Setting
0Eh	VCCCLPS_TH_SET	Read/Write Word	2	VCC Collapse Detect Threshold Voltage Setting
0Fh	CHGWDI_SET	Read/Write Word	2	Charger WDT Setting
10h	BATWDT_SET	Read/Write Word	2	Battery Temperature and Battery Short Current WDT Setting
11h	VSYSREG_SET	Read/Write Word	2	VSYS Regulation Setting
12h	VSYSVAL_THH_SET	Read/Write Word	2	VSYS Valid Threshold High Setting (Hysteresis)
13h	VSYSVAL_THL_SET	Read/Write Word	2	VSYS Valid Threshold Low Setting (Hysteresis)
14h	ITRICH_SET	Read/Write Word	2	Trickle-charge Current Setting
15h	IPRECH_SET	Read/Write Word	2	Pre-charge Current Setting
16h	ICHG_SET	Read/Write Word	2	Fast-charge Current Setting
17h	ITERM_SET	Read/Write Word	2	Charge Termination Current Setting
18h	VPRECHG_TH_SET	Read/Write Word	2	Pre-charge Voltage Threshold Setting
19h	VRBOOST_SET	Read/Write Word	2	Reverse Buck Boost Voltage Setting
1Ah	VFASTCHG_REG_SET1	Read/Write Word	2	Fast Charge Voltage Regulation Setting 1
1Bh	VFASTCHG_REG_SET2	Read/Write Word	2	Fast Charge Voltage Regulation Setting 2 (Hot 1)
1Ch	VFASTCHG_REG_SET3	Read/Write Word	2	Fast Charge Voltage Regulation Setting 3 (Hot 2)
1Dh	VRECHG_SET	Read/Write Word	2	Re-charge Battery Voltage Setting
1Eh	VBATOV_P_SET	Read/Write Word	2	Battery Over Voltage Protection Setting
1Fh	IBATSHORT_SET	Read/Write Word	2	Battery Short Current Protection Setting
20h	PROCHOT_CTRL_SET	Read/Write Word	2	PROCHOT# Pin Control Setting
21h	PROCHOT_ICRIT_SET	Read/Write Word	2	Peak Input Current Threshold Setting for the PROCHOT# pin
22h	PROCHOT_INORM_SET	Read/Write Word	2	Average Input Current Threshold Setting for the PROCHOT# pin
23h	PROCHOT_IDCHG_SET	Read/Write Word	2	Dis-charge Current Threshold Setting for the PROCHOT# pin
24h	PROCHOT_VSYS_SET	Read/Write Word	2	VSYS Voltage Threshold Setting for the PROCHOT# pin
25h	PMON_IOUT_CTRL_SET	Read/Write Word	2	PMON and IOUT Output Control Setting
26h	PMON_DACIN_VAL	Read Word	2	PMON DAC Input Value (for debug and production test)
27h	IOUT_DACIN_VAL	Read Word	2	IOUT DAC Input Value (for debug and production test)
28h	VCC_UCD_SET	Read/Write Word	2	BCS1.2 Charger Detector on the VCC Side Setting
29h	VCC_UCD_STATUS	Read Word	2	BCS1.2 Charger Detect Status on the VCC Side
2Ah	(reserved)	-	-	-
2Bh	VCC_UCD_FCTRL_SET	Read/Write Word	2	BCS1.2 Charger Detector on the VCC Side Manual Control Setting
2Ch	VCC_UCD_FCTRL_EN	Read/Write Word	2	BCS1.2 Charger Detector on the VCC Side Manual Control Enable
2Dh	(reserved)	-	-	-
2Eh	(reserved)	-	-	-
2Fh	(reserved)	-	-	-
30h	VBUS_UCD_SET	Read/Write Word	2	BCS1.2 Charger Detector on the VBUS side Setting
31h	VBUS_UCD_STATUS	Read Word	2	BCS1.2 Charger Detect Status on the VBUS side
32h	(reserved)	-	-	-
33h	VBUS_UCD_FCTRL_SET	Read/Write Word	2	BCS1.2 Charger Detector on the VBUS side Manual Control Setting
34h	VBUS_UCD_FCTRL_EN	Read/Write Word	2	BCS1.2 Charger Detector on the VBUS side Manual Control Enable

8.3.2. Extended Commands - continued

Code	Command	Protocols	Byte Size	Description
35h	(reserved)	-	-	-
36h	(reserved)	-	-	-
37h	(reserved)	-	-	-
38h	CHIP_ID	Read Word	2	Chip ID
39h	CHIP_REV	Read Word	2	Chip Revision
3Ah	IC_SET1	Read/Write Word	2	1-Cell Mode Setting, ACP Discharge Control and ACOK Control Setting.
3Bh	IC_SET2	Read/Write Word	2	IC Setting Register (for debug and production test)
3Ch	SYSTEM_STATUS	Read Word	2	System Power-on Status
3Dh	SYSTEM_CTRL_SET	Read/Write Word	2	Software Reset and Reload OTP
3Eh	PROTECT_SET	Read/Write Word	2	Access Un-protect Setting for Address 3Fh
3Fh	MAP_SET	Read/Write Word	2	Change Command Code Map
40h	VM_CTRL_SET	Read/Write Word	2	SAR-ADC Measurement Control Setting
41h	THERM_WINDOW_SET1	Read/Write Word	2	JEITA Battery Temperature Window Setting 1
42h	THERM_WINDOW_SET2	Read/Write Word	2	JEITA Battery Temperature Window Setting 2
43h	THERM_WINDOW_SET3	Read/Write Word	2	JEITA Battery Temperature Window Setting 3
44h	THERM_WINDOW_SET4	Read/Write Word	2	JEITA Battery Temperature Window Setting 4
45h	THERM_WINDOW_SET5	Read/Write Word	2	JEITA Battery Temperature Window Setting 5
46h	IBATP_TH_SET	Read/Write Word	2	Battery Current (Charge) Interrupt Threshold Setting
47h	IBATM_TH_SET	Read/Write Word	2	Battery Current (Dis-charge) Interrupt Threshold Setting
48h	VBAT_TH_SET	Read/Write Word	2	Battery Voltage Interrupt Threshold Setting
49h	THERM_TH_SET	Read/Write Word	2	Battery Temperature Interrupt Threshold Setting
4Ah	IACP_TH_SET	Read/Write Word	2	Input Current (between ACP and ACN) Interrupt Threshold Setting
4Bh	VACP_TH_SET	Read/Write Word	2	Input Voltage (ACP) Interrupt Threshold Setting
4Ch	VBUS_TH_SET	Read/Write Word	2	VBUS Voltage Interrupt Threshold Setting
4Dh	VCC_TH_SET	Read/Write Word	2	VCC Voltage Interrupt Threshold Setting
4Eh	VSYS_TH_SET	Read/Write Word	2	VSYS Voltage Interrupt Threshold Setting
4Fh	EXTIADP_TH_SET	Read/Write Word	2	IADP (Input current limit setting pin) Voltage Interrupt Threshold Setting
50h	IBATP_VAL	Read Word	2	Battery Current (Charge) Measurement Value
51h	IBATP_AVE_VAL	Read Word	2	Battery Current (Charge) Measurement Average Value
52h	IBATM_VAL	Read Word	2	Battery Current (Dis-charge) Measurement Value
53h	IBATM_AVE_VAL	Read Word	2	Battery Current (Dis-charge) Measurement Average Value
54h	VBAT_VAL	Read Word	2	Battery Voltage Measurement Value
55h	VBAT_AVE_VAL	Read Word	2	Battery Voltage Measurement Average Value
56h	THERM_VAL	Read/Write Word	2	Thermistor Temperature Measurement Value
57h	VTH_VAL	Read Word	2	Thermistor Measurement Voltage Value
58h	IACP_VAL	Read Word	2	Input Current (between ACP and ACN) Measurement Value
59h	IACP_AVE_VAL	Read Word	2	Input Current (between ACP and ACN) Measurement Average Value
5Ah	VACP_VAL	Read Word	2	Input Voltage (ACP) Measurement Value
5Bh	VACP_AVE_VAL	Read Word	2	Input Voltage (ACP) Measurement Average Value
5Ch	VBUS_VAL	Read Word	2	VBUS Voltage Measurement Value
5Dh	VBUS_AVE_VAL	Read Word	2	VBUS Voltage Measurement Average Value
5Eh	VCC_VAL	Read Word	2	VCC Voltage Measurement Value
5Fh	VCC_AVE_VAL	Read Word	2	VCC Voltage Measurement Average Value
60h	VSYS_VAL	Read Word	2	VSYS Voltage Measurement Value
61h	VSYS_AVE_VAL	Read Word	2	VSYS Voltage Measurement Average Value
62h	EXTIADP_VAL	Read Word	2	IADP (Input current limit setting pin) Voltage Measurement Value
63h	EXTIADP_AVE_VAL	Read Word	2	IADP (Input current limit setting pin) Voltage Measurement Average Value
64h	VACPCLPS_TH_SET	Read/Write Word	2	VACP Collapse Detect Threshold Voltage Setting
65h	(reserved)	-	-	-
66h	(reserved)	-	-	-
67h	(reserved)	-	-	-
68h	INT0_SET	Read/Write Word	2	1st Level Interrupt Setting
69h	INT1_SET	Read/Write Word	2	2nd Level Interrupt Setting 1 (VBUS)
6Ah	INT2_SET	Read/Write Word	2	2nd Level Interrupt Setting 2 (VCC)
6Bh	INT3_SET	Read/Write Word	2	2nd Level Interrupt Setting 3 (Battery)
6Ch	INT4_SET	Read/Write Word	2	2nd Level Interrupt Setting 4 (VSYS)

8.3.2. Extended Commands - continued

Code	Command	Protocols	Byte Size	Description
6Dh	INT5_SET	Read/Write Word	2	2nd Level Interrupt Setting 5 (Charger)
6Eh	INT6_SET	Read/Write Word	2	2nd Level Interrupt Setting 6 (Charger)
6Fh	INT7_SET	Read/Write Word	2	2nd Level Interrupt Setting 7 (SAR-ADC)
70h	INT0_STATUS	Read/Write Word	2	1st Level Interrupt Status
71h	INT1_STATUS	Read/Write Word	2	2nd Level Interrupt Status 1 (VBUS)
72h	INT2_STATUS	Read/Write Word	2	2nd Level Interrupt Status 2 (VCC)
73h	INT3_STATUS	Read/Write Word	2	2nd Level Interrupt Status 3 (Battery)
74h	INT4_STATUS	Read/Write Word	2	2nd Level Interrupt Status 4 (VSYS)
75h	INT5_STATUS	Read/Write Word	2	2nd Level Interrupt Status 5 (Charger)
76h	INT6_STATUS	Read/Write Word	2	2nd Level Interrupt Status 6 (Charger)
77h	INT7_STATUS	Read/Write Word	2	2nd Level Interrupt Status 7 (SAR-ADC)
78h	REG0	Read/Write Word	2	Reserved Register 0 (for future use)
79h	REG1	Read/Write Word	2	Reserved Register 1 (for future use)
7Ah	OTPREG0	Read/Write Word	2	Input current limit degradation setting.
7Bh	OTPREG1	Read/Write Word	2	Reserved OTP-loaded Register 1 (for future use)
7Ch	SMBREG	Read/Write Word	2	Power Save Mode Setting.
7Dh	(reserved)	-	-	-
7Eh	(reserved)	-	-	-
7Fh	DEBUG_MODE_SET	Read/Write Word	2	Debug Mode Setting

8.3.3. Debug Commands

Following is a table of "Debug Commands" which BD99958GW supports. "Debug Commands" is used for debug purpose or in production test.

Reserved command should not be accessed. If accessed, operation is not guaranteed.

8.4. Resister Default Value

Register Address	Address Name	Read/Write	OTP	Bit																OTP/POR Value(HEX)	OTP/POR Value(DEC)	Unit
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
00h	CHGSTM_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
01h	VBAT/VSYS_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
02h	VBUS/VCC_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
03h	CHGOP_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
04h	WDT_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
05h	CUR_ILIM_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
06h	SEL_ILIM_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
07h	IBUS_LIM_SET	R/W	Yes	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	05C0	1472	mA
08h	ICC_LIM_SET	R/W	Yes	0	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	05C0	1472	mA
09h	IOTG_LIM_SET	R/W	Yes	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	05E0	1504	mA
0Ah	VIN_CTRL_SET	R/W	Yes	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	00E0	-	HEX
0Bh	CHGOP_SET1	R/W	Yes	0	1	1	0	1	1	0	0	0	1	1	0	1	0	0	0	6C68	-	HEX
0Ch	CHGOP_SET2	R/W	Yes	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	002E	-	HEX
0Dh	VBUSCLPS_TH_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	V
0Eh	VCCCLPS_TH_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	V
0Fh	CHGWDI_SET	R/W	Yes	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	3010	192,16	min
10h	BATTWDT_SET	R/W	Yes	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0630	24,48	min
11h	VSYSREG_SET	R/W	Yes	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	2300	8.96	V
12h	VSYSVAL_THH_SET	R/W	Yes	0	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	1580	5.504	V
13h	VSYSVAL_THL_SET	R/W	Yes	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	1340	4.928	V
14h	ITRICH_SET	R/W	Yes	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0100	256	mA
15h	IPRECH_SET	R/W	Yes	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0100	256	mA
16h	ICHG_SET	R/W	Yes	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0A00	2560	mA
17h	ITERM_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	mA
18h	VPRECHG_TH_SET	R/W	Yes	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0800	2.048	V
19h	VRBOOST_SET	R/W	Yes	0	0	0	1	0	0	1	1	1	1	0	0	0	0	0	0	13C0	5.056	V
1Ah	VFASTCHG_REG_SET1	R/W	Yes	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	20D0	8.4	V
1Bh	VFASTCHG_REG_SET2	R/W	Yes	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	20D0	8.4	V
1Ch	VFASTCHG_REG_SET3	R/W	Yes	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	20D0	8.4	V
1Dh	VRECHG_SET	R/W	Yes	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	0	1FB0	8.112	V
1Eh	VBATOVP_SET	R/W	Yes	0	0	1	0	0	0	1	0	1	1	0	1	0	0	0	0	22D0	8.912	V
1Fh	IBATSHORT_SET	R/W	Yes	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000	16384	mA
20h	PROCHOT_CTRL_SET	R/W	Yes	0	1	0	0	0	1	0	1	0	0	0	1	1	0	0	1	4519	-	HEX
21h	PROCHOT_ICRIT_SET	R/W	Yes	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	2710	10000	mA
22h	PROCHOT_INORM_SET	R/W	Yes	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	1388	5000	mA
23h	PROCHOT_IDCHG_SET	R/W	Yes	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000	16384	mA
24h	PROCHOT_VSYS_SET	R/W	Yes	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	1340	4.928	V
25h	PMON_IOUT_CTRL_SET	R/W	Yes	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	0	00AC	-	HEX
26h	PMON_DACIN_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
27h	IOUT_DACIN_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
28h	VCC_UCD_SET	R/W	Yes	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0080	-	HEX
29h	VCC_UCD_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
2Bh	VCC_UCD_FCTRL_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
2Ch	VCC_UCD_FCTRL_EN	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
30h	VBUS_UCD_SET	R/W	Yes	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0080	-	HEX
31h	VBUS_UCD_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
33h	VBUS_UCD_FCTRL_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX

8.4. Resister Default Value - continued

Register Address	Address Name	Read/Write	OTP	Bit																OTP/POR Value(HEX)	OTP/POR Value(DEC)	Unit
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
34h	VBUS_UCD_FCTRL_EN	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
38h	CHIP_ID	R	Yes	0	0	0	0	0	0	1	1	0	1	0	0	0	1	1	0	0346	-	HEX
39h	CHIP_REV	R	Yes	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0009	-	HEX
3Ah	IC_SET1	R/W	Yes	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0200	-	HEX
3Bh	IC_SET2																					
3Ch	SYSTEM_STATUS	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
3Dh	SYSTEM_CTRL_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
3Eh	PROTECT_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
3Fh	MAP_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
40h	VM_CTRL_SET	R/W	Yes	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	13FF	-	HEX
41h	THERM_WINDOW_SET1	R/W	Yes	1	1	0	0	0	0	1	1	1	1	0	0	0	1	1	0	C3C6	5,2	°C
42h	THERM_WINDOW_SET2	R/W	Yes	1	0	1	1	1	0	1	1	1	0	1	1	1	1	1	0	BBBE	13,10	°C
43h	THERM_WINDOW_SET3	R/W	Yes	1	0	0	1	1	0	1	1	1	0	0	1	1	1	1	0	9B9E	45,42	°C
44h	THERM_WINDOW_SET4	R/W	Yes	1	0	0	0	1	1	1	0	1	0	0	1	0	0	0	1	8E91	58,55	°C
45h	THERM_WINDOW_SET5	R/W	Yes	1	0	0	1	0	1	1	0	1	0	0	1	1	0	0	1	9699	50,47	°C
46h	IBATP_TH_SET	R/W	Yes	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	0	1656	5718	mA
47h	IBATM_TH_SET	R/W	Yes	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000	16384	mA
48h	VBAT_TH_SET	R/W	Yes	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1800	6.144	V
49h	THERM_TH_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0032	150	°C
4Ah	IACP_TH_SET	R/W	Yes	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	1388	5000	mA
4Bh	VACP_TH_SET	R/W	Yes	0	0	0	0	1	1	1	0	1	1	0	1	1	0	0	0	0ED8	3.8	V
4Ch	VBUS_TH_SET	R/W	Yes	0	0	0	0	1	1	1	0	1	1	0	1	1	0	0	0	0ED8	3.8	V
4Dh	VCC_TH_SET	R/W	Yes	0	0	0	0	1	1	1	0	1	1	0	1	1	0	0	0	0ED8	3.8	V
4Eh	VSYS_TH_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	V
4Fh	EXTIADP_TH_SET	R/W	Yes	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	1	0777	1.911	V
50h	IBATP_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
51h	IBATP_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
52h	IBATM_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
53h	IBATM_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
54h	VBAT_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
55h	VBAT_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
56h	THERM_VAL	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
57h	VTH_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
58h	IACP_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
59h	IACP_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Ah	VACP_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Bh	VACP_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Ch	VBUS_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Dh	VBUS_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Eh	VCC_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
5Fh	VCC_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
60h	VSYS_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
61h	VSYS_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
62h	EXTIADP_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
63h	EXTIADP_AVE_VAL	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
64h	VACPCLPS_TH_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	V
68h	INT0_SET	R/W	Yes	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	00FF	-	HEX

8.4. Resister Default Value - continued

Register Address	Address Name	Read/Write	OTP	Bit																OTP/POR Value(HEX)	OTP/POR Value(DEC)	Unit
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
69h	INT1_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Ah	INT2_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Bh	INT3_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Ch	INT4_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Dh	INT5_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Eh	INT6_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
6Fh	INT7_SET	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
70h	INT0_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
71h	INT1_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
72h	INT2_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
73h	INT3_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
74h	INT4_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
75h	INT5_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
76h	INT6_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
77h	INT7_STATUS	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
78h	REG0	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
79h	REG1	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
7Ah	OTPREG0	R/W	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	0	mA
7Bh	OTPREG1	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
7Ch	SMBREG	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
7Dh	(reserved)	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
7Eh	(reserved)	R	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX
7Fh	DEBUG_MODE_SET	R/W	No	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000	-	HEX

8.5. Battery Charger Commands Description

Following is a description of "Battery Charger Commands" that are supported by BD99958GW.

8.5.1. ChargingCurrent

The Battery, System Host or other master device sends the desired charging rate (mA).

Command Code: 14h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	ICHG_SET[13]	Charging current setting. 0 mA to 16,320 mA, 64 mA steps.
12	ICHG_SET[12]	
11	ICHG_SET[11]	
10	ICHG_SET[10]	
9	ICHG_SET[9]	
8	ICHG_SET[8]	
7	ICHG_SET[7]	
6	ICHG_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.2. ChargingVoltage

The Battery, System Host or other master device sends the desired charging voltage to the Smart Battery Charger (mV).

Command Code: 15h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VFASTCHG_REG_SET1[14]	Charging Regulation Voltage. 3,072 mV to 19,200 mV, 16 mV steps. The register range: 0 mV to 32,752 mV. But the actual range: 3,072 mV to 19,200 mV.
13	VFASTCHG_REG_SET1[13]	
12	VFASTCHG_REG_SET1[12]	
11	VFASTCHG_REG_SET1[11]	
10	VFASTCHG_REG_SET1[10]	
9	VFASTCHG_REG_SET1[9]	
8	VFASTCHG_REG_SET1[8]	
7	VFASTCHG_REG_SET1[7]	
6	VFASTCHG_REG_SET1[6]	
5	VFASTCHG_REG_SET1[5]	
4	VFASTCHG_REG_SET1[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.3. IBUS_LIM_SET

VBUS Input Current Limit Setting

Command Code: 3Ch

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	IBUS_LIM_SET1[13]	VBUS input current limitation. 0 mA to 16,352 mA, 32 mA steps.
12	IBUS_LIM_SET1[12]	
11	IBUS_LIM_SET1[11]	
10	IBUS_LIM_SET1[10]	
9	IBUS_LIM_SET1[9]	
8	IBUS_LIM_SET1[8]	
7	IBUS_LIM_SET1[7]	
6	IBUS_LIM_SET1[6]	
5	IBUS_LIM_SET1[5]	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.4. ICC_LIM_SET

VCC Input Current Limit Setting

Command Code: 3Dh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	ICC_LIM_SET1[13]	VCC input current limitation. 0 mA to 16,352 mA, 32 mA steps.
12	ICC_LIM_SET1[12]	
11	ICC_LIM_SET1[11]	
10	ICC_LIM_SET1[10]	
9	ICC_LIM_SET1[9]	
8	ICC_LIM_SET1[8]	
7	ICC_LIM_SET1[7]	
6	ICC_LIM_SET1[6]	
5	ICC_LIM_SET1[5]	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.5.5. PROTECT_SET

Access Un-protect Setting for the “debug command map” (debug and production test only)

Command Code: 3Eh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROTECT_SET[15]	Access Un-protect Setting for the “debug command map” (debug and production test only)
14	PROTECT_SET[14]	
13	PROTECT_SET[13]	
12	PROTECT_SET[12]	
11	PROTECT_SET[11]	
10	PROTECT_SET[10]	
9	PROTECT_SET[9]	
8	PROTECT_SET[8]	
7	PROTECT_SET[7]	
6	PROTECT_SET[6]	
5	PROTECT_SET[5]	
4	PROTECT_SET[4]	
3	PROTECT_SET[3]	
2	PROTECT_SET[2]	
1	PROTECT_SET[1]	
0	PROTECT_SET[0]	

8.5.6. MAP_SET

Change Command Code Map

Command Code: 3Fh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	MAP_SET [15]	Change Command Code Map
14	MAP_SET [14]	
13	MAP_SET[13]	
12	MAP_SET[12]	
11	MAP_SET[11]	
10	MAP_SET[10]	
9	MAP_SET[9]	
8	MAP_SET[8]	
7	MAP_SET[7]	
6	MAP_SET[6]	
5	MAP_SET[5]	
4	MAP_SET[4]	
3	MAP_SET[3]	
2	MAP_SET[2]	
1	MAP_SET[1]	
0	MAP_SET[0]	

8.6. Extended Commands Description

Following is a description of "Extended Commands" that are supported by BD99958GW.

8.6.1. CHGSTM_STATUS

Charger State Machine Status

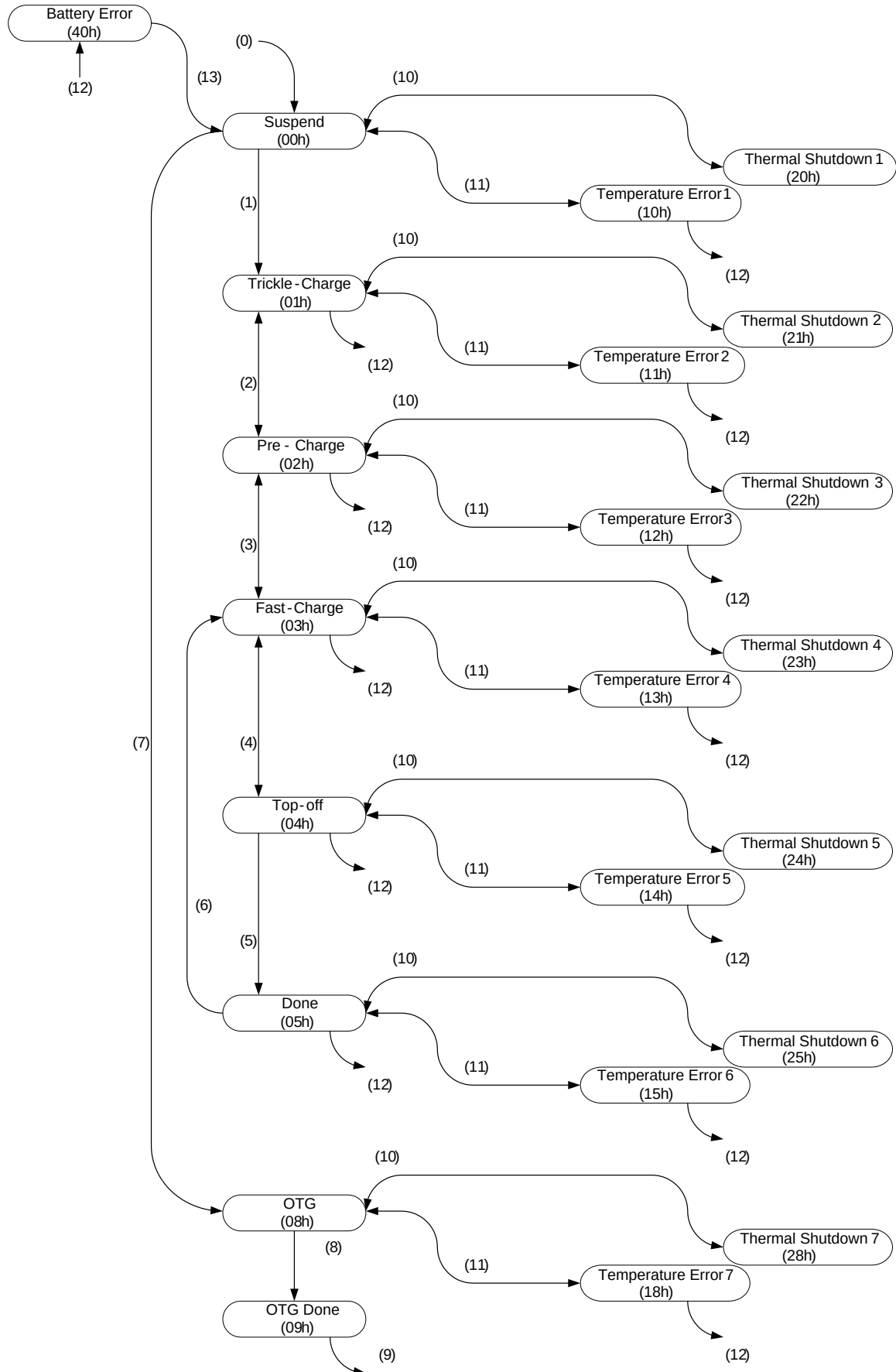
Command Code: 00h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	The previous state of the charger state-machine.
14	PREV_CHGSTM_STATE[6]	
13	PREV_CHGSTM_STATE[5]	
12	PREV_CHGSTM_STATE[4]	
11	PREV_CHGSTM_STATE[3]	
10	PREV_CHGSTM_STATE[2]	
9	PREV_CHGSTM_STATE[1]	
8	PREV_CHGSTM_STATE[0]	
7	reserved	The current state of the charger state-machine.
6	CHGSTM_STATE[6]	
5	CHGSTM_STATE[5]	
4	CHGSTM_STATE[4]	
3	CHGSTM_STATE[3]	
2	CHGSTM_STATE[2]	
1	CHGSTM_STATE[1]	
0	CHGSTM_STATE[0]	

State definition. CHGSTM_STATE PREV_CHGSTM_STATE	State Name	Description
00h	Suspend	Suspend charging
01h	Trickle-Charge	Trickle-charging
02h	Pre-Charge	Pre-charging
03h	Fast-Charge	Fast Charging
04h	Top-off	Reached to Termination Current
05h	Done	Charging finished
08h	OTG	USB On The Go (Reverse Buck Boost Operation)
09h	OTG Done	OTG Done
10h	Temperature Error 1	Out of standard temperature while Suspend State
11h	Temperature Error 2	Out of standard temperature while Trickle-Charge State
12h	Temperature Error 3	Out of standard temperature while Pre-Charge State
13h	Temperature Error 4	Out of standard temperature while Fast-Charge State
14h	Temperature Error 5	Out of standard temperature while Top-off State
15h	Temperature Error 6	Out of standard temperature while after Top-off State (DONE)
18h	Temperature Error 7	Out of standard temperature while OTG State
20h	Thermal Shutdown 1	Thermal Shutdown while Suspend State
21h	Thermal Shutdown 2	Thermal Shutdown while Trickle-Charge State
22h	Thermal Shutdown 3	Thermal Shutdown while Pre-Charge State
23h	Thermal Shutdown 4	Thermal Shutdown while Fast-Charge State
24h	Thermal Shutdown 5	Thermal Shutdown while Top-off State
25h	Thermal Shutdown 6	Thermal Shutdown after Top-off State (DONE)
28h	Thermal Shutdown 7	Thermal Shutdown while OTG State
40h	Battery Error	Battery Error

8.6.1. CHGSTM_STATUS – continued



8.6.1. CHGSTM_STATUS - continued

Arc #	Condition to next state	back to previous state
(0)	CHG_EN is 0, disabled or USB_SUS is 1, suspended. or VBUS and VCC and VACP are undetected or disabled. or Thermistor is open. or Power Path is changed. or Anti-collapse is occurred. or VSYS SCP timer is expired (20 ms).	-
(1)	VBUS or VCC or VACP detected. and SDP_CHG_TRIG bit set if SDP_CHG_TRIG_EN=1 and SDP port detected. and Charge enable. and DCDC Soft started. and State Transition Timer expired (25 ms). and No anti-collapse occurred. and No VSYS short occurred.	-
(2)	VBATT > VPRECHG_TH_SET and State Transition Timer expired (25 ms).	and VBATT ≤ VPRECHG_TH_SET State Transition Timer expired (25 ms).
(3)	VBATT > VSYSREG_SET and AUTO_FST=1 and State Transition Timer expired (25 ms).	and VBATT ≤ VSYSREG_SET State Transition Timer expired (25 ms).
(4)	ITERM comparator asserted. and AUTO_TOF=1 and VBATT > Re-charge Battery Voltage and State Transition Timer expired (25 ms).	and ITERM comparator deasserted or VBATT ≤ Re-charge Battery Voltage State Transition Timer expired (25 ms).
(5)	Charging Termination Timer expired (15 s).	-
(6)	-	and VBATT ≤ Re-charge Battery Voltage State Transition Timer expired (25 ms).
(7)	OTG Device is detected or VRBOOST_EN is enabled. and VRBOOST_TRIG=1 and VBUS and VCC and VACP is undetected. and Power Path with OTG Device is enabled, VBUS_EN=1, VCC_EN=1 and State Transition Timer expired (25 ms).	-
(8)	OTG Device is undetected or VRBOOST_EN is disabled or VRBOOST_TRIG=0. and State Transition Timer expired (25 ms).	-
(9)	State Transition Timer expired (25 ms). and Reverse Buck Boost Voltage is under UVLO level.	-
(10)	TSD comparator asserted.	and TSD comparator de-asserted. State Transition Timer expired (25 ms).
(11)	Thermal range is HOT3 or COLD2. and State Transition Timer expired (25 ms).	and Thermal range isn't HOT3 and COLD2. State Transition Timer expired (25 ms).
(12)	Charger WDT is expired or Thermal WDT is expired or VBATT ≥ Battery Over voltage	-
(13)	<Charging> VBATT < Battery Over voltage and Charge is disabled or suspended. Or VBUS and VCC and VACP are undetected or disabled. Or Thermistor is open. Or Power Path is changed. <OTG> OTG Device is undetected or RBOOST_EN is disabled. or USB_SUS=1, suspended.	-

8.6.2. VBATT/VSYS_STATUS

VBATT and VSYS Status

Command Code: 01h

Bus Protocol: Read Word

Bit	Symbol	Description
15	VSYS_OV	VSYS over voltage status. "1": $VSYS \geq VSYS_OVP$ / "0": $VSYS < VSYS_OVP$
14	VSYS_SSD	DCDC Soft Start completion status. "1": Soft Start finished / "0": Not finished.
13	VSYS_SCP	VSYS short-circuit detection status. "1": VSYS SCP timer expired. / "0": Normal operation.
12	VSYS_UVN	VSYS UVLO detection status. "1": Low voltage. / "0": Normal voltage.
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	reserved	
6	IBAT_SHORT	Battery short-circuits detection status. "1": Battery Short Current Detected / "0": Normal operation
5	reserved	
4	reserved	
3	VBAT_OV	VBATT over voltage Status. "1": $VBATT \geq VBAT_OVP$ / "0": $VBATT < VBAT_OVP$ with Hysteresis
2	reserved	
1	reserved	
0	DEAD_BAT	Dead Battery status. "1": Dead Battery, $VBATT < VSYSREG_SET$, Detected / "0": Normal operation, $VBATT \geq VSYSREG_SET$.

8.6.3. VBUS/VCC_STATUS

VBUS and VCC Status

Command Code: 02h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	VACP_DET	VACP detection status. "1": VACP detected (over UVLO level) / "0": Not detected or low level.
11	VCC_OVP	VCC/VACP over voltage status. "1": VCC > VCC_OVP / "0": Normal voltage. (When VCC_EN = 1) "1": VACP > VCC_OVP / "0": Normal voltage. (When VCC_EN = VBUS_EN = 0)
10	ILIM_VCC_MOD	VCC/VACP input current limit control status. "1": VCC input current limit controlled. / "0": No. (When VCC_EN = 1) "1": VACP input current limit controlled. / "0": No. (When VCC_EN = VBUS_EN = 0)
9	VCC_CLPS	VCC/VACP anti-collapse status. "1": VCC Anti-collapse / "0": Normal operation. (When VCC_EN = 1) "1": VACP Anti-collapse / "0": Normal operation. (When VCC_EN = VBUS_EN = 0)
8	VCC_DET	VCC detection status. "1": VCC detected (over UVLO level) / "0": Not detected or low level.
7	reserved	
6	reserved	
5	reserved	
4	reserved	
3	VBUS_OVP	VBUS over voltage status. "1": VBUS > VBUS_OVP / "0": Normal voltage.
2	ILIM_VBUS_MOD	VBUS current limit control status. "1": Limit controlled. / "0": No.
1	VBUS_CLPS	VBUS anti-collapse status. "1": Anti-collapse / "0": Normal operation.
0	VBUS_DET	VBUS detection status. "1": VBUS detected (over UVLO level) / "0": Not detected or low level.

8.6.4. CHGOP_STATUS

Charger Operation Status

Command Code: 03h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	BATTEMP[2]	Battery temperature range and the thermistor status. Please see next table.
9	BATTEMP[1]	
8	BATTEMP[0]	
7	reserved	
6	VRECHG_DET	Re-charge voltage detection status. "1": VBATT < VRECHG_SET / "0": VBATT keeps enough voltage.
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	RBOOST_UV	Reverse Buck Boost UVLO detection status. "1": Normal voltage. / "0": Low voltage.
0	RBOOSTS	Reverse Buck Boost status. "1": Boosting / "0": Not boosting.

BAT_TEMP	Temperature Range	Description
0h	Room Temp	T2 < Thermistor temperature < T3
1h	HOT1	T3 < Thermistor temperature < T5
2h	HOT2	T5 < Thermistor temperature < T4
3h	HOT3	T4 < Thermistor temperature
4h	COLD1	T1 < Thermistor temperature < T2
5h	COLD2	Thermistor temperature < T1
6h	Temp. Disable	Disable thermal control (No Thermistor)
7h	Battery Open	TSENSE_BATT port is open.

Register Name	Description	Default Value	Note
TMPTHR1A[7:0]	Lower threshold of T1	C6h (2 deg.)	T1 in JEITA profile
TMPTHR1B[7:0]	Upper threshold of T1	C3h (5 deg.)	T1 in JEITA profile
TMPTHR2A[7:0]	Lower threshold of T2	BEh (10 deg.)	T2 in JEITA profile
TMPTHR2B[7:0]	Upper threshold of T2	BBh (13 deg.)	T2 in JEITA profile
TMPTHR3A[7:0]	Lower threshold of T3	9Eh (42 deg.)	T3 in JEITA profile
TMPTHR3B[7:0]	Upper threshold of T3	9Bh (45 deg.)	T3 in JEITA profile
TMPTHR4A[7:0]	Lower threshold of T4	91h (55 deg.)	T4 in JEITA profile
TMPTHR4B[7:0]	Upper threshold of T4	8Eh (58 deg.)	T4 in JEITA profile
TMPTHR5A[7:0]	Lower threshold of T5	9Dh (47 deg.)	Between T3 and T4
TMPTHR5B[7:0]	Upper threshold of T5	96h (50 deg.)	Between T3 and T4

8.6.5. WDT_STATUS

Charger WDT and Battery Temperature WDT Status

Command Code: 04h

Bus Protocol: Read Word

Bit	Symbol	Description
15	THERMWDT_VAL[7]	Current Battery Temperature Watchdog Timer Count Value 0 ms to 255 ms, 1 ms steps.
14	THERMWDT_VAL[6]	
13	THERMWDT_VAL[5]	
12	THERMWDT_VAL[4]	
11	THERMWDT_VAL[3]	
10	THERMWDT_VAL[2]	
9	THERMWDT_VAL[1]	
8	THERMWDT_VAL[0]	
7	CHGWDT_VAL[7]	Current Charge Watchdog Timer Count Value For pre-charging, 0 ms to 255 ms, 1 ms steps. For fast-charging, 0 ms to 1020 ms, 4 ms steps.
6	CHGWDT_VAL[6]	
5	CHGWDT_VAL[5]	
4	CHGWDT_VAL[4]	
3	CHGWDT_VAL[3]	
2	CHGWDT_VAL[2]	
1	CHGWDT_VAL[1]	
0	CHGWDT_VAL[0]	

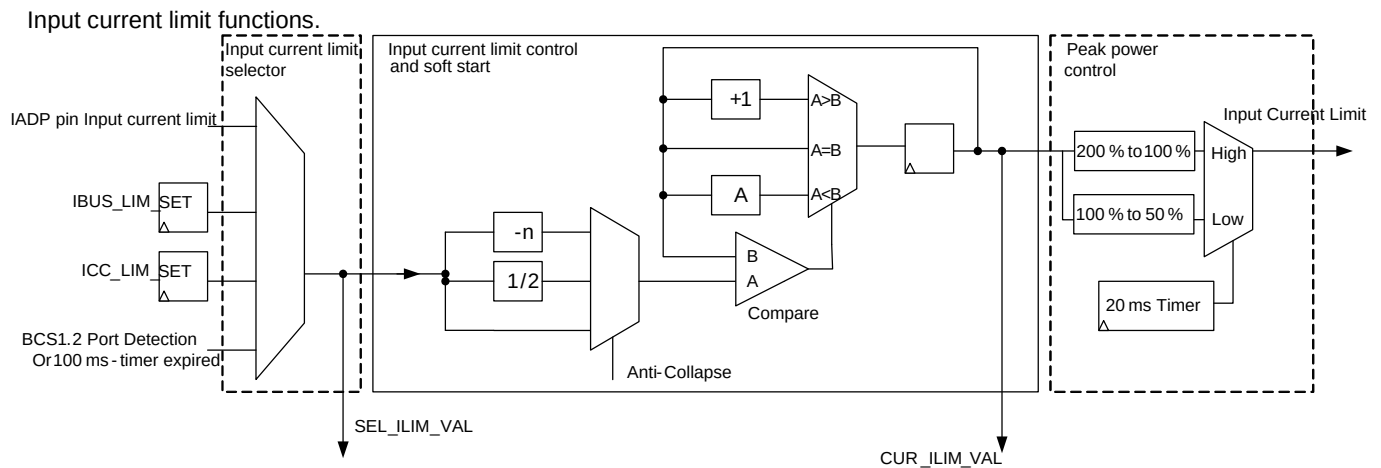
8.6.6. CUR_ILIM_VAL

Actual Input Current Limit

Command Code: 05h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	CUR_ILIM_VAL[13]	Current Input Current Limit Value 0 mA to 16,383 mA, 1 mA steps.
12	CUR_ILIM_VAL[12]	
11	CUR_ILIM_VAL[11]	
10	CUR_ILIM_VAL[10]	
9	CUR_ILIM_VAL[9]	
8	CUR_ILIM_VAL[8]	
7	CUR_ILIM_VAL[7]	
6	CUR_ILIM_VAL[6]	
5	CUR_ILIM_VAL[5]	
4	CUR_ILIM_VAL[4]	
3	CUR_ILIM_VAL[3]	
2	CUR_ILIM_VAL[2]	
1	CUR_ILIM_VAL[1]	
0	CUR_ILIM_VAL[0]	

Input current limit selector:

The “Input current limit selector” block selects an original input current limit from the register setting or detected BCS1.2, DCP/CDP/SDP, result.

Input current limit control and soft start:

The “Input current limit control and soft start” block controls the input current limit slope 1 mA/10 μ s for soft start. And this block modifies the input current limit, -N or 1/2, when the anti-collapse occurs.

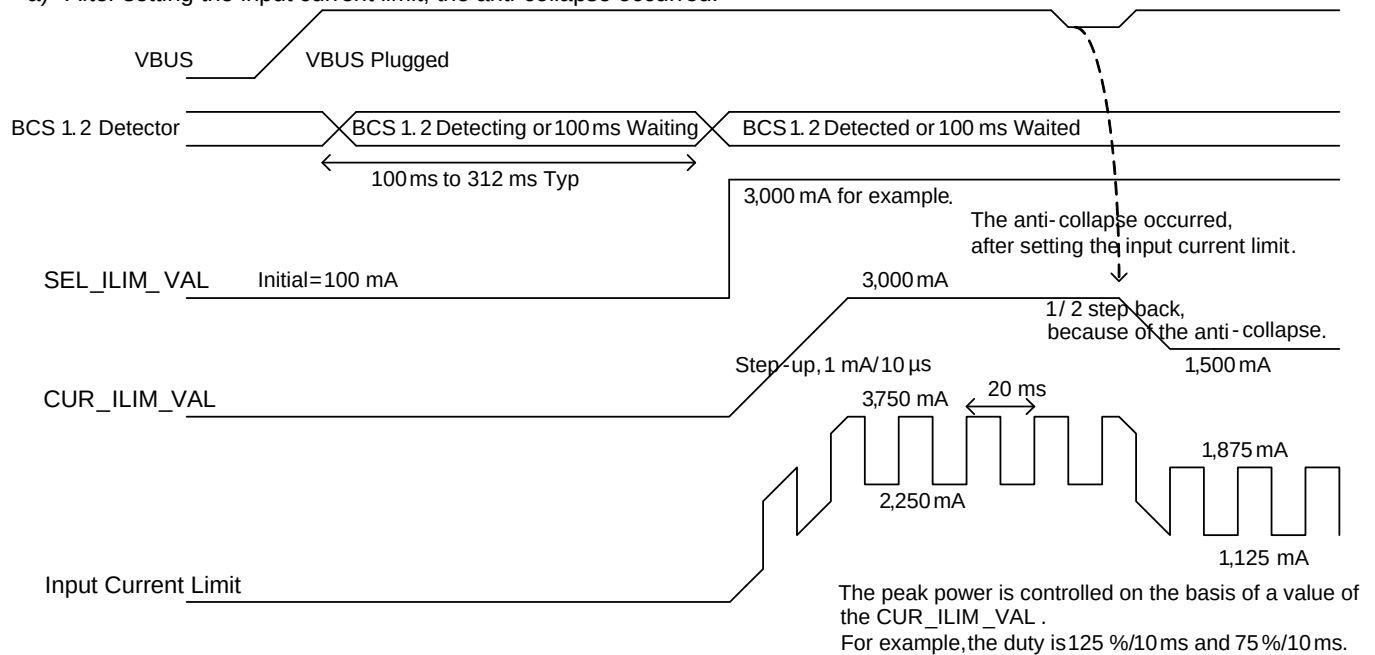
Peak power control:

The “Peak power control” block controls the peak of the input current limit. It is defined by VIN_CTRL_SET.PPC_CAP[1:0] and PPC_SUB_CAP[1:0] registers.

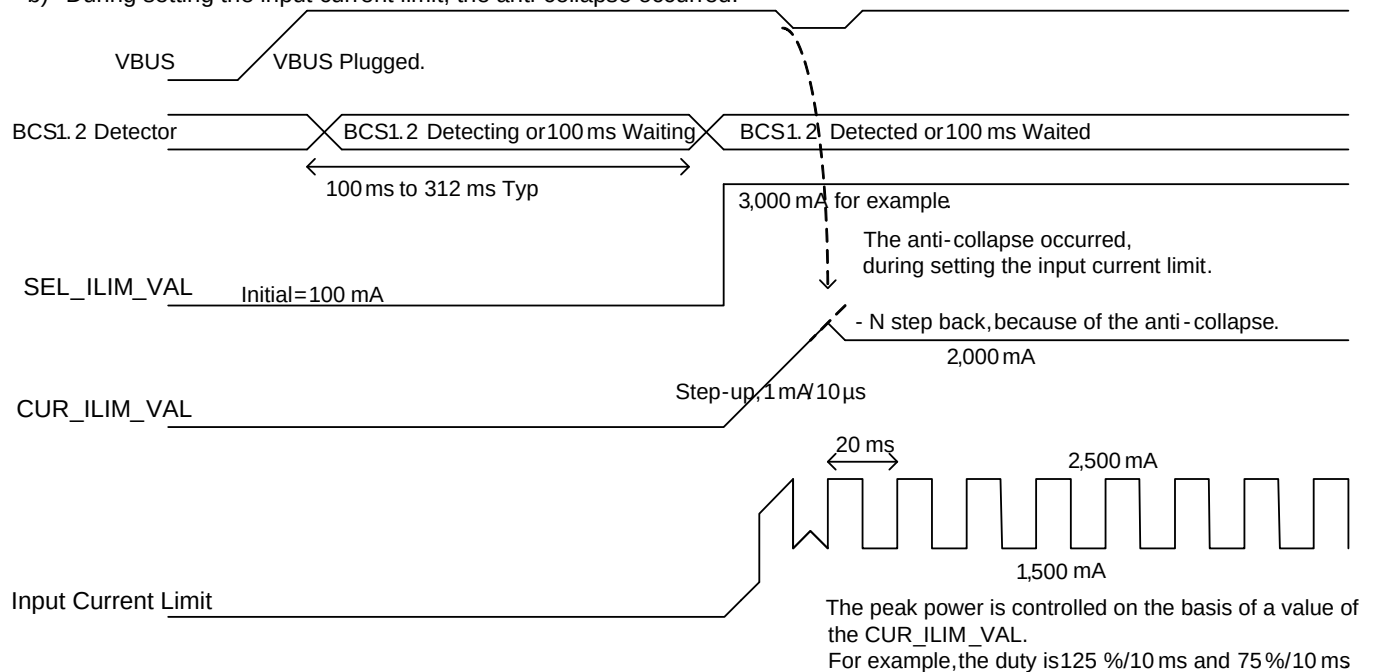
8.6.6. CUR_ILIM_VAL - continued

Sample case timing chart: Input current limit with peak control.

a) After setting the input current limit, the anti-collapse occurred.

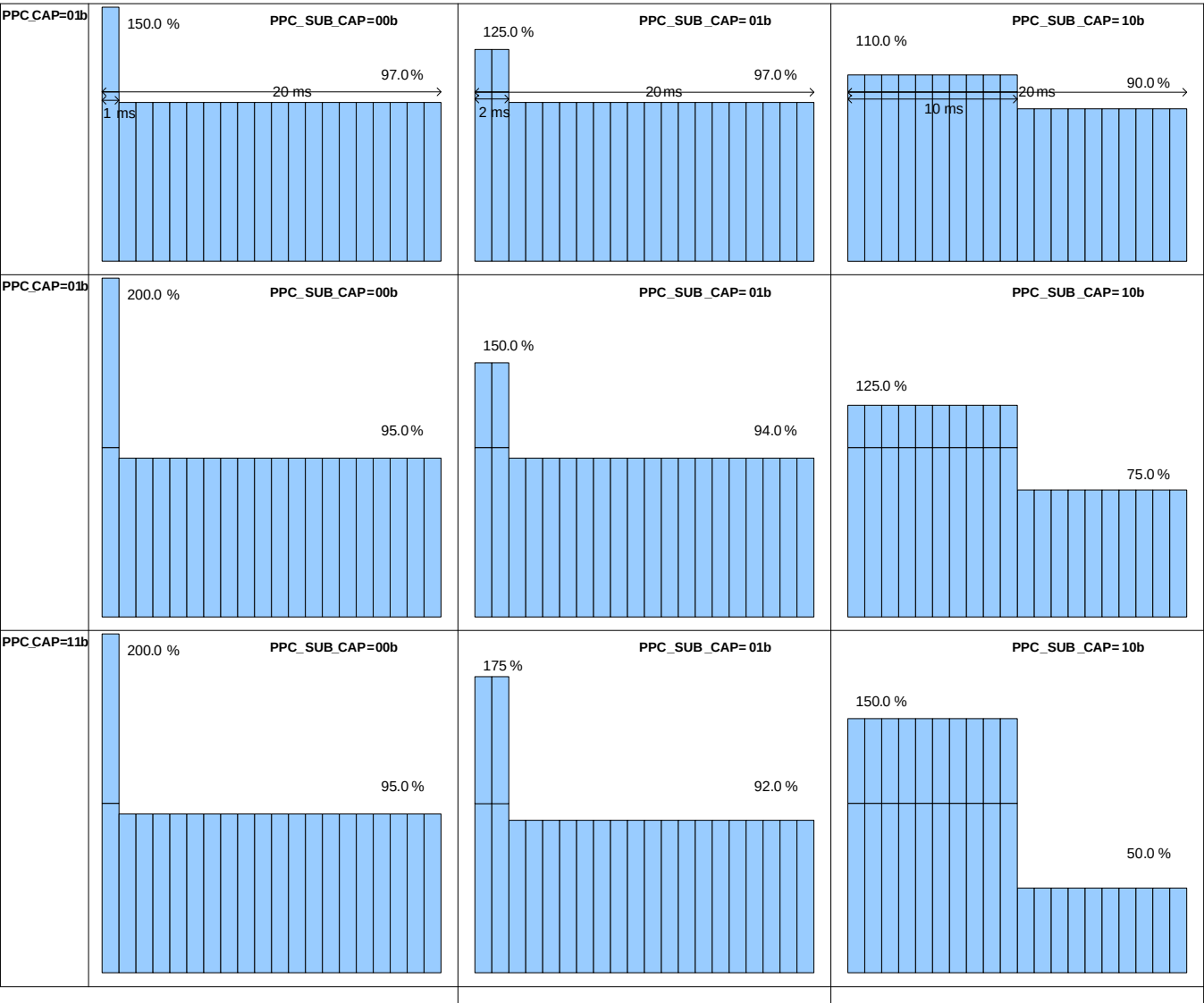


b) During setting the input current limit, the anti-collapse occurred.



8.6.6. CUR_ILIM_VAL - continued

Peak input current control operation is defined by VIN_CTRL_SET.PPC_CAP[1:0] and PPC_SUB_CAP[1:0] as below demonstrates.



8.6.7. SEL_ILIM_VAL

Selected Input Current Limit

Command Code: 06h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	SEL_ILIM_VAL[13]	Selected Input Current Limit Setting 0 mA to 16,383 mA, 1 mA steps.
12	SEL_ILIM_VAL[12]	
11	SEL_ILIM_VAL[11]	
10	SEL_ILIM_VAL[10]	
9	SEL_ILIM_VAL[9]	
8	SEL_ILIM_VAL[8]	
7	SEL_ILIM_VAL[7]	
6	SEL_ILIM_VAL[6]	
5	SEL_ILIM_VAL[5]	
4	SEL_ILIM_VAL[4]	
3	SEL_ILIM_VAL[3]	
2	SEL_ILIM_VAL[2]	
1	SEL_ILIM_VAL[1]	
0	SEL_ILIM_VAL[0]	

8.6.8. IBUS_LIM_SET

VBUS Input Current Limit Setting

Command Code: 07h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	IBUS_LIM_SET[13]	VBUS input current limitation. 0 mA to 16,352 mA, 32 mA steps.
12	IBUS_LIM_SET[12]	
11	IBUS_LIM_SET[11]	
10	IBUS_LIM_SET[10]	
9	IBUS_LIM_SET[9]	
8	IBUS_LIM_SET[8]	
7	IBUS_LIM_SET[7]	
6	IBUS_LIM_SET[6]	
5	IBUS_LIM_SET[5]	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.9. ICC_LIM_SET

VCC/VACP Input Current Limit Setting

Command Code: 08h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	ICC_LIM_SET[13]	VCC input current limitation. (When VCC_EN=1) VACP input current limitation. (When VCC_EN=VBUS_EN=0) 0 mA to 16,352 mA, 32 mA steps.
12	ICC_LIM_SET[12]	
11	ICC_LIM_SET[11]	
10	ICC_LIM_SET[10]	
9	ICC_LIM_SET[9]	
8	ICC_LIM_SET[8]	
7	ICC_LIM_SET[7]	
6	ICC_LIM_SET[6]	
5	ICC_LIM_SET[5]	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.10. IOTG_LIM_SET

OTG Output Current Limit Setting

Command Code: 09h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	IOTG_LIM_SET[13]	VBUS/VCC output current limit when OTG. 0 mA to 16,352 mA, 32 mA steps.
12	IOTG_LIM_SET[12]	
11	IOTG_LIM_SET[11]	
10	IOTG_LIM_SET[10]	
9	IOTG_LIM_SET[9]	
8	IOTG_LIM_SET[8]	
7	IOTG_LIM_SET[7]	
6	IOTG_LIM_SET[6]	
5	IOTG_LIM_SET[5]	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.11. VIN_CTRL_SET

VBUS and VCC Control Setting

Command Code: 0Ah

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	OTG_BOTH_EN	"Enabling OTG reverse buck boost output to VBUS and VCC both. "1": Enable / "0": Disable." When OTG_BOTH_EN=1 and VBUS_EN=VCC_EN=1, OTG reverse buck boost output same voltage at VBUS and VCC, VBUS=VCC=VRBOOST_SEL[14:6].
14	VRBOOST_TRIG	Reverse buck Boost operation Trigger. "1": Trigger/ "0": No trigger
13	VRBOOST_EN[1]	Enabling VCC Reverse buck Boost operation. "1": Enable / "0": Disable.
12	VRBOOST_EN[0]	Enabling VBUS Reverse buck Boost operation. "1": Enable / "0": Disable.
11	PP_BOTH_THRU	"Enabling output to VBUS and VCC both. "1": Enable / "0": Disable." When PP_BOTH_THRU=1 and VBUS_EN=VCC_EN=1, VIN_ORD=0: Power path output same voltage from VCC to VBUS, VIN_ORD=1: Power path output same voltage from VBUS to VCC.
10	reserved	
9	reserved	
8	reserved	
7	VIN_ORD	VBUS / VCC input priority. "1": VBUS prior / "0": VCC prior.
6	VBUS_EN	Enabling VBUS input. "1": Enable / "0": Disable.
5	VCC_EN	Enabling VCC input. "1": Enable / "0": Disable.
4	VSYS_PRIORITY	Disabling the input current limit for avoiding VSYS drop when VBATT is the dead-battery, VBATT is < VSYSREG_SET. "1": Disable the input current limit / "0": Enable the input current limit.
3	PPC_SUB_CAP[1]	Power source peak current sub-capability
2	PPC_SUB_CAP[0]	
1	PPC_CAP[1]	
0	PPC_CAP[0]	Power source peak current capability

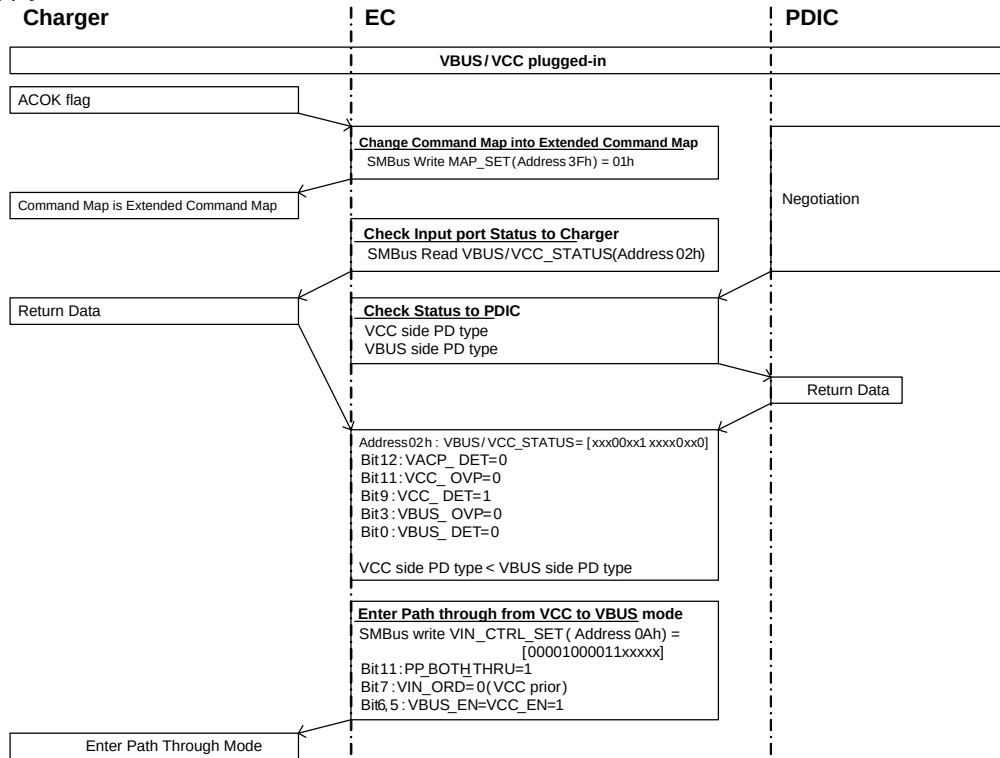
PPC_CAP	PPC_SUB_CAP	Overload Capabilities Description
00b	*b	Peak current equals (IBUS_LIM_SET or ICC_LIM_SET) .
01b	00b	Peak current equals 150.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 1 ms. Low current equals 97.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 19 ms.
	01b	Peak current equals 125.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 2 ms. Low current equals 97.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 18 ms.
	10b	Peak current equals 110.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 10 ms. Low current equals 90.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 10 ms.
10b	00b	Peak current equals 200.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 1 ms. Low current equals 95.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 19 ms.
	01b	Peak current equals 150.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 2 ms. Low current equals 94.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 18 ms.
	10b	Peak current equals 125.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 10 ms. Low current equals 75.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 10 ms.
11b	00b	Peak current equals 200.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 1 ms. Low current equals 95.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 19 ms.
	01b	Peak current equals 175.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 2 ms. Low current equals 92.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 18 ms.
	10b	Peak current equals 150.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 10 ms. Low current equals 50.0 % (IBUS_LIM_SET or ICC_LIM_SET) for 10 ms.

8.6.11. VIN_CTRL_SET - continued

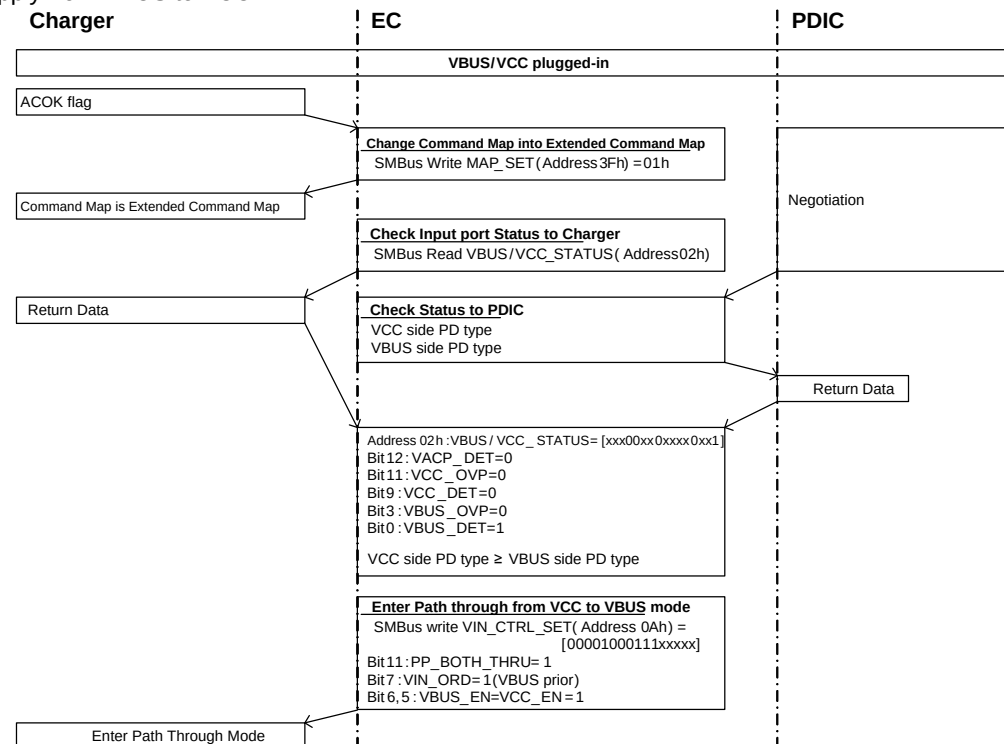
Power Path Control Flow Chart

Path through mode: ON

✧ Power supply from VCC to VBUS

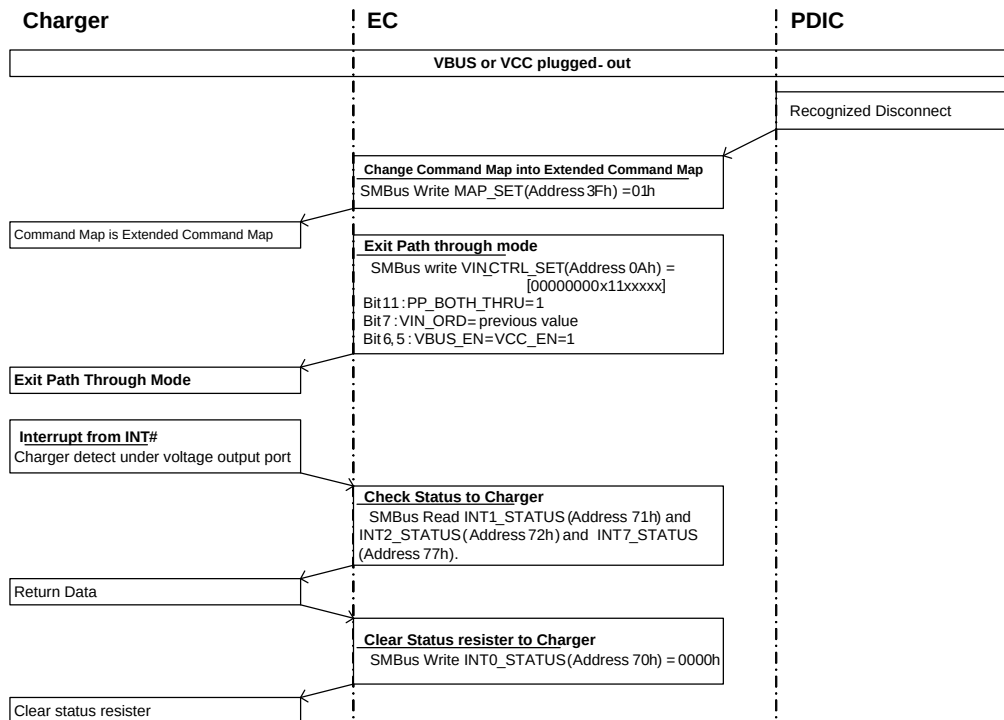


✧ Power supply from VBUS to VCC



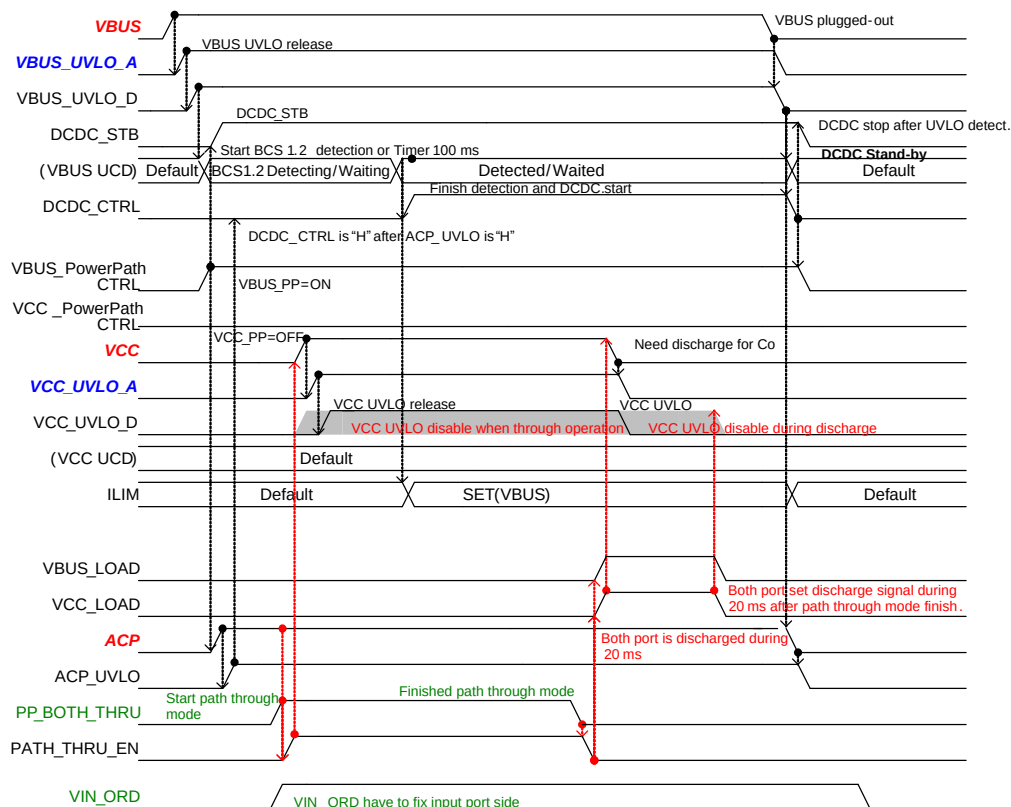
8.6.11. VIN_CTRL_SET - continued

Path through mode: OFF



✧ Timing Chart

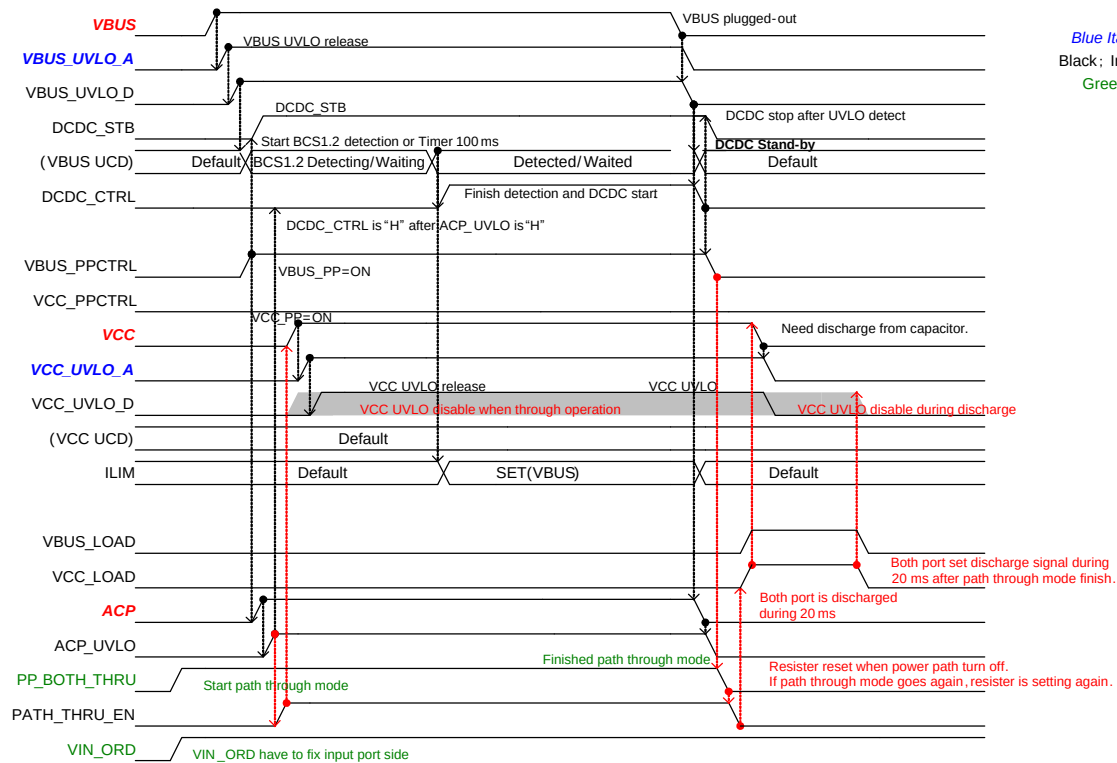
Path Through mode after VBUS input



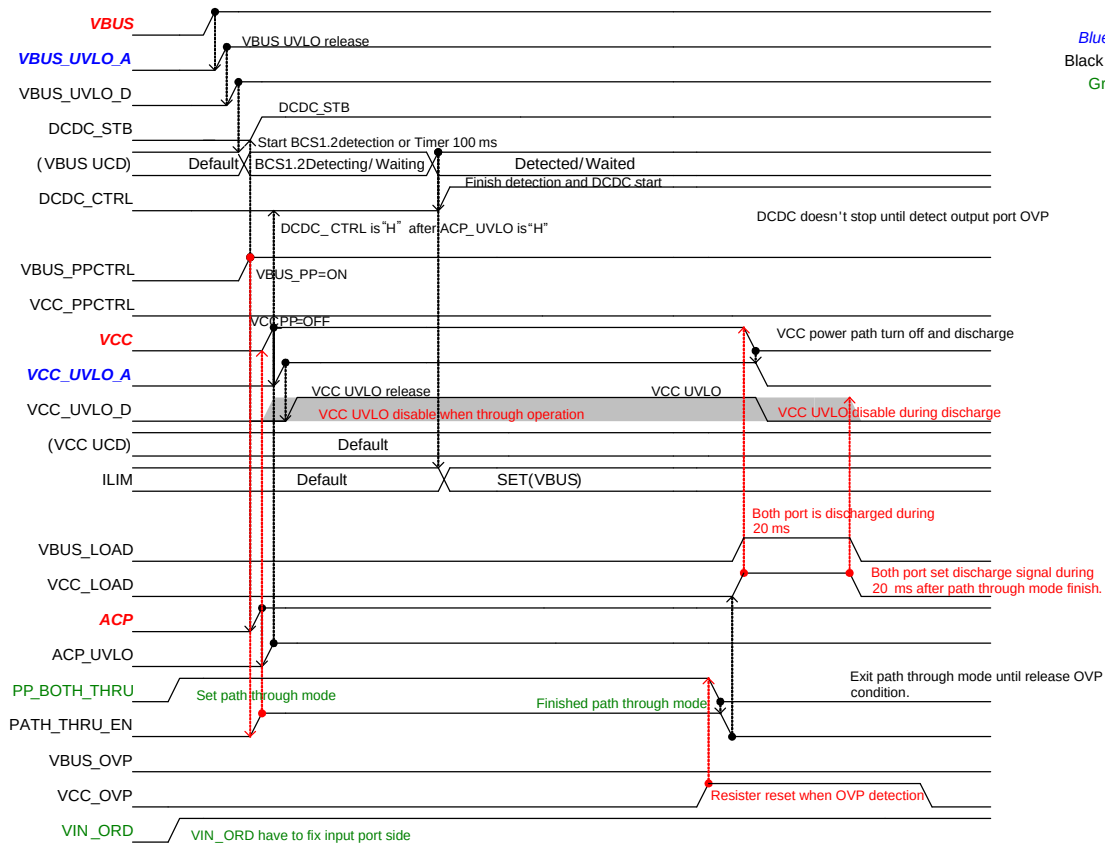
Red Italic: Power
 Blue Italic: Analog Signal
 Black: Internal Digital Signal
 Green: Resistor settings

8.6.11. VIN_CTRL_SET - continued

VBUS path through mode after register setting

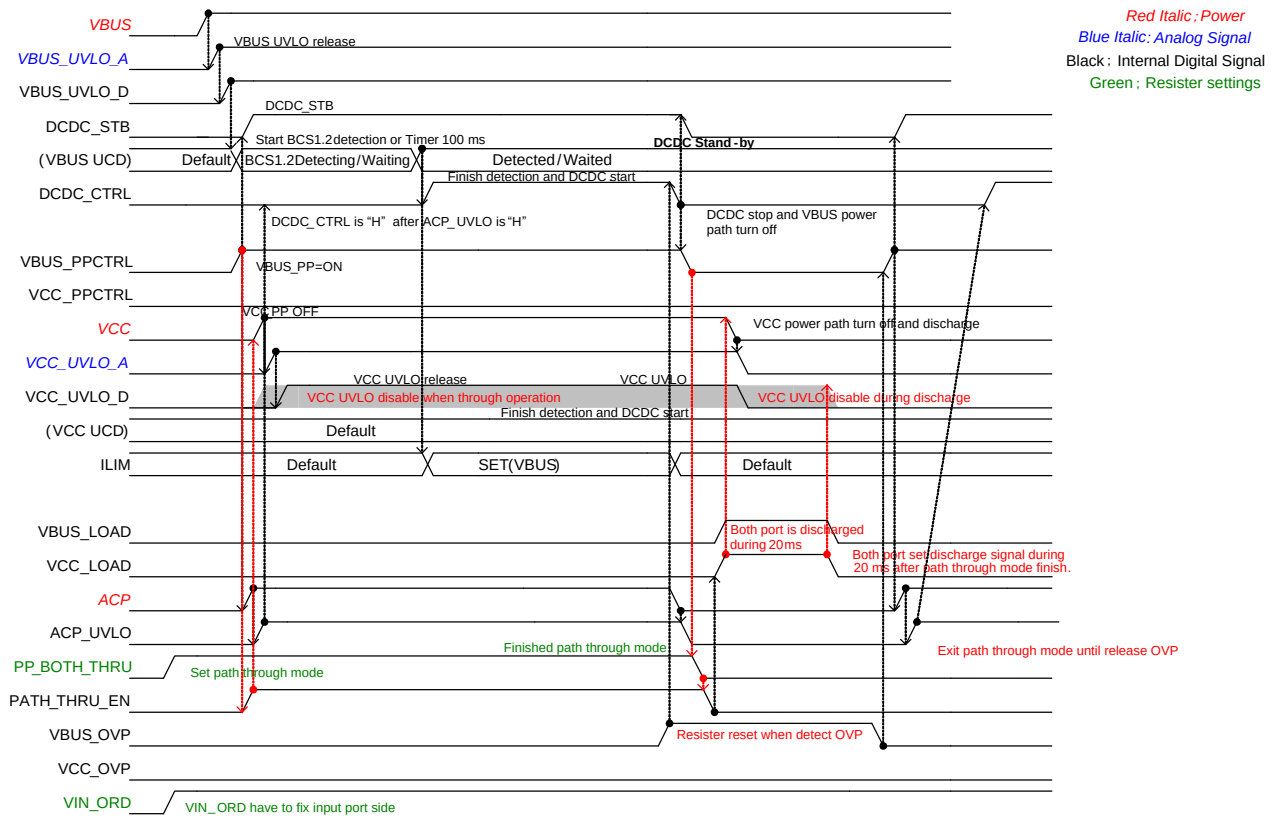


Detect OVP at Output port

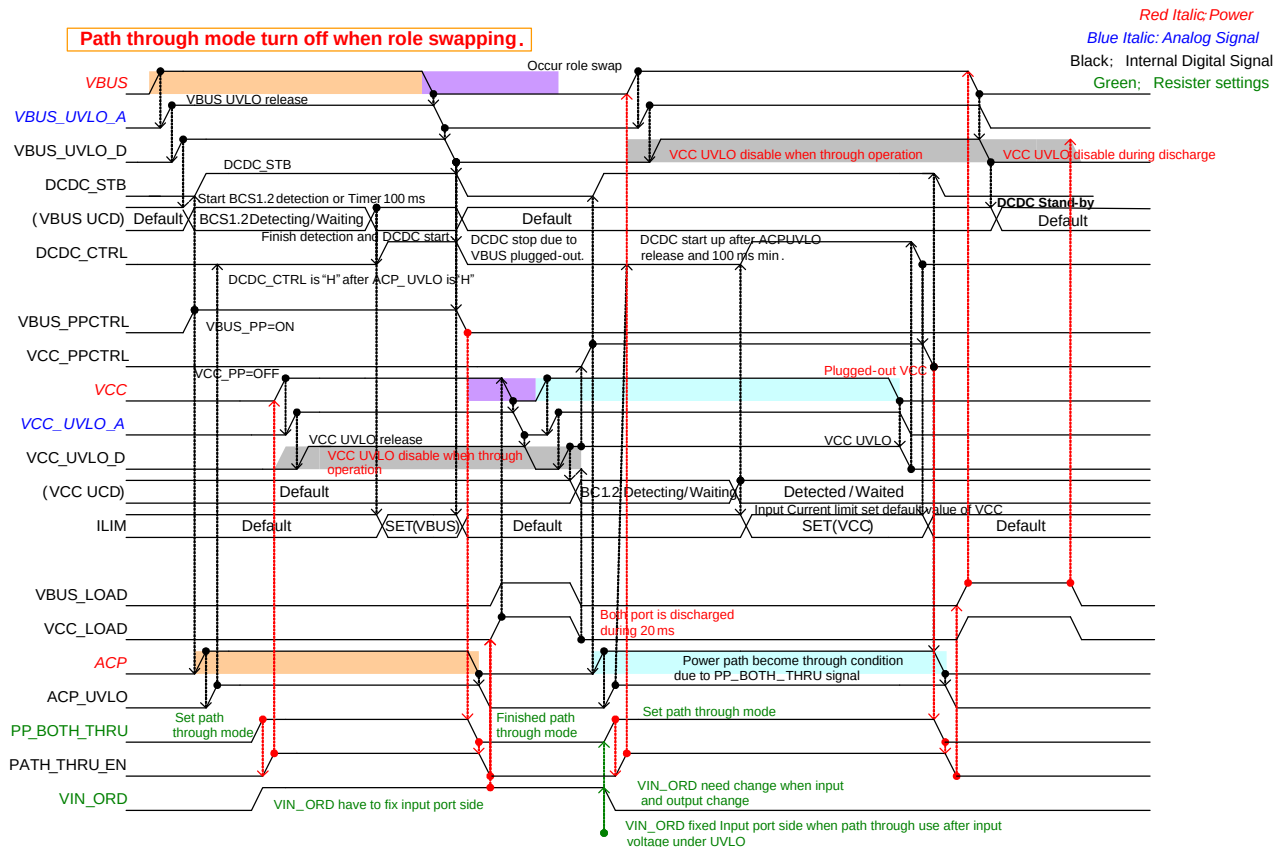


8.6.11. VIN_CTRL_SET - continued

Detect OVP at Input port



Role swap from VBUS to VCC when path through mode



8.6.12. CHGOP_SET1

Charger Operation Control Setting 1

Command Code: 0Bh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	DCP_2500_SEL	Select current limitation when DCP charger attached.
14	SDP_500_SEL	Select current limitation when SDP charger attached.
13	ILIM_AUTO_DISEN	Disable automatic limitation of the input current. "1": Disable / "0": Enable.
12	reserved	
11	VCC_BC_DISEN	Disable charging trigger by BCS1.2 detection. If this bit is "1: disable", after 100 ms when VBUS/VCC plugged in, BD99958GW starts charging without BCS1.2 detection. "1": Disable / "0": Enable.
10	VBUS_BC_DISEN	Disable charging trigger by BCS1.2 detection. If this bit is "1: disable", after 100 ms when VBUS/VCC plugged in, BD99958GW starts charging without BCS1.2 detection. "1": Disable / "0": Enable.
9	SDP_CHG_TRIG_EN	Enable the charging trigger after SDP charger attached. "1": Enable SDP_CHG_TRIG bit as charging trigger / "0": Disable SDP_CHG_TRIG bit as charging trigger.
8	SDP_CHG_TRIG	Charging trigger after SDP charger attached. "1": Start charging / "0": Not start charging.
7	reserved	
6	AUTO_TOF	Top-off transition mode. This bit is trigger to move to the top-off charge state. This bit is only effective when the charging state transitions from fast-charge to top-off charge. "1": Auto control / "0": Manual control.
5	AUTO_FST	Fast charging transition mode. This bit is only effective when the charging state transitions from pre-charge to fast-charge. "1": Auto control / "0": Manual control.
4	reserved	
3	AUTO_RECH	Automatic re-charging mode. "1": Auto control / "0": Manual control.
2	reserved	
1	reserved	
0	reserved	

8.6.13. CHGOP_SET2

Charger Operation Control Setting 2

Command Code: 0Ch

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	ILIM_RESET_EN	Enabling the input current limit re-setting when starting fast charge. "1": Enable. / "0": Disable.
13	DCDC_1MS_SEL[1]	Select ILIM re-setting step period.
12	DCDC_1MS_SEL[0]	00b: 10 μ s/ 01b: 50 μ s/ 10b: 100 μ s/ 11b: 1 ms
11	reserved	
10	SEL_ILIM_DIV	Select ILIM drop width when Anti-collapse. or VBATT<VIN comparator asserted. "1": The input current limit drop into 1/4. / "0": 1/2.
9	reserved	
8	BATT_LEARN	Enabling Battery Learning operation, suspend charging and DC/DC convertor. This bit is cleared automatically when VBATT is the dead battery, VBATT < VSYSREG_SET. "1": Enable / "0": Disable.
7	CHG_EN	Enabling Charger operation. "1": Enable / "0": Disable.
6	USB_SUS	Suspend USB charging and DC/DC convertor. "1": Suspend / "0": Active.
5	CHOP_SS_INIT	Initialization value for CHOP_SS (Chopper Mode during DCDC soft start.) "1": Chopper Mode during DCDC soft start / "0": Synchronized Mode. This register is "Read-Only" and is loaded from OTP.
4	CHOP_ALL_INIT	Initialization value for CHOP_ALL (Continuous Chopper Mode.) "1": Always in Chopper Mode / "0": Synchronized Mode. This register is "Read-Only" and is loaded from OTP.
3	DCDC_CLK_SEL[1]	DCDC Clock Select.
2	DCDC_CLK_SEL[0]	00b: 600 kHz (H:L=1:1)/ 01b: 857 kHz (H:L=3:4)/ 10b: 1000 kHz (H:L=1:2)/ 11b: 1200 kHz (H:L=2:3)
1	CHOP_SS	Enable operation in Chopper Mode during DCDC soft start. "1": Chopper Mode during DCDC soft start / "0": Synchronized Mode. Initial value is loaded from CHOP_SS_INIT during DCDC standby.
0	CHOP_ALL	Force continuous Chopper Mode operation. "1": Continuous Chopper Mode / "0": Synchronized Mode. Initial value is loaded from CHOP_ALL_INIT during DCDC standby.

8.6.14. VBUSCLPS_TH_SET

VBUS Collapse Detect Threshold Voltage Setting

Command Code: 0Dh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VBUSCLPS_TH_SET[14]	VBUS Anti-collapse entry voltage threshold. 3,840 mV to 32,640 mV, 128 mV steps. The register range: 0 mV to 32,640 mV. But the actual range: 3,840 mV to 25,088 mV. "00h" setting disables VBUS collapse detection.
13	VBUSCLPS_TH_SET[13]	
12	VBUSCLPS_TH_SET[12]	
11	VBUSCLPS_TH_SET[11]	
10	VBUSCLPS_TH_SET[10]	
9	VBUSCLPS_TH_SET[9]	
8	VBUSCLPS_TH_SET[8]	
7	VBUSCLPS_TH_SET[7]	
6	reserved	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.15. VCCCLPS_TH_SET

VCC Collapse Detect Threshold Voltage Setting

Command Code: 0Eh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VCCCLPS_TH_SET[14]	VCC Anti-collapse entry voltage threshold 3,840 mV to 32,640 mV, 128 mV steps. The register range: 0 mV to 32,640 mV. But the actual range: 3,840 mV to 25,088 mV. "00h" setting disables VCC collapse detection.
13	VCCCLPS_TH_SET[13]	
12	VCCCLPS_TH_SET[12]	
11	VCCCLPS_TH_SET[11]	
10	VCCCLPS_TH_SET[10]	
9	VCCCLPS_TH_SET[9]	
8	VCCCLPS_TH_SET[8]	
7	VCCCLPS_TH_SET[7]	
6	reserved	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.16. CHGWDT_SET

Charger WDT Setting

Command Code: 0Fh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	WDT_FST[7]	Watchdog Timer setting for Fast Charging. 4 ms to 1020 ms range, 4 ms steps. "00h" setting stops this timer.
14	WDT_FST[6]	
13	WDT_FST[5]	
12	WDT_FST[4]	
11	WDT_FST[3]	
10	WDT_FST[2]	
9	WDT_FST[1]	
8	WDT_FST[0]	
7	WDT_PRE[7]	Watchdog Timer setting for Pre-charging. 1ms to 255 ms range, 1 ms steps. "00h" setting stops this timer.
6	WDT_PRE[6]	
5	WDT_PRE[5]	
4	WDT_PRE[4]	
3	WDT_PRE[3]	
2	WDT_PRE[2]	
1	WDT_PRE[1]	
0	WDT_PRE[0]	

8.6.17. BATTWDT_SET

Battery Temperature and Battery Short Current WDT Setting

Command Code: 10h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	WDT_IBAT_SHORT[7]	Watchdog Timer setting for Battery Short Current. 4 ms to 1020 ms range, 4 ms steps. “00h” setting stops this timer.
14	WDT_IBAT_SHORT[6]	
13	WDT_IBAT_SHORT[5]	
12	WDT_IBAT_SHORT[4]	
11	WDT_IBAT_SHORT[3]	
10	WDT_IBAT_SHORT[2]	
9	WDT_IBAT_SHORT[1]	
8	WDT_IBAT_SHORT[0]	
7	WDT_THERM[7]	Watchdog Timer setting for Battery Temperature. 1 ms to 255 ms range, 1 ms steps. “00h” setting stops this timer.
6	WDT_THERM[6]	
5	WDT_THERM[5]	
4	WDT_THERM[4]	
3	WDT_THERM[3]	
2	WDT_THERM[2]	
1	WDT_THERM[1]	
0	WDT_THERM[0]	

8.6.18. VSYSREG_SET

VSYS Regulation Setting

Command Code: 11h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VSYSREG_SET[14]	VSYS regulation voltage setting and threshold voltage from Pre-charging to Fast-charging. 2,560 mV to 19,200 mV, 64 mV steps. The register range: 0 mV to 32,704 mV. But the actual range: 2,560 mV to 19,200 mV.
13	VSYSREG_SET[13]	
12	VSYSREG_SET[12]	
11	VSYSREG_SET[11]	
10	VSYSREG_SET[10]	
9	VSYSREG_SET[9]	
8	VSYSREG_SET[8]	
7	VSYSREG_SET[7]	
6	VSYSREG_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.19. VSYSVAL_THH_SET

VSYS Valid Threshold High Setting (Hysteresis)

Command Code: 12h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VSYSVAL_THH_SET[14]	VSYS voltage rising detection threshold with hysteresis. 2,560 mV to 19,200 mV, 64 mV steps. The register range: 0 mV to 32,704 mV. But the actual range: 2,560 mV to 19,200 mV.
13	VSYSVAL_THH_SET[13]	
12	VSYSVAL_THH_SET[12]	
11	VSYSVAL_THH_SET[11]	
10	VSYSVAL_THH_SET[10]	
9	VSYSVAL_THH_SET[9]	
8	VSYSVAL_THH_SET[8]	
7	VSYSVAL_THH_SET[7]	
6	VSYSVAL_THH_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.20. VSYSVAL_THL_SET

VSYS Valid Threshold Low Setting (Hysteresis)

Command Code: 13h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VSYSVAL_THL_SET[14]	VSYS voltage falling detection threshold with hysteresis. 2,560 mV to 19,200 mV, 64 mV steps. The register range: 0 mV to 32,704 mV. But the actual range: 2,560 mV to 19,200 mV.
13	VSYSVAL_THL_SET[13]	
12	VSYSVAL_THL_SET[12]	
11	VSYSVAL_THL_SET[11]	
10	VSYSVAL_THL_SET[10]	
9	VSYSVAL_THL_SET[9]	
8	VSYSVAL_THL_SET[8]	
7	VSYSVAL_THL_SET[7]	
6	VSYSVAL_THL_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.21. ITRICH_SET

Trickle-charge Current Setting

Command Code: 14h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	ITRICH_SET[10]	Trickle-charging current setting. 0 mA to 1,024 mA, 64 mA steps. The register range: 0 mA to 1,984 mA.
9	ITRICH_SET[9]	
8	ITRICH_SET[8]	
7	ITRICH_SET[7]	
6	ITRICH_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.22. IPRECH_SET

Pre-charge Current Setting

Command Code: 15h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	IPRECH_SET[10]	Pre-charging current setting. 0 mA to 1,024 mA, 64 mA steps. The register range: 0 mA to 1,984 mA.
9	IPRECH_SET[9]	
8	IPRECH_SET[8]	
7	IPRECH_SET[7]	
6	IPRECH_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.23. ICHG_SET

Fast-charge Current Setting

Command Code: 16h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	ICHG_SET[13]	Fast-charging current setting. 0 mA to 16,320 mA, 64 mA steps.
12	ICHG_SET[12]	
11	ICHG_SET[11]	
10	ICHG_SET[10]	
9	ICHG_SET[9]	
8	ICHG_SET[8]	
7	ICHG_SET[7]	
6	ICHG_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.24. ITERM_SET

Charge Termination Current Setting

Command Code: 17h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	ITERM_SET[10]	Charging Termination Current. 0 mA to 1,024 mA, 64 mA steps. The register range: 0 mA to 1,984 mA. But the actual range: 0 mA to 1,024 mA.
9	ITERM_SET[9]	
8	ITERM_SET[8]	
7	ITERM_SET[7]	
6	ITERM_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.25. VPRECHG_TH_SET

Pre-charge Voltage Threshold Setting

Command Code: 18h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VPRECHG_TH_SET[14]	Threshold voltage from Trickle-charging to Pre-charging 2,048 mV to 19,200 mV, 64 mV steps. The register range: 0 mV to 32,704 mV. But the actual range: 2,048 mV to 19,200 mV.
13	VPRECHG_TH_SET[13]	
12	VPRECHG_TH_SET[12]	
11	VPRECHG_TH_SET[11]	
10	VPRECHG_TH_SET[10]	
9	VPRECHG_TH_SET[9]	
8	VPRECHG_TH_SET[8]	
7	VPRECHG_TH_SET[7]	
6	VPRECHG_TH_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.26. VRBOOST_SET

Reverse Buck Boost Voltage Setting

Command Code: 19h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VRBOOST_SET[14]	Reverse buck boost voltage setting. 4,032 mV to 22,016 mV, 64 mV steps. The register range: 0 mV to 32,704 mV. But the actual range: 4,032 mV to 22,016 mV.
13	VRBOOST_SET[13]	
12	VRBOOST_SET[12]	
11	VRBOOST_SET[11]	
10	VRBOOST_SET[10]	
9	VRBOOST_SET[9]	
8	VRBOOST_SET[8]	
7	VRBOOST_SET[7]	
6	VRBOOST_SET[6]	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.27. VFASTCHG_REG_SET1

Fast Charge Voltage Regulation Setting 1

Command Code: 1Ah

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VFASTCHG_REG_SET1[14]	Fast Charging Regulation Voltage. 2,560 mV to 19,200 mV, 16 mV steps. The register range: 0 mV to 32,752 mV. But the actual range: 2,560 mV to 19,200 mV.
13	VFASTCHG_REG_SET1[13]	
12	VFASTCHG_REG_SET1[12]	
11	VFASTCHG_REG_SET1[11]	
10	VFASTCHG_REG_SET1[10]	
9	VFASTCHG_REG_SET1[9]	
8	VFASTCHG_REG_SET1[8]	
7	VFASTCHG_REG_SET1[7]	
6	VFASTCHG_REG_SET1[6]	
5	VFASTCHG_REG_SET1[5]	
4	VFASTCHG_REG_SET1[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.28. VFASTCHG_REG_SET2

Fast Charge Voltage Regulation Setting 2 (Hot 1)

Command Code: 1Bh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VFASTCHG_REG_SET2[14]	Fast Charging Regulation Voltage for the JEITA temperature range T3 to T5. 2,560 mV to 19,200 mV, 16 mV steps. The register range: 0 mV to 32,752 mV. But the actual range: 2,560 mV to 19,200 mV.
13	VFASTCHG_REG_SET2[13]	
12	VFASTCHG_REG_SET2[12]	
11	VFASTCHG_REG_SET2[11]	
10	VFASTCHG_REG_SET2[10]	
9	VFASTCHG_REG_SET2[9]	
8	VFASTCHG_REG_SET2[8]	
7	VFASTCHG_REG_SET2[7]	
6	VFASTCHG_REG_SET2[6]	
5	VFASTCHG_REG_SET2[5]	
4	VFASTCHG_REG_SET2[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.29. VFASTCHG_REG_SET3

Fast Charge Voltage Regulation Setting 3 (Hot 2)

Command Code: 1Ch

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VFASTCHG_REG_SET3[14]	Fast Charging Regulation Voltage for the JEITA temperature range T5 to T4 and T1 to T2. 2,560 mV to 19,200 mV, 16 mV steps. The register range: 0 mV to 32,752 mV. But the actual range: 2,560 mV to 19,200 mV.
13	VFASTCHG_REG_SET3[13]	
12	VFASTCHG_REG_SET3[12]	
11	VFASTCHG_REG_SET3[11]	
10	VFASTCHG_REG_SET3[10]	
9	VFASTCHG_REG_SET3[9]	
8	VFASTCHG_REG_SET3[8]	
7	VFASTCHG_REG_SET3[7]	
6	VFASTCHG_REG_SET3[6]	
5	VFASTCHG_REG_SET3[5]	
4	VFASTCHG_REG_SET3[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.30. VRECHG_SET

Re-charge Battery Voltage Setting

Command Code: 1Dh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VRECHG_SET[14]	Re-charge Battery Voltage. 2,560 mV to 19,200 mV, 16 mV steps. The register range: 0 mV to 32,752 mV. But the actual range: 2,560 mV to 19,200 mV.
13	VRECHG_SET[13]	
12	VRECHG_SET[12]	
11	VRECHG_SET[11]	
10	VRECHG_SET[10]	
9	VRECHG_SET[9]	
8	VRECHG_SET[8]	
7	VRECHG_SET[7]	
6	VRECHG_SET[6]	
5	VRECHG_SET[5]	
4	VRECHG_SET[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.31. VBATOVP_SET

Battery Over Voltage Protection Setting

Command Code: 1Eh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VBATOVP_SET[14]	Battery over voltage detection threshold. 2,560 mV to 19,200 mV, 16 mV steps. The register range: 0 mV to 32,752 mV. But the actual range: 2,560 mV to 19,200 mV.
13	VBATOVP_SET[13]	
12	VBATOVP_SET[12]	
11	VBATOVP_SET[11]	
10	VBATOVP_SET[10]	
9	VBATOVP_SET[9]	
8	VBATOVP_SET[8]	
7	VBATOVP_SET[7]	
6	VBATOVP_SET[6]	
5	VBATOVP_SET[5]	
4	VBATOVP_SET[4]	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.32. IBATSHORT_SET

Battery Short Current Protection Setting

Command Code: 1Fh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	IBATM_SHORT_SET[14]	Battery Short Current Protection Threshold 0 mA to 25,000 mA, 1 mA steps. The register range: 0 mA to 32,752 mA. But the actual range: 0 mA to 25,000 mA.
13	IBATM_SHORT_SET[13]	
12	IBATM_SHORT_SET[12]	
11	IBATM_SHORT_SET[11]	
10	IBATM_SHORT_SET[10]	
9	IBATM_SHORT_SET[9]	
8	IBATM_SHORT_SET[8]	
7	IBATM_SHORT_SET[7]	
6	IBATM_SHORT_SET[6]	
5	IBATM_SHORT_SET[5]	
4	IBATM_SHORT_SET[4]	
3	IBATM_SHORT_SET[3]	
2	IBATM_SHORT_SET[2]	
1	IBATM_SHORT_SET[1]	
0	IBATM_SHORT_SET[0]	

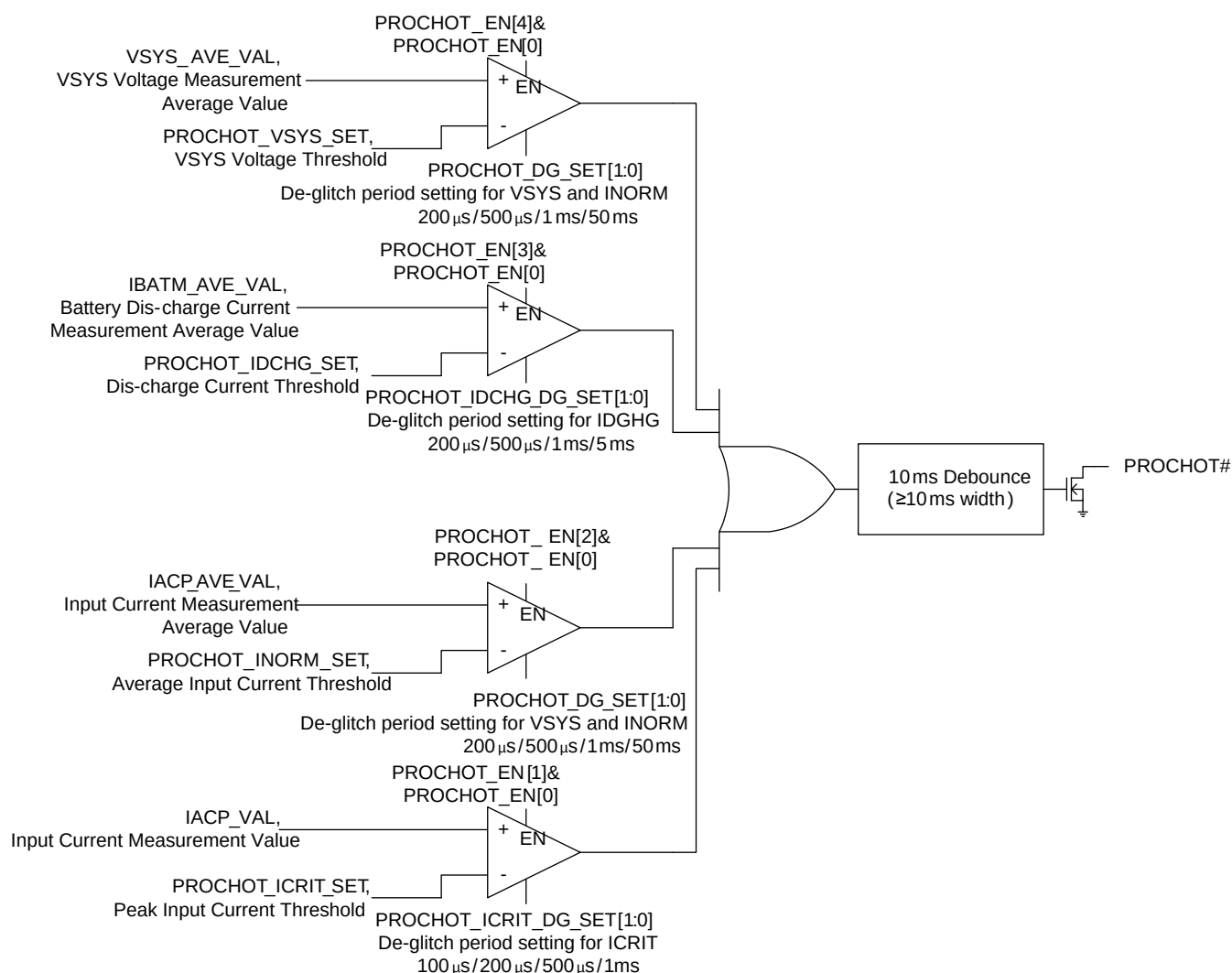
8.6.33. PROCHOT_CTRL_SET

PROCHOT# Pin Control Setting

Command Code: 20h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROCHOT_DG_SET[1]	PROCHOT# de-glitch period (VSYS, INORM) setting. 00b: 200 μ s/ 01b: 500 μ s/ 10b: 1 ms/ 11b: 50 ms
14	PROCHOT_DG_SET[0]	
13	reserved	
12	reserved	
11	PROCHOT_ICRIT_DG_SET[1]	PROCHOT# de-glitch period (ICRIT) setting. 00b: 100 μ s/ 01b: 200 μ s/ 10b: 500 μ s/ 11b: 1 ms
10	PROCHOT_ICRIT_DG_SET[0]	
9	PROCHOT_IDCHG_DG_SET[1]	PROCHOT# de-glitch period (IDCHG) setting. 00b: 200 μ s/ 01b: 500 μ s/ 10b: 1 μ s/ 11b: 5 ms
8	PROCHOT_IDCHG_DG_SET[0]	
7	reserved	
6	reserved	
5	reserved	
4	PROCHOT_EN[4]	PROCHOT# 2nd level enable (VSYS)
3	PROCHOT_EN[3]	PROCHOT# 2nd level enable (IDCHG)
2	PROCHOT_EN[2]	PROCHOT# 2nd level enable (INORM)
1	PROCHOT_EN[1]	PROCHOT# 2nd level enable (ICRIT)
0	PROCHOT_EN[0]	PROCHOT# 1st level enable



8.6.34. PROCHOT_ICRIT_SET

Peak Input Current Threshold Setting for the PROCHOT# pin

Command Code: 21h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	PROCHOT_ICRIT_SET[14]	Peak Input Current Threshold for the PROCHOT# pin 0 mA to 16,384 mA, 1 mA steps. The register range: 0 mA to 32,752 mA. But the actual range: 0 mA to 16,383 mA.
13	PROCHOT_ICRIT_SET[13]	
12	PROCHOT_ICRIT_SET[12]	
11	PROCHOT_ICRIT_SET[11]	
10	PROCHOT_ICRIT_SET[10]	
9	PROCHOT_ICRIT_SET[9]	
8	PROCHOT_ICRIT_SET[8]	
7	PROCHOT_ICRIT_SET[7]	
6	PROCHOT_ICRIT_SET[6]	
5	PROCHOT_ICRIT_SET[5]	
4	PROCHOT_ICRIT_SET[4]	
3	PROCHOT_ICRIT_SET[3]	
2	PROCHOT_ICRIT_SET[2]	
1	PROCHOT_ICRIT_SET[1]	
0	PROCHOT_ICRIT_SET[0]	

8.6.35. PROCHOT_INORM_SET

Average Input Current Threshold Setting for the PROCHOT# pin

Command Code: 22h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	PROCHOT_INORM_SET[14]	Average Input Current Threshold for the PROCHOT# pin 0 mA to 16,384 mA, 1 mA steps. The register range: 0 mA to 32,752 mA. But the actual range: 0 mA to 16,383 mA.
13	PROCHOT_INORM_SET[13]	
12	PROCHOT_INORM_SET[12]	
11	PROCHOT_INORM_SET[11]	
10	PROCHOT_INORM_SET[10]	
9	PROCHOT_INORM_SET[9]	
8	PROCHOT_INORM_SET[8]	
7	PROCHOT_INORM_SET[7]	
6	PROCHOT_INORM_SET[6]	
5	PROCHOT_INORM_SET[5]	
4	PROCHOT_INORM_SET[4]	
3	PROCHOT_INORM_SET[3]	
2	PROCHOT_INORM_SET[2]	
1	PROCHOT_INORM_SET[1]	
0	PROCHOT_INORM_SET[0]	

8.6.36. PROCHOT_IDCHG_SET

Dis-charge Current Threshold Setting for the PROCHOT# pin

Command Code: 23h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	PROCHOT_IDCHG_SET[13]	Dis-charge Current Threshold for the PROCHOT# pin 0 mA to 25,000 mA, 1 mA steps. The register range: 0 mA to 32,752 mA. But the actual range: 0 mA to 25,000 mA.
13	PROCHOT_IDCHG_SET[14]	
12	PROCHOT_IDCHG_SET[12]	
11	PROCHOT_IDCHG_SET[11]	
10	PROCHOT_IDCHG_SET[10]	
9	PROCHOT_IDCHG_SET[9]	
8	PROCHOT_IDCHG_SET[8]	
7	PROCHOT_IDCHG_SET[7]	
6	PROCHOT_IDCHG_SET[6]	
5	PROCHOT_IDCHG_SET[5]	
4	PROCHOT_IDCHG_SET[4]	
3	PROCHOT_IDCHG_SET[3]	
2	PROCHOT_IDCHG_SET[2]	
1	PROCHOT_IDCHG_SET[1]	
0	PROCHOT_IDCHG_SET[0]	

8.6.37. PROCHOT_VSYS_SET

VSYS Voltage Threshold Setting for the PROCHOT# pin

Command Code: 24h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	PROCHOT_VSYS_SET[14]	VSYS Voltage Threshold for the PROCHOT# pin 0 mV to 19,200 mV, 1 mV steps. The register range: 0 mV to 32,752 mV. But the actual range: 0 mV to 19,200 mV.
13	PROCHOT_VSYS_SET[13]	
12	PROCHOT_VSYS_SET[12]	
11	PROCHOT_VSYS_SET[11]	
10	PROCHOT_VSYS_SET[10]	
9	PROCHOT_VSYS_SET[9]	
8	PROCHOT_VSYS_SET[8]	
7	PROCHOT_VSYS_SET[7]	
6	PROCHOT_VSYS_SET[6]	
5	PROCHOT_VSYS_SET[5]	
4	PROCHOT_VSYS_SET[4]	
3	PROCHOT_VSYS_SET[3]	
2	PROCHOT_VSYS_SET[2]	
1	PROCHOT_VSYS_SET[1]	
0	PROCHOT_VSYS_SET[0]	

8.6.38. PMON_IOUT_CTRL_SET

PMON and IOUT Output Control Setting

Command Code: 25h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	IMON_INSEL	IOUT Input source select. 0b: Measurement Average Value/ 1b: Measurement Value
8	PMON_INSEL	PMON Input source select. 0b: Measurement Average Value/ 1b: Measurement Value
7	IOUT_OUT_EN	IOUT enable. "1": Enable / "0": Disable.
6	IOUT_SOURCE_SEL	IOUT source select. "1": Input Current / "0": Battery Dis-charge Current.
5	IOUT_GAIN_SET[1]	IOUT gain select. 00b: 5 V/V / 01b: 10 V/V / 10b: 20 V/V / 11b: 40 V/V
4	IOUT_GAIN_SET[0]	
3	PMON_OUT_EN	PMON Enable. "1": Enable / "0": Disable.
2	PMON_GAIN_SET[2]	PMON gain select. 0h: x1/ 1h: x2/ 2h: x4/ 3h: x8/ 4h: x16/ 5h: x32/ 6h: x64
1	PMON_GAIN_SET[1]	
0	PMON_GAIN_SET[0]	

8.6.39. PMON_DACIN_VAL

PMON DAC Input Value (for debug and production test)

Command Code: 26h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	PMON_DACIN_VAL[9]	PMON DAC Input Value (for debug and production test)
8	PMON_DACIN_VAL[8]	
7	PMON_DACIN_VAL[7]	
6	PMON_DACIN_VAL[6]	
5	PMON_DACIN_VAL[5]	
4	PMON_DACIN_VAL[4]	
3	PMON_DACIN_VAL[3]	
2	PMON_DACIN_VAL[2]	
1	PMON_DACIN_VAL[1]	
0	PMON_DACIN_VAL[0]	

8.6.40. IOUT_DACIN_VAL

IOUT DAC Input Value (for debug and production test)

Command Code: 27h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	IOUT_DACIN_VAL[11]	IOUT DAC Input Value (for debug and production test)
10	IOUT_DACIN_VAL[10]	
9	IOUT_DACIN_VAL[9]	
8	IOUT_DACIN_VAL[8]	
7	IOUT_DACIN_VAL[7]	
6	IOUT_DACIN_VAL[6]	
5	IOUT_DACIN_VAL[5]	
4	IOUT_DACIN_VAL[4]	
3	IOUT_DACIN_VAL[3]	
2	IOUT_DACIN_VAL[2]	
1	IOUT_DACIN_VAL[1]	
0	IOUT_DACIN_VAL[0]	

8.6.41. VCC_UCD_SET

BCS1.2 Charger Detector on the VCC Side Setting

Command Code: 28h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	BCSRETRY	Trigger for re-trial of the USB Charger Port detection. "1": Start detection / "0": Release the operation.
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	USBDETEN	Enabling USB Charger port detection. "1": Enable / "0": Disable.
6	reserved	
5	ENUMRDY	Setting USB Enumeration to Ready. "1": Skip Secondary Detection / "0": Normal operation.
4	reserved	
3	DCDMODE	DCD timeout period setting. "1": 1280 ms / "0": 640 ms.
2	reserved	
1	USB_SW_EN	Enabling automatic USB-Switch control. "1": Enable (auto) / "0": Disable (manual).
0	USB_SW	USB Switch manual control. "1": Switch ON / "0": Switch OFF.

8.6.42. VCC_UCD_STATUS

BCS1.2 Charger Detect Status on the VCC Side

Command Code: 29h

Bus Protocol: Read Word

Bit	Symbol	Description
15	DCDFAIL	DCD (USB Data Contact Detection) failed (timeout) status. "1": Failed / "0": Succeeded.
14	reserved	
13	CHGPORT[1]	USB Charger Port Detection result. 00b: No charger port/ 01b: SDP/ 10b: CDP/ 11b: DCP
12	CHGPORT[0]	
11	PUPDET	Pull-up detected at Primary Detection after DCDFAIL. "1": Detected / "0": Not detected.
10	reserved	
9	reserved	
8	reserved	
7	VBUS_VLD	USB VBUS valid voltage detection status. "1": Valid / "0": Not valid.
6	CHGDET	USB Charger Port detection status. "1": Detected / "0": Not detected.
5	reserved	
4	reserved	
3	OTGDET	USB OTG Device detection status. "1": Detected / "0": Not detected.
2	reserved	
1	reserved	
0	reserved	

BCS1.2 Charger Detect Status Matrix

	CHGDET	PUPDET	DCDFAIL	CHGPORT[1]	CHGPORT[0]
VBUS Open	0	0	0	0	0
SDP	0	0	0	0	1
CDP	1	0	0	1	0
DCP	1	0	0	1	1
Pull-up Port	0	1	1	0	1
Open Port	0	0	1	0	1
Unstable Port	0	0	1	0	1

8.6.43. VCC_UCD_FCTRL_SET

BCS1.2 Charger Detector on the VCC Side Manual Control Setting

Command Code: 2Bh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	In normal operation, do not set these registers.
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	UCDSWEN	
9	RREF_EN	
8	DPPU_EN	
7	DPREF_EN	
6	DMREF_EN	
5	DPDET_EN	
4	DMDDET_EN	
3	DPSINK_EN	
2	DMSINK_EN	
1	DP_BUFF_EN	
0	DM_BUFF_EN	

8.6.44. VCC_UCD_FCTRL_EN

BCS1.2 Charger Detector on the VCC Side Manual Control Enable

Command Code: 2Ch

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	EXTCLKENBL	In normal operation, do not set these registers.
14	PLSTESTEN	
13	reserved	
12	reserved	
11	reserved	In normal operation, do not set these registers.
10	UCDSWEN_TSTENB	
9	RREF_EN_TSTENB	
8	DPPU_EN_TSTENB	
7	DPREF_EN_TSTENB	
6	DMREF_EN_TSTENB	
5	DPDET_EN_TSTENB	
4	DMDDET_EN_TSTENB	
3	DPSINK_EN_TSTENB	
2	DMSINK_EN_TSTENB	
1	DP_BUFF_EN_TSTENB	
0	DM_BUFF_EN_TSTENB	

8.6.45. VBUS_UCD_SET

BCS1.2 Charger Detector on the VBUS Side Setting

Command Code: 30h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	BCSRETRY	Trigger for re-trial of the USB Charger Port detection. "1": Start detection / "0": Release the operation.
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	USBDETEN	Enabling USB Charger port detection. "1": Enable / "0": Disable.
6	reserved	
5	ENUMRDY	Setting USB Enumeration to Ready. "1": Skip Secondary Detection / "0": Normal operation.
4	reserved	
3	DCDMODE	DCD timeout period setting. "1": 1280 ms / "0": 640 ms.
2	reserved	
1	USB_SW_EN	Enabling automatic USB-Switch control. "1": Enable (auto) / "0": Disable (manual).
0	USB_SW	USB Switch manual control. "1": Switch ON / "0": Switch OFF.

8.6.46. VBUS_UCD_STATUS

BCS1.2 Charger Detect Status on the VBUS Side

Command Code: 31h

Bus Protocol: Read Word

Bit	Symbol	Description
15	DCDFAIL	DCD (USB Data Contact Detection) failed (timeout) status. "1": Failed / "0": Succeeded.
14	reserved	
13	CHGPORT[1]	USB Charger Port Detection result. 00b: No charger port/ 01b: SDP/ 10b: CDP/ 11b: DCP
12	CHGPORT[0]	
11	PUPDET	Pull-up detected at Primary Detection after DCDFAIL. "1": Detected / "0": Not detected.
10	reserved	
9	reserved	
8	reserved	
7	VBUS_VLD	USB VBUS valid voltage detection status. "1": Valid / "0": Not valid.
6	CHGDET	USB Charger Port detection status. "1": Detected / "0": Not detected.
5	reserved	
4	reserved	
3	OTGDET	USB OTG Device detection status. "1": Detected / "0": Not detected.
2	reserved	
1	reserved	
0	reserved	

BCS1.2 Charger Detect Status Matrix

	CHGDET	PUPDET	DCDFAIL	CHGPORT[1]	CHGPORT[0]
VBUS Open	0	0	0	0	0
SDP	0	0	0	0	1
CDP	1	0	0	1	0
DCP	1	0	0	1	1
Pull-up Port	0	1	1	0	1
Open Port	0	0	1	0	1
Unstable Port	0	0	1	0	1

8.6.47. VBUS_UCD_FCTRL_SET

BCS1.2 Charger Detector on the VBUS Side Manual Control Setting

Command Code: 33h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	In normal operation, do not set these registers.
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	UCDSWEN	
9	RREF_EN	
8	DPPU_EN	
7	DPREF_EN	
6	DMREF_EN	
5	DPDET_EN	
4	DMDDET_EN	
3	DPSINK_EN	
2	DMSINK_EN	
1	DP_BUFF_EN	
0	DM_BUFF_EN	

8.6.48. VBUS_UCD_FCTRL_EN

BCS1.2 Charger Detector on the VBUS Side Manual Control Enable

Command Code: 34h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	EXTCLKENBL	In normal operation, do not set these registers.
14	PLSTESTEN	
13	reserved	
12	reserved	In normal operation, do not set these registers.
11	reserved	
10	UCDSWEN_TSTENB	
9	RREF_EN_TSTENB	
8	DPPU_EN_TSTENB	
7	DPREF_EN_TSTENB	
6	DMREF_EN_TSTENB	
5	DPDET_EN_TSTENB	
4	DMDDET_EN_TSTENB	
3	DPSINK_EN_TSTENB	
2	DMSINK_EN_TSTENB	
1	DP_BUFF_EN_TSTENB	
0	DM_BUFF_EN_TSTENB	

8.6.49. CHIP_ID

Chip ID

Command Code: 38h

Bus Protocol: Read Word

Bit	Symbol	Description
15	CHIP_ID[15]	Chip ID
14	CHIP_ID[14]	
13	CHIP_ID[13]	
12	CHIP_ID[12]	
11	CHIP_ID[11]	
10	CHIP_ID[10]	
9	CHIP_ID[9]	
8	CHIP_ID[8]	
7	CHIP_ID[7]	
6	CHIP_ID[6]	
5	CHIP_ID[5]	
4	CHIP_ID[4]	
3	CHIP_ID[3]	
2	CHIP_ID[2]	
1	CHIP_ID[1]	
0	CHIP_ID[0]	

8.6.50. CHIP_REV

Chip Revision

Command Code: 39h

Bus Protocol: Read Word

Bit	Symbol	Description
15	CHIP_REV[15]	Chip Revision
14	CHIP_REV[14]	
13	CHIP_REV[13]	
12	CHIP_REV[12]	
11	CHIP_REV[11]	
10	CHIP_REV[10]	
9	CHIP_REV[9]	
8	CHIP_REV[8]	
7	CHIP_REV[7]	
6	CHIP_REV[6]	
5	CHIP_REV[5]	
4	CHIP_REV[4]	
3	CHIP_REV[3]	
2	CHIP_REV[2]	
1	CHIP_REV[1]	
0	CHIP_REV[0]	

8.6.51. IC_SET1

1-Cell Mode Setting, ACP Discharge Control and ACOK Control Setting.

Command Code: 3Ah

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	ONE_CELL_MODE	1 cell battery mode. "1": 1 cell battery mode/ "0": 2 to 4 cells battery mode "1": VFASTCHG_REG_SET1, VFASTCHG_REG_SET 2, and VFASTCHG_REG_SET 3 is set 4.6 V or less and VSYSREG_SET set 5.0 V or less "0": VSYSREG_SET set more than 5.0 V
10	reserved	
9	VACP_AUTO_DISCHG	VACP Auto Discharge control is enable when the Power path is changed. "1": VACP Auto discharge control is enabled./ "0": Disabled.
8	VACP_LOAD	VACP Discharge control when the VACP power path is plugged off. "1": VACP load on and discharged./ "0": VACP load off.
7	reserved	
6	reserved	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	ACOK_POL	ACOK open drain output polarity control. "1": ACOK polarity is inverted, L=Asserted, Hi-z=Deasserted. "0": ACOK polarity is normal, L=Deasserted, Hi-z=Asserted.
0	ACOK_DISEN	ACOK open drain output disable. "1": Disable, ACOK is Hi-z. / "0": Enable.

8.6.52. IC_SET2

IC Setting Register (for debug and production test)

Command Code: 3Bh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	DEBUG_SET[8]	Debug Setting (for debug and production test)
7	DEBUG_SET[7]	Debug Setting (for debug and production test)
6	DEBUG_SET[6]	Debug Setting (for debug and production test)
5	DEBUG_SET[5]	Debug Setting (for debug and production test)
4	DEBUG_SET[4]	Debug Setting (for debug and production test)
3	reserved	
2	reserved	
1	reserved	
0	DEBUG_SET[0]	Debug Setting (for debug and production test)

8.6.53. SYSTEM_STATUS

System Power-on Status

Command Code: 3Ch

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	reserved	
6	MONRST_STATE	Reset status for MONRST. "1": Reset asserted / "0": Reset released.
5	ALMRST_STATE	Reset status for ALMRST. "1": Reset asserted / "0": Reset released.
4	CHGRST_STATE	Reset status for CHGRST. "1": Reset asserted / "0": Reset released.
3	reserved	
2	reserved	
1	OTPLD_STATE	OTPROM loading status. "1": shows the OTPROM loading is finished./ "0": Not finished.
0	ALLRST_STATE	Reset status for ALLRST. "1": Reset asserted / "0": Reset released.

8.6.54. SYSTEM_CTRL_SET

Software Reset and Reload OTP

Command Code: 3Dh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	reserved	
6	MONRST	Writing "1" resets Voltage Meter block and the status registers. But the setting registers are not initialized. Writing "0" releases reset operation.
5	ALMRST	Writing "1" resets Interrupt block and the status registers. But the setting registers are not initialized. Writing "0" releases reset operation.
4	CHGRST	Writing "1" resets Battery Charger block and USB Detector block and the status registers. But the setting registers are not initialized. Writing "0" releases reset operation.
3	reserved	
2	reserved	
1	OTPLD	Writing "1" starts to load the OTPROM data into the internal registers. OTPROM data is loaded automatically for power-on sequence. But if necessary, user is able to reload the OTPROM data by writing this bit "1".
0	ALLRST	Writing "1" resets Voltage Meter block, Interrupt block, Battery Charger block and USB Detector blocks and the status registers. But the setting registers are not initialized. Writing "0" release reset operation.

8.6.55. PROTECT_SET

Access Un-protect Setting for Address 3Fh

Command Code: 3Eh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROTECT_SET[15]	Access Un-protect Setting for the “debug command map” (debug and production test only)
14	PROTECT_SET[14]	
13	PROTECT_SET[13]	
12	PROTECT_SET[12]	
11	PROTECT_SET[11]	
10	PROTECT_SET[10]	
9	PROTECT_SET[9]	
8	PROTECT_SET[8]	
7	PROTECT_SET[7]	
6	PROTECT_SET[6]	
5	PROTECT_SET[5]	
4	PROTECT_SET[4]	
3	PROTECT_SET[3]	
2	PROTECT_SET[2]	
1	PROTECT_SET[1]	
0	PROTECT_SET[0]	

8.6.56. MAP_SET

Change Command Code Map

Command Code: 3Fh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	MAP_SET[15]	Change Command Code Map
14	MAP_SET[14]	
13	MAP_SET[13]	
12	MAP_SET[12]	
11	MAP_SET[11]	
10	MAP_SET[10]	
9	MAP_SET[9]	
8	MAP_SET[8]	
7	MAP_SET[7]	
6	MAP_SET[6]	
5	MAP_SET[5]	
4	MAP_SET[4]	
3	MAP_SET[3]	
2	MAP_SET[2]	
1	MAP_SET[1]	
0	MAP_SET[0]	

8.6.57. VM_CTRL_SET

SAR-ADC Measurement Control Setting

Command Code: 40h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	ADCINTERVAL[1]	SAR-ADC Operating Interval Setting.
14	ADCINTERVAL[0]	00b: No Interval/ 01b: 1 ms/ 10b: 10 ms/ 11b: 100 ms
13	ADCMOD[1]	Operation Mode Setting
12	ADCMOD[0]	00b: Power Down/ 01b: Normal Operation
11	ADCTMOD[1]	Test Mode Setting
10	ADCTMOD[0]	00b: Normal Operation/ 01b: Test Mode
9	EXTIADPEN	IADP (Input current Limit setting pin) voltage measurement. "1": Enable / "0": Disable.
8	VSYSENB	VSYS voltage measurement. "1": Enable / "0": Disable.
7	VCCENB	VCC voltage measurement. "1": Enable / "0": Disable.
6	VBUSENB	VBUS voltage measurement. "1": Enable / "0": Disable.
5	VACPENB	VACP voltage measurement. "1": Enable / "0": Disable.
4	IACPENB	IACP voltage measurement. "1": Enable / "0": Disable.
3	THERMENB	TSENSE voltage measurement. "1": Enable / "0": Disable.
2	VBATENB	VBATT voltage measurement. "1": Enable / "0": Disable.
1	IBATMENB	IBATTM current (discharge) measurement. "1": Enable / "0": Disable.
0	IBATPENB	IBATTP current (current) measurement. "1": Enable / "0": Disable.

8.6.58. THERM_WINDOW_SET1

JEITA Battery Temperature Window Setting 1

Command Code: 41h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TMPTHR1B[7]	Upper threshold of T1, JEITA profile. (200-TMPTHR1B [7:0]) °C. -55 °C to +200 °C, 1 °C steps.
14	TMPTHR1B[6]	
13	TMPTHR1B[5]	
12	TMPTHR1B[4]	
11	TMPTHR1B[3]	
10	TMPTHR1B[2]	
9	TMPTHR1B[1]	
8	TMPTHR1B[0]	
7	TMPTHR1A[7]	Lower threshold of T1, JEITA profile. (200-TMPTHR1A [7:0]) °C. -55 °C to +200 °C, 1 °C steps.
6	TMPTHR1A[6]	
5	TMPTHR1A[5]	
4	TMPTHR1A[4]	
3	TMPTHR1A[3]	
2	TMPTHR1A[2]	
1	TMPTHR1A[1]	
0	TMPTHR1A[0]	

8.6.59. THERM_WINDOW_SET2

JEITA Battery Temperature Window Setting 2

Command Code: 42h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TMPTHR2B[7]	Upper threshold of T2, JEITA profile. (200-TMPTHR2B [7:0]) °C. -55 °C to +200 °C, 1 °C steps.
14	TMPTHR2B[6]	
13	TMPTHR2B[5]	
12	TMPTHR2B[4]	
11	TMPTHR2B[3]	
10	TMPTHR2B[2]	
9	TMPTHR2B[1]	
8	TMPTHR2B[0]	
7	TMPTHR2A[7]	Lower threshold of T2, JEITA profile. (200-TMPTHR2A [7:0]) °C. -55 °C to + 200 °C, 1 °C steps.
6	TMPTHR2A[6]	
5	TMPTHR2A[5]	
4	TMPTHR2A[4]	
3	TMPTHR2A[3]	
2	TMPTHR2A[2]	
1	TMPTHR2A[1]	
0	TMPTHR2A[0]	

8.6.60. THERM_WINDOW_SET3

JEITA Battery Temperature Window Setting 3

Command Code: 43h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TMPTHR3B[7]	Upper threshold of T3, JEITA profile. (200-TMPTHR3B [7:0]) °C. -55 °C to +200 °C, 1 °C steps.
14	TMPTHR3B[6]	
13	TMPTHR3B[5]	
12	TMPTHR3B[4]	
11	TMPTHR3B[3]	
10	TMPTHR3B[2]	
9	TMPTHR3B[1]	
8	TMPTHR3B[0]	
7	TMPTHR3A[7]	Lower threshold of T3, JEITA profile. (200-TMPTHR3A [7:0]) °C. -55 °C to +200 °C, 1 °C steps.
6	TMPTHR3A[6]	
5	TMPTHR3A[5]	
4	TMPTHR3A[4]	
3	TMPTHR3A[3]	
2	TMPTHR3A[2]	
1	TMPTHR3A[1]	
0	TMPTHR3A[0]	

8.6.61. THERM_WINDOW_SET4

JEITA Battery Temperature Window Setting 4

Command Code: 44h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TMPTHR4B[7]	Upper threshold of T4, JEITA profile. (200-TMPTHR4B [7:0]) °C. -55 °C to +200 °C, 1 °C steps.
14	TMPTHR4B[6]	
13	TMPTHR4B[5]	
12	TMPTHR4B[4]	
11	TMPTHR4B[3]	
10	TMPTHR4B[2]	
9	TMPTHR4B[1]	
8	TMPTHR4B[0]	
7	TMPTHR4A[7]	Lower threshold of T4, JEITA profile. (200-TMPTHR4A [7:0]) °C. -55 °C to +200 °C, 1 °C steps.
6	TMPTHR4A[6]	
5	TMPTHR4A[5]	
4	TMPTHR4A[4]	
3	TMPTHR4A[3]	
2	TMPTHR4A[2]	
1	TMPTHR4A[1]	
0	TMPTHR4A[0]	

8.6.62. THERM_WINDOW_SET5

JEITA Battery Temperature Window Setting 5

Command Code: 45h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TMPTHR5B[7]	Upper threshold of T5, between T3 and T4. (200-TMPTHR5B [7:0]) °C. -55 °C to +200 °C, 1 °C steps.
14	TMPTHR5B[6]	
13	TMPTHR5B[5]	
12	TMPTHR5B[4]	
11	TMPTHR5B[3]	
10	TMPTHR5B[2]	
9	TMPTHR5B[1]	
8	TMPTHR5B[0]	
7	TMPTHR5A[7]	Lower threshold of T5, between T3 and T4. (200-TMPTHR5A [7:0]) °C. -55 °C to +200 °C, 1 °C steps.
6	TMPTHR5A[6]	
5	TMPTHR5A[5]	
4	TMPTHR5A[4]	
3	TMPTHR5A[3]	
2	TMPTHR5A[2]	
1	TMPTHR5A[1]	
0	TMPTHR5A[0]	

8.6.63. IBATP_TH_SET

Battery Current (Charge) Interrupt Threshold Setting

Command Code: 46h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	IBATP_TH_SET[14]	Battery Current (Charge) Interrupt Threshold. 0 mA to 25,000 mA, 1 mA steps. The register range: 0 mA to 32,752 mA. But the actual range: 0 mA to 25,000 mA.
13	IBATP_TH_SET[13]	
12	IBATP_TH_SET[12]	
11	IBATP_TH_SET[11]	
10	IBATP_TH_SET[10]	
9	IBATP_TH_SET[9]	
8	IBATP_TH_SET[8]	
7	IBATP_TH_SET[7]	
6	IBATP_TH_SET[6]	
5	IBATP_TH_SET[5]	
4	IBATP_TH_SET[4]	
3	IBATP_TH_SET[3]	
2	IBATP_TH_SET[2]	
1	IBATP_TH_SET[1]	
0	IBATP_TH_SET[0]	

8.6.64. IBATM_TH_SET

Battery Current (Dis-charge) Interrupt Threshold Setting

Command Code: 47h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	IBATM_TH_SET[14]	Battery Current (Dis-charge) Interrupt Threshold. 0 mA to 25,000 mA, 1 mA steps. The register range: 0 mA to 32,752 mA. But the actual range: 0 mA to 25,000 mA.
13	IBATM_TH_SET[13]	
12	IBATM_TH_SET[12]	
11	IBATM_TH_SET[11]	
10	IBATM_TH_SET[10]	
9	IBATM_TH_SET[9]	
8	IBATM_TH_SET[8]	
7	IBATM_TH_SET[7]	
6	IBATM_TH_SET[6]	
5	IBATM_TH_SET[5]	
4	IBATM_TH_SET[4]	
3	IBATM_TH_SET[3]	
2	IBATM_TH_SET[2]	
1	IBATM_TH_SET[1]	
0	IBATM_TH_SET[0]	

8.6.65. VBAT_TH_SET

Battery Voltage Interrupt Threshold Setting

Command Code: 48h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VBAT_TH_SET[14]	Battery Voltage Interrupt Threshold. 0 mV to 19,200 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 19,200 mV.
13	VBAT_TH_SET[13]	
12	VBAT_TH_SET[12]	
11	VBAT_TH_SET[11]	
10	VBAT_TH_SET[10]	
9	VBAT_TH_SET[9]	
8	VBAT_TH_SET[8]	
7	VBAT_TH_SET[7]	
6	VBAT_TH_SET[6]	
5	VBAT_TH_SET[5]	
4	VBAT_TH_SET[4]	
3	VBAT_TH_SET[3]	
2	VBAT_TH_SET[2]	
1	VBAT_TH_SET[1]	
0	VBAT_TH_SET[0]	

8.6.66. THERM_TH_SET

Battery Temperature Interrupt Threshold Setting

Command Code: 49h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	THERM_TH_SET[7]	Battery Temperature Interrupt Threshold Setting (200-THERM_TH_SET[7:0]) °C. -55 °C to +200 °C range, 1 °C steps.
6	THERM_TH_SET[6]	
5	THERM_TH_SET[5]	
4	THERM_TH_SET[4]	
3	THERM_TH_SET[3]	
2	THERM_TH_SET[2]	
1	THERM_TH_SET[1]	
0	THERM_TH_SET[0]	

8.6.67. IACP_TH_SET

Input Current (between ACP and ACN) Interrupt Threshold Setting

Command Code: 4Ah

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	IACP_TH_SET[14]	Input Current (between ACP and ACN) Interrupt Threshold. 0 mA to 16,384 mA, 1 mA steps. The register range: 0 mA to 32,752 mA. But the actual range: 0 mA to 16,383 mA.
13	IACP_TH_SET[13]	
12	IACP_TH_SET[12]	
11	IACP_TH_SET[11]	
10	IACP_TH_SET[10]	
9	IACP_TH_SET[9]	
8	IACP_TH_SET[8]	
7	IACP_TH_SET[7]	
6	IACP_TH_SET[6]	
5	IACP_TH_SET[5]	
4	IACP_TH_SET[4]	
3	IACP_TH_SET[3]	
2	IACP_TH_SET[2]	
1	IACP_TH_SET[1]	
0	IACP_TH_SET[0]	

8.6.68. VACP_TH_SET

Input Voltage (ACP) Interrupt Threshold Setting

Command Code: 4Bh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VACP_TH_SET[14]	Input Voltage (ACP) Interrupt Threshold. 0 mV to 25,600 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 25,600 mV.
13	VACP_TH_SET[13]	
12	VACP_TH_SET[12]	
11	VACP_TH_SET[11]	
10	VACP_TH_SET[10]	
9	VACP_TH_SET[9]	
8	VACP_TH_SET[8]	
7	VACP_TH_SET[7]	
6	VACP_TH_SET[6]	
5	VACP_TH_SET[5]	
4	VACP_TH_SET[4]	
3	VACP_TH_SET[3]	
2	VACP_TH_SET[2]	
1	VACP_TH_SET[1]	
0	VACP_TH_SET[0]	

8.6.69. VBUS_TH_SET

VBUS Voltage Interrupt Threshold Setting

Command Code: 4Ch

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VBUS_TH_SET[14]	VBUS Voltage Interrupt Threshold. 0 mV to 25,600 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 25,600 mV.
13	VBUS_TH_SET[13]	
12	VBUS_TH_SET[12]	
11	VBUS_TH_SET[11]	
10	VBUS_TH_SET[10]	
9	VBUS_TH_SET[9]	
8	VBUS_TH_SET[8]	
7	VBUS_TH_SET[7]	
6	VBUS_TH_SET[6]	
5	VBUS_TH_SET[5]	
4	VBUS_TH_SET[4]	
3	VBUS_TH_SET[3]	
2	VBUS_TH_SET[2]	
1	VBUS_TH_SET[1]	
0	VBUS_TH_SET[0]	

8.6.70. VCC_TH_SET

VCC Voltage Interrupt Threshold Setting

Command Code: 4Dh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VCC_TH_SET[14]	VCC Voltage Interrupt Threshold. 0 mV to 25,600 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 25,600 mV.
13	VCC_TH_SET[13]	
12	VCC_TH_SET[12]	
11	VCC_TH_SET[11]	
10	VCC_TH_SET[10]	
9	VCC_TH_SET[9]	
8	VCC_TH_SET[8]	
7	VCC_TH_SET[7]	
6	VCC_TH_SET[6]	
5	VCC_TH_SET[5]	
4	VCC_TH_SET[4]	
3	VCC_TH_SET[3]	
2	VCC_TH_SET[2]	
1	VCC_TH_SET[1]	
0	VCC_TH_SET[0]	

8.6.71. VSYS_TH_SET

VSYS Voltage Interrupt Threshold Setting

Command Code: 4Eh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VSYS_TH_SET[14]	VSYS Voltage Interrupt 0 mV to 19,200 mV, 1 mV steps. The register range: 0 mV to 32,752 mV. But the actual range: 0 mV to 19,200 mV.
13	VSYS_TH_SET[13]	
12	VSYS_TH_SET[12]	
11	VSYS_TH_SET[11]	
10	VSYS_TH_SET[10]	
9	VSYS_TH_SET[9]	
8	VSYS_TH_SET[8]	
7	VSYS_TH_SET[7]	
6	VSYS_TH_SET[6]	
5	VSYS_TH_SET[5]	
4	VSYS_TH_SET[4]	
3	VSYS_TH_SET[3]	
2	VSYS_TH_SET[2]	
1	VSYS_TH_SET[1]	
0	VSYS_TH_SET[0]	

8.6.72. EXTIADP_TH_SET

IADP (Input current limit setting pin) Voltage Interrupt Threshold Setting

Command Code: 4Fh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	EXTIADP_TH_SET[11]	IADP (Input current Limit setting pin) voltage Interrupt (for Debug use)
10	EXTIADP_TH_SET[10]	
9	EXTIADP_TH_SET[9]	
8	EXTIADP_TH_SET[8]	
7	EXTIADP_TH_SET[7]	
6	EXTIADP_TH_SET[6]	
5	EXTIADP_TH_SET[5]	
4	EXTIADP_TH_SET[4]	
3	EXTIADP_TH_SET[3]	
2	EXTIADP_TH_SET[2]	
1	EXTIADP_TH_SET[1]	
0	EXTIADP_TH_SET[0]	

8.6.73. IBATP_VAL

Battery Current (Charge) Measurement Value

Command Code: 50h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IBATP_VAL[14]	Battery Current (Charge) Measurement Value 0 mA to 25,000 mA, 1 mA steps.
13	IBATP_VAL[13]	
12	IBATP_VAL[12]	
11	IBATP_VAL[11]	
10	IBATP_VAL[10]	
9	IBATP_VAL[9]	
8	IBATP_VAL[8]	
7	IBATP_VAL[7]	
6	IBATP_VAL[6]	
5	IBATP_VAL[5]	
4	IBATP_VAL[4]	
3	IBATP_VAL[3]	
2	IBATP_VAL[2]	
1	IBATP_VAL[1]	
0	IBATP_VAL[0]	

8.6.74. IBATP_AVE_VAL

Battery Current (Charge) Measurement Average Value

Command Code: 51h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IBATP_AVE_VAL[14]	Battery Current (Charge) Measurement Average Value 0 mA to 25,000 mA, 1 mA steps.
13	IBATP_AVE_VAL[13]	
12	IBATP_AVE_VAL[12]	
11	IBATP_AVE_VAL[11]	
10	IBATP_AVE_VAL[10]	
9	IBATP_AVE_VAL[9]	
8	IBATP_AVE_VAL[8]	
7	IBATP_AVE_VAL[7]	
6	IBATP_AVE_VAL[6]	
5	IBATP_AVE_VAL[5]	
4	IBATP_AVE_VAL[4]	
3	IBATP_AVE_VAL[3]	
2	IBATP_AVE_VAL[2]	
1	IBATP_AVE_VAL[1]	
0	IBATP_AVE_VAL[0]	

8.6.75. IBATM_VAL

Battery Current (Dis-charge) Measurement Value

Command Code: 52h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IBATM_VAL[14]	Battery Current (Dis-charge) Measurement Value 0 mA to 25,000 mA, 1 mA steps.
13	IBATM_VAL[13]	
12	IBATM_VAL[12]	
11	IBATM_VAL[11]	
10	IBATM_VAL[10]	
9	IBATM_VAL[9]	
8	IBATM_VAL[8]	
7	IBATM_VAL[7]	
6	IBATM_VAL[6]	
5	IBATM_VAL[5]	
4	IBATM_VAL[4]	
3	IBATM_VAL[3]	
2	IBATM_VAL[2]	
1	IBATM_VAL[1]	
0	IBATM_VAL[0]	

8.6.76. IBATM_AVE_VAL

Battery Current (Dis-charge) Measurement Average Value

Command Code: 53h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IBATM_AVE_VAL[14]	Battery Current (Dis-charge) Measurement Average Value 0 mA to 25,000 mA, 1 mA steps.
13	IBATM_AVE_VAL[13]	
12	IBATM_AVE_VAL[12]	
11	IBATM_AVE_VAL[11]	
10	IBATM_AVE_VAL[10]	
9	IBATM_AVE_VAL[9]	
8	IBATM_AVE_VAL[8]	
7	IBATM_AVE_VAL[7]	
6	IBATM_AVE_VAL[6]	
5	IBATM_AVE_VAL[5]	
4	IBATM_AVE_VAL[4]	
3	IBATM_AVE_VAL[3]	
2	IBATM_AVE_VAL[2]	
1	IBATM_AVE_VAL[1]	
0	IBATM_AVE_VAL[0]	

8.6.77. VBAT_VAL

Battery Voltage Measurement Value

Command Code: 54h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VBAT_VAL[14]	Battery Voltage Measurement Value 0 mV to 19,200 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 19,200 mV.
13	VBAT_VAL[13]	
12	VBAT_VAL[12]	
11	VBAT_VAL[11]	
10	VBAT_VAL[10]	
9	VBAT_VAL[9]	
8	VBAT_VAL[8]	
7	VBAT_VAL[7]	
6	VBAT_VAL[6]	
5	VBAT_VAL[5]	
4	VBAT_VAL[4]	
3	VBAT_VAL[3]	
2	VBAT_VAL[2]	
1	VBAT_VAL[1]	
0	VBAT_VAL[0]	

8.6.78. VBAT_AVE_VAL

Battery Voltage Measurement Average Value

Command Code: 55h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VBAT_AVE_VAL[14]	Battery Voltage Measurement Average Value 0 mV to 19,200 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 19,200 mV.
13	VBAT_AVE_VAL[13]	
12	VBAT_AVE_VAL[12]	
11	VBAT_AVE_VAL[11]	
10	VBAT_AVE_VAL[10]	
9	VBAT_AVE_VAL[9]	
8	VBAT_AVE_VAL[8]	
7	VBAT_AVE_VAL[7]	
6	VBAT_AVE_VAL[6]	
5	VBAT_AVE_VAL[5]	
4	VBAT_AVE_VAL[4]	
3	VBAT_AVE_VAL[3]	
2	VBAT_AVE_VAL[2]	
1	VBAT_AVE_VAL[1]	
0	VBAT_AVE_VAL[0]	

8.6.79. THERM_VAL

Thermistor Temperature Measurement Value

Command Code: 56h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	THERM_VAL[7]	Temperature Measurement Value (200-THERM_VAL[7:0]) °C. -55 °C to +200 °C, 1 °C steps. Write Word access is available when VM_CTRL_SET.THERMENB bit = 0.
6	THERM_VAL[6]	
5	THERM_VAL[5]	
4	THERM_VAL[4]	
3	THERM_VAL[3]	
2	THERM_VAL[2]	
1	THERM_VAL[1]	
0	THERM_VAL[0]	

8.6.80. VTH_VAL

Thermistor Measurement Voltage Value

Command Code: 57h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	VTH_VAL[11]	Thermistor Measurement Voltage Value (for Debug use)
10	VTH_VAL[10]	
9	VTH_VAL[9]	
8	VTH_VAL[8]	
7	VTH_VAL[7]	
6	VTH_VAL[6]	
5	VTH_VAL[5]	
4	VTH_VAL[4]	
3	VTH_VAL[3]	
2	VTH_VAL[2]	
1	VTH_VAL[1]	
0	VTH_VAL[0]	

8.6.81. IACP_VAL

Input Current (between ACP and ACN) Measurement Value

Command Code: 58h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IACP_VAL[14]	Input Current (between ACP and ACN) Measurement Value 0 mA to 16,384 mA, 1 mA steps.
13	IACP_VAL[13]	
12	IACP_VAL[12]	
11	IACP_VAL[11]	
10	IACP_VAL[10]	
9	IACP_VAL[9]	
8	IACP_VAL[8]	
7	IACP_VAL[7]	
6	IACP_VAL[6]	
5	IACP_VAL[5]	
4	IACP_VAL[4]	
3	IACP_VAL[3]	
2	IACP_VAL[2]	
1	IACP_VAL[1]	
0	IACP_VAL[0]	

8.6.82. IACP_AVE_VAL

Input Current (between ACP and ACN) Measurement Average Value

Command Code: 59h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	IACP_AVE_VAL[14]	Input Current (between ACP and ACN) Measurement Average Value 0 mA to 16,384 mA, 1 mA steps.
13	IACP_AVE_VAL[13]	
12	IACP_AVE_VAL[12]	
11	IACP_AVE_VAL[11]	
10	IACP_AVE_VAL[10]	
9	IACP_AVE_VAL[9]	
8	IACP_AVE_VAL[8]	
7	IACP_AVE_VAL[7]	
6	IACP_AVE_VAL[6]	
5	IACP_AVE_VAL[5]	
4	IACP_AVE_VAL[4]	
3	IACP_AVE_VAL[3]	
2	IACP_AVE_VAL[2]	
1	IACP_AVE_VAL[1]	
0	IACP_AVE_VAL[0]	

8.6.83. VACP_VAL

Input Voltage (ACP) Measurement Value

Command Code: 5Ah

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VACP_VAL[14]	Input Voltage (ACP) Measurement Value 0 mV to 25,600 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 25,600 mV.
13	VACP_VAL[13]	
12	VACP_VAL[12]	
11	VACP_VAL[11]	
10	VACP_VAL[10]	
9	VACP_VAL[9]	
8	VACP_VAL[8]	
7	VACP_VAL[7]	
6	VACP_VAL[6]	
5	VACP_VAL[5]	
4	VACP_VAL[4]	
3	VACP_VAL[3]	
2	VACP_VAL[2]	
1	VACP_VAL[1]	
0	VACP_VAL[0]	

8.6.84. VACP_AVE_VAL

Input Voltage (ACP) Measurement Average Value

Command Code: 5Bh

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VACP_AVE_VAL[14]	Input Voltage (ACP) Measurement Average Value 0 mV to 25,600 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 25,600 mV.
13	VACP_AVE_VAL[13]	
12	VACP_AVE_VAL[12]	
11	VACP_AVE_VAL[11]	
10	VACP_AVE_VAL[10]	
9	VACP_AVE_VAL[9]	
8	VACP_AVE_VAL[8]	
7	VACP_AVE_VAL[7]	
6	VACP_AVE_VAL[6]	
5	VACP_AVE_VAL[5]	
4	VACP_AVE_VAL[4]	
3	VACP_AVE_VAL[3]	
2	VACP_AVE_VAL[2]	
1	VACP_AVE_VAL[1]	
0	VACP_AVE_VAL[0]	

8.6.85. VBUS_VAL

VBUS Voltage Measurement Value

Command Code: 5Ch

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VBUS_VAL[14]	VBUS Voltage Measurement Value 0 mV to 25,600 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 25,600 mV.
13	VBUS_VAL[13]	
12	VBUS_VAL[12]	
11	VBUS_VAL[11]	
10	VBUS_VAL[10]	
9	VBUS_VAL[9]	
8	VBUS_VAL[8]	
7	VBUS_VAL[7]	
6	VBUS_VAL[6]	
5	VBUS_VAL[5]	
4	VBUS_VAL[4]	
3	VBUS_VAL[3]	
2	VBUS_VAL[2]	
1	VBUS_VAL[1]	
0	VBUS_VAL[0]	

8.6.86. VBUS_AVE_VAL

VBUS Voltage Measurement Average Value

Command Code: 5Dh

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VBUS_AVE_VAL[14]	VBUS Voltage Measurement Average Value 0 mV to 25,600 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 25,600 mV.
13	VBUS_AVE_VAL[13]	
12	VBUS_AVE_VAL[12]	
11	VBUS_AVE_VAL[11]	
10	VBUS_AVE_VAL[10]	
9	VBUS_AVE_VAL[9]	
8	VBUS_AVE_VAL[8]	
7	VBUS_AVE_VAL[7]	
6	VBUS_AVE_VAL[6]	
5	VBUS_AVE_VAL[5]	
4	VBUS_AVE_VAL[4]	
3	VBUS_AVE_VAL[3]	
2	VBUS_AVE_VAL[2]	
1	VBUS_AVE_VAL[1]	
0	VBUS_AVE_VAL[0]	

8.6.87. VCC_VAL

VCC Voltage Measurement Value

Command Code: 5Eh

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VCC_VAL[14]	VCC Voltage Measurement Value 0 mV to 25,600 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 25,600 mV.
13	VCC_VAL[13]	
12	VCC_VAL[12]	
11	VCC_VAL[11]	
10	VCC_VAL[10]	
9	VCC_VAL[9]	
8	VCC_VAL[8]	
7	VCC_VAL[7]	
6	VCC_VAL[6]	
5	VCC_VAL[5]	
4	VCC_VAL[4]	
3	VCC_VAL[3]	
2	VCC_VAL[2]	
1	VCC_VAL[1]	
0	VCC_VAL[0]	

8.6.88. VCC_AVE_VAL

VCC Voltage Measurement Average Value

Command Code: 5Fh

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VCC_AVE_VAL[14]	VCC Voltage Measurement Average Value 0 mV to 25,600 mV, 1 mV steps. The register range: 0 mV to 32,767 mV. But the actual range: 0 mV to 25,600 mV.
13	VCC_AVE_VAL[13]	
12	VCC_AVE_VAL[12]	
11	VCC_AVE_VAL[11]	
10	VCC_AVE_VAL[10]	
9	VCC_AVE_VAL[9]	
8	VCC_AVE_VAL[8]	
7	VCC_AVE_VAL[7]	
6	VCC_AVE_VAL[6]	
5	VCC_AVE_VAL[5]	
4	VCC_AVE_VAL[4]	
3	VCC_AVE_VAL[3]	
2	VCC_AVE_VAL[2]	
1	VCC_AVE_VAL[1]	
0	VCC_AVE_VAL[0]	

8.6.89. VSYS_VAL

VSYS Voltage Measurement Value

Command Code: 60h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VSYS_VAL[14]	VSYS Voltage Measurement Value 0 mV to 19,200 mV, 1 mV steps. The register range: 0 mV to 32,752 mV. But the actual range: 0 mV to 19,200 mV.
13	VSYS_VAL[13]	
12	VSYS_VAL[12]	
11	VSYS_VAL[11]	
10	VSYS_VAL[10]	
9	VSYS_VAL[9]	
8	VSYS_VAL[8]	
7	VSYS_VAL[7]	
6	VSYS_VAL[6]	
5	VSYS_VAL[5]	
4	VSYS_VAL[4]	
3	VSYS_VAL[3]	
2	VSYS_VAL[2]	
1	VSYS_VAL[1]	
0	VSYS_VAL[0]	

8.6.90. VSYS_AVE_VAL

VSYS Voltage Measurement Average Value

Command Code: 61h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	VSYS_AVE_VAL[14]	VSYS Voltage Measurement Average Value 0 mV to 19,200 mV, 1 mV steps. The register range: 0 mV to 32,752 mV. But the actual range: 0 mV to 19,200 mV.
13	VSYS_AVE_VAL[13]	
12	VSYS_AVE_VAL[12]	
11	VSYS_AVE_VAL[11]	
10	VSYS_AVE_VAL[10]	
9	VSYS_AVE_VAL[9]	
8	VSYS_AVE_VAL[8]	
7	VSYS_AVE_VAL[7]	
6	VSYS_AVE_VAL[6]	
5	VSYS_AVE_VAL[5]	
4	VSYS_AVE_VAL[4]	
3	VSYS_AVE_VAL[3]	
2	VSYS_AVE_VAL[2]	
1	VSYS_AVE_VAL[1]	
0	VSYS_AVE_VAL[0]	

8.6.91. EXTIADP_VAL

IADP (Input current limit setting pin) Voltage Measurement Value

Command Code: 62h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	EXTIADP_VAL[11]	IADP (Input current limit setting pin) voltage Measurement Value (for Debug use)
10	EXTIADP_VAL[10]	
9	EXTIADP_VAL[9]	
8	EXTIADP_VAL[8]	
7	EXTIADP_VAL[7]	
6	EXTIADP_VAL[6]	
5	EXTIADP_VAL[5]	
4	EXTIADP_VAL[4]	
3	EXTIADP_VAL[3]	
2	EXTIADP_VAL[2]	
1	EXTIADP_VAL[1]	
0	EXTIADP_VAL[0]	

8.6.92. EXTIADP_AVE_VAL

IADP (Input current limit setting pin) Voltage Measurement Average Value

Command Code: 63h

Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	EXTIADP_AVE_VAL[11]	IADP (Input current limit setting pin) voltage Measurement Average Value (for Debug use)
10	EXTIADP_AVE_VAL[10]	
9	EXTIADP_AVE_VAL[9]	
8	EXTIADP_AVE_VAL[8]	
7	EXTIADP_AVE_VAL[7]	
6	EXTIADP_AVE_VAL[6]	
5	EXTIADP_AVE_VAL[5]	
4	EXTIADP_AVE_VAL[4]	
3	EXTIADP_AVE_VAL[3]	
2	EXTIADP_AVE_VAL[2]	
1	EXTIADP_AVE_VAL[1]	
0	EXTIADP_AVE_VAL[0]	

8.6.93. VACPCLPS_TH_SET

VACP Collapse Detect Threshold Voltage Setting

Command Code: 64h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	VACPCLPS_TH_SET[14]	VACP Anti-collapse entry voltage threshold. 3,840 mV to 32,640 mV, 128 mV steps. The register range: 0 mV to 32,640 mV. But the actual range: 3,840 mV to 25,088 mV. "00h" setting disables VACP collapse detection.
13	VACPCLPS_TH_SET[13]	
12	VACPCLPS_TH_SET[12]	
11	VACPCLPS_TH_SET[11]	
10	VACPCLPS_TH_SET[10]	
9	VACPCLPS_TH_SET[9]	
8	VACPCLPS_TH_SET[8]	
7	VACPCLPS_TH_SET[7]	
6	reserved	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	reserved	

8.6.94. INT0_SET

1st Level Interrupt Setting

Command Code: 68h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	INT7_EN	2nd Level Interrupt 7 (SAR-ADC) Enable. "1": Enable / "0": Disable.
6	INT6_EN	2nd Level Interrupt 6 (Charger) Enable. "1": Enable / "0": Disable.
5	INT5_EN	2nd Level Interrupt 5 (Charger) Enable. "1": Enable / "0": Disable.
4	INT4_EN	2nd Level Interrupt 4 (VSYS) Enable. "1": Enable / "0": Disable.
3	INT3_EN	2nd Level Interrupt 3 (Battery) Enable. "1": Enable / "0": Disable.
2	INT2_EN	2nd Level Interrupt 2 (VCC) Enable. "1": Enable / "0": Disable.
1	INT1_EN	2nd Level Interrupt 1 (VBUS) Enable. "1": Enable / "0": Disable.
0	INT0_EN	1st Level Interrupt Enable. "1": Enable / "0": Disable.

8.6.95. INT1_SET

2nd Level Interrupt Setting 1 (VBUS)

Command Code: 69h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	VBUS_RBUV_DET	Enabling interrupt of entering to VBUS reverse buck boost voltage low. "1": Enable / "0": Disable.
14	VBUS_RBUV_RES	Enabling interrupt of exit from VBUS reverse buck boost voltage low. "1": Enable / "0": Disable.
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VBUS_TH_DET	Enabling interrupt VBUS Voltage > VBUS_TH_SET. "1": Enable / "0": Disable.
8	VBUS_TH_RES	Enabling interrupt VBUS Voltage $\leq$ VBUS_TH_SET. "1": Enable / "0": Disable.
7	reserved	
6	VBUS_IIN_MOD	Enabling interrupt of VBUS input current-limit modified. "1": Enable / "0": Disable.
5	VBUS_OV_DET	Enabling interrupt of VBUS over voltage detected. "1": Enable / "0": Disable.
4	VBUS_OV_RES	Enabling interrupt of VBUS over voltage resumed "1": Enable / "0": Disable.
3	VBUS_CLPS_DET	Enabling interrupt of entering to VBUS Anti-collapse operation. "1": Enable / "0": Disable.
2	VBUS_CLPS RES	Enabling interrupt of exit from VBUS Anti-collapse operation. "1": Enable / "0": Disable.
1	VBUS_DET	Enabling interrupt of VBUS detect. "1": Enable / "0": Disable.
0	VBUS_RES	Enabling interrupt of VBUS removal. "1": Enable / "0": Disable.

8.6.96. INT2_SET

2nd Level Interrupt Setting 2 (VCC)

Command Code: 6Ah

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	VCC_RBUV_DET	Enabling interrupt of entering to VCC reverse buck boost voltage low. "1": Enable / "0": Disable.
14	VCC_RBUV_RES	Enabling interrupt of exit from VCC reverse buck boost voltage low. "1": Enable / "0": Disable.
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VCC_TH_DET	Interrupt VCC Voltage > VCC_TH_SET. "1": Enable / "0": Disable.
8	VCC_TH_RES	Interrupt VCC Voltage ≤ VCC_TH_SET. "1": Enable / "0": Disable.
7	reserved	
6	VCC_IIN_MOD	Interrupt of VCC/VACP input current-limit modified. "1": Enable / "0": Disable. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
5	VCC_OVP_DET	Interrupt of VCC over voltage detected. "1": Enable / "0": Disable.
4	VCC_OVP_RES	Interrupt of VCC over voltage resumed "1": Enable / "0": Disable.
3	VCC_CLPS_DET	Interrupt of entering to VCC/VACP Anti-collapse operation. "1": Enable / "0": Disable. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
2	VCC_CLPS_RES	Interrupt of exit from VCC/VACP Anti-collapse operation. "1": Enable / "0": Disable. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
1	VCC_DET	Interrupt of VCC detect. "1": Enable / "0": Disable.
0	VCC_RES	Interrupt of VCC removal. "1": Enable / "0": Disable.

8.6.97. INT3_SET

2nd Level Interrupt Setting 3 (Battery)

Command Code: 6Bh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TH_DET	Interrupt of the thermistor detected. "1": Enable / "0": Disable.
14	TH_RMV	Interrupt of the thermistor removal. "1": Enable / "0": Disable.
13	reserved	
12	reserved	
11	TMP_OUT_DET	Interrupt of the thermistor out of the charging range. "1": Enable / "0": Disable.
10	TMP_OUT_RES	Interrupt of the thermistor in to the charging range. "1": Enable / "0": Disable.
9	VBAT_TH_DET	Interrupt VBATT Voltage > VBAT_TH_SET. "1": Enable / "0": Disable.
8	VBAT_TH_RES	Interrupt VBATT Voltage ≤ VBAT_TH_SET. "1": Enable / "0": Disable.
7	IBAT_SHORT_DET	Interrupt of Battery over current detected. "1": Enable / "0": Disable.
6	IBAT_SHORT_RES	Interrupt of Battery over current resumed. "1": Enable / "0": Disable.
5	VBAT_OV_DET	Interrupt of VBATT over voltage detected. "1": Enable / "0": Disable.
4	VBAT_OV_RES	Interrupt of VBATT over voltage resumed. "1": Enable / "0": Disable.
3	BAT_ASSIST_DET	Interrupt of Entering to Battery-assist mode. "1": Enable / "0": Disable.
2	BAT_ASSIST_RES	Interrupt of Exiting from Battery-assist mode. "1": Enable / "0": Disable.
1	reserved	
0	reserved	

8.6.98. INT4_SET

2nd Level Interrupt Setting 4 (VSYS)

Command Code: 6Ch

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VSYS_TH_DET	Interrupt VSYS Voltage > VSYS_TH_SET. "1": Enable / "0": Disable.
8	VSYS_TH_RES	Interrupt VSYS Voltage ≤ VSYS_TH_SET. "1": Enable / "0": Disable.
7	reserved	
6	reserved	
5	VSYS_OV_DET	Interrupt of VSYS over voltage detected. "1": Enable / "0": Disable.
4	VSYS_OV_RES	Interrupt of VSYS over voltage resumed. "1": Enable / "0": Disable.
3	VSYS_SHT_DET	Interrupt of VSYS short circuit detected. "1": Enable / "0": Disable.
2	VSYS_SHT_RES	Interrupt of VSYS short circuit resumed. "1": Enable / "0": Disable.
1	VSYS_UV_DET	Interrupt of VSYS under voltage detected. "1": Enable / "0": Disable.
0	VSYS_UV_RES	Interrupt of VSYS under voltage resumed. "1": Enable / "0": Disable.

8.6.99. INT5_SET

2nd Level Interrupt Setting 5 (Charger)

Command Code: 6Dh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	OTP_LOAD_DONE	Interrupt of OTP load done. "1": Enable / "0": Disable.
12	PWR_ON	Interrupt of Power-on. "1": Enable / "0": Disable.
11	EXTIADP_TRNS	Interrupt IADP voltage range transition. "1": Enable / "0": Disable.
10	reserved	
9	EXTIADP_TH_DET	Interrupt IADP (Input current Limit setting pin) voltage > EXTIADP_TH_SET. "1": Enable / "0": Disable.
8	EXTIADP_TH_RES	Interrupt IADP (Input current Limit setting pin) voltage ≤ EXTIADP_TH_SET. "1": Enable / "0": Disable.
7	BAT_MNT_DET	Interrupt of entering to Battery Maintenance charging. "1": Enable / "0": Disable.
6	BAT_MNT_RES	Interrupt of exit from Battery Maintenance charging. "1": Enable / "0": Disable.
5	TSD_DET	Interrupt of the TSD detected. "1": Enable / "0": Disable.
4	TSD_RES	Interrupt of the TSD resumed. "1": Enable / "0": Disable.
3	CHGWDT_EXP	Interrupt of Charger Watchdog Timer expired. "1": Enable / "0": Disable.
2	THERMWDT_EXP	Interrupt of Battery Temperature Watchdog Timer expired. "1": Enable / "0": Disable.
1	TMP_TRNS	Interrupt of the Battery Temperature range transition. "1": Enable / "0": Disable.
0	CHG_TRNS	Interrupt of Charger-State transition. "1": Enable / "0": Disable.

8.6.100. INT6_SET

2nd Level Interrupt Setting 6 (Charger)

Command Code: 6Eh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	VBUS_UCD_PORT_DET	Interrupt of USB Port contact detected on the VBUS side. "1": Enable / "0": Disable.
12	VBUS_UCD_UCHG_DET	Interrupt of USB Charger detected on the VBUS side. "1": Enable / "0": Disable.
11	reserved	
10	VBUS_UCD_OTG_DET	Interrupt of USB OTG device detected on the VBUS side. "1": Enable / "0": Disable.
9	reserved	
8	reserved	
7	reserved	
6	reserved	
5	VCC_UCD_PORT_DET	Interrupt of USB Port contact detected on the VCC side. "1": Enable / "0": Disable.
4	VCC_UCD_UCHG_DET	Interrupt of USB Charger detected on the VCC side. "1": Enable / "0": Disable.
3	reserved	
2	VCC_UCD_OTG_DET	Interrupt of USB OTG device detected on the VCC side. "1": Enable / "0": Disable.
1	reserved	
0	reserved	

8.6.101. INT7_SET

2nd Level Interrupt Setting 7 (SAR and ADC)

Command Code: 6Fh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROCHOT_DET	Interrupt of PROCHOT# asserted. "1": Enable / "0": Disable.
14	PROCHOT_RES	Interrupt of PROCHOT# de-asserted. "1": Enable / "0": Disable.
13	reserved	
12	reserved	
11	VACP_DET	Interrupt of VACP detect. "1": Enable / "0": Disable.
10	VACP_RES	Interrupt of VACP removal. "1": Enable / "0": Disable.
9	VACP_TH_DET	Interrupt Input Voltage (ACP) Voltage > VACP_TH_SET. "1": Enable / "0": Disable.
8	VACP_TH_RES	Interrupt Input Voltage (ACP) Voltage ≤ VACP_TH_SET. "1": Enable / "0": Disable.
7	IACP_TH_DET	Interrupt Input Current (between ACP and ACN) > IACP_TH_SET. "1": Enable / "0": Disable.
6	IACP_TH_RES	Interrupt Input Current (between ACP and ACN) ≤ IACP_TH_SET. "1": Enable / "0": Disable.
5	THERM_TH_DET	Interrupt TSENSE Voltage > THERM_TH_SET. "1": Enable / "0": Disable.
4	THERM_TH_RES	Interrupt TSENSE Voltage ≤ THERM_TH_SET. "1": Enable / "0": Disable.
3	IBATM_TH_DET	Interrupt Battery Current (Dis-charge) > IBATM_TH_SET. "1": Enable / "0": Disable.
2	IBATM_TH_RES	Interrupt Battery Current (Dis-charge) ≤ IBATM_TH_SET. "1": Enable / "0": Disable.
1	IBATP_TH_DET	Interrupt Battery Current (Charge) > IBATP_TH_SET. "1": Enable / "0": Disable.
0	IBATP_TH_RES	Interrupt Battery Current (Charge) ≤ IBATP_TH_SET. "1": Enable / "0": Disable.

8.6.102. INT0_STATUS

1st Level Interrupt Status

Command Code: 70h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	INT7_STATUS	2nd Level Interrupt 7 (SAR-ADC) Status. "1": Event occurred / "0": No event. "1-Write": Status clear.
6	INT6_STATUS	2nd Level Interrupt 6 (Charger) Status. "1": Event occurred / "0": No event. "1-Write": Status clear.
5	INT5_STATUS	2nd Level Interrupt 5 (Charger) Status. "1": Event occurred / "0": No event. "1-Write": Status clear.
4	INT4_STATUS	2nd Level Interrupt 4 (VSYS) Status. "1": Event occurred / "0": No event. "1-Write": Status clear.
3	INT3_STATUS	2nd Level Interrupt 3 (Battery) Status. "1": Event occurred / "0": No event. "1-Write": Status clear.
2	INT2_STATUS	2nd Level Interrupt 2 (VCC) Status. "1": Event occurred / "0": No event. "1-Write": Status clear.
1	INT1_STATUS	2nd Level Interrupt 1 (VBUS) Status. "1": Event occurred / "0": No event. "1-Write": Status clear.
0	INT0_STATUS	1st Level Interrupt Status. "1": Event occurred / "0": No event. "1-Write": Status clear.

8.6.103. INT1_STATUS

2nd Level Interrupt Status 1 (VBUS)

Command Code: 71h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	VBUS_RBUV_DET	Interrupt status of entering to VBUS reverse buck boost voltage low. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
14	VBUS_RBUV_RES	Interrupt status of exit from VBUS reverse buck boost voltage low. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VBUS_TH_DET	Interrupt status VBUS Voltage > VBUS_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
8	VBUS_TH_RES	Interrupt status VBUS Voltage ≤ VBUS_TH_SET. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
7	reserved	
6	VBUS_IIN_MOD	Interrupt status of VBUS input current-limit modified. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
5	VBUS_OV_DET	Interrupt status of VBUS over voltage detected. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
4	VBUS_OV_RES	Interrupt status of VBUS over voltage resumed. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
3	VBUS_CLPS_DET	Interrupt status of entering to VBUS Anti-collapse operation. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
2	VBUS_CLPS_RES	Interrupt status of exit from VBUS Anti-collapse operation. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
1	VBUS_DET	Interrupt status of VBUS detect. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.
0	VBUS_RES	Interrupt status of VBUS removal. “1”: Event occurred / “0”: No event. “1-Write”: Status clear.

8.6.104. INT2_STATUS

2nd Level Interrupt Status 2 (VCC)

Command Code: 72h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	VCC_RBUV_DET	Interrupt status of entering to VCC reverse buck boost voltage low. "1": Event occurred / "0": No event. "1-Write": Status clear.
14	VCC_RBUV_RES	Interrupt status of exit from VCC reverse buck boost voltage low. "1": Event occurred / "0": No event. "1-Write": Status clear.
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VCC_TH_DET	Interrupt status VCC Voltage > VCC_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
8	VCC_TH_RES	Interrupt status VCC Voltage ≤ VCC_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
7	reserved	
6	VCC_IIN_MOD	Interrupt status of VCC/VACP input current-limit modified. "1": Event occurred / "0": No event. "1-Write": Status clear. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
5	VCC_OVP_DET	Interrupt status of VCC over voltage detected. "1": Event occurred / "0": No event. "1-Write": Status clear.
4	VCC_OVP_RES	Interrupt status of VCC over voltage resumed. "1": Event occurred / "0": No event. "1-Write": Status clear.
3	VCC_CLPS_DET	Interrupt status of entering to VCC/VACP Anti-collapse operation. "1": Event occurred / "0": No event. "1-Write": Status clear. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
2	VCC_CLPS_RES	Interrupt status of exit from VCC/VACP Anti-collapse operation. "1": Event occurred / "0": No event. "1-Write": Status clear. (VACP-input is enabled when VCC_EN=VBUS_EN=0/ VCC-input is enabled when VCC_EN=1)
1	VCC_DET	Interrupt status of VCC detect. "1": Event occurred / "0": No event. "1-Write": Status clear.
0	VCC_RES	Interrupt status of VCC removal. "1": Event occurred / "0": No event. "1-Write": Status clear.

8.6.105. INT3_STATUS

2nd Level Interrupt Status 3 (Battery)

Command Code: 73h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	TH_DET	Interrupt status of the thermistor detected. "1": Event occurred / "0": No event. "1-Write": Status clear.
14	TH_RMV	Interrupt status of the thermistor removal. "1": Event occurred / "0": No event. "1-Write": Status clear.
13	reserved	
12	reserved	
11	TMP_OUT_DET	Interrupt status of the thermistor out of the charging range. "1": Event occurred / "0": No event. "1-Write": Status clear.
10	TMP_OUT_RES	Interrupt status of the thermistor in to the charging range. "1": Event occurred / "0": No event. "1-Write": Status clear.
9	VBAT_TH_DET	Interrupt status VBAT Voltage > VBAT_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
8	VBAT_TH_RES	Interrupt status VBAT Voltage ≤ VBAT_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
7	IBAT_SHORT_DET	Interrupt status of Battery over current detected. "1": Event occurred / "0": No event. "1-Write": Status clear.
6	IBAT_SHORT_RES	Interrupt status of Battery over current resumed. "1": Event occurred / "0": No event. "1-Write": Status clear.
5	VBAT_OV_DET	Interrupt status of VBAT over voltage detected. "1": Event occurred / "0": No event. "1-Write": Status clear.
4	VBAT_OV_RES	Interrupt status of VBAT over voltage resumed. "1": Event occurred / "0": No event. "1-Write": Status clear.
3	BAT_ASSIST_DET	Interrupt status of Entering to Battery-assist mode. "1": Event occurred / "0": No event. "1-Write": Status clear.
2	BAT_ASSIST_RES	Interrupt status of Exiting from Battery-assist mode. "1": Event occurred / "0": No event. "1-Write": Status clear.
1	reserved	
0	reserved	

8.6.106. INT4_STATUS

2nd Level Interrupt Status 4 (VSYS)

Command Code: 74h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	VSYS_TH_DET	Interrupt status VSYS Voltage > VSYS_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
8	VSYS_TH_RES	Interrupt status VSYS Voltage ≤ VSYS_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
7	reserved	
6	reserved	
5	VSYS_OV_DET	Interrupt status of VSYS over voltage detected. "1": Event occurred / "0": No event. "1-Write": Status clear.
4	VSYS_OV_RES	Interrupt status of VSYS over voltage resumed. "1": Event occurred / "0": No event. "1-Write": Status clear.
3	VSYS_SHT_DET	Interrupt status of VSYS short circuit detected. "1": Event occurred / "0": No event. "1-Write": Status clear.
2	VSYS_SHT_RES	Interrupt status of VSYS short circuit resumed. "1": Event occurred / "0": No event. "1-Write": Status clear.
1	VSYS_UV_DET	Interrupt status of VSYS under voltage detected. "1": Event occurred / "0": No event. "1-Write": Status clear.
0	VSYS_UV_RES	Interrupt status of VSYS under voltage resumed. "1": Event occurred / "0": No event. "1-Write": Status clear.

8.6.107. INT5_STATUS

2nd Level Interrupt Status 5 (Charger)

Command Code: 75h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	OTP_LOAD_DONE	Interrupt status of OTP load done. "1": Event occurred / "0": No event. "1-Write": Status clear.
12	PWR_ON	Interrupt status of Power-on. "1": Event occurred / "0": No event. "1-Write": Status clear.
11	EXTIADP_TRNS	Interrupt status of IADP voltage range transition. "1": Event occurred / "0": No event. "1-Write": Status clear.
10	reserved	
9	EXTIADP_TH_DET	Interrupt status of IADP (Input current Limit setting pin) voltage > EXTIADP_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
8	EXTIADP_TH_RES	Interrupt status of IADP (Input current Limit setting pin) voltage ≤ EXTIADP_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
7	BAT_MNT_DET	Interrupt status of entering to Battery Maintenance charging. "1": Event occurred / "0": No event. "1-Write": Status clear.
6	BAT_MNT_RES	Interrupt status of exit from Battery Maintenance charging. "1": Event occurred / "0": No event. "1-Write": Status clear.
5	TSD_DET	Interrupt status of the TSD detected. "1": Event occurred / "0": No event. "1-Write": Status clear.
4	TSD_RES	Interrupt status of the TSD resumed. "1": Event occurred / "0": No event. "1-Write": Status clear.
3	CHGWDT_EXP	Interrupt status of Charger Watchdog Timer expired. "1": Event occurred / "0": No event. "1-Write": Status clear.
2	THERMWDT_EXP	Interrupt status of Battery Temperature Watchdog Timer expired. "1": Event occurred / "0": No event. "1-Write": Status clear.
1	TMP_TRNS	Interrupt status of Temperature range transition. "1": Event occurred / "0": No event. "1-Write": Status clear.
0	CHG_TRNS	Interrupt status of Charger-State transition. "1": Event occurred / "0": No event. "1-Write": Status clear.

8.6.108. INT6_STATUS

2nd Level Interrupt Status 6 (Charger)

Command Code: 76h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	VBUS_UCD_PORT_DET	Interrupt status of USB Port contact detected on the VBUS side. "1": Event occurred / "0": No event. "1-Write": Status clear.
12	VBUS_UCD_UCHG_DET	Interrupt status of USB Charger detected on the VBUS side. "1": Event occurred / "0": No event. "1-Write": Status clear.
11	reserved	
10	VBUS_UCD_OTG_DET	Interrupt status of USB OTG device detected on the VBUS side. "1": Event occurred / "0": No event. "1-Write": Status clear.
9	reserved	
8	reserved	
7	reserved	
6	reserved	
5	VCC_UCD_PORT_DET	Interrupt status of USB Port contact detected on the VCC side. "1": Event occurred / "0": No event. "1-Write": Status clear.
4	VCC_UCD_UCHG_DET	Interrupt status of USB Charger detected on the VCC side. "1": Event occurred / "0": No event. "1-Write": Status clear.
3	reserved	
2	VCC_UCD_OTG_DET	Interrupt status of USB OTG device detected on the VCC side. "1": Event occurred / "0": No event. "1-Write": Status clear.
1	reserved	
0	reserved	

8.6.109. INT7_STATUS

2nd Level Interrupt Status 7 (SAR and ADC)

Command Code: 77h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROCHOT_DET	Interrupt status of PROCHOT# asserted. "1": Event occurred / "0": No event. "1-Write": Status clear.
14	PROCHOT_RES	Interrupt status of PROCHOT# de-asserted. "1": Event occurred / "0": No event. "1-Write": Status clear.
13	reserved	
12	reserved	
11	VACP_DET	Interrupt status of VACP detect. "1": Event occurred / "0": No event. "1-Write": Status clear.
10	VACP_RES	Interrupt status of VACP removal. "1": Event occurred / "0": No event. "1-Write": Status clear.
9	VACP_TH_DET	Interrupt status Input Voltage (ACP) Voltage > VADP_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
8	VACP_TH_RES	Interrupt status Input Voltage (ACP) Voltage ≤ VADP_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
7	IACP_TH_DET	Interrupt status Input Current (between ACP and ACN) > IADP_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
6	IACP_TH_RES	Interrupt status Input Current (between ACP and ACN) ≤ IADP_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
5	THERM_TH_DET	Interrupt status TSENSE Voltage > THERM_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
4	THERM_TH_RES	Interrupt status TSENSE Voltage ≤ THERM_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
3	IBATM_TH_DET	Interrupt status Battery Current (Dis-charge) > IBATM_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
2	IBATM_TH_RES	Interrupt status Battery Current (Dis-charge) ≤ IBATM_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
1	IBATP_TH_DET	Interrupt status Battery Current (Charge) > IBATP_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.
0	IBATP_TH_RES	Interrupt status Battery Current (Charge) ≤ IBATP_TH_SET. "1": Event occurred / "0": No event. "1-Write": Status clear.

8.6.110. REG0

Reserved Register 0 (for future use)

Command Code: 78h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	RESERVE_REG0[15]	Reserved Register 0 (for future use)
14	RESERVE_REG0[14]	
13	RESERVE_REG0[13]	
12	RESERVE_REG0[12]	
11	RESERVE_REG0[11]	
10	RESERVE_REG0[10]	
9	RESERVE_REG0[9]	
8	RESERVE_REG0[8]	
7	RESERVE_REG0[7]	
6	RESERVE_REG0[6]	
5	RESERVE_REG0[5]	
4	RESERVE_REG0[4]	
3	RESERVE_REG0[3]	
2	RESERVE_REG0[2]	
1	RESERVE_REG0[1]	
0	RESERVE_REG0[0]	

8.6.111. REG1

Reserved Register 1 (for future use)

Command Code: 79h

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	RESERVE_REG1[15]	Reserved Register 1 (for future use)
14	RESERVE_REG1[14]	
13	RESERVE_REG1[13]	
12	RESERVE_REG1[12]	
11	RESERVE_REG1[11]	
10	RESERVE_REG1[10]	
9	RESERVE_REG1[9]	
8	RESERVE_REG1[8]	
7	RESERVE_REG1[7]	
6	RESERVE_REG1[6]	
5	RESERVE_REG1[5]	
4	RESERVE_REG1[4]	
3	RESERVE_REG1[3]	
2	RESERVE_REG1[2]	
1	RESERVE_REG1[1]	
0	RESERVE_REG1[0]	

8.6.112. OTPREG0

Input current limit degradation setting. For details, please see 8.6.6. CUR_ILIM_VAL.

Command Code: 7Ah

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	RESERVE_OTPREG0[15]	Reserved OTP-loaded Register 0 (for future use)
14	RESERVE_OTPREG0[14]	
13	RESERVE_OTPREG0[13]	
12	RESERVE_OTPREG0[12]	
11	ILIM_DECREASE[11]	Input current limit degradation setting when anti-collapse occurs.
10	ILIM_DECREASE[10]	
9	ILIM_DECREASE[9]	
8	ILIM_DECREASE[8]	
7	ILIM_DECREASE[7]	
6	ILIM_DECREASE[6]	
5	ILIM_DECREASE[5]	
4	ILIM_DECREASE[4]	
3	ILIM_DECREASE[3]	
2	ILIM_DECREASE[2]	
1	ILIM_DECREASE[1]	
0	ILIM_DECREASE[0]	

8.6.113. OTPREG1

Reserved OTP-loaded Register 1 (for future use)

Command Code: 7Bh

Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	RESERVE_OTPREG1[15]	Reserved OTP-loaded Register 1 (for future use)
14	RESERVE_OTPREG1[14]	
13	RESERVE_OTPREG1[13]	
12	RESERVE_OTPREG1[12]	
11	RESERVE_OTPREG1[11]	
10	RESERVE_OTPREG1[10]	
9	RESERVE_OTPREG1[9]	
8	RESERVE_OTPREG1[8]	
7	RESERVE_OTPREG1[7]	
6	RESERVE_OTPREG1[6]	
5	RESERVE_OTPREG1[5]	
4	RESERVE_OTPREG1[4]	
3	RESERVE_OTPREG1[3]	
2	RESERVE_OTPREG1[2]	
1	RESERVE_OTPREG1[1]	
0	RESERVE_OTPREG1[0]	

8.6.114. SMBREG

Power Save Mode Setting.

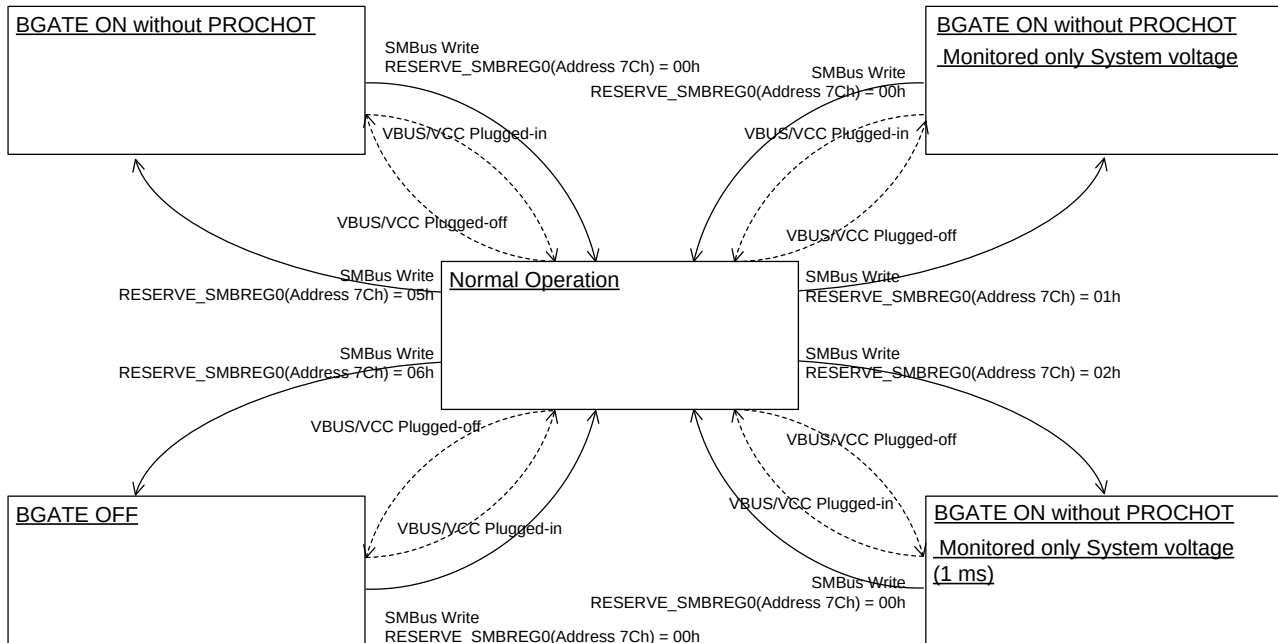
Command Code: 7Ch

Bus Protocol: Read/Write Word

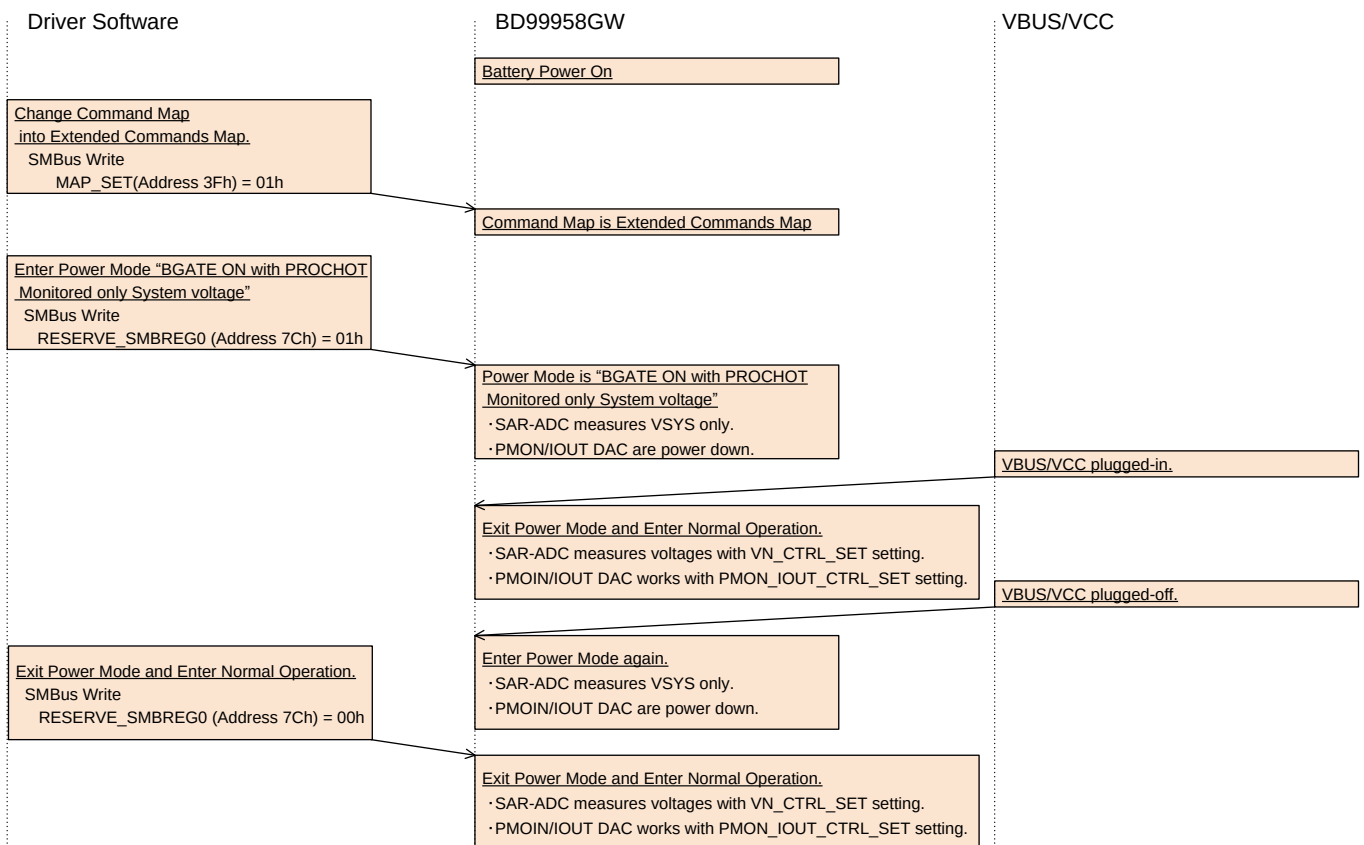
Bit	Symbol	Description
15	SMBREG[15]	Reserved SMBus Clock Domain Register (for future use)
14	SMBREG[14]	
13	SMBREG[13]	
12	SMBREG[12]	
11	SMBREG[11]	
10	SMBREG[10]	
9	SMBREG[9]	
8	SMBREG[8]	
7	SMBREG[7]	
6	SMBREG[6]	
5	SMBREG[5]	
4	SMBREG[4]	
3	SMBREG[3]	
2	POWER_SAVE_MODE[2]	Power Save Mode Setting. 0h: Normal Operation 1h: BGATE ON with PROCHOT# Monitored only System voltage 2h: BGATE ON with PROCHOT# Monitored only System voltage (1 ms) 5h: BGATE ON without PROCHOT# 6h: BGATE OFF Other: reserved.
1	POWER_SAVE_MODE[1]	
0	POWER_SAVE_MODE[0]	

8.6.114. SMBREG - continued

BD99958GW enters into 4 power modes by SMBus writing RESERVE_SMBREG0SMBREG. POWER_SAVE_MODE[2:0] register.
 And BD99958GW exits from a power mode by SMBus clearing RESERVE_SMBREG0SMBREG. POWER_SAVE_MODE[2:0] register.
 If BD99958GW is in a power mode, BD99958GW exits from power mode automatically by VBUS/VCC plugged-in and goes back to power mode automatically by VBUS/VCC plugged-off.

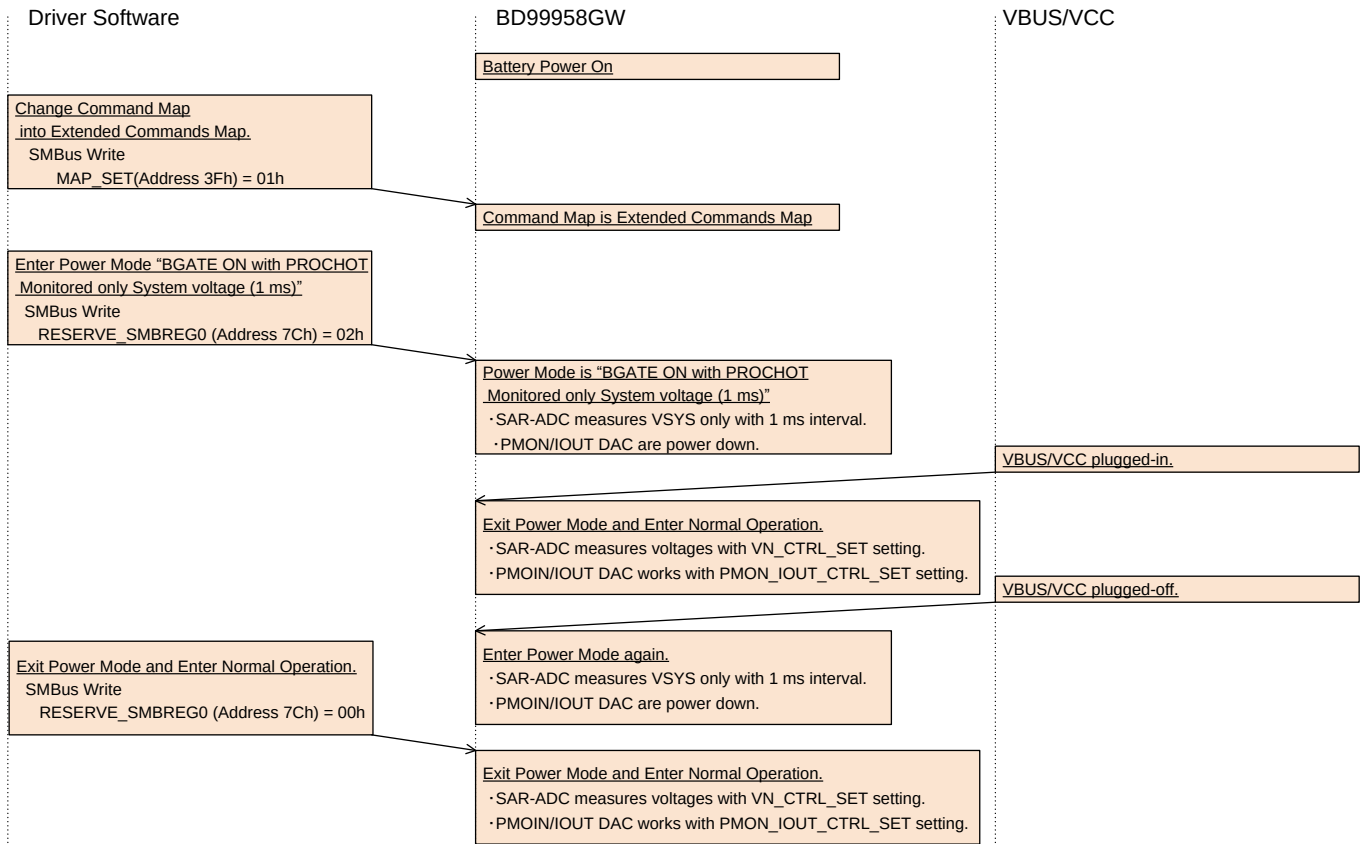


POWER_SAVE_MODE[2:0]=1h: (BGATE ON with PROCHOT# Monitored only System voltage) sample operation flow.



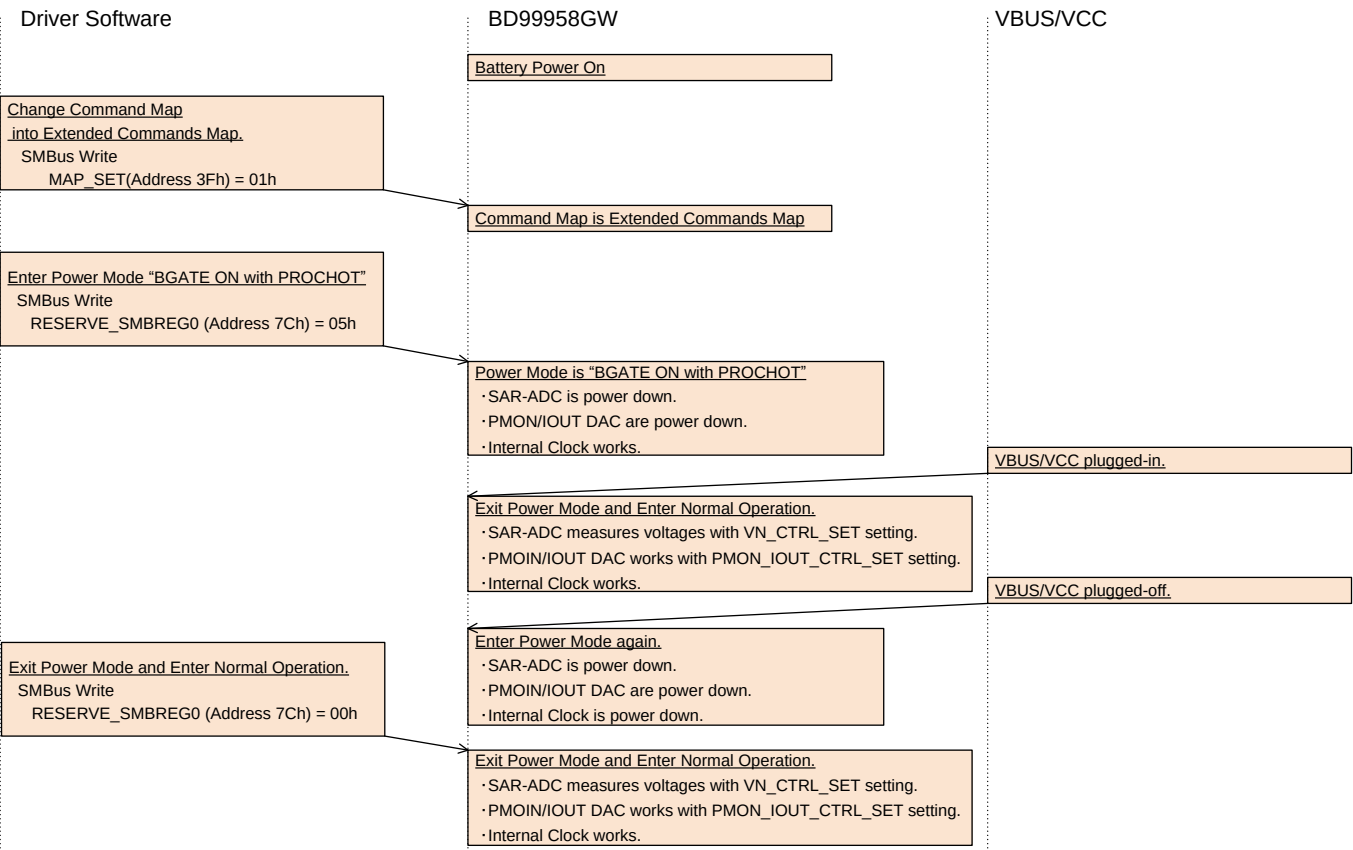
8.6.114. SMBREG - continued

POWER_SAVE_MODE[2:0] = 2h: BGATE ON with PROCHOT# Monitored only System voltage (1 ms interval) sample operation flow.



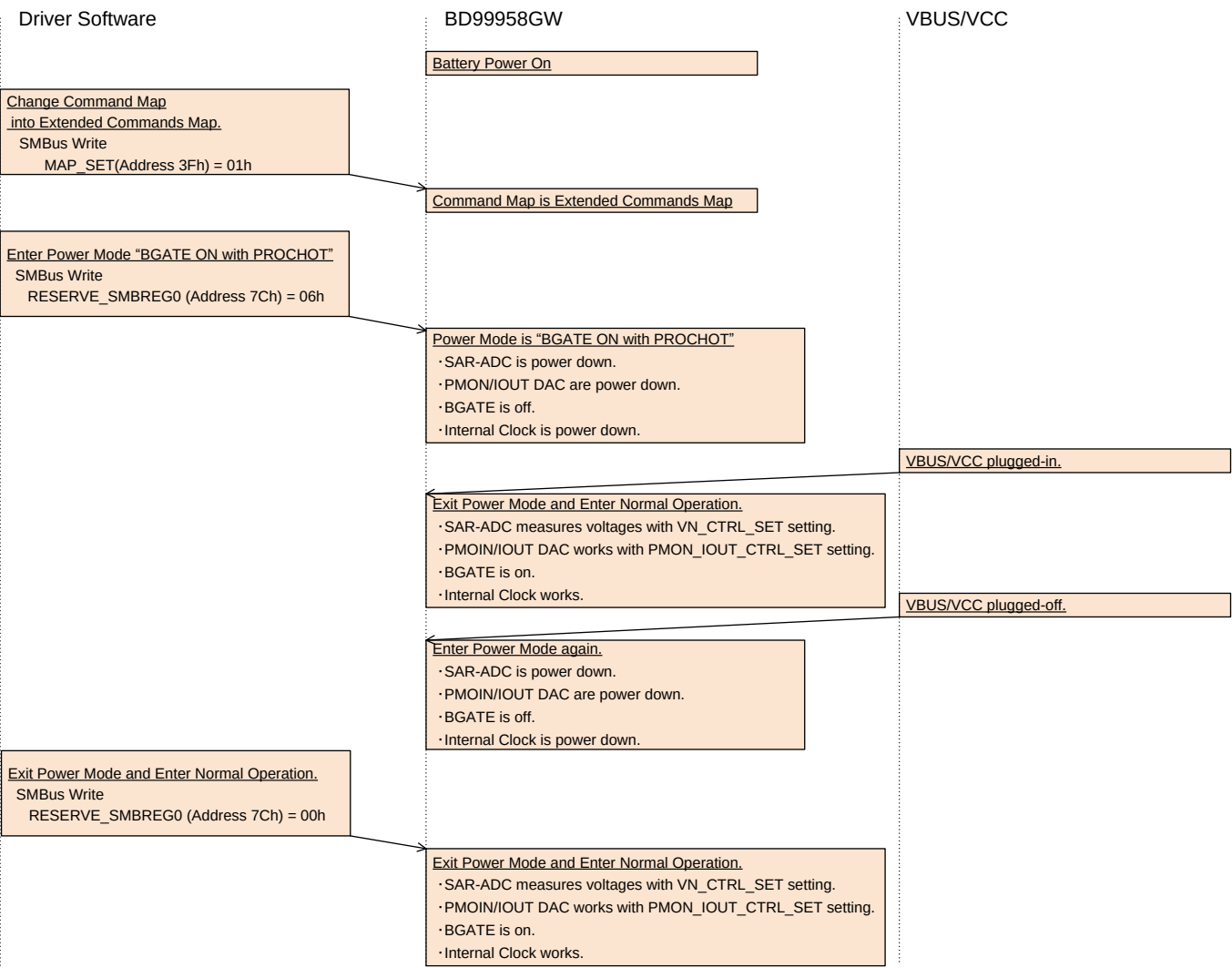
8.6.114. SMBREG - continued

POWER_SAVE_MODE[2:0]=5h: BGATE ON without PROCHOT# sample operation flow.



8.6.114. SMBREG - continued

POWER_SAVE_MODE[2:0]=6h: BGATE OFF sample operation flow.



8.6.115. DEBUG_MODE_SET

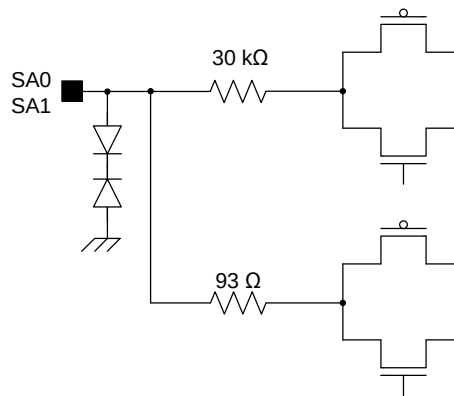
Debug Mode Setting

Command Code: 7Fh
Bus Protocol: Read/Write Word

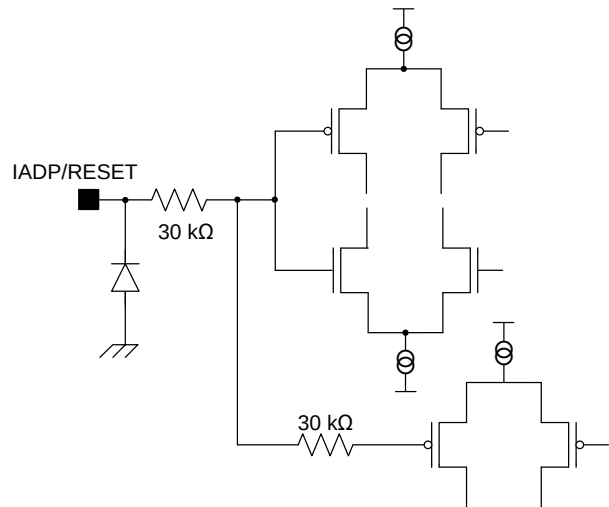
Bit	Symbol	Description
15	DEBUG_MODE_SET[15]	Debug Mode Setting
14	DEBUG_MODE_SET[14]	
13	DEBUG_MODE_SET[13]	
12	DEBUG_MODE_SET[12]	
11	DEBUG_MODE_SET[11]	
10	DEBUG_MODE_SET[10]	
9	DEBUG_MODE_SET[9]	
8	DEBUG_MODE_SET[8]	
7	DEBUG_MODE_SET[7]	
6	DEBUG_MODE_SET[6]	
5	DEBUG_MODE_SET[5]	
4	DEBUG_MODE_SET[4]	
3	DEBUG_MODE_SET[3]	
2	DEBUG_MODE_SET[2]	
1	DEBUG_MODE_SET[1]	
0	DEBUG_MODE_SET[0]	

9. I/O Equivalence Circuit

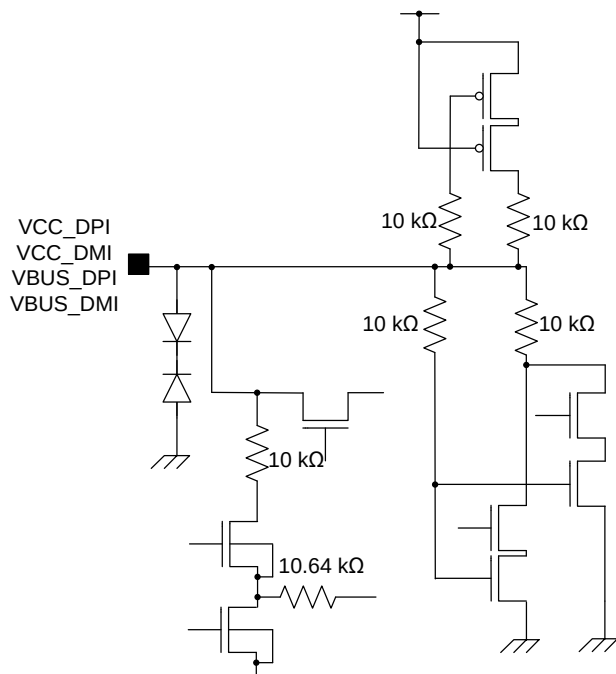
SA0, SA1



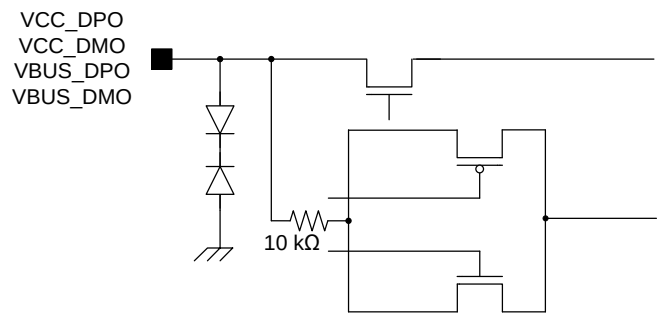
IADP/RESET



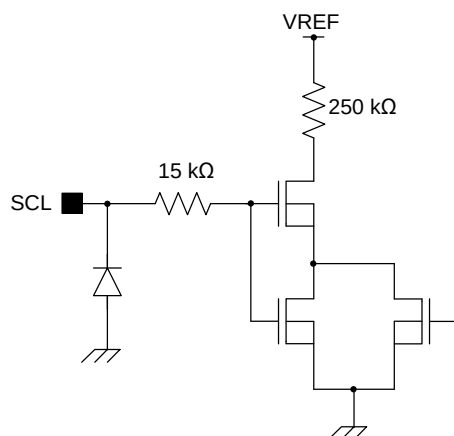
VCC_DPI, VCC_DMI, VBUS_DPI, VBUS_DMI



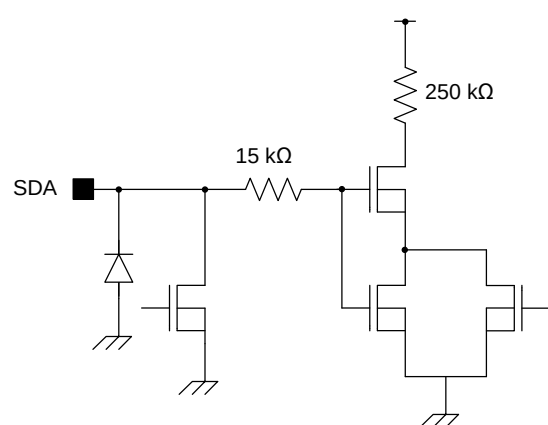
VCC_DPO, VCC_DMO, VBUS_DPO, VBUS_DMO



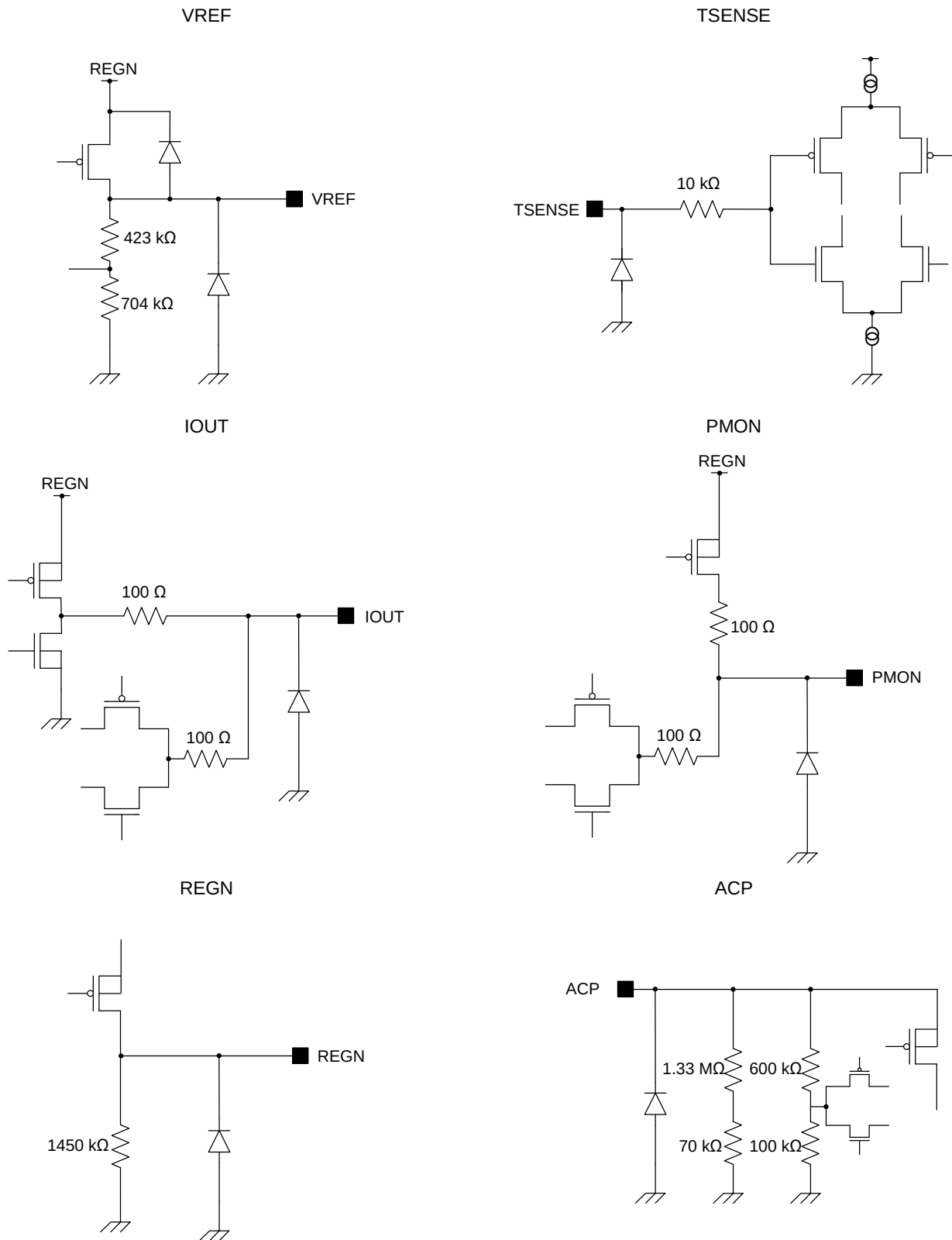
SCL



SDA

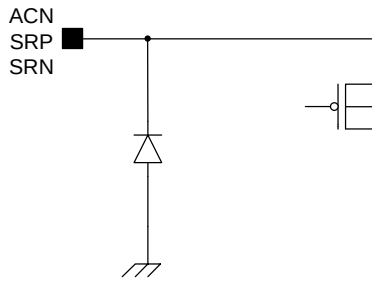


9. I/O Equivalence Circuit - continued

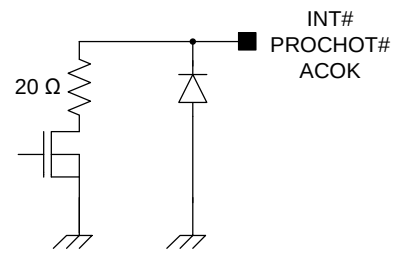


9. I/O Equivalence Circuit - continued

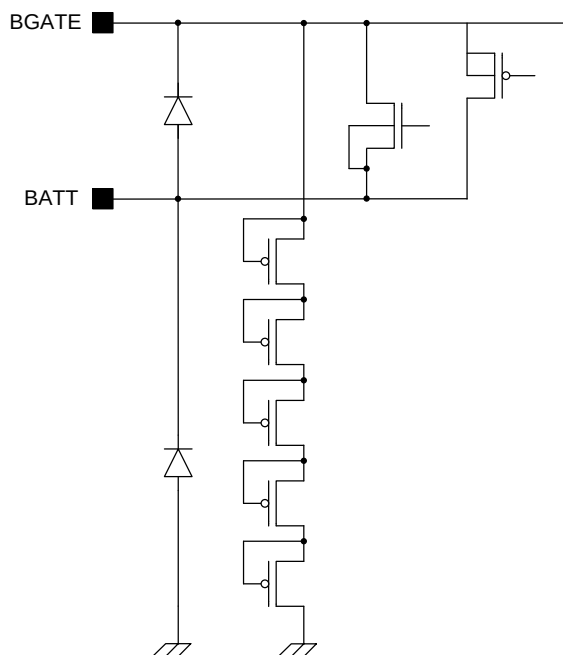
ACN, SRP, SRN



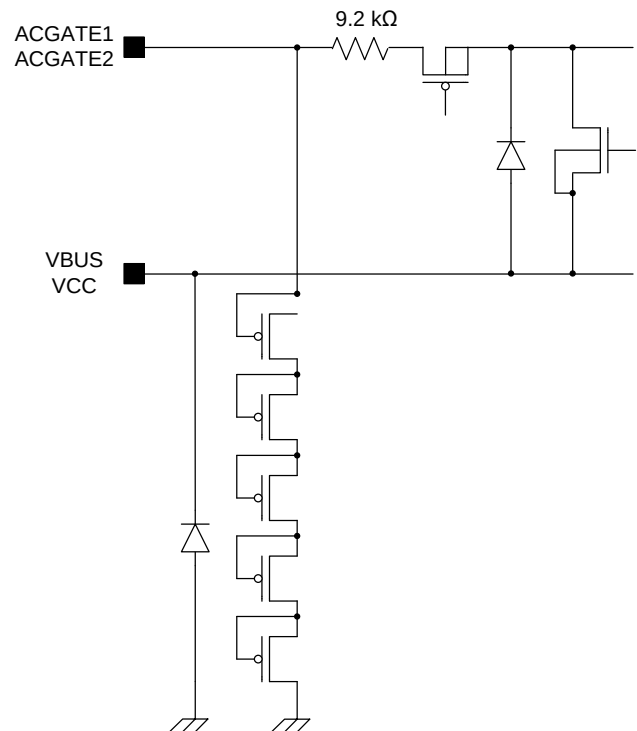
INT#, PROCHOT#, ACOK



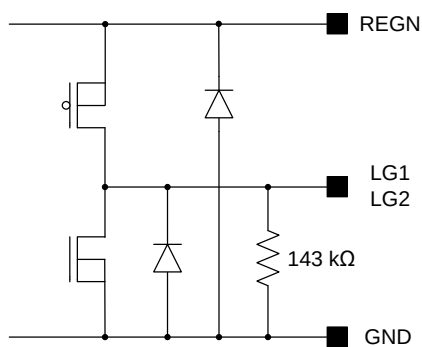
BGATE, BATT



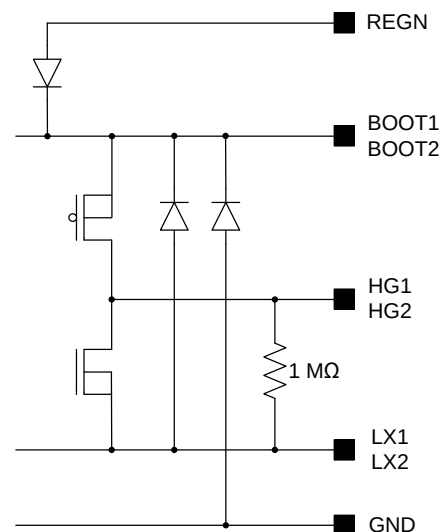
ACGATE1, ACGATE2, VBUS, VCC



LG1, LG2



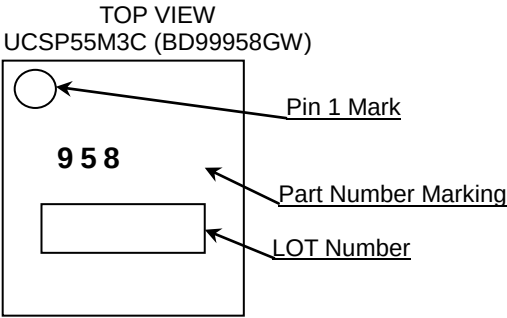
BOOT1, BOOT2, HG1, HG2, LX1, LX2



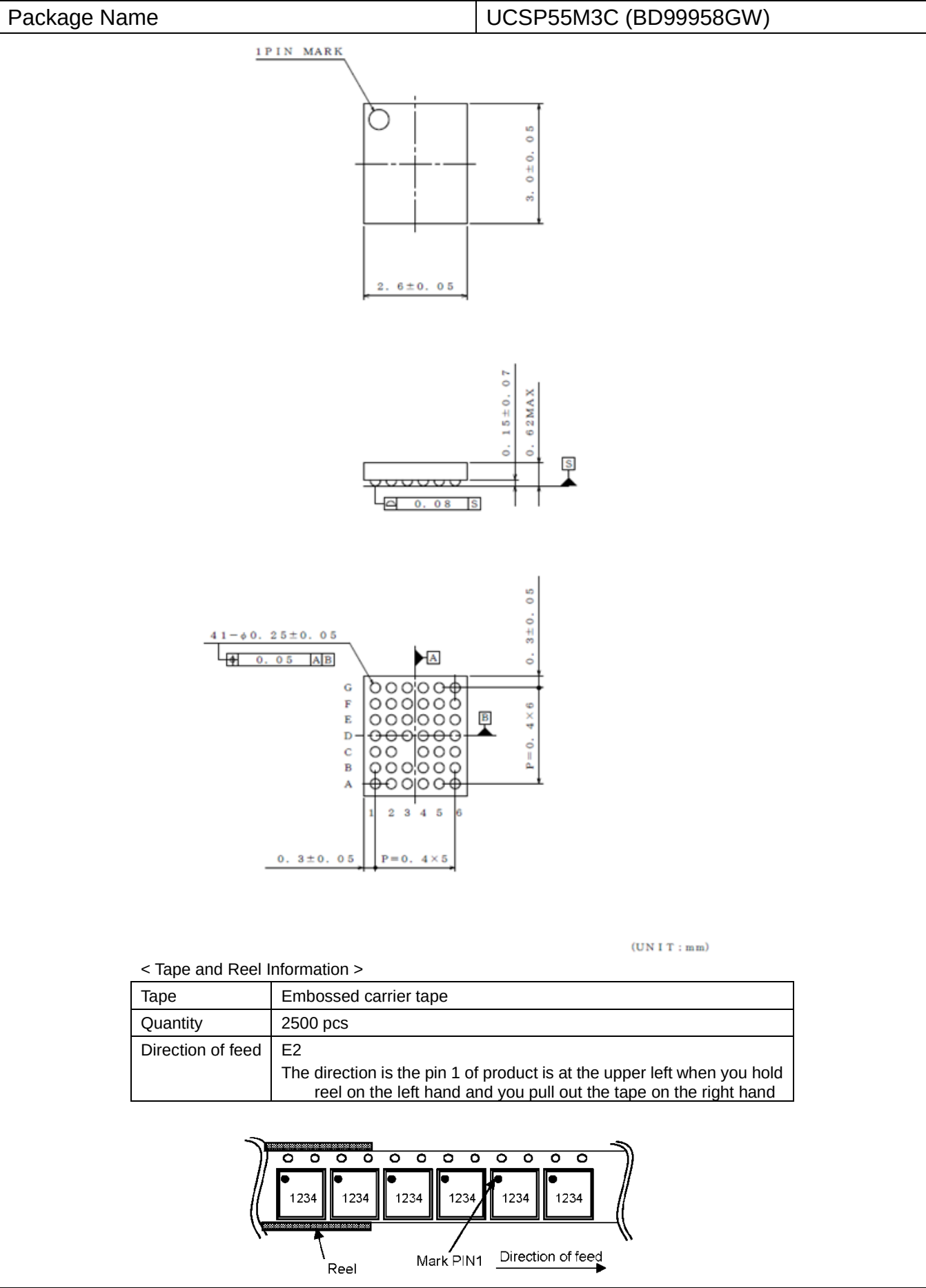
10. Ordering Information



11. Marking Diagram



12. Physical Dimension and Packing Information



13. Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

13. Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

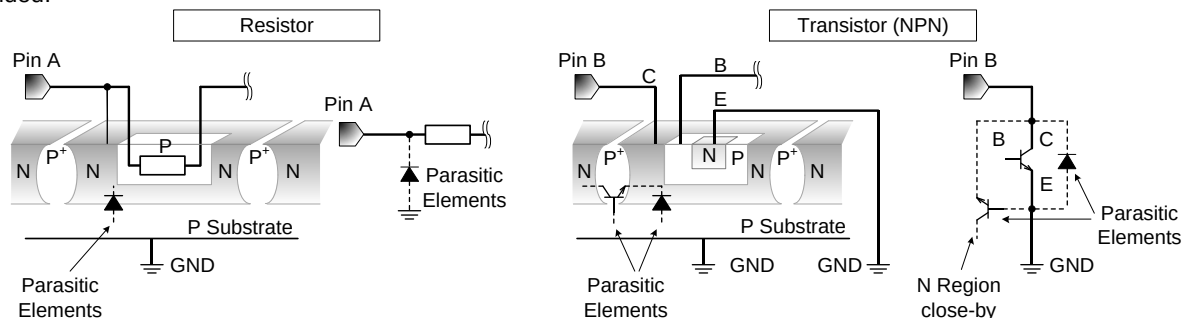


Figure 6. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Disturbance Light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

15. Power Path Sequence

This product is capable of turning both VCC and VBUS power paths ON simultaneously.

Please immediately turn the simultaneous power path ON if one of the VCC or VBUS port has been disconnected and simultaneous ON is not needed.

If the simultaneous power path is not turned off immediately, and a new device is connected to the disconnected port, there is a possibility that this device gets damaged.

In that case, ROHM cannot assume responsibility for the damage.

13. Operational Notes - continued**16. VBUS Overshoot**

There is possibility of voltage overshoot on VCC or VBUS inputs depending on settings and conditions for the following parameters: input voltage (VBUS and VCC), input voltage for IADP (set by external voltage divider), total system capacitance and respective ESR.

Please refer carefully to this datasheet and the separate application notes when making selection of those parameters and register settings to properly match your design.

14. Revision History

Date	Revision	Changes
21.Aug.2018	001	Initial release

Notice

Precaution on using ROHM Products

- Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

- ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
 - Installation of protection circuits or other protective devices to improve system safety
 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
- Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
 - Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.
2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).
3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.
2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.
3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.
4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.
2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.
3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.