Click here for production status of specific part numbers.

MAX20471/MAX20472

Low-Voltage Synchronous Boost Converter

General Description

The MAX20471 and MAX20472 are high-efficiency, low-voltage DC-DC converters that boost a 3.0V to 4.0V input supply to between 3.8V and 5.25V (factory configurable) at 500mA or 1A. The boost converters achieve ±1.5% output error over load, line, and temperature ranges.

The ICs feature a 2.2MHz fixed-frequency, forced pulse-width modulation (FPWM) mode for better noise immunity and load-transient response, as well as a pulse-frequency modulation (skip) mode for increased efficiency during light-load operation. The 2.2MHz frequency operation enables the use of all-ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads, which make the layout a much simpler task with respect to discrete solutions.

Other features of the parts include true output shutdown, soft-start ramping, overcurrent limiting, and overtemperature protection.

Applications

- Automotive Point of Load
- Automotive CAN Transceivers

Benefits and Features

- Synchronous Boost Converter
  - 3.8V to 5.25V Factory-Preset Output in 50mV Steps
  - 500mA or 1A Output Versions
- 3.0V to 4.0V Operating Supply Voltage
- True Output Shutdown
- 2.2MHz Switching Operation
- Open-Drain Reset Output Pin ($\overline{RESET}$)
- Spread-Spectrum Enable Pin (EN)
- High Precision
  - ±1.5% Output-Voltage Accuracy
  - 93 ±2% Undervoltage Monitoring
  - 107 ±2% Overvoltage Monitoring
  - Good Load-Transient Performance
- Robust for the Automotive Environment
  - Current-Mode Control, Forced-PWM, and Skip Operation
  - Overtemperature and Overcurrent Protection
  - 12-Pin (3mm x 3mm) TDFN
  - 12-Pin (3mm x 3mm) SWTDFN
  - 8-Pin (0.150”) SOIC (MAX20471 Only)
  - -40°C to +125°C Automotive Temperature Range

***Ordering Information* appears at end of data sheet.**

19-100163; Rev 9; 8/19

maxim integrated™

Absolute Maximum Ratings (Note 1)

EN, SYNC to GND .....-0.3V to +6V
V_{AV} to GND .....-0.3V to +6V
$\overline{RESET}$ to GND .....-0.3V to +6V
OUT to PGND .....-0.3V to +6V
SSEN to GND..... -0.3V to V_{AV} + 0.3V
LX to PGND (Note 1) ..... -0.3V to V_{OUT} + 0.3V
GND to PGND .....-0.3V to +0.3V
LX Continuous RMS Current.....2.5A
Output Short-Circuit Duration .....Continuous

Continuous Power Dissipation (T_A = +70°C)
12-Pin TDFN-EP (derate 24.4mW/°C > +70°C).....1951mW
12-Pin SWTDFN-EP (derate 25mW/°C > +70°C).....1951mW
8-Pin SOIC (derate 7.8mW/°C > +70°C).....623mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Soldering Temperature Range .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.

Package Information

PACKAGE TYPE: 12 TDFN	
Package Code	TD1233+2C
Outline Number	**21-0664**
Land Pattern Number	**90-0397**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8.5°C/W
PACKAGE TYPE: 12 SWTDFN	
Package Code	TD1233Y+2C
Outline Number	**21-100176**
Land Pattern Number	**90-100072**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8.5°C/W
PACKAGE TYPE: 8 SOIC	
Package Code	S8+2C
Outline Number	**21-0041**
Land Pattern Number	**90-0096**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	128.4°C/W
Junction to Case (θ_{JC})	36°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{AV} = 3.3V, V_{EN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}		3		4	V
UVLO, Rising	V_{UVLOR}		2.48	2.55	2.65	V
UVLO, Falling	V_{UVLOF}			2.475		V
Shutdown Supply Current	I_{SD}	EN = low		0.1	2	µA
Supply Current	I_{IN}	EN = high, I_{OUT} = 0mA, SYNC = low		130		µA
FPWM Switching Frequency	f_{SW}	Internally generated	2	2.2	2.4	MHz
Spread-Spectrum Range	SS	SSEN high		±3		%
OUT						
Voltage Accuracy	V_{OUT}	I_{LOAD} = 0A to I_{MAX}, 3V ≤ V_{AV} ≤ 4V	-1.5		+1.5	%
pMOS On-Resistance	R_{HS}	V_{AV} = 3.3V, I_{LX} = 0.18A		150		mΩ
nMOS On-Resistance	R_{LS}	V_{AV} = 3.3V, I_{LX} = 0.18A		100		mΩ
nMOS Current-Limit Threshold	I_{LIM1}	MAX20471	1.4	1.8	4	A
	I_{LIM2}	MAX20472	2.8	4.2	7	
pMOS Turn-Off Threshold	I_{ZX}			50		mA
LX Leakage Current	I_{LXLKG}	V_{AV} = 6V, LX = PGND or OUT, T_A = +25°C		0.1		µA
Maximum Duty Cycle	DC_{MAX}		90			%
OUT Discharge Resistance	R_{DISCH}	V_{EN} = 0V (connected to OUT)		300		Ω
Skip Threshold	TH_{SKIP}	Percentage of nMOS current-limit threshold		15		%
Soft-Start Time	t_{SS}			1.9		ms
THERMAL OVERLOAD						
Thermal-Shutdown Temperature	T_{SHDN}	TJ rising (Note 3)		165		°C
Hysteresis	T_{HYST}	(Note 3)		15		°C

Electrical Characteristics (continued)

(V_{AV} = 3.3V, V_{EN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{RESET}}$						
Overvoltage Threshold	OV_{ACC}	Rising, percentage of nominal output	105	107	109	%
Undervoltage Threshold	UV_{ACC}	Falling, percentage of nominal output	91	93	95	%
Active Hold Period	t_{HOLD1}	Option 1 (default)		0.5		ms
	t_{HOLD2}	Option 2		3.7		
	t_{HOLD3}	Option 3		7.4		
	t_{HOLD4}	Option 4		14.8		
Undervoltage Delay	t_{UVDEL}	10% below/above threshold		10		µs
Output High-Leakage Current	I_{RLKG}	T_A = +25°C	-0.5	0.1	+0.5	mA
Output Low Level	V_{ROL}	3V ≤ V_{AV} ≤ 4V, sinking -2mA			0.2	V
EN AND SYNC INPUTS						
Input High Level	V_{IH}	3V ≤ V_{AV} ≤ 4V	1.5			V
Input Low Level	V_{IL}	3V ≤ V_{AV} ≤ 4V			0.5	V
Input Hysteresis	V_{HYST}			0.1		V
EN Pulldown Current	I_{ENPD}		0.5	1	2	µA
SYNC Input Pulldown	R_{SYNCPD}	EN high		100		kΩ
SYNC Input Frequency Range	f_{SYNC}		1.7		2.6	MHz

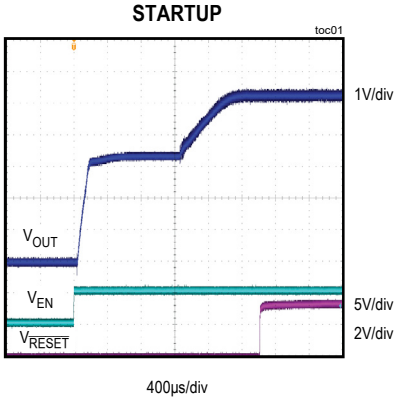
Note 2: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 3: T_{SHDN} and T_{HYST} are not tested.

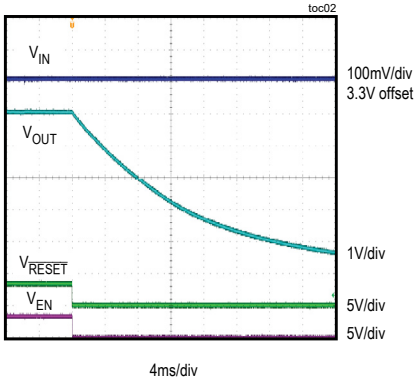
Typical Operating Characteristics

(V_{AV} = 3.3V, V_{EN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.)

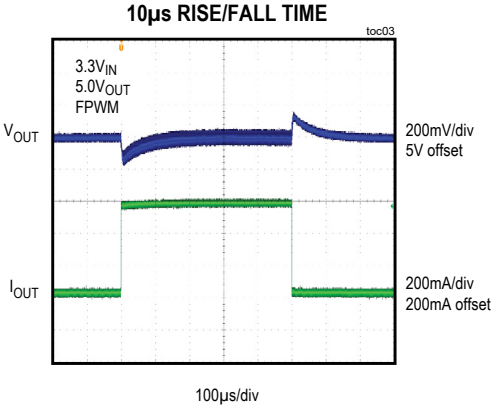
STARTUP



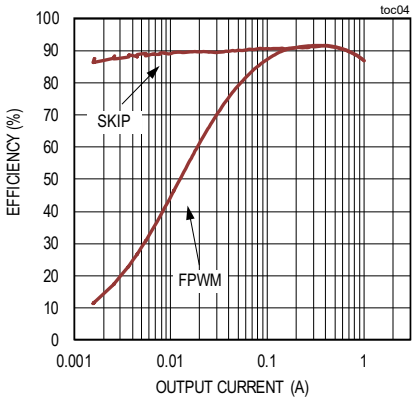
SHUTDOWN



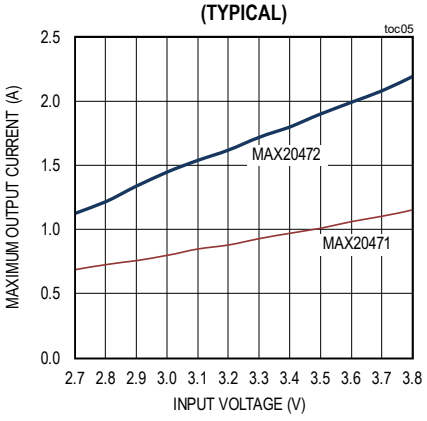
LOAD-TRANSIENT RESPONSE
20%-80%-20% STEP
10µs RISE/FALL TIME



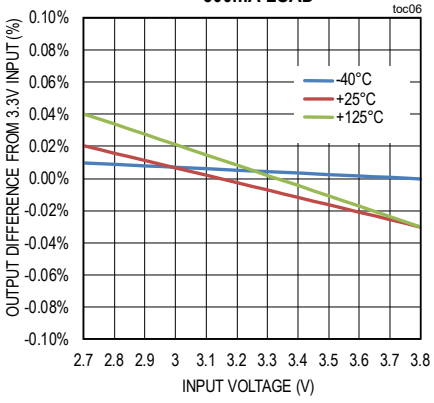
EFFICIENCY
5.0V OUTPUT, 3.3V INPUT



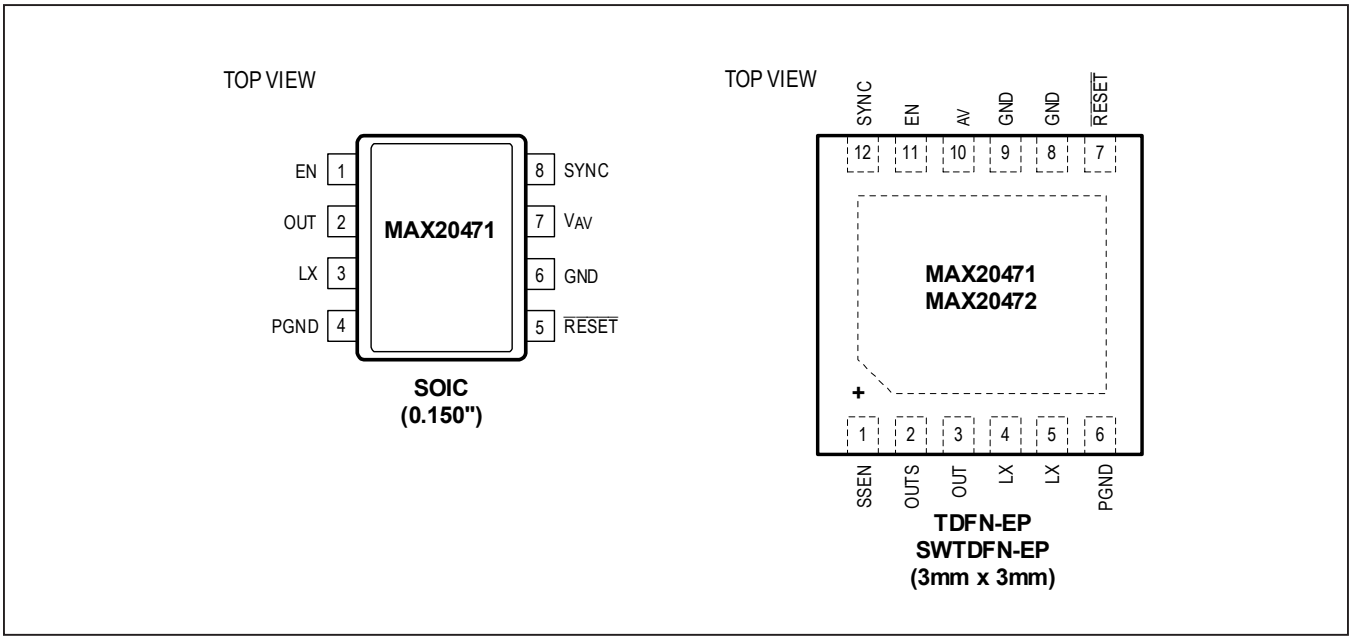
MAXIMUM OUTPUT CURRENT
(TYPICAL)



LINE REGULATION
300mA LOAD



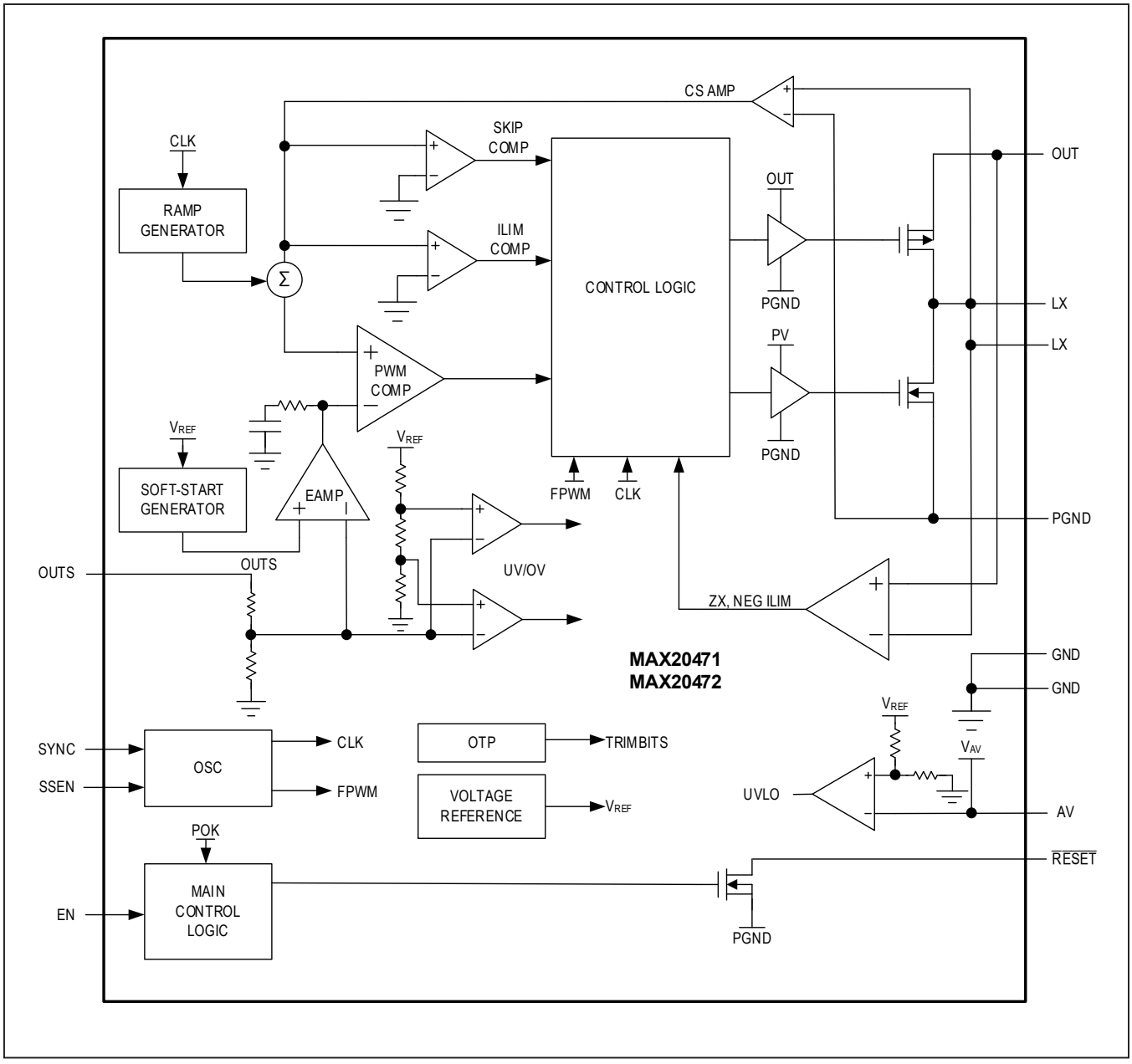
Pin Configurations



Pin Description

PIN	NAME		FUNCTION
	SOIC	TDFN	
SSEN	—	1	Spread-Spectrum Enable. Connect to V_{AV} to enable spread spectrum.
OUTS	—	2	Output-Voltage Feedback Pin. Connect this pin to the output capacitor.
OUT	2	3	Output Voltage
LX	3	4, 5	Inductor Connection. Connect LX to the switched side of the inductor.
PGND	4	6	Power Ground
$\overline{RESET}$	5	7	Open-Drain, Active-Low Reset Output. To obtain a logic signal, pull $\overline{RESET}$ up with an external resistor.
GND	—	8	Ground. Connect all ground pins together.
AGND	6	9	Analog Ground. Connect all ground pins together.
V_{AV}	7	10	Analog Power Input Supply. Connect a 1µF ceramic capacitor from V_{AV} to GND.
EN	1	11	Active-High Enable. Drive EN high for normal operation.
SYNC	8	12	SYNC Input. Connect SYNC to GND or leave unconnected to enable skip-mode operation under light loads. Connect SYNC to V_{AV} or an external clock to enable fixed-frequency FPWM mode operation.
EP	—	—	Exposed Pad. Connect EP to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to GND and PGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Functional Diagram



Detailed Description

The MAX20471 and MAX20472 are high-efficiency, low-voltage 500mA and 1A synchronous DC-DC boost converter ICs that boost the 3.0V to 4.0V input supply to a fixed output voltage between 3.8V and 5.25V. The boost converters have True Shutdown™, so the output voltage will be 0V when off. The ICs achieve ±1.5% output error over load, line, and temperature ranges.

The ICs feature a 2.2MHz fixed-frequency FPWM mode for better noise immunity and load-transient response, as well as pulse-frequency operation that allows the use of all-ceramic capacitors, thus minimizing external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. The spread modulation is factory set to pseudorandom. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads, which makes the layout a much simpler task with respect to discrete solutions.

The ICs contain high-accuracy, factory-set OV/UV thresholds for each output mapped to the $\overline{RESET}$ pin. There are diagnostics on the $\overline{RESET}$ and OUT pins to guarantee high reliability and fail-safe operation. In light-load applications, a logic input (SYNC) allows the ICs to operate either in skip mode for reduced current consumption, or fixed-frequency FPWM mode to eliminate frequency variation and help minimize EMI.

Enable Input (EN)

The EN input activates the ICs' channels from their low-power shutdown state. EN has an input threshold of 1.0V (typ), with hysteresis of 100mV (typ). When EN goes high, the associated output voltage ramps up with the programmed soft-start time.

$\overline{RESET}$ Output

The ICs feature an individual open-drain, active-low reset output for each output that asserts low when the corresponding output voltage is outside the UV/OV window. $\overline{RESET}$ remains asserted for a fixed timeout period after the output rises to its regulated voltage. The fixed timeout period is selectable between 0.5ms (default), 3.7ms, 7.4ms, and 14.9ms. To obtain a logic signal, install a resistor pullup between the $\overline{RESET}$ pin and the system I/O voltage.

Internal Oscillator

The ICs have a spread-spectrum oscillator that varies the internal operating frequency by ±3%, relative to the internally generated 2.2MHz (typ) operating frequency. This function does not apply to externally applied oscillation frequency. The spread frequency generated is pseudorandom with a repeat rate well below the audio band. Spread spectrum on MAX20471ASAA is enabled as an internal setting. Contact customer support for more details.

Synchronization (SYNC)

The ICs have an on-chip oscillator that provides a 2.2MHz (typ) switching frequency. Depending on the condition of SYNC, two operation modes exist. If SYNC is unconnected or at GND and the load current is below the skip-mode current threshold, the ICs will operate in a highly efficient pulse-skipping mode. If the current is above the threshold, the ICs automatically change to FPWM mode. If SYNC is at V_{AV} or has a frequency applied to it, the ICs will always operate in FPWM mode. The ICs can be switched during operation between FPWM or skip mode by pulling SYNC up to V_{AV} or down to GND.

Soft-Start

The ICs include a fixed 1.9ms soft-start. Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Forced-PWM and Skip Modes

The ICs feature an input pin (SYNC) that puts the converter either in skip or FPWM mode of operation. See the *Pin Description* table for more information. In FPWM mode, the converter switches at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load-dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the FPWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off, as often is the case in the FPWM mode of operation. Consequently, the gate charge and switching losses are much lower in skip mode.

True Shutdown is a trademark of Maxim Integrated Products, Inc.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the ICs. When the junction temperature exceeds 165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the ICs to cool. The thermal sensor turns on the ICs again after the junction temperature cools by 15°C.

Boost Converter Short Protection

The boost has protection against startup into short and also protection against short/overload after startup.

Startup into Short

After the boost is enabled, the internal PMOS rectifier is configured as a 2A (typ) current source. This mode of operation is referred to as “charge mode” and is used to charge the output to within 600mV of the input. Under normal circumstances, charge mode is successful and the boost begins switching soft-start to 5.0V. If the output is shorted or overloaded, charge mode will be unable to charge the output to within 600mV of the input. If charge mode lasts for more than 1.9ms, the boost shuts off and automatically attempts restart after 120ms. This automatic restart is called “hiccup mode” and continues indefinitely. Disabling, then reenabling the boost overrides the 120ms timer and retries immediately.

Short or Overload after Soft-Start

After soft-start is complete, the boost is still monitoring to make sure the output is always greater than the 600mV input. If a short or overload condition pulls the output below the 600mV input, the boost stops switching and reenters the charge-mode configuration. If the output continues to fall below 3.125V, independent of the input voltage, the boost shuts off, and enters hiccup mode, as described above.

Applications Information

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit’s switching. A 2.2µF, X7R ceramic capacitor is recommended for the DC-DC input. A 1µF, X7R ceramic capacitor is recommended for the V_{AV} pin.

Inductor Selection

Use a 1µH inductor for the MAX20471/MAX20472. For a ferrite core, the saturation current should be greater than the maximum current limit. For a soft-saturation core, the saturation current can be less than the maximum current limit as long as the inductance at the maximum current limit is greater than 50% of the nominal inductance.

Output Capacitor

The ICs are designed for stability with low-ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The output capacitor calculations below are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify that proper stability is achieved.

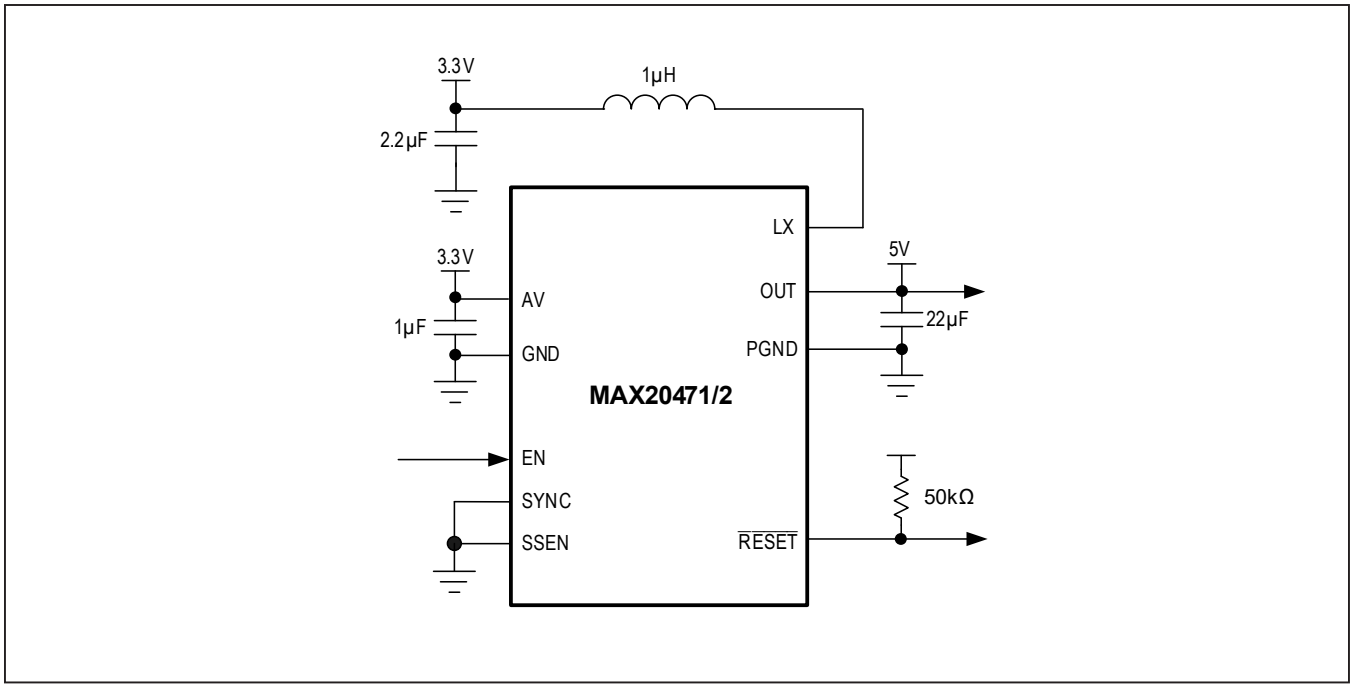
$$COUT_{MIN} = \frac{55\mu s}{V_{OUT}}$$

$$COUT_{NOM} = \frac{110\mu s}{V_{OUT}}$$

PCB Layout Guidelines

When laying out the PCB, keep the DC-DC power components close together and the routes short to minimize loop area. The output capacitor, power inductor, and input capacitor should be placed close to the IC package. The output capacitor experiences the greatest amount of ripple current, and should be placed closest to the IC. The higher current-carrying traces, such as the input (LX) and OUT, should be wide. Vias should connect the exposed pad of the ICs to provide optimal ground and thermal dissipation connections. A large ground plane should be placed directly below the power traces.

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	V_{OUT} (V)	Input Current Limit (A)
MAX20471ATCA/V+	-40°C to +125°C	12 TDFN-EP*	5	1.8
MAX20471ATCB/V+	-40°C to +125°C	12 TDFN-EP*	5.15	1.8
MAX20471ATCA/VY+**	-40°C to +125°C	12 SWTDFN-EP*	5	1.8
MAX20471ASAA/V+	-40°C to +125°C	8 SOIC	5	1.8
MAX20472ATCA/V+	-40°C to +125°C	12 TDFN-EP*	5	4.2
MAX20472ATCB/V+	-40°C to +125°C	12 TDFN-EP*	5.15	4.2
MAX20472ATCC/V+	-40°C to +125°C	12 TDFN-EP*	3.85	4.2
MAX20472ATCA/VY+**	-40°C to +125°C	12 SWTDFN-EP*	5	4.2

Note: *For variants with different options, contact factory.*

/V denotes an automotive qualified part.

Y denotes side-wettable

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel

**EP = Exposed pad.*

***Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/17	Initial release	—
1	1/18	Changed part in *Ordering Information* table from MAX20471ASA/V+** to MAX20471ASAA/V+** and removed future product status from MAX20472ATCA/V*	9
2	5/18	Updated *Internal Oscillator* section and added *Boost Converter Short Protection*, *Startup into Short*, and *Short or Overload after Soft-Start* sections	7, 8
3	6/18	Added MAX20472ATCB/V+** (future product) to *Ordering Information* table.	10
4	9/18	Removed all references to MAX20473 and 2A convertor operation; updated *Pin Configuration*; updated *Functional Diagram*; updated *Inductor Selection* and *Output Capacitor* sections; updated *Typical Application Circuit*; removed MAX20473ATCA/V+** and future-part designation for MAX20471ATCB/V+ from the *Ordering Information* table	1-11
5	11/18	Removed future-part designation for MAX20472ATCB/V+ from the *Ordering Information* table	11
6	12/18	Updated *Package Information* table	2
7	3/19	Added information for SWTDFN package to *Benefits and Features*, *Absolute Maximum Ratings*, *Package Information*, *Pin Configurations*, and *Ordering Information*; added MAX20472ATCC/V+** to *Ordering Information*	1, 2, 6, 11
8	6/19	Removed future-part designation from MAX20471ASAA/V+ in the *Ordering Information* table	11
9	8/19	Added notes to *Ordering Information* table	11

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at **https://www.maximintegrated.com/en/storefront/storefront.html**.

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