



SILEGO

**GreenPAK DIP Development Platform
User Guide**

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1 Introduction

Thank you for choosing Silego Technology products. The GreenPAK DIP Development Platform allows you to develop your custom design using GreenPAK mixed signal ICs. You can design your own projects starting from a blank project or by altering the sample projects provided at [Silego website](#).

1.1 GreenPAK Designer

GreenPAK Designer is an easy-to-use full-featured integrated development environment (IDE) that allows you to specify exactly how you want the device to be configured. This provides you a direct access to all GreenPAK device features and complete control over the routing and configuration of a PAK project with just one tool.

With GreenPAK Designer, you can:


- design the configuration which corresponds to your project needs
- verify the project using software interface to GreenPAK DIP Development Platform hardware
- with simple-to-use and intuitive software and hardware tools you can reduce your project development time and get to market faster

To start working with GreenPAK Designer please take the following steps:

- download and install GreenPAK Designer software
- configure modules that you will need for your project
- interconnect and configure modules
- specify the pin out
- test your design with the GreenPAK DIP Development Board

1.2 Support

Free support for GreenPAK DIP Development Platform is available online at <http://www.silego.com/>.

At  : [Silego-Technology](#)

GreenPAK Designer will automatically notify you when a new version of software is available. For manual updates please go to <http://www.silego.com/softdoc/software.html>.

These resources are also available under the **Help** menu of GreenPAK Designer.



2 Getting Started

2.1 Introduction

This chapter describes how to install and configure the GreenPAK DIP Development Platform. *Chapter 3* provides the details of hardware operation. *Chapter 4* provides instructions on how to create a simple project example.

2.2 Install Software

GreenPAK Designer software is available free of charge from the Silego website at <http://www.silego.com/softdoc/software.html> page.

2.3 Uninstall Software

The software can be uninstalled in the way typical for your operating system. Please refer to your operating system support documentation if you need the specific instructions or visit [Support](#) section of this document for additional support from Silego.



3 Hardware

3.1 Overview

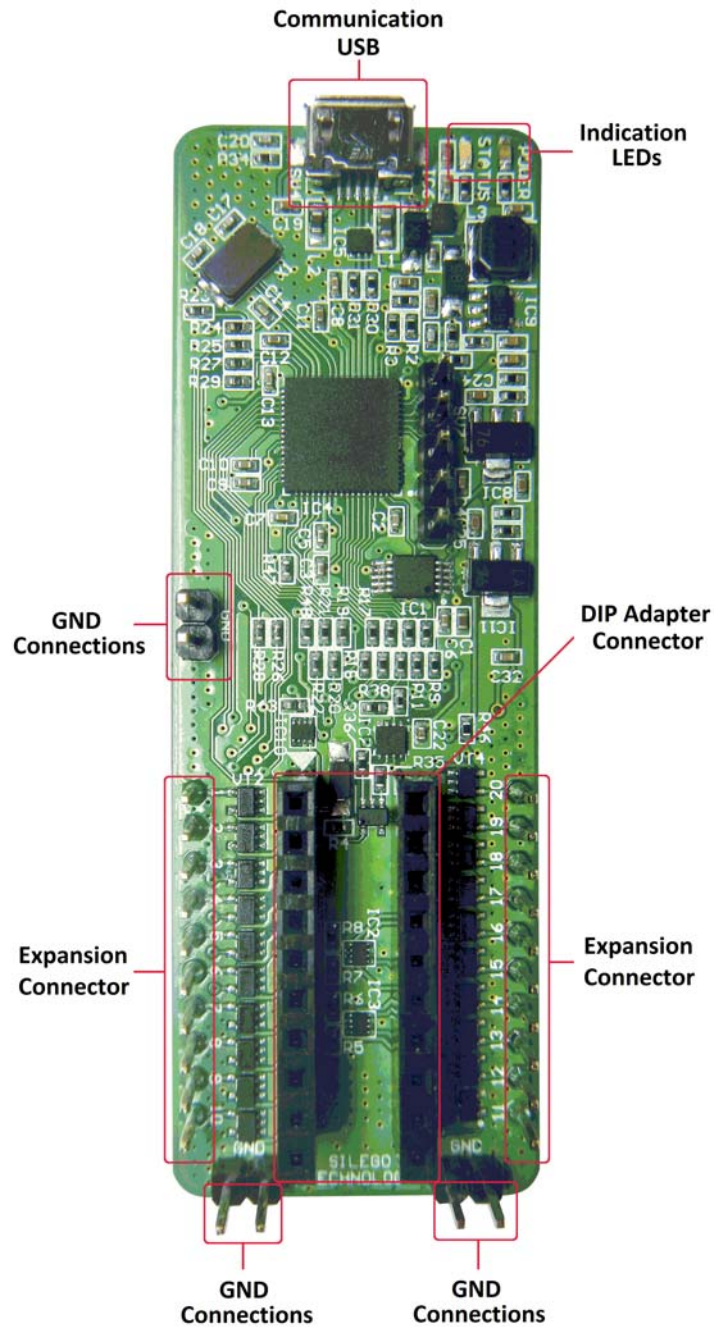


Figure 1. GreenPAK DIP Development Board, Top View



3.2 Functional Description

3.2.1 Power Supply

The main power source of the GreenPAK DIP Development Board is the USB power line. The Development Board can deliver power from 1.7 to 5.5 V. To provide this power range, the Development Board is equipped with a boost converter.

3.2.2 USB Communication

The board has the USB communications interface that uses the USB mini-B connector. This interface provides communication with the software control tool and supplies power to the board, as described in [Power Supply](#) chapter.

3.2.3 GND Connections

There are 4 GND pins on the left side, 2 pins on the right side. These can be used for test equipment (oscilloscope, multimeter etc.) ground reference connection or to connect external test circuitry ground.

3.2.4 DIP Adapter Connections

The GreenPAK DIP Development Board should be used with a DIP Adapter board. Its main purpose is to connect the GreenPAK chip to the GreenPAK DIP Development Board. Information about DIP Adapters is available online at http://www.silego.com/softdoc/user_guides.html.

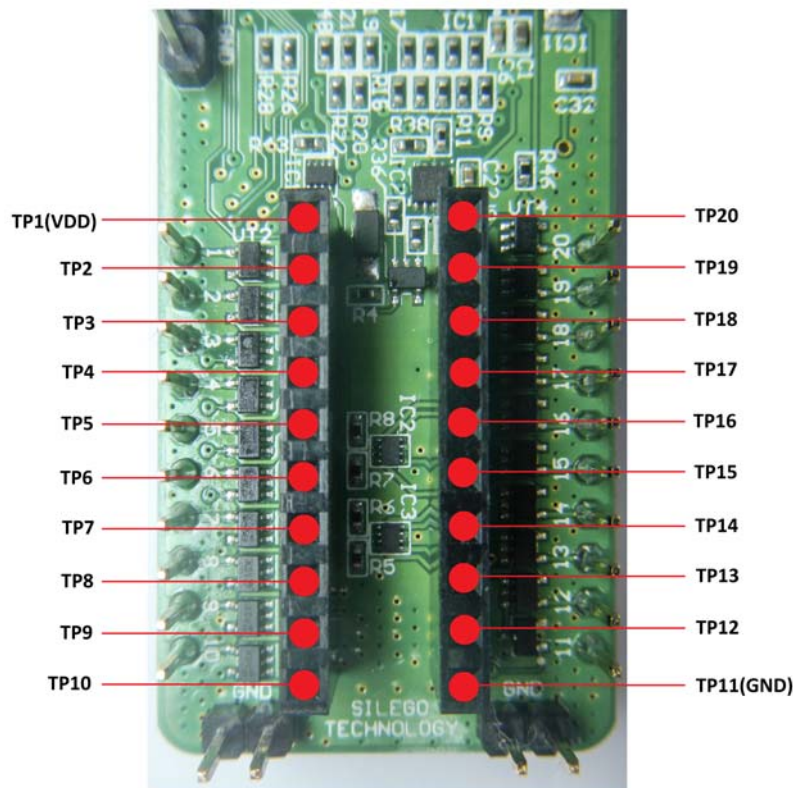


Figure 2. DIP Adapter Connector Pinout



3.2.5 Expansion Connector

This 20-pins connector is in the right and left bottom part of the Development Board. The Expansion Connector is a standard 0.1" female connector compatible with breadboard (see *Figure 3*).

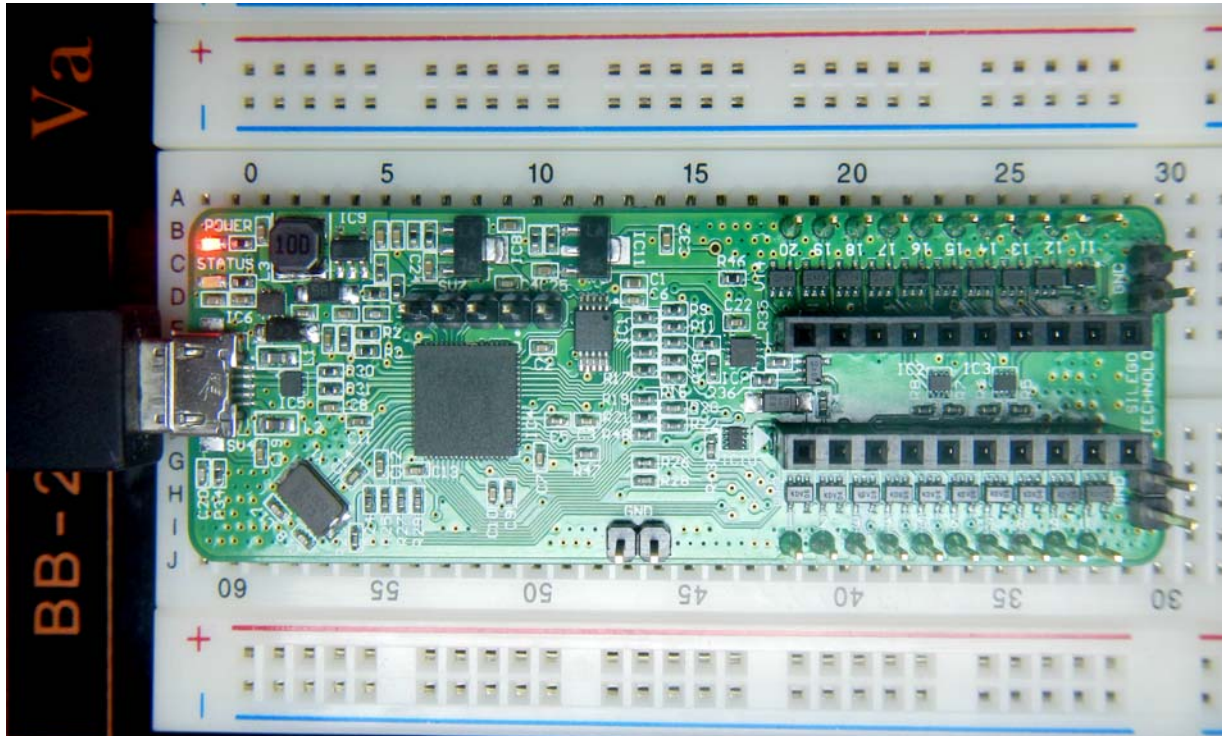


Figure 3. Breadboard with GreenPAK DIP Development Board

This port was designed to connect the GreenPAK DIP Development Board to external circuits and apply external power, signal sources and loads. It can be used to apply the GreenPAK chip into your custom design with minimal additional tools.

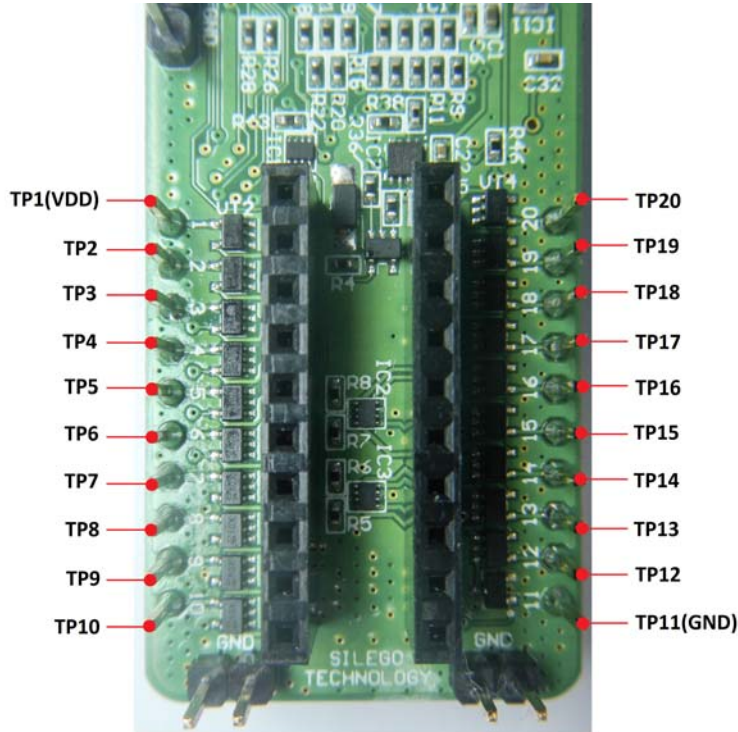


Figure 4. Expansion Connector Pinout

Each pin except GND and NC is controlled through individual analog switch. GreenPAK Designer can enable or disable external pins, as it is shown on the *Figure 5*. There is no individual control of each key: when one key is turned on, all others are also turned on.

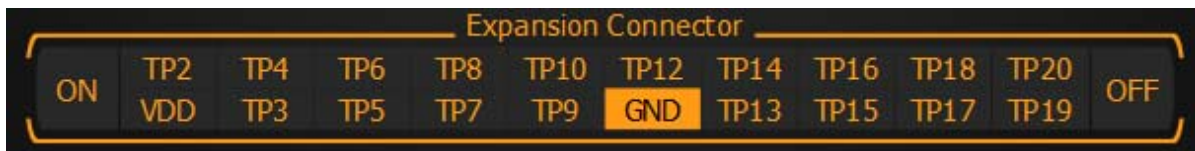


Figure 5. Expansion Connector Control in GreenPAK Designer

The Expansion Connector is enabled only in Emulation mode or Test mode. To enter either of these two modes, the target GreenPAK device must be inside the socket the DIP Adapter Connector. When the Test mode button is pressed, the software will first read the chip to verify if it was inserted correctly, and then configure the GreenPAK DIP Development Board as it was set in Emulation mode. After the Emulation button is pressed, the software will automatically perform the following steps:

- check chip presence
- open all expansion port switches (allowing external signals/loads to be left connected to Expansion Connector)
- load target configuration into the target GreenPAK device using internal power
- configure Development Board as it was selected in Emulation Tool window



Note that the GreenPAK device has internal OTP memory which is normally loaded into RAM registers at initialization time. "Emulation mode" will bypass this load, and write the updated version of the project directly into the RAM register inside the GreenPAK chip many times, but after power loss all internal data will be lost. Also, when the GreenPAK chip is already programmed - user can use Emulation mode to load another project and test it on the emulation tool during the Emulation mode, in that case emulation data will be cleared. The "Emulation" mode is not necessary for checking programmed parts: in this case the "Test mode" will supply power to the device, which will perform the standard load of configuration data from OTP to RAM. The difference between the "Emulation" and the "Test mode" is that in the "Test mode", the process of loading configuration memory is skipped, and after the chip power, the OTP memory loads into RAM registers.

The Expansion Connector has the following type of connections:

1. VDD
2. GND
3. Data

The VDD connection allows the user to both use internal power supply to power the external circuit, and use external power source as the on-board chip power. This selection to use either internal or external power is made in the Emulator Controls window.

The GND connection is connected directly to the GreenPAK DIP Development Board ground, and cannot be controlled or switched.

Data connections are the easiest way to connect external signals to the GreenPAK chip. They are software controlled switches that are controlled in the Emulator Controls window.

3.2.6 Pins Connectivity

The Socket connector has the following type of connections:

1. VDD
2. GND
3. Data

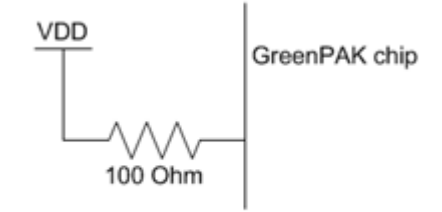
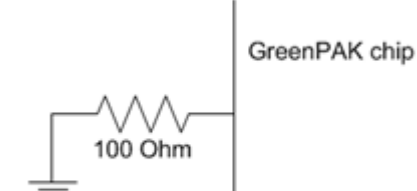
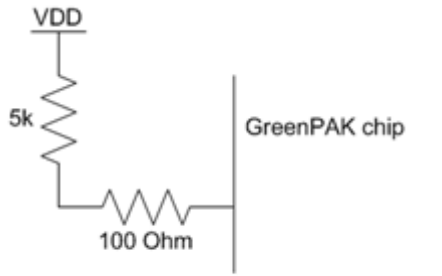
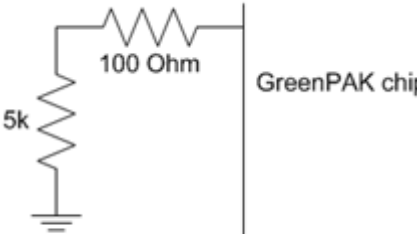
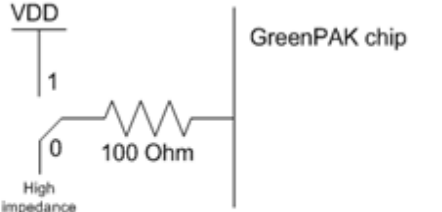
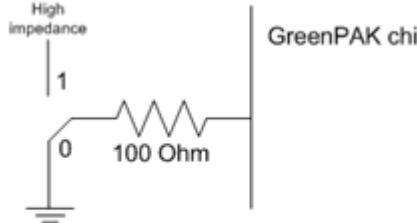
The GreenPAK DIP Development Board supports connecting five types of loads and signal sources. Each source has its own special purpose.

For VDD pins is only available a signal generator connection.

For the Data pins the following connections are available: VDD, GND, Pull Up, Pull Down, Configurable Button.



Data pins connections schematics:

<p>Connect PIN to VDD through 100 Ω resistor</p>	 <p>Set to VDD</p>	<p>Connect PIN to GND through 100 Ω resistor</p>	 <p>Set to GND</p>
<p>Connect PIN to VDD through MCU 5 kΩ Pull Up resistor + 100 Ω resistor</p>	 <p>Pull up</p>	<p>Connect PIN to GND through MCU 5 kΩ Pull Down resistor + 100 Ω resistor</p>	 <p>Pull down</p>
<p>Upper connection to VDD through 100 Ω resistor; bottom connection to high impedance MCU input</p>	 <p>Button VDD – HI-Z</p>	<p>Upper connection to high impedance MCU input; bottom connection to GND through 100 Ω resistor</p>	 <p>Button HI-Z – GND</p>



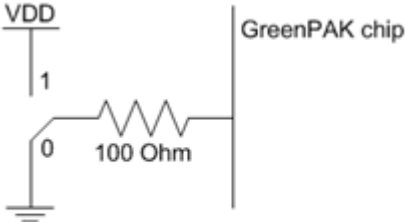
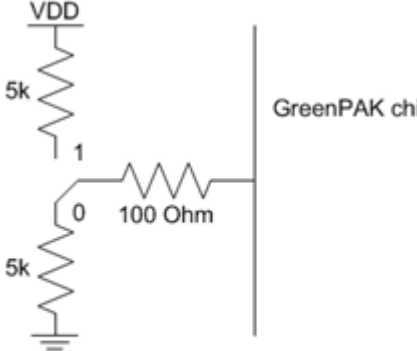
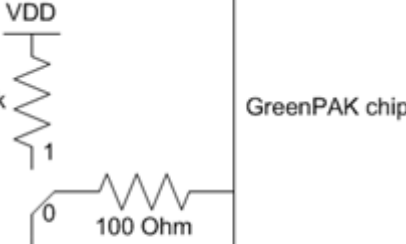
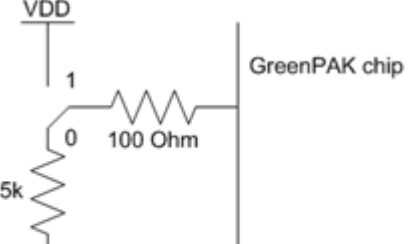
<p>Upper connection to VDD through 100 Ω resistor; bottom connection to GND through 100 Ω resistor</p>	 <p style="text-align: center;">Button VDD – GND</p>	<p>Upper connection to VDD through MCU 5 kΩ Pull Up resistor + 100 Ω resistor; bottom connection to GND through MCU 5k Pull Down resistor + 100 Ω resistor</p>	 <p style="text-align: center;">Button Pull up – Pull down</p>
<p>Upper connection to VDD through MCU 5 kΩ Pull Up resistor + 100 Ω resistor; bottom connection to GND through 100 Ω resistor</p>	 <p style="text-align: center;">Button Pull up – GND</p>	<p>Upper connection to VDD through 100 Ω resistor; bottom connection to GND through MCU 5 kΩ Pull Down resistor + 100 Ω resistor</p>	 <p style="text-align: center;">Button VDD – Pull down</p>

Figure 6 shows the schematic connection of the GP VDD pins.

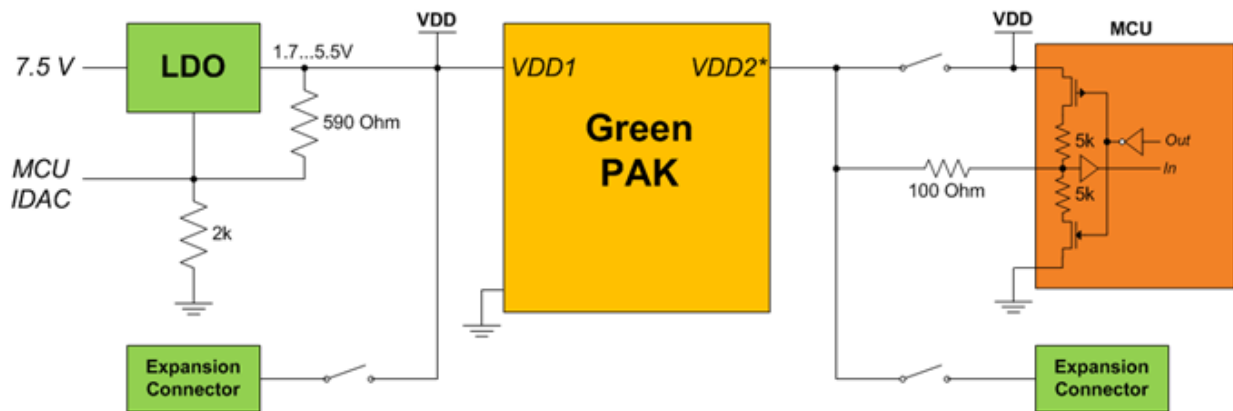


Figure 6. Schematic Connection of the VDD Pin

Note*: If chip has VDD2. For more information see chip datasheet.



Figure 7 shows the schematic connection of the GP data pins.

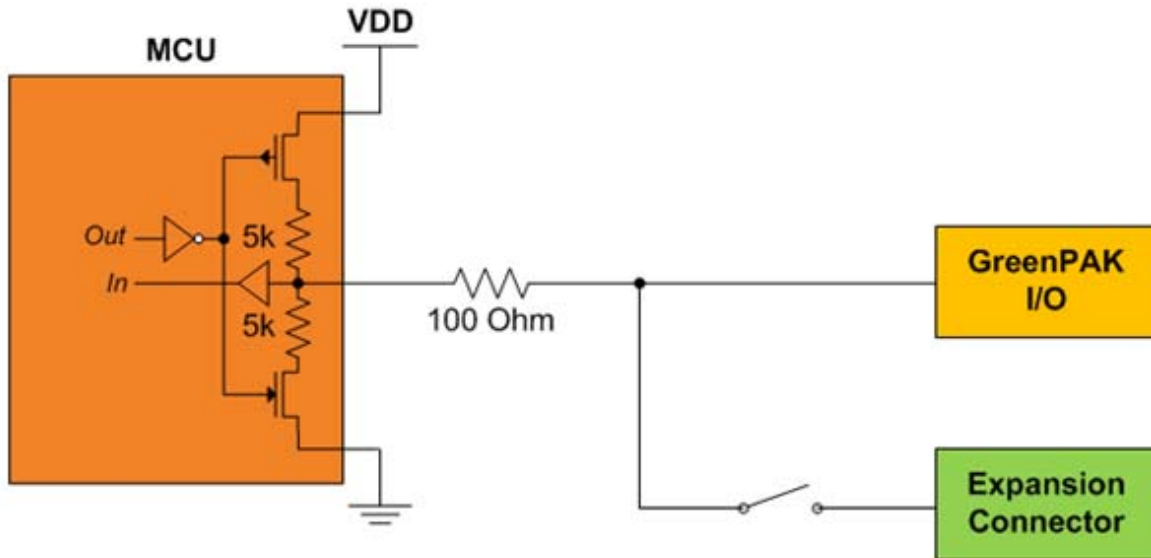


Figure 7. Schematic Connection of the Data Pin

3.2.7 Chip PIN versus Development Board Test Point (TP)

Before you start working with a chip, you need to understand the difference between such concepts as PIN (chip pin) and TP (the Development Board test point). *Figure 8* shows where PINs and TPs are.

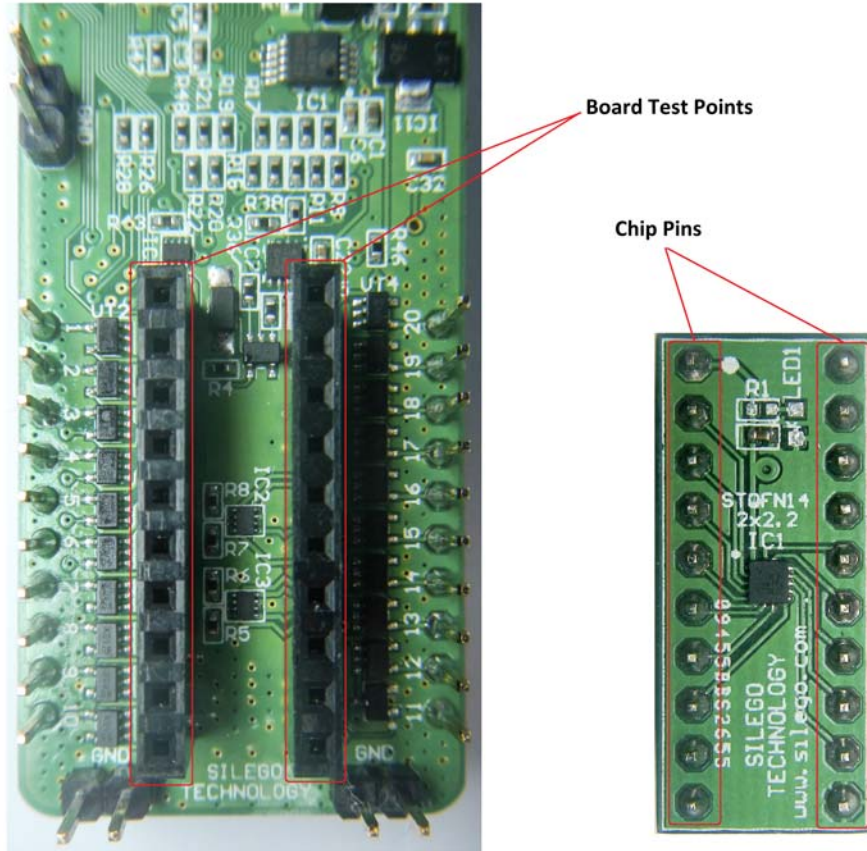


Figure 8. Pins and TPs Location

PINs refer to the physical pins that are on the chip package (their marking can be seen in the datasheet). TPs refer to the DIP Adapter and Expansion connector pins. TP and PIN numbers may not match since different PINs on the chip have different functions (see *Figure 9*).

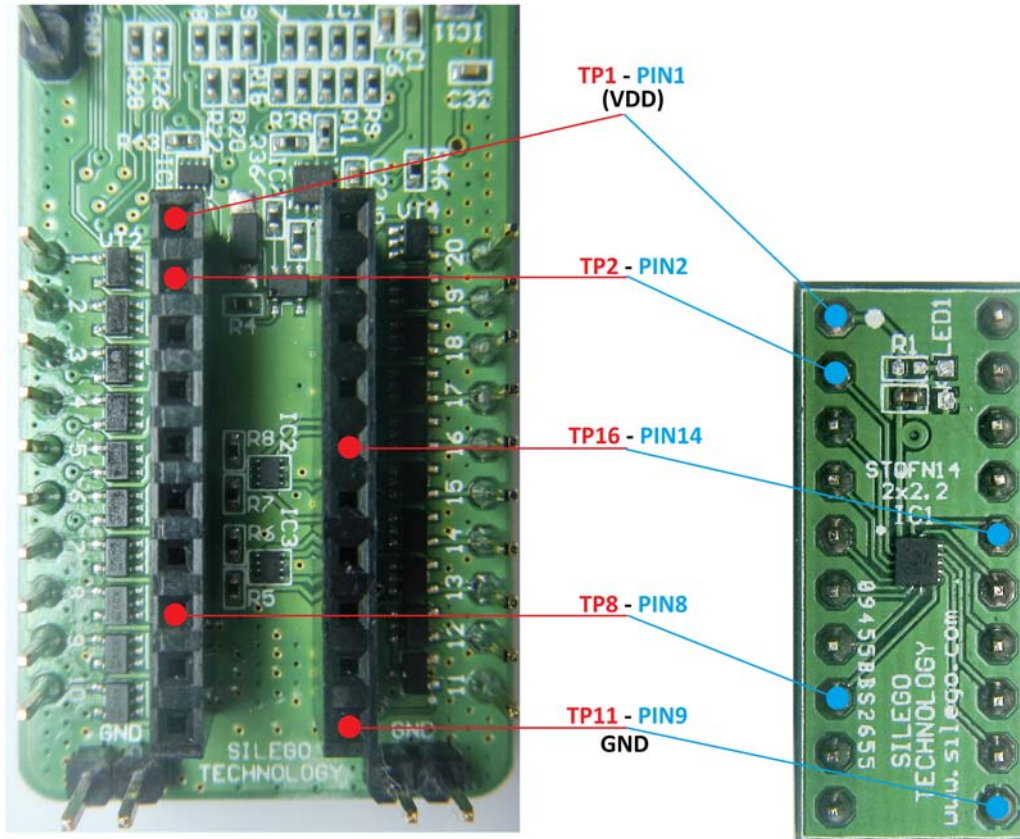


Figure 9. Pins and TPs Accordance (for SLG46534)



4 Example Projects using SLG46534

4.1 Project: Counter with Clock Enable

Blocks required:

- 1 digital input
- 2 digital outputs
- 2 Look-Up tables with two inputs
- 1 Counter
- 1 Oscillator

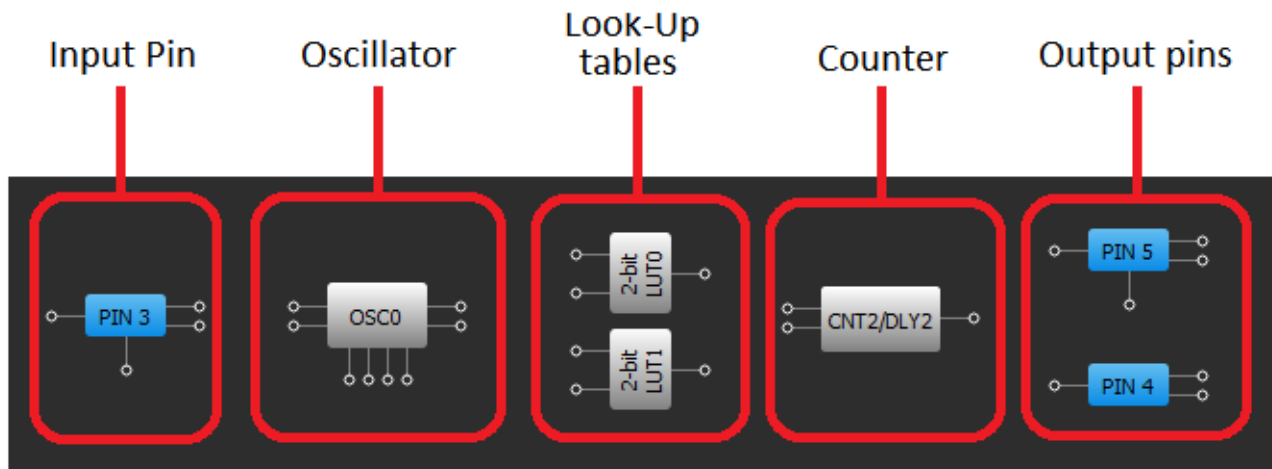


Figure 10. GreenPAK Designer Components

All these components can be found in Components List. If there are no components on the work area - make sure this component is enabled by checking appropriate boxes.

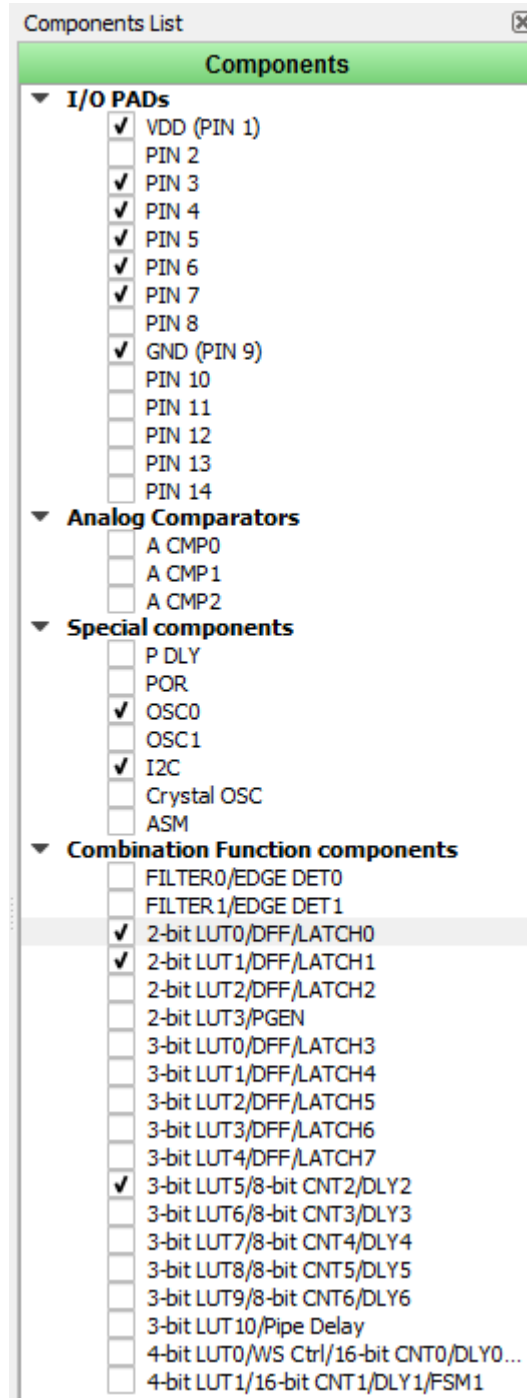


Figure 11. GreenPAK Designer Components List



GreenPAK Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
3	Enable	Digital Input	Digital Input
4	Counter Output	Push Pull Output	Digital Output
5	Oscillator Output	Push Pull Output	Digital Output
9	GND	GND	Ground

All components used in this project are shown on *Figure 10*; next step is to configure selected blocks. Double click on PIN4 to open “Properties” panel. Select “Digital output” in **I/O Selection** field and then select “1x push pull” from the drop-down menu in **Output mode** field and hit “Apply” button. Make the same settings for PIN5.

Properties ✕

PIN 4

I/O selection: Digital output ▼

Input mode: None ▼
OE = 0

Output mode: 1x push pull ▼
OE = 1

Resistor: Floating ▼

Resistor value: Floating ▼

Information

Electrical Specifications

	1.8 V min/max	3.3 V min/max	5.0 V min/max
V _{OH} (V)	1.690/-	2.700/-	4.150/-
V _{OL} (V)	-/0.013	-/0.230	-/0.240
I _{OH} (mA)	1.070/-	6.050/-	22.080/-
I _{OL} (mA)	0.920/-	4.880/-	7.220/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-

i
↶
↷
Apply

Properties ✕

PIN 5

I/O selection: Digital output ▼

Input mode: None ▼
OE = 0

Output mode: 1x push pull ▼
OE = 1

Resistor: Floating ▼

Resistor value: Floating ▼

Information

Electrical Specifications

	1.8 V min/max	3.3 V min/max	5.0 V min/max
V _{OH} (V)	1.690/-	2.700/-	4.150/-
V _{OL} (V)	-/0.013	-/0.230	-/0.240
I _{OH} (mA)	1.070/-	6.050/-	22.080/-
I _{OL} (mA)	0.920/-	4.880/-	7.220/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-

i
↶
↷
Apply

Figure 12. Pin 4, 5 Mode



The next component in this design is Look-Up table. First Look-Up Table (LUT0) is used to generate logic “1” only when there are high logic levels on both inputs (AND gate). Select AND gate from “Standard gates” drop-down menu or set table manually. Second Look-Up Table (LUT1) is configured as NOR gate. It is used to generate reset signal for counter on PIN3 falling edge.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Figure 13. Look-Up Table Properties Configured as an AND Gate



Properties ✕

2-bit LUT1/DFF/LATCH1

Type: LUT

IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates All to 0

NOR All to 1

Regular shape Invert

i ↶ ↷ Apply

Figure 14. Look-Up Table Properties Configured as a NOR Gate

Figure 15 shows counter properties.



The image shows a 'Properties' dialog box for a '3-bit LUT5/8-bit CNT2/DLY2' component. The dialog is titled 'Properties' and has a close button in the top right corner. The title bar is green and contains the text '3-bit LUT5/8-bit CNT2/DLY2'. The main area is divided into several sections:

- Type:** A dropdown menu set to 'CNT/DLY'.
- Mode:** A dropdown menu set to 'Counter'.
- Counter data:** A numeric input field containing '4', with a range of '(Range: 1 - 255)' below it.
- Output period (typical):** A field containing 'N/D' and a 'Formula' link.
- Edge select:** A dropdown menu set to 'Rising'.
- Output polarity:** A dropdown menu set to 'Non-inverted (OUT)'.
- Q mode:** A dropdown menu set to 'None'.
- Stop and restart:** A dropdown menu set to 'None'.

Below these settings is a section titled 'Connections' with the following fields:

- Clock:** A dropdown menu set to 'Ext. Clk. (From mat)'.
- Clock source:** A field containing 'Ext. Clk. (matrix)'.
- Clock frequency:** A field containing 'N/D'.

At the bottom of the dialog are three icons: an information icon (i), a refresh icon, and a save icon, followed by an 'Apply' button.

Figure 15. Counter Properties

Figure 16 shows oscillator properties.



Properties

OSC0

Control pin mode: Power down

OSC Power Mode: Force Power On

Clock selector: OSC

Fast start-up: Disable

RC OSC Frequency: 25 kHz

'CLK' predivider by: 8

'OUT0' second divider by: 64

'OUT1' second divider by: 1

Information

Frequency

Clock output configuration:

RC OSC Output	Value
CLK /4	RC OSC Freq. /8 /4
CLK /12	RC OSC Freq. /8 /12
CLK /24	RC OSC Freq. /8 /24
CLK /64	RC OSC Freq. /8 /64
OUT0	RC OSC Freq. /8 /64
OUT1	RC OSC Freq. /8

Apply

Figure 16. Oscillator Properties


The Final step is to connect each of the selected components. Use Wire tool to perform this action. To connect two pins select "Set Wire"  and then click on the first and the second pins of the module or modules that you want to connect. The trace will be automatically routed.

Figure 17 displays ready project with configured blocks and wire connections.

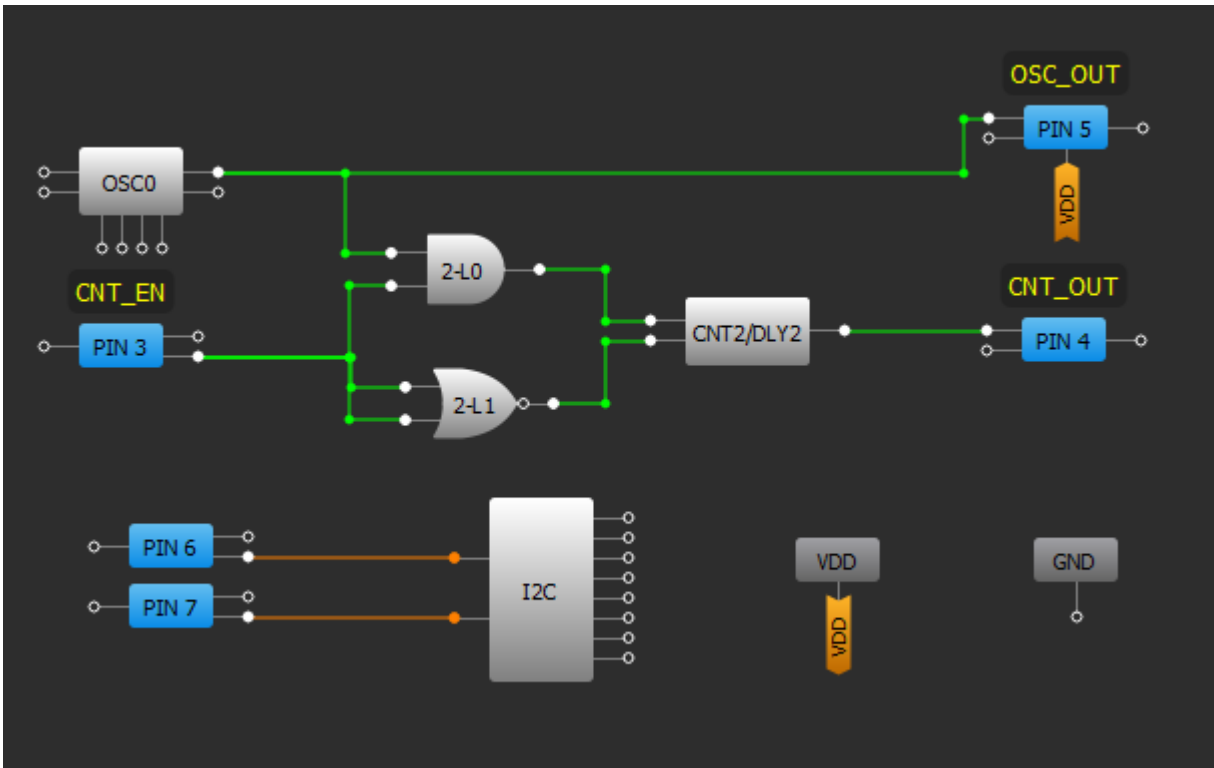


Figure 17. Ready Project in GreenPAK Designer

Use the GreenPAK DIP Development Board to test this project. Connect USB cable to GreenPAK DIP Development Board, if everything is correct, you will see two blinks of green LED, and then LED becomes red. Then press “Emulation” button. This will open emulation tool. Using it you can load code of your project to the chip.

In emulation tool from drop down menu in the right down corner select “GreenPAK DIP Development Board” (see *Figure 18*).



Figure 18. GreenPAK Designer, Emulation Tool

To test this project, we will use the following tools:

- Signal generator. Signal generator is applied to VDD pin to power GreenPAK chip
- Button is a software simulation of the real button. It switches PIN between VDD and GND signal levels

The Signal generator is presented as power source for the GreenPAK chip (at VDD pin). By default, it's configured to output source constant 3.3 V. To see signal generators settings, click on the "Edit" button near the VDD pin (see Figure 19).

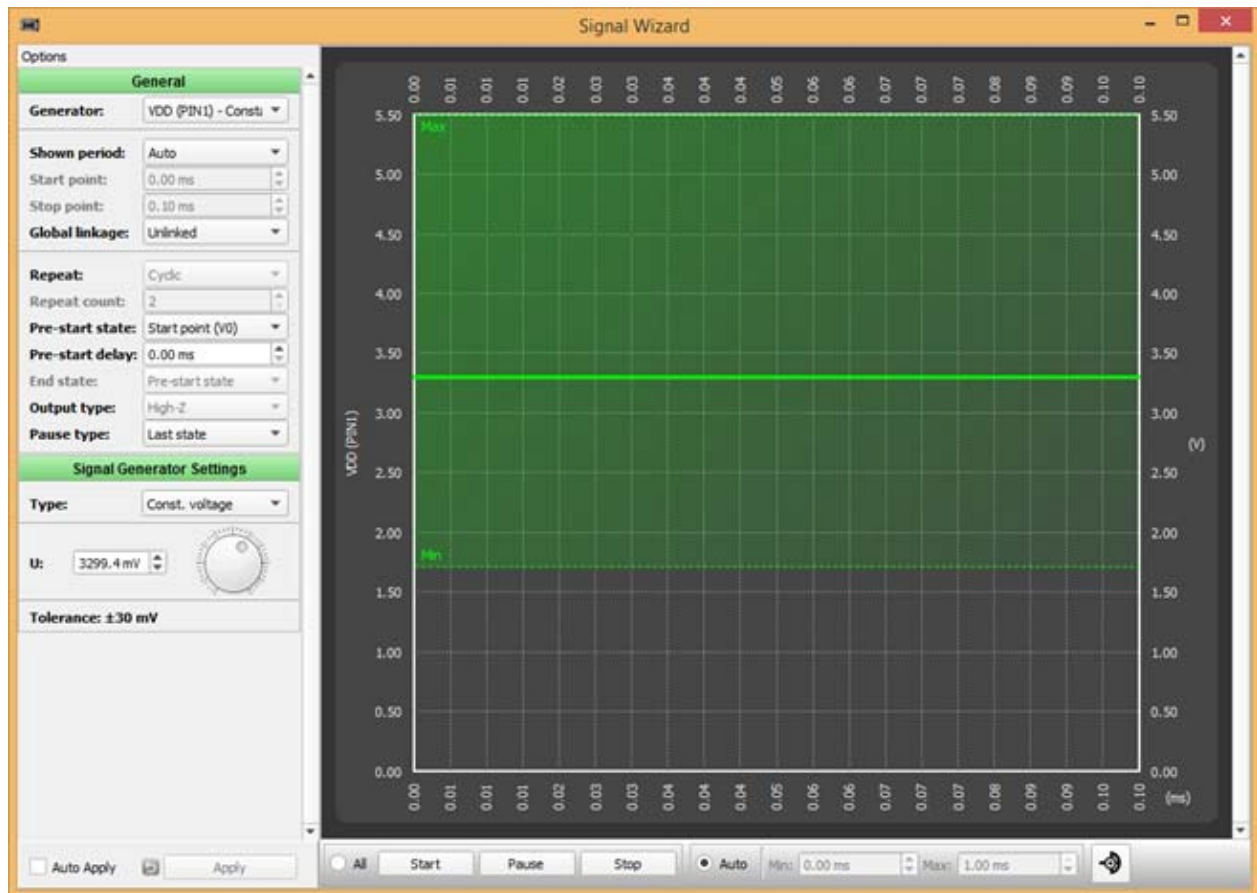


Figure 19. Generator Settings Window

It is necessary to connect virtual button to the PIN3. To do so click on “Button” item in TP3 context menu.

After all settings have done, click button “Emulation” from Emulation Tool window to start emulation process.



Functionality Waveform

Channel 1 (yellow/top) – Oscillator Output

Channel 2 (light blue/2nd line) – Button, 1 - enable Counter; 0 - disable Counter

Channel 3 (magenta/3rd line) – Counter output

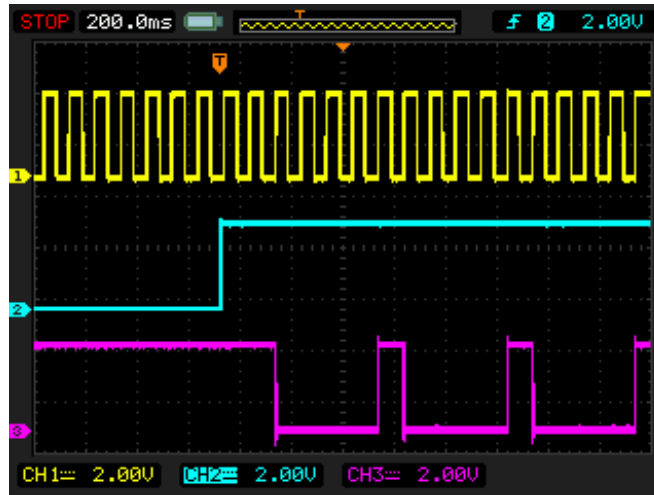


Figure 20. Waveform, Triggered on Button Pressed

Channel 1 (yellow/top) – Oscillator Output

Channel 2 (light blue/2nd line) – Button, 1 - enable Counter; 0 - disable Counter

Channel 3 (magenta/3rd line) – Counter output

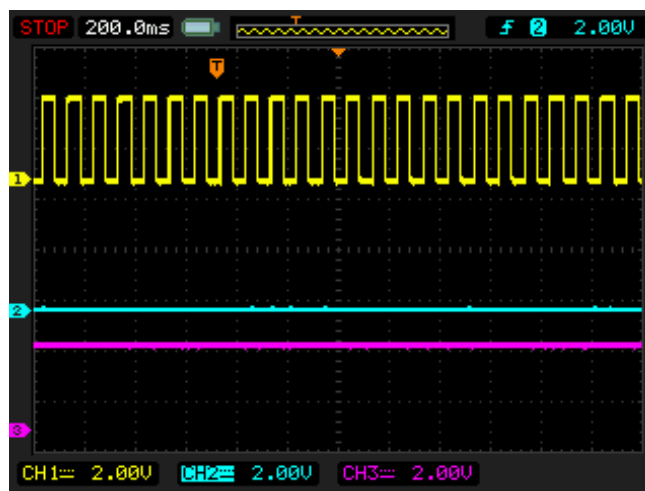


Figure 21. Waveform, no Triggered on Button Released



Channel 1 (yellow/top) – Oscillator Output
Channel 2 (light blue/2nd line) – Button, 1 - enable Counter; 0 - disable Counter
Channel 3 (magenta/3rd line) – Counter output

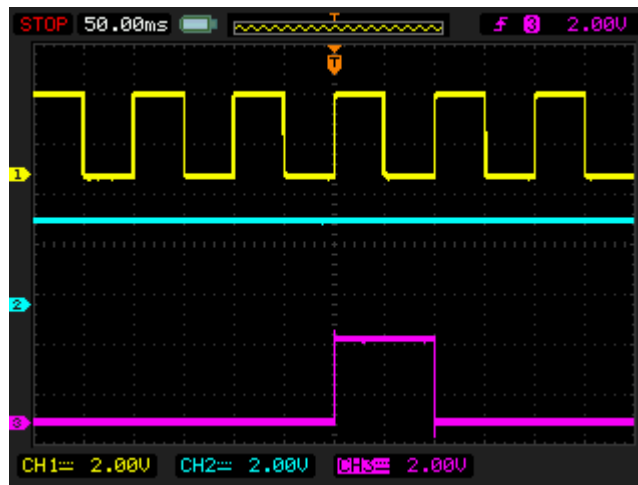


Figure 22. Waveform of the Pulse Width of the Logic Generator and Count End Signal

As shown on *Figure 21* and *Figure 22* Counter works only when the button is pressed.



Conclusion

This Development Platform is a truly versatile tool. It allows the designer to create a custom project within minutes.

For more information please visit our website <http://www.silego.com/>.



5 Appendix A - Electrical Specification

Mode	Parameter	Min.	Typ.	Max.	Units
General	Test Point Capacitance	20	--	--	pF
	Input Leakage Current	--	--	1	uA
	Max. Current through Protection Diode to VDD	--	--	0.1	mA
Power Supply	Voltage Range	1.7	--	5.5	V
	VDD Max. Current	--	--	100	mA
	Voltage Output Total Error	--	--	±30	mV
Virtual Button, VDD/GND, Pull Up/Down Driver	Output Level High	--	VDD	--	--
	Output Level Low	--	GND	--	--
	Strong Drive (VDD/GND) Resistance	--	100	--	Ω
	Pull Up/Down Resistance	3.5	5.6	8.5	kΩ
Expansion Connector Switch	Max. Voltage	--	--	5.5	V
	Continuous Current through Any Terminal	--	--	±400	mA
	Switch On-Resistance	--	1.2		Ω
	External VDD Switch On-Resistance	--	1.2		Ω
	On Leakage Current	-1	--	1	uA
	Off Leakage Current	-1	--	1	uA