# KPS-MCL Low-Loss High Temperature 200°C SMPS Stacks, 200 – 2,000 VDC (Industrial Grade)

## Overview

KEMET Power Solutions - Low loss (KPS MCL) High Temperature SMPS Ceramic Stacked Capacitors combine a robust and proprietary C0G/NPO base metal electrode (BME) dielectric system with a durable lead-frame technology for high temperature and high power SMPS applications. These devices are specifically designed to withstand the demands of harsh industrial environments such as down-hole oil exploration and automotive/avionics engine compartment circuitry.

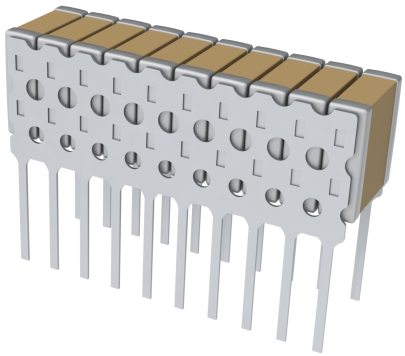
The KPS-MCL is constructed with large chip multilayer ceramic capacitors (MLCCs), vertically stacked and secured to a lead-frame termination system, using a high melting point (HMP) solder alloy. Vertically stacking the capacitors in lead frames allows for much lower ESR (low loss) and thermal resistance, which translates to very high ripple current capability. The lead-frame isolates the MLCCs from the printed circuit board (PCB), while establishing a parallel circuit configuration.

Mechanically isolating the capacitors from the PCB improves mechanical and thermal stress performance, while the parallel circuit configuration allows for bulk capacitance in the same or smaller design footprint.

KEMET's high temperature C0G capacitors are temperature-compensating and are well suited for resonant circuit applications, or for those where Q and stability of capacitance characteristics are required. They exhibit no change in capacitance with respect to time and voltage, and boast a negligible change in capacitance with reference to ambient temperature. Capacitance change is limited to ±30 ppm/ºC from −55°C to +200°C. In addition, these capacitors exhibit high insulation resistance with low dissipation factor at elevated temperatures up to +200°C. They also exhibit low ESR at high frequencies and offer greater volumetric efficiency over competitive high temperature BME ceramic capacitor devices.

## Benefits

- Low-Loss
- Low ESR and ESL
- High thermal stability
- High ripple current capability
- Straight Pin lead wires for "through-hole" mounting
- Formed "J" and "L" lead wires for surface mounting
- Operating temperature range of −55°C to +200°C
- Case Codes (Case Sizes) – 69 (2220) and 70 (2225)
- DC voltage ratings of 200 – 2,000 V
- Capacitance offerings ranging from 11 nF – 1.2 µF
- Industrial grade
- High frequency performance and bulk capacitance in a reduced footprint



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## Applications

- Industrial
- Down-hole
- Defense and aerospace
- Hybrid and Electric Vehicles (HEVs, BEVs)
- SMPS
- Input and output filtering on power supplies, often found on “capacitor banks“
- Snubber circuits and DC link
- Resonator circuits

## Ordering Information

| L1 | G | N | 69 | C | 224 | K | A | 03 |
|---|---|---|---|---|---|---|---|---|
| Product Family | Dielectric Classification/ Characteristic | Lead Configuration[1] | Case Size/ Case Code (CC) | Rated Voltage (DC) | Capacitance Code (pF) | Capacitance Tolerance | Lead/ Termination Finish[2] | Number of Chips |
| L1 | G = 200°C C0G (BME) | N = Straight pin<br>L = Formed "L"<br>J = Formed "J" | 69<br>70 | 2 = 200 V<br>C = 500 V<br>B = 630 V<br>D = 1,000 V<br>F = 1,500 V<br>G = 2,000 V | Two Significant Digits and number of zeros | J = ±5%<br>K = ±10% | A = Silver<br>H = Solder Coated (60/40) | 03 – 3 Chips<br>05 – 5 Chips<br>10 – 10 Chips |

*[1] Lead configuration and dimension details are outlined in the "Dimensions" section of this document. Additional lead configurations may be available. Contact KEMET for details.*

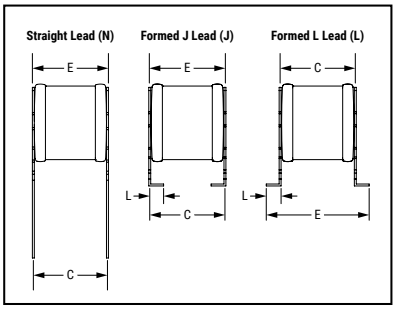
*[2] Solder coated (60/40) lead termination finish (H) only available for Straight pin (N) lead configuration.*

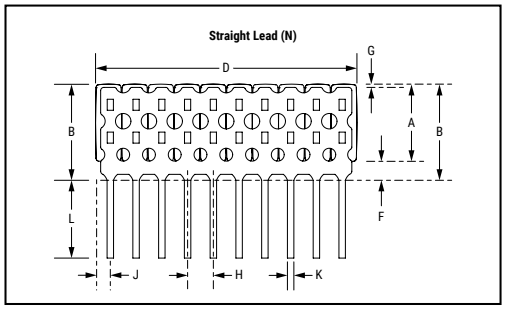
## Lead Configurations – Inches (Millimeters)

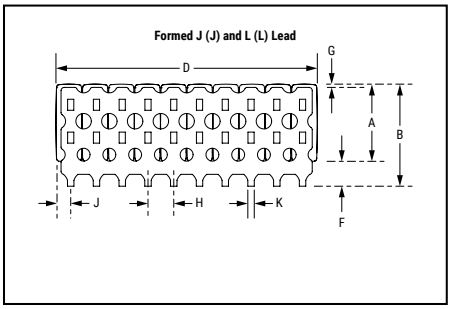
| Lead Style Symbol | Lead Style | L Lead Length |
|---|---|---|
| N | (N) Straight | 0.250 minimum (6.35) |
| L | (L) Formed | 0.055±0.005 (1.4±0.13) |
| J | (J) Formed | 0.055±0.005 (1.4±0.13) |

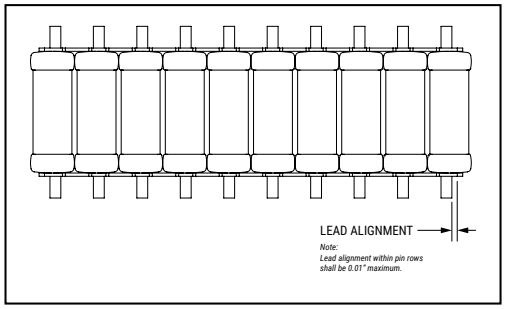
*Additional lead configurations may be available. Contact KEMET for details.*

## Dimensions – Inches (Millimeters)




| Case Code | C Lead Spacing[2] ±0.025 (0.635) | E Length | Number Of Leads Per Side | D Width ±0.025 (0.635) | A Height Maximum | B Height Maximum | H Lead Pitch | K Lead Width | F Seating Plane[1] ±0.010 (0.250) | Mounting Technique |
|---|---|---|---|---|---|---|---|---|---|---|
| 69 | 0.25 (6.35) | For straight lead (N) and (J) lead: E = 0.30 (7.62) maximum<br>For (L) lead: E = 0.38 (9.65) maximum | 3 | 0.32 (8.13) | 0.21 (5.33) | 0.29 (7.37) | 0.1 (2.54) | 0.02 (0.5) | For straight lead (N), seating plane is 0.055"<br>For (L) and (J) lead, seating plane is 0.070" | Solder reflow only |
| | | | 5 | 0.53 (13.5) | | | | | | |
| | | | 10 | 1.06 (26.9) | | | | | | |
| 70 | | | 3 | 0.32 (8.13) | 0.26 (6.60) | 0.34 (8.64) | | | | |
| | | | 5 | 0.53 (13.5) | | | | | | |
| | | | 10 | 1.06 (26.9) | | | | | | |

*[1] Seating plane is the distance between the circuit board and the bottom of the lowest capacitor in the stack.*
*[2] Lead spacing dimension from outside of lead frame.*

## Environmental Compliance

KPS-MCL part types ≥ 500 V with silver (Ag) plating are RoHS compliant with exemption 7a.

## Electrical Parameters/Performance Characteristics

| Item | Parameters/Characteristics |
|---|---|
| Operating Temperature Range | –55°C to +200°C |
| Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC) | ±30 ppm/°C (up to 200°C) |
| Aging Rate (Maximum % Capacitance Loss/Decade Hour) | 0% |
| Dielectric Withstanding Voltage (DWV)[1] | 250% of rated voltage for voltage rating of < 500 V<br>130% of rated voltage for voltage rating of ≥ 500 to < 1,000 V<br>120% of rated voltage for voltage rating of ≥ 1,000 V<br>(5 ±1 seconds and charge/discharge not exceeding 50 mA) |
| Dissipation Factor (DF) Maximum Limit at 25°C[2] | 0.1% |
| Insulation Resistance (IR) Minimum Limit at 25°C[3] | 1,000 MΩ µF or 100 GΩ<br>(Rated voltage applied for 120 ±5 seconds at 25°C) |

*[1] DWV is the voltage a capacitor can withstand for a short period of time. It exceeds the nominal and continuous working voltage of a capacitor.*

*[2] Capacitance and dissipation factor (DF) measured under the following conditions:*

*1 MHz ±100 kHz and 1.0 ±0.2 $V_{rms}$ if capacitance ≤ 1,000 pF.*

*1 kHz ±50 Hz and 1.0 ±0.2 $V_{rms}$ if capacitance > 1,000 pF.*

*[3] To obtain IR limit, divide MΩ - µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.*

*Note: When measuring capacitance, it is important to ensure the set voltage level is held constant. The HP4284 and Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON."*

## Table 1 - Product Ordering Codes & Ratings

| KEMET Part Number[1] | Capacitance (µF)[2,3] | Case Code | Chip Size | Number of Chips | Height A Inch (mm) Maximum | D Inch (mm) Maximum | RoHS Compliance |
|---|---|---|---|---|---|---|---|
| **200 V** | | | | | | | |
| L1G(a)692284(b)(c)03 | 0.28 | 69 | 2220 | 3 | 0.21 (5.3) | 0.32 (8.13) | No |
| L1G(a)702364(b)(c)03 | 0.36 | 70 | 2225 | 3 | 0.26 (6.6) | 0.32 (8.13) | No |
| L1G(a)692464(b)(c)05 | 0.46 | 69 | 2220 | 5 | 0.21 (5.3) | 0.53 (13.5) | No |
| L1G(a)702604(b)(c)05 | 0.6 | 70 | 2225 | 5 | 0.26 (6.6) | 0.53 (13.5) | No |
| L1G(a)692924(b)(c)10 | 0.92 | 69 | 2220 | 10 | 0.21 (5.3) | 1.06 (26.92) | No |
| L1G(a)702125(b)(c)10 | 1.2 | 70 | 2225 | 10 | 0.26 (6.6) | 1.06 (26.92) | No |
| **500 V** | | | | | | | |
| L1G(a)69C114(b)(c)03 | 0.11 | 69 | 2220 | 3 | 0.21 (5.3) | 0.32 (8.13) | |
| L1G(a)70C144(b)(c)03 | 0.14 | 70 | 2225 | 3 | 0.26 (6.6) | 0.32 (8.13) | |
| L1G(a)69C184(b)(c)05 | 0.18 | 69 | 2220 | 5 | 0.21 (5.3) | 0.53 (13.5) | Yes |
| L1G(a)70C234(b)(c)05 | 0.23 | 70 | 2225 | 5 | 0.26 (6.6) | 0.53 (13.5) | (see Note 4) |
| L1G(a)69C364(b)(c)10 | 0.36 | 69 | 2220 | 10 | 0.21 (5.3) | 1.06 (26.9) | |
| L1G(a)70C474(b)(c)10 | 0.47 | 70 | 2225 | 10 | 0.26 (6.6) | 1.06 (26.9) | |
| **630 V** | | | | | | | |
| L1G(a)69B663(b)(c)03 | 0.066 | 69 | 2220 | 3 | 0.21 (5.3) | 0.32 (8.13) | |
| L1G(a)70B843(b)(c)03 | 0.084 | 70 | 2225 | 3 | 0.26 (6.6) | 0.32 (8.13) | |
| L1G(a)69B114(b)(c)05 | 0.11 | 69 | 2220 | 5 | 0.21 (5.3) | 0.53 (13.5) | Yes |
| L1G(a)70B144(b)(c)05 | 0.14 | 70 | 2225 | 5 | 0.26 (6.6) | 0.53 (13.5) | (see Note 4) |
| L1G(a)69B224(b)(c)10 | 0.22 | 69 | 2220 | 10 | 0.21 (5.3) | 1.06 (26.9) | |
| L1G(a)70B284(b)(c)10 | 0.28 | 70 | 2225 | 10 | 0.26 (6.6) | 1.06 (26.9) | |
| **1,000 V** | | | | | | | |
| L1G(a)69D393(b)(c)03 | 0.039 | 69 | 2220 | 3 | 0.21 (5.3) | 0.32 (8.13) | |
| L1G(a)70D543(b)(c)03 | 0.054 | 70 | 2225 | 3 | 0.26 (6.6) | 0.32 (8.13) | |
| L1G(a)69D653(b)(c)05 | 0.065 | 69 | 2220 | 5 | 0.21 (5.3) | 0.53 (13.5) | Yes |
| L1G(a)70D903(b)(c)05 | 0.090 | 70 | 2225 | 5 | 0.26 (6.6) | 0.53 (13.5) | (see Note 4) |
| L1G(a)69D134(b)(c)10 | 0.130 | 69 | 2220 | 10 | 0.21 (5.3) | 1.06 (26.9) | |
| L1G(a)70D184(b)(c)10 | 0.180 | 70 | 2225 | 10 | 0.26 (6.6) | 1.06 (26.9) | |
| **1,500 V** | | | | | | | |
| L1G(a)69F163(b)(c)03 | 0.016 | 69 | 2220 | 3 | 0.21 (5.3) | 0.32 (8.13) | |
| L1G(a)70F203(b)(c)03 | 0.020 | 70 | 2225 | 3 | 0.26 (6.6) | 0.32 (8.13) | |
| L1G(a)69F273(b)(c)05 | 0.027 | 69 | 2220 | 5 | 0.21 (5.3) | 0.53 (13.5) | Yes |
| L1G(a)70F343(b)(c)05 | 0.034 | 70 | 2225 | 5 | 0.26 (6.6) | 0.53 (13.5) | (see Note 4) |
| L1G(a)69F533(b)(c)10 | 0.053 | 69 | 2220 | 10 | 0.21 (5.3) | 1.06 (26.9) | |
| L1G(a)70F683(b)(c)10 | 0.068 | 70 | 2225 | 10 | 0.26 (6.6) | 1.06 (26.9) | |
| **2,000 V** | | | | | | | |
| L1G(a)69G113(b)(c)03 | 0.011 | 69 | 2220 | 3 | 0.21 (5.3) | 0.32 (8.13) | |
| L1G(a)70G143(b)(c)03 | 0.014 | 70 | 2225 | 3 | 0.26 (6.6) | 0.32 (8.13) | |
| L1G(a)69G183(b)(c)05 | 0.018 | 69 | 2220 | 5 | 0.21 (5.3) | 0.53 (13.5) | Yes |
| L1G(a)70G233(b)(c)05 | 0.023 | 70 | 2225 | 5 | 0.26 (6.6) | 0.53 (13.5) | (see Note 4) |
| L1G(a)69G363(b)(c)10 | 0.036 | 69 | 2220 | 10 | 0.21 (5.3) | 1.06 (26.9) | |
| L1G(a)70G473(b)(c)10 | 0.047 | 70 | 2225 | 10 | 0.26 (6.6) | 1.06 (26.9) | |
| **KEMET Part Number[1]** | **Capacitance (µF)[2,3]** | **Case Code** | **Chip Size** | **Number of Chips** | **Height A Inch (mm) Maximum** | **D Inch (mm) Maximum** | **RoHS Compliance** |

*[1] Complete part number requires additional characters in the numbered positions provided in order to indicate lead configuration, capacitance tolerance and lead finish. For each numbered position, available options are as follows:*

*(a) Lead style character "N," "L," or "J."*

*(b) Capacitance tolerance character "J" or "K."*

*(c) Lead finish character "A" for 100% Ag, "H" for solder coated.*

*[2] Capacitance values listed are for stacked components and do not follow E12, E24 format defined by BS 2488 standard. Please contact factory to inquire about capacitance values not listed.*

*[3] Identical capacitance values may be listed for the same voltage rating. User can select which case size and chip count is desired for the given capacitance value.*

*[4] KPS-MCL Stacked Capacitors ≥ 500 V with Ag plating are RoHS compliant by exemption 7a.*

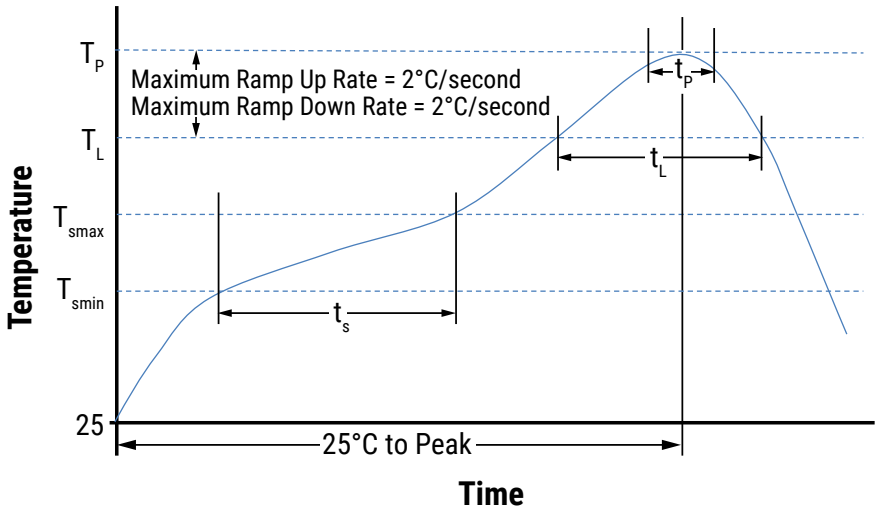
## Soldering Process

The capacitors and assemblies outlined in this specification sheet are susceptible to thermal shock damage due to their large ceramic mass. Temperature profiles used should provide adequate temperature rise and cool-down time to prevent damage from thermal shock. In general, KEMET recommends against hand-soldering for these types of large ceramic devices, but if hand-soldering cannot be avoided, refer to hand-soldering section below.

**Recommended Soldering Technique:**

- Solder reflow

**Recommended Reflow Soldering Profile:**




| Profile Feature | Sn-Pb | Pb-Free |
|---|---|---|
| **Preheat/Soak** | | |
| Temperature Minimum ($T_{Smin}$) | 100°C | 150°C |
| Temperature Maximum ($T_{Smax}$) | 150°C | 200°C |
| Time ($t_s$) from $T_{smin}$ to $T_{smax}$) | 60 – 90 seconds | 60 – 120 seconds |
| Ramp-up rate ($T_L$ to $T_P$) | 2°C/second | 3°C/second |
| Liquidous temperature ($T_L$) | 183°C | 217°C |
| Time above liquidous ($t_L$) | 95 seconds | 95 seconds |
| Peak temperature ($T_P$) | 240°C | 260°C |
| Time within 5°C of maximum peak temperature ($t_P$) | 5 seconds | 5 seconds |
| Ramp-down rate ($T_P$ to $T_L$) | 2°C/second | 2°C/second |
| Time 25°C to peak temperature | 3.5 minutes | 3.5 minutes |

*Note: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow.*

***Preheating and Reflow Profile Notes:***

*Due to the differences in the coefficient of the thermal expansion for the different materials of construction, it is critical to monitor and control the heating and cooling rates during the soldering process. To ensure optimal component reliability, KEMET's recommended heating and cooling rate is 2°C/second. After soldering, the capacitors should be air cooled to room temperature before further processing. Forced air cooling is not recommended.*

## Soldering Process cont.

**Recommendations for Hand-Soldering:**
Care should be taken when hand-soldering large ceramic stacks. Excessive thermal shock on the ceramic material can lead to cracking and reliability issues. To reduce risk of thermal shock, KEMET recommends solder reflow, but if hand soldering cannot be avoided, please see recommended guidelines below.

**Pre-Heating**
Stacks should be preheated to a temperature within 50°C of reflow temperature. KEMET recommends a ramp rate of 2°C/second to avoid thermal shock during the pre-heating process.

**Hand-Soldering**
When using a solder iron, keep tip of the iron as far away from ceramic body to avoid excessive heating.

**Cool Down**
After reflow, stacks should be allowed to cool at a preferable rate of 2°C/second until room temperature is reached.

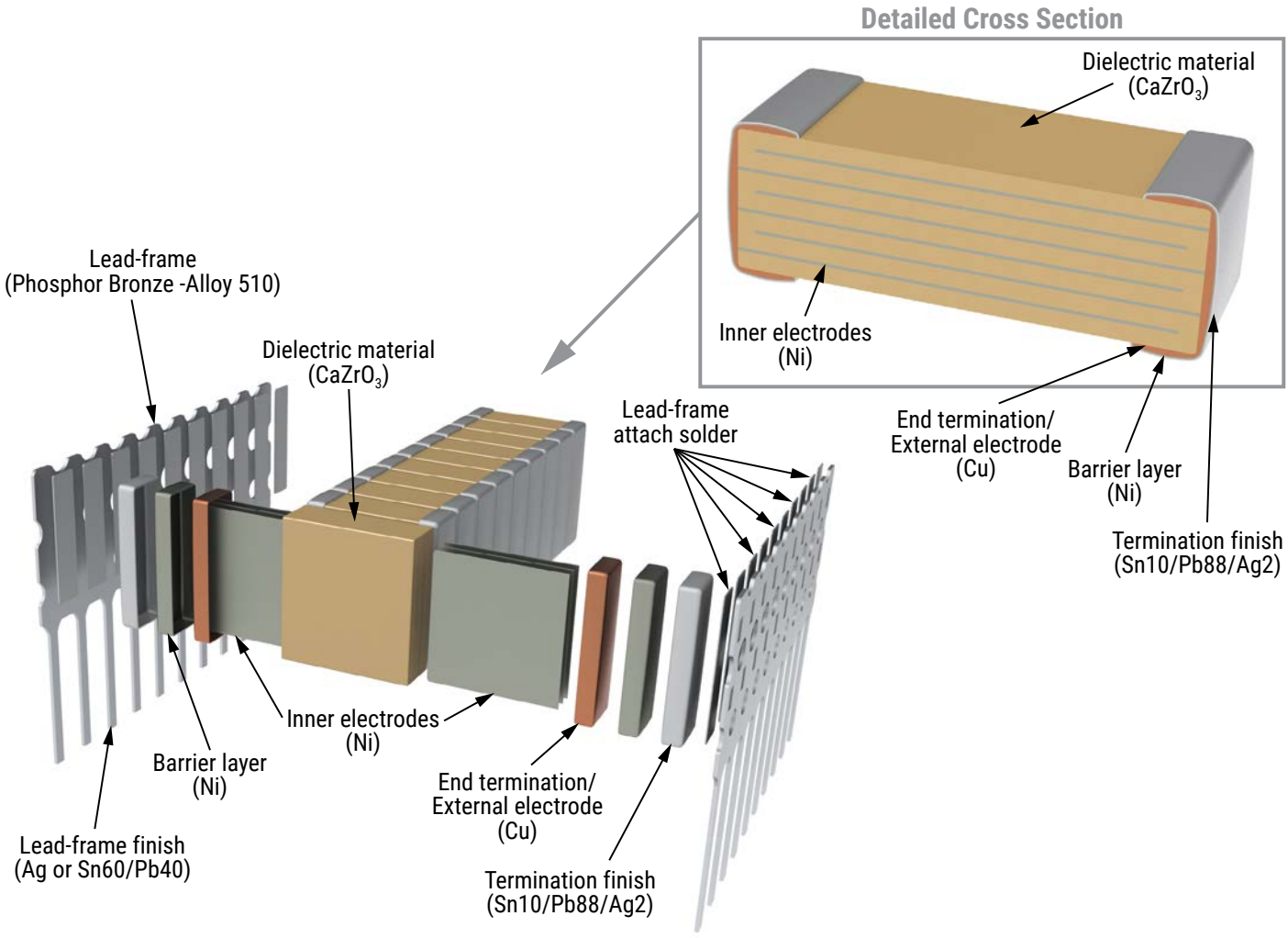
## Storage & Handling

Ceramic capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature–reels and may soften or warp, and tape peel force may increase. KEMET recommends that maximum storage temperature does not exceed 40°C and maximum storage humidity does not exceed 70% relative humidity. Temperature fluctuations should be minimized to avoid condensation on the parts. Atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability chip stock should be used promptly, preferably within 1.5 years of receipt.

## Table 2 - Performance & Reliability: Test Methods & Conditions

| Inspection | Test Method | Test Conditions |
|---|---|---|
| **Reliability/Environmental Tests** | | |
| High Temperature Life | MIL–STD–202, Method 108 | 200°C, rated voltage, 1,000 hours |
| Temperature Cycling | JESD22, Method JA–104 | –55°C to +200°C, 300 cycles |
| Thermal Shock | MIL–STD–202, Method 107 | –55°C to +200°C, 20 seconds transfer, 15 minutes dwell, 20 cycles |
| Moisture Resistance | MIL–STD–202, Method 106 | 20 cycles, no voltage applied |
| **Physical, Mechanical and Process Tests** | | |
| Vibration | MIL–STD–202, Method 204 | Condition D per MIL–PRF–49470, simple harmonic, 20 g peak, 10 – 2,000 Hz, 20 minute sweep, 12 sweeps per axis |
| Resistance to Soldering Heat | MIL–STD–202, Method 210 | Condition B, 260°C, 10 seconds |
| Terminal Strength | MIL–STD–202, Method 202 | Condition A |
| Immersion | MIL–STD–202, Method 104 | Condition B |
| Solderability | J–STD–002C | Category 3<br>For Sn-Pb solder alloy:<br>Method A, 245°C, 5 seconds<br>Method S, 220°C peak<br>For Pb-Free solder alloy:<br>Method A1, 260°C, 5 seconds<br>Method S1, 245°C peak |

## Construction




## Packaging

**Waffle Packaging Quantities**

| Case Code | Lead Style | Number of Chips in Stack | Waffle Pack Quantity[1] |
|---|---|---|---|
| 69 | L/J/N | 3 and 5 | 50 |
| | | 10 | 25 |
| 70 | L/J/N | 3 and 5 | 50 |
| | | 10 | 25 |

[1] *Minimum order value applies. Contact KEMET for details.*

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Although KEMET designs and manufactures its products to the most stringent quality and safety standards, given the current state of the art, isolated component failures may still occur. Accordingly, customer applications which require a high degree of reliability or safety should employ suitable designs or other safeguards (such as installation of protective circuitry or redundancies) in order to ensure that the failure of an electrical component does not result in a risk of personal injury or property damage.

Although all product–related warnings, cautions and notes must be observed, the customer should not assume that all safety measures are indicted or that other measures may not be required.