PROTO-1

Prototyping Board

User Manual

Proto-1

User Manual

Document Part N°	0127-0156
Document Reference	0127-0156.Doc
Document Issue Level	0.2
Manual covers PCBs identified	Proto 1 Rev A

Blue Chip Technology Ltd.
Chowley Oak, Tattenhall
Chester, Cheshire
CH3 9EX.
Telephone : 01829 772000 Facsimile : 01829 772001.

Amendment History

Issue Level	Issue Date	Author	Amendment Details
0.1	11.09.89	L.C	First draft
0.2	14.10.97	SEJ	Window front cover and logo

OUTLINE DESCRIPTION

PROTO-1 provides a means of rapidly developing I/O mapped PC bus cards. It is ideal for prototyping I/O cards and other interfacing cards.

The full length PC card includes the logic necessary to interface with the PC bus. A selectable base address can be set in the range 0-3FFF Hex and the board can occupy up to 32 ports from this base port.

Both Data bus and Address bus are buffered and decoded D0-D7 and A0-A4 respectively. Control lines I/O Read/Write (IORD, IOWR) and Memory Read/Write (MRD, MWR) are also provided together with all voltage rails.

An extensive patch area with 1.0mm holes is available to mount IC's resistors and other components.

1.0 SPECIFICATION

1.1 Electrical Specification

Number of Ports Used	16
Power Requirement	5V D.C
Power Dissipation	150mW

1.2 Physical Specification

Height	107mm
Width	11mm
Length	335.5mm

1.3 Prototyping Area

Component Points (2000)	1mm
Pads	1.5mm
Pitch	2.54mm

Note: The total width of the card should not exceed 12.7mm.

Electromagnetic Compatibility (EMC)

The PROTO-1 prototyping card is an incomplete design and is a development tool. It has a PC bus interface and address decoder built on the board and a large wire-wrap area onto which the user builds his own prototype circuitry. The board is not intended for use without modification by the user.

Since it can have no function in the form that it is supplied, it is classed as a component and as such is excluded from the scope of the EMC Directive (89/336/EEC) and is not required to be CE marked.

It is the responsibility of the OEM to ensure that his product meets the requirements of the Directive. The following advice is offered in good faith to facilitate meeting the requirements, but Blue Chip Technology cannot accept responsibility for the compliance of the final equipment.

- The OEM should ensure that he understands which of the standards are applicable to his product. Where specific standards exist for a product type these will take precedence over any generic standards.

- The board must be installed in a computer system which provides screening suitable for the required environment.

- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.

- The board must be installed with the backplate securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact. The backplate provides the earth path for interference on the external cabling, preventing it getting into or out of the PC.

- Most EMC problems are caused by the external cabling to the board. Analogue boards require particularly careful installation of the external cabling. It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal end bracket of the board and hence to earth. The cabling must be totally screened. Round screened cables with a braided wire screen should be used in preference to those with a foil screen and drain wire. Use metal connector shells which connect around the full circumference of the screen; they are far superior to those which earth the screen by a simple “pig-tail”. Standard ribbon cables will not be adequate unless contained wholly within the cabinetry housing the industrial PC.

- If difficulty with interference is experienced the external cable should also be fitted with a ferrite clamp as close possible to the connector. A suitable type is the Chomerics clip-on style, type H8FE-1004-AS.

- It is recommended that cables are kept as short as possible, particularly when dealing with low level signals. Cables carrying TTL signals should not exceed 2 metres in length.

- Ensure that the screen of the external cable is bonded to a good RF earth at the remote end of the cable.

2.0 USER ADJUSTMENTS

2.1 Selecting the Base Address

The board may be located in any 62 pin slot in the PC motherboard but must be set up to appear at a specified position (or 'address') in the port map. Available positions are shown in the IBM-PC Technical Reference Guide. However, for those who do not possess a copy of this document a good place is the location normally allocated to the prototyping card as supplied by IBM. This address is 300 Hex or 768 decimal.

All Blue Chip Technology cards are preset to this address at the factory. However, no two devices should be used while set to the same address since contention will occur and neither board will work. If your machine contains a card with a conflicting address then another reasonably safe address is 200 to 21F (Hex).

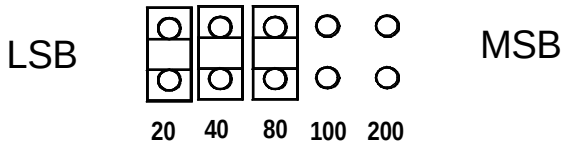
A set of links is provided on the board to set the base address of the board within the IBM-PC port map. The address is in binary with the presence of a link representing a 0 and the absence of a link representing a 1.

To set the base address to 768 Decimal (300 Hex) set the following pattern on the links as indicated below:

Figure 1 - Selecting the Base Address

Note: View board with back panel on RHS.

Middle 5 Bits of port address on links.



More example addresses are shown in Appendix A.

Note: No two cards must occupy the same address.

2.2 Port Map

The PROTO-1 occupies 16 input/output ports with 7 chip selects programmed to appear over set intervals within those ports (see below).

Address	Chip Select	Access
Base + 0	1	Read Only
Base + 1	2	Write Only
Base + 2	3	Read/Write
Base + 3	4	Read/Write
Base + 4	4	Read/Write
Base + 5	5	Read/Write
Base + 6	5	Read/Write
Base + 7	5	Read/Write
Base + 8	6	Read/Write
Base + 9	6	Read/Write
Base + 10	6	Read/Write
Base + 11	6	Read/Write
Base + 12	7	Read/Write
Base + 13	7	Read/Write
Base + 14	7	Read/Write
Base + 15	7	Read/Write

These chip selects are generated by the PAL in the IC2 position. To review the source listing see Appendix H.

3.0 ELECTRICAL OPTIONS

3.1 Board Voltages

The PROTO-1 contains all the PC voltage and ground rails. Each bus is situated between the patch area and the interfacing circuitry (see Appendix F), with the ground bus on the front (component side) and the +/-5V, +/-12V busses on the back (pin side).

3.2 PC Bus Lines

The following bus lines are brought onto the PROTO-1 board and buffered and can thus be loaded with up to 10 LS TTL loads.

DO-D7 (Bi-directional)
A0-A4
IOR, IOW
MEMR, MEMW

The data bus buffer direction is controlled by the board I/O read signal. All other PC lines are accessible and can be loaded with a maximum of 2 LS TTL loads.

3.3 Input/Output Connections

Because there may be a large number of options interfaced to the system, the computer's I/O bus loading should be limited to 2 LS TTL loads.

The current requirements of circuitry in the prototyping area should not exceed the following values.

+5V	1.5 Amp
+12V	0.5 Amp
-12V	0.1 Amp

3.4 Input/Output Connections

A 50 way insulation displacement connector (IDC) is located at the front of the PROTO-1 for connection to the outside circuitry.

Blue Chip Technology offer a range of screw terminal adaptors and signal conditioning cards that are compatible with your PROTO-1 board.

4.0 SOFTWARE DISK

Along with your PROTO-1 board you will also have received a floppy disk which contains the following files:

READPORT.BAS
READPORT.EXE
PROT.PLD
PROT.JED

The basic program READPORT.BAS is compatible with GWBASIC and can run on any IBM-PC or compatible with a copy of GWBASIC. The executable program is the compiled version and can thus be run from the command prompt.

The files PROT.PLD and PROT.JED are the PAL equation listing and Jedec file respectively generated by CUPL (The universal compiler for programming logic), for the 1618a PAL located in the IC2 chip socket on the PROTO-1.

The CUPL equation listing can be seen in Appendix H.

4.1 Readport

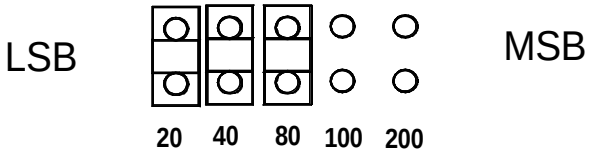
Readport prompts for the I/O address that you have set your board to appear at, the minimum 1, maximum 18) and then displays those ports on screen. By using the keys shown in the program you can step or jump, forward or backward one or multiple port (s) at a time, or move the entire window up or down the port map.

Whilst every effort has been taken to ensure that the information provided is accurate, Blue Chip Technology cannot assume responsibility for any errors in this manual or their consequences. Should any errors be detected, the company would greatly appreciate being informed of them. A policy of continuos product development is operated, resulting in the contents of this document being subject to change without notice.

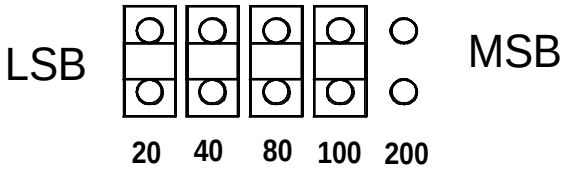
APPENDIX A

(Note: View board with back panel on RHS).

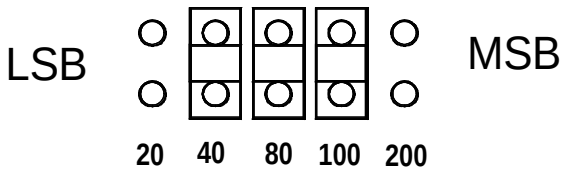
Address Settings for Port 300H



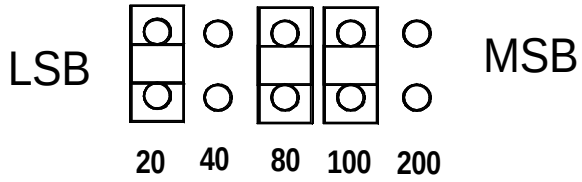
Address Settings for Port 200H



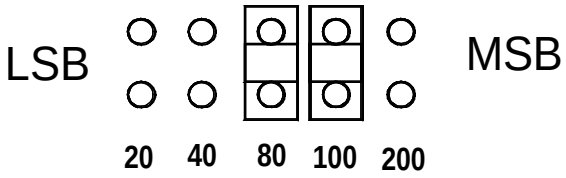
Address Settings for Port 220H



Address Settings for Port 240H



Address Settings for Port 260H



APPENDIX B

PC/XT/AT Port Map

I/O Address Map

Address	Allocated to:
000-01F	DMA Controller 1 (8237A-5)
020-03F	Interrupt Controller 1 (8259A)
040-05F	Timer (8254)
060-06F	Keyboard Controller (8742) Control Port B
070-07F	RTC and CMOS RAM, NMI Mask (Write)
080-09F	DMA Page Register (Memory Mapper)
0A0-0BF	Interrupt Controller 2 (8259)
0F0	Clear NPX (80287) Busy
0F1	Reset NPX (80287)
0F8-0FF	Numeric Processor Extension (80287)
1F0-1F8	Hard Disk Drive Controller
200-207	Reserved
278-27F	Reserved for Parallel Printer Port 2
2F8-2FF	Reserved for Serial Port 2
300-31F	Reserved
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	Reserved for SDLC Communications, Bisync 2
3A0-3AF	Reserved for Bisync 1
3B0-3BF	Reserved
3C0-3CF	Reserved
3D0-3DF	Display Controller
3F0-3F7	Diskette Drive Controller
3F8-3FF	Serial Port 1

APPENDIX C

PC/XT Interrupt Map

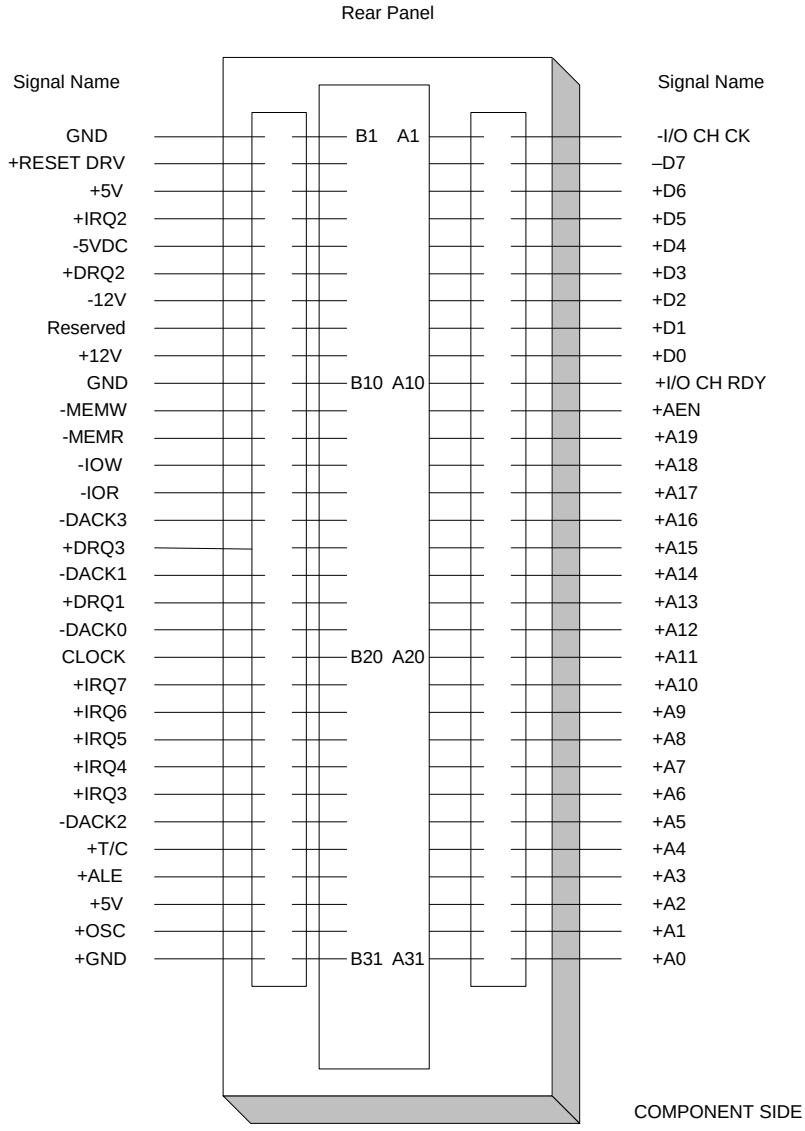
Number	Allocated to:
NMI	Parity
0	Timer
1	Keyboard
2	Reserved
3	Asynchronous Communications (Secondary) SDLC Communications
4	Asynchronous Communications (Primary) SDLC Communications
5	Fixed Disk
6	Diskette
7	Parallel Printer

APPENDIX D

PC/AT Interrupt Map

Level		Allocated to:
Microprocessor NMI		Parity or I/O Channel Check
CTLR 1	CTLR 2	(Interrupt Controllers)
IRQ 0		Timer Output 0
IRQ 1		Keyboard (Output Buffer Full)
IRQ 2		Interrupt from CTLR 2
	IRQ 8	Real-time Clock Interrupt
	IRQ 9	Software Redirected to INT 0AH (IRQ 2)
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Co-processor
	IRQ 14	Fixed Disk Controller
	IRQ 15	Reserved
IRQ 3		Serial Port 2
IRQ 4		Serial Port 1
IRQ 5		Parallel Port 2
IRQ 6		Diskette Controller
IRQ 7		Parallel Port 1

APPENDIX G


Rear Panel
Signal Name
Signal Name
GND
+RESET DRV
+5V
+IRQ2
-5VDC
+DRQ2
-12V
Reserved
+12V
GND
-MEMW
-MEMR
-IOW
-IOR
-DACK3
+DRQ3
-DACK1
+DRQ1
-DACK0
CLOCK
+IRQ7
+IRQ6
+IRQ5
+IRQ4
+IRQ3
-DACK2
+T/C
+ALE
+5V
+OSC
+GND
B1 A1
B10 A10
B20 A20
B31 A31
-I/O CH CK
–D7
+D6
+D5
+D4
+D3
+D2
+D1
+D0
+I/O CH RDY
+AEN
+A19
+A18
+A17
+A16
+A15
+A14
+A13
+A12
+A11
+A10
+A9
+A8
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
COMPONENT SIDE