DPA-Switch™ DC-DC Forward Converter Design Guide

Application Note AN-31

Introduction

The single-ended forward converter topology is usually the best solution for DC-DC applications in industrial controls, Telecom central office equipment, digital feature phones, and systems that use distributed power architectures.

The feature set of *DPA-Switch* offers the following advantages in DC-DC single-ended forward converter designs:

- Low component count
- High efficiency (typically >91% with synchronous rectification)
- Built in soft-start to minimize stress and overshoot
- Built in accurate line under-voltage detection
- Built-in accurate line overvoltage shutdown protection
- Built in adjustable current limit
- Built-in overload and open loop fault protection
- Built-in thermal shutdown
- Programmable duty cycle reduction to limit duty cycle excursion at high line and transient load conditions
- Very good light-load efficiency
- Selectable 300 kHz or 400 kHz operation
- Lossless integrated cycle-by-cycle current limit

The example circuits in this design guide illustrate the use of these and other features of *DPA-Switch*.

Scope

This document gives guidance for the design of a single-ended forward converter with *DPA-Switch* in applications that require a single output voltage. It is intended for systems engineers and circuit designers who wish to become familiar with the capabilities and requirements of *DPA-Switch* in DC-DC applications. This application note provides background material that will assist users of the *DPA-Switch* DC-DC forward converter design utility that is included in the software design tool, *PI Expert*. Subsequent application notes will provide comprehensive procedures for designs of greater complexity. Designers are advised to check Power Integrations' Web site at *www.powerint.com* for the latest application information and design tools.

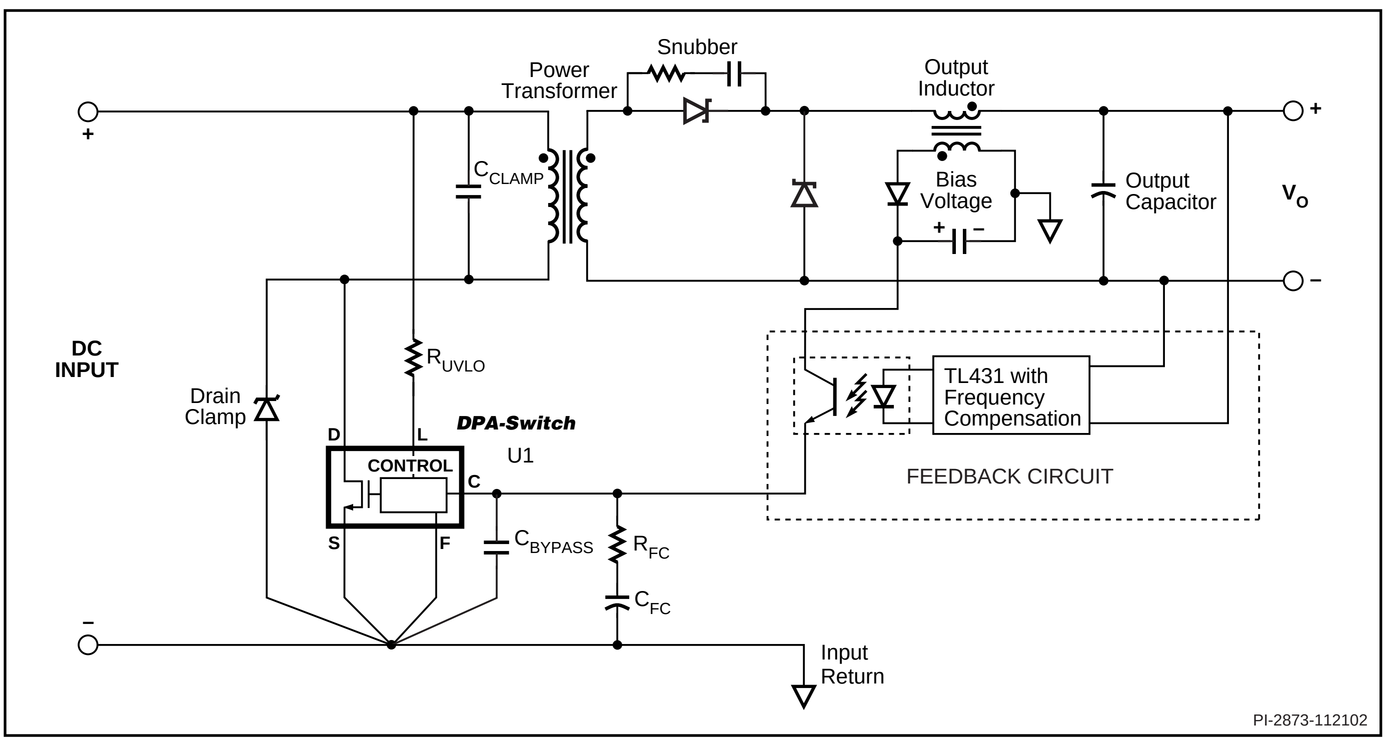

Figure 1. Typical Configuration of DPA-Switch in a Single-Ended DC-DC Forward Converter with One Output.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Input Voltage	V_{IN}	36	48	75	VDC	Typical operational range
Input Voltage UV Turn On				36	VDC	
Input Voltage UV Turn Off		29			VDC	
Input Voltage OV Turn On				72	VDC	
Input Voltage OV Turn Off				90	VDC	
Output						
Output Voltage	V_{OUT}	4.8	5.00	5.2	V	±4%
Output Ripple and Noise	V_{RIPPLE}		50		mV	20 MHz Bandwidth
Output Current	I_{OUT}	0		6.00	A	
Line Regulation			±0.2	%		
Load Regulation			±0.5	%		
Transient Response Peak Deviation			3		% of V_{OUT}	50-75% load step, 100 mA/μs 48 VDC input
Transient Response Recovery			200		μs	To 1% of final output voltage, 50-75% load step 48 VDC input
Total Output Power						
Continuous Output Power	P_{OUT}			30	W	
Efficiency						
Low-Cost design	η_{Cost}		84		%	Measured at P_{OUT} (30 W), 25 °C, 48 VDC Input
Enhanced (non-sync rect)	$\eta_{Enhanced}$		87		%	
Synchronous rectified design	$\eta_{SyncRect}$		91		%	
Environmental						
Input-Output Isolation Voltage		1500			VDC	
Ambient Temperature	T_{AMB}	-40		85	°C	Free convection, sea level

Table 1. Typical Specifications for a Single Output DC-DC Converter.

Figure 1 shows a typical implementation of *DPA-Switch* in a power supply with a single regulated output. This design guide discusses considerations for selection of components for a practical implementation of the circuit in Figure 1. It also addresses options and tradeoffs in cost, efficiency and complexity that include the substitution of synchronous rectifiers and alternative generation of the bias voltage.

System Requirements

The design begins with an evaluation of the requirements. Table 1 gives the specifications for the example converters described here, that have been constructed and evaluated as engineering prototypes. Variants of the basic design achieve higher efficiencies with minor increases in complexity.

Input Voltage Range

The actual input voltage range required for operation of the converter is greater than that indicated by the specification. The specification requires the converter to operate and to deliver full performance at a minimum input of 36 V. Therefore, the designer must guarantee that the converter becomes active and fully functional at a voltage that is lower than the minimum.

Tolerance variations of the Line Undervoltage Threshold of *DPA-Switch* with prudent design margin put the practical minimum operating voltage closer to 30 V. Similarly, the converter must be designed to operate at voltages higher than the maximum specified input. The actual input voltage range should be considered to be from about 30 V to 90 V for the typical nominal input voltage of 48 VDC.

Output Characteristics

The output voltage can be maintained to ±4% over the range of line, load and operational temperature range with an ordinary feedback circuit that uses a TL431 regulator. Transient response is controlled with proper frequency compensation. The design of the feedback network with guidance for selection of

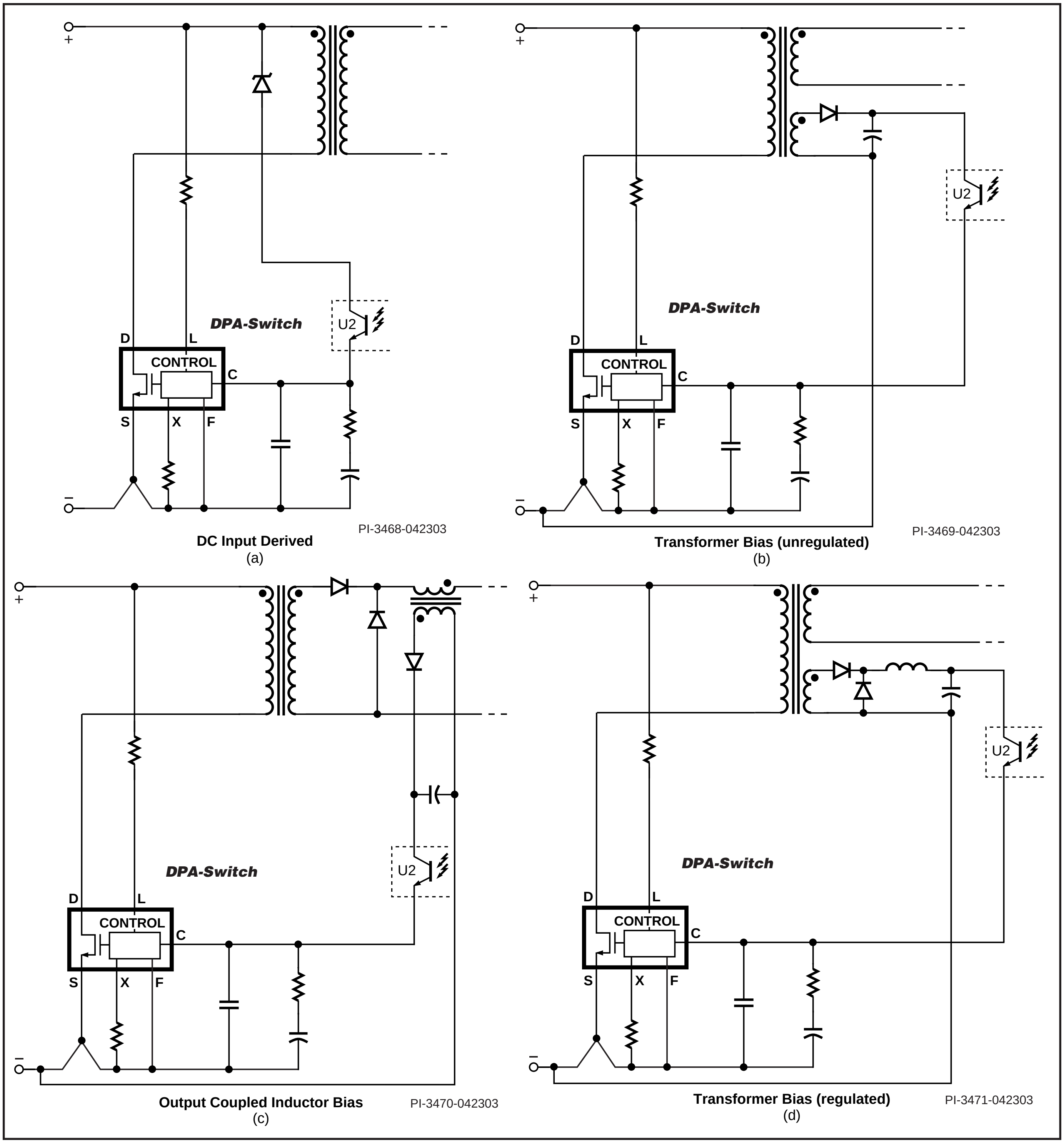

Figure 2. Methods for Generation of Bias Voltage.

component values is addressed in a separate section. Ripple and noise are strongly influenced by the size of the output inductor and the choice of output capacitors. These topics are discussed more thoroughly later in this document.

Output Rectifiers

Output rectification may be accomplished with discrete Schottky diodes for lowest cost or synchronous rectifiers for highest efficiency. This document discusses synchronous rectification in greater detail in a separate section. Ultra-fast PN junction diodes are not suitable at *DPA-Switch* operating frequencies.

Efficiency

Designing a DC-DC converter with *DPA-Switch* involves several engineering tradeoffs that weigh efficiency against cost and complexity. The circuit configuration in Figure 1 achieves efficiencies greater than 85% over the range of input voltage at medium loads. In typical applications without synchronous rectifcation, approximately 25% of the total power loss will be in the *DPA-Switch* (see *DPA-Switch* data sheet), 40% in the output rectifiers, and 30% in the magnetic devices. The remainder is distributed among other devices and circuit traces.

Higher efficiencies of approximately 91% can be obtained when Schottky rectifiers are replaced by synchronous rectifiers, allowing lower voltage drops. The efficiency can be raised even higher with the use of the next larger device in the *DPA-Switch* family that has lower $R_{DS(ON)}$. Further increases in device size may not improve the efficiency due to increased device switching losses. Losses in the magnetic devices can be reduced by using larger cores and by switching at 300 kHz instead of 400 kHz. All these alternatives have compromises in size, cost and complexity that the designer must evaluate.

Temperature

DC-DC converters usually must operate over an extended range of temperature that goes beyond the limits for ordinary consumer electronics. Designers should be aware that the characteristics of passive components are likely to change significantly with temperature. Attention to these effects to choose suitable components can prevent unexpected and undesirable behavior.

Designers must pay particular attention to the selection of the output capacitors and the components in the feedback circuit to guarantee specified performance throughout the temperature range. The details are addressed later in the sections on Output Capacitor Selection and Feedback Design.

Bias Voltage

There are four ways to generate the bias voltage required for operation of *DPA-Switch*:

(a) DC input derived
(b) Transformer bias (unregulated)
(c) Output coupled inductor winding
(d) Transformer bias (regulated)

Figure 2 illustrates the four alternatives. Each one must provide a minimum of 8 V at the collector of the optocoupler under worst case operating conditions (minimum input voltage and minimum load). The lowest bias voltage under typical conditions should be 12 V. The output coupled inductor and the regulated transformer bias techniques give the highest efficiency of the four solutions because the voltage across the optocoupler is controlled. This is countered by increased complexity. Optocoupler dissipation can be significant and should be verified. Maximum optocoupler phototransistor current is equal to the maximum CONTROL pin current ($I_{C(SKIP)}$) for the selected *DPA-Switch.* Maximum dissipation therefore occurs at the highest bias voltage (highest input voltage for (a) and (b)) and minimum load. Table 2 provides a comparison of complexity vs performance for all the solutions.

a) The DC input derived bias is the simplest of the three solutions. It uses a Zener diode between the positive DC input and the collector of the phototransistor of the optocoupler to reduce the maximum collector-to-emitter voltage, and more importantly, to limit the dissipation in the optocoupler. The penalty for simplicity is a reduction in efficiency that can be significant at high input voltages. This alternative is best for industrial applications where the input voltage is low (18 V to 36 V). The input voltage in industrial applications is usually low enough to eliminate the Zener diode because the breakdown voltages for standard optocouplers can be as high as 70 V. Designers must check the maximum power dissipation in the optocoupler in either case.

b) The transformer bias (unregulated) is created from a winding on the power transformer. The forward bias winding should be connected to the rectifier in a polarity such that it conducts when the *DPA-Switch* is on. Since the bias voltage is proportional to the input voltage, efficiency is reduced at high input voltages, but the effect is less than with the direct connection to the input. Again, the designer needs to check the power dissipation in the optocoupler at the maximum bias voltage. For this bias type worst case is minimum output load and high input voltage. Flyback bias windings are not recommended for *DPA-Switch* applications since they will affect the transformer reset.

c) Output coupled inductor bias uses a winding on the output inductor to develop the bias voltage. This technique provides a well regulated bias voltage when the converter operates in the continuous conduction mode. Regulation is accomplished by phasing the winding such that the bias voltage is proportional to the output voltage by transformer action when the *DPA-Switch* turns off. The penalty for the higher efficiency is the cost and complexity of a custom output inductor. The bias voltage can be adjusted by modifying turns ratio, bias capacitor size and minimum load on the main output. The designer should verify a minimum bias voltage of 8 V at minimum load and maximum input voltage.

d) The transformer bias (regulated) solution peforms the same function as the output coupled inductor bias (c). The bias

Bias Type	Input Voltage Range (V)	Efficiency	Cost Complexity	Comment
DC Input Derived Bias	18 to 36	⇓	⇓	Recommended for 18 to 36 V only
Transformer Bias (unregulated)	36 to 72	⇔	⇓	Recommended for low-cost design
Output Coupled Inductor Bias	36 to 72	⇑	⇑	Only recommended if supply already requires coupled output inductor
Transformer Bias (regulated)	36 to 72	⇑	⇔	Recommended for high efficiency designs

Table 2. Bias Voltage Solution Comparison.

voltage regulation is not quite as good as with the output coupled inductor bias. However, the solution does provide a reasonably constant bias voltage over a variety of input voltage and output load conditions. This solution works best if the independent inductor is maintained in the continuous conduction mode. The solution can be implemented with a low current, low cost (off-the-shelf) inductor, but the inductance value will be high enough to ensure continuous conduction mode over the majority of operating conditions.

Transformer Design

The power transformer is critical to the success of the converter design. Requirements for efficiency, component height and footprint will determine the details of construction. System engineers and circuit designers may choose to specify the electrical parameters and mechanical limits, and delegate the construction details to a supplier of custom transformers. Use the *PI Expert* design tool to determine the proper parameters. This section gives guidance for specification of the transformer.

Turns Ratio

The most important parameter for the power transformer is the primary-to-secondary turns ratio. It must be low enough to provide the regulated output voltage at the minimum input voltage. Determine the minimum input voltage from the system specification and the tolerance of the line under-voltage lockout circuit.

Whereas the minimum input voltage may be specified at 36 V, worst case tolerances of the under-voltage circuit are likely to allow the *DPA-Switch* to operate at an input as low as 29 V. From this voltage, subtract the estimated drain-to-source voltage of *DPA-Switch* at the maximum load. Reduce it further by an estimate of the voltage drop from the high frequency AC resistance of the transformer windings at full load.

Multiply the result by the maximum guaranteed duty ratio and divide by the sum of the output voltage and the drop on the output rectifier at full load. The duty ratio can be greater than 50% because *DPA-Switch* uses a voltage mode control. The quotient is the upper limit for the turns ratio.

Core and Copper

The actual number of turns for the transformer will depend on the dimensions of the particular core. The core material should be low loss at the *DPA-Switch* operating frequencies. Technical data on properties of Ferrite Cores are available from several suppliers. See references [1], [2] and [3]. Skin effect and proximity effect will set a practical limit for wire size. Foil windings become attractive when the output current is higher than about 6 amperes.

Thermal considerations often dominate selection of the core. The selection of the core is a complex trade-off between winding area, core cross-section and ratio of core surface area to core volume. These parameters determine the power loss as well as the thermal resistance of the transformer. A small core may meet the requirements in every respect except temperature rise, forcing the use of a larger core. The only practical way to check temperature rise is with bench evaluation of a prototype. Temperature must be measured at the hottest spot in the transformer, which is usually next to the center of the core under the windings. Wire temperatures above 110 °C need special considerations and UL Class F materials.

Other Practical Considerations

Minimize the number of turns within the limits of other constraints. Resistive losses depend on the length of the wire. Maximize the amount of copper (wire) that can be fitted within the winding window. Leakage inductance must be kept low to reduce losses associated with clamp components. This is best

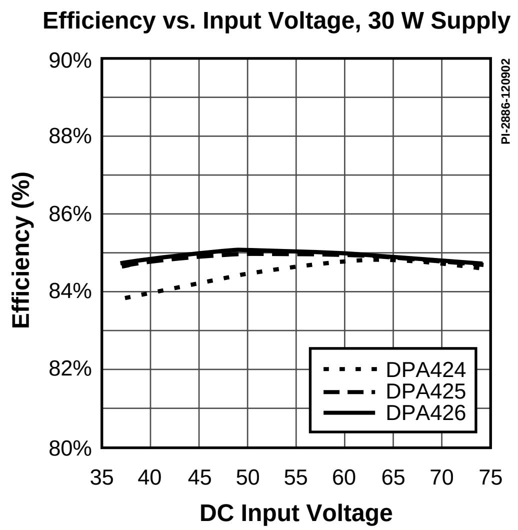

Figure 3. Efficiency of the Low Cost EP-21 Prototype with Different Devices in the DPA-Switch Family (Synchronous Rectification Would Improve Efficiency).

accomplished with a split primary construction that has the secondary between the layers of the primary winding. Also, all transformers should have no air gap.

If the transformer has a winding for the bias voltage, be sure that it has enough turns to maintain a minimum of 8 V bias at the lowest input voltage. Perform bench verification to confirm that the converter shuts off at low input voltages by virtue of the under-voltage lockout circuit, and not because the bias voltage is too low.

With the actual number of turns on the transformer, verify that the duty ratio to regulate the output at the minimum input voltage is less than the minimum DC_{MAX} specified for *DPA-Switch*.

The AC flux density contributes to the core losses. For this reason the AC flux density should be maintained in the range between 1000 and 1500 gauss (0.1 to 0.15 tesla).

Output Inductor

For a single output application with no bias winding, the inductor can be a standard off-the-shelf component. Inductors with multiple windings are typically custom designs.

The inductor value is determined chiefly by the amount of current ripple that the designer is willing to tolerate. Higher ripple current will allow an inductor that is smaller both electrically and physically. The consequence of higher ripple current is the requirement for more output capacitance with lower equivalent series resistance (ESR) to meet the specification for output ripple. Higher current ripple in the inductor also translates to higher peak current in the *DPA-Switch* for a given output power. It also leads to generally greater loss and lower efficiency because the RMS value of all the currents will be higher.

A convenient design parameter for selection of the inductor is $K_{\Delta I}$, defined as the ratio of the peak-to-peak ripple current to the average current in the inductor. Smaller $K_{\Delta I}$ corresponds to lower ripple and a larger inductor. Recommended values for $K_{\Delta I}$ are between 15 and 20 percent. The choice of $K_{\Delta I}$ involves a trade-off between the size of the inductor, the number and type of output capacitors, efficiency, and cost. Higher values of $K_{\Delta I}$ are not recommended, as these higher ripple currents increase both the stress and the ripple voltage on the output capacitor.

Whether the inductor is standard off-the-shelf or custom, the design should minimize the number of turns to reduce the resistive loss. The construction should also use a low loss core material.

With user input, the *PI Expert* design tool computes the inductance, the RMS current and the peak stored energy to aid in the selection or specification of the inductor. Peak stored energy is a useful parameter to select designs that use a closed toroid core, where magnetic saturation is generally a concern.

Additional Winding for Bias Voltage

If the configuration in Figure 2 (c) is chosen for generation of the bias voltage, choose the number of turns on the bias winding to give 12 V at the optocoupler under nominal conditions. Compute the required number of turns from the lowest regulated output voltage and the highest forward voltage drops for the output rectifier and the bias rectifier. Check the bias voltage at minimum load, maximum line, and add a preload if necessary to maintain the bias voltage at 8 V minimum. It may also be necessary to increase the bias winding turns to meet the minimum voltage requirement with a reasonably small pre-load.

DPA-Switch Selection

The first criterion for the selection of the *DPA-Switch* is peak current capability. From the turns ratio of the transformer and the peak current in the output inductor, estimate the peak current in the primary of the transformer. The magnetization current of the transformer should be negligible for this estimate. For lowest cost, select the smallest *DPA-Switch* that has a minimum current limit that is at least 10% greater than the maximum primary current. The allowance of 10% greater current gives design margin with the ability to respond to transient loading.

The second criterion for the selection is power dissipation. The smallest *DPA-Switch* that will handle the current may dissipate too much power to meet the efficiency requirements. Even if efficiency is not a concern, the smallest device may get too hot if system constraints prevent good thermal design. Multiplication of the $R_{DS(ON)}$ by the square of the RMS current in the primary gives a reasonable estimate of the power dissipation in the *DPA-Switch*. The *DPA-Switch* dissipates approximately 25% of the total system loss in designs without synchronous rectifiers.

If power dissipation is a problem with the smallest device, select the next larger device and program the current limit with the X pin to 10% above the peak primary current. This is done to limit overload power capability. Refer to the *DPA-Switch* data sheet to determine the value of the resistor on the X pin that corresponds to the desired current limit.

Figure 3 illustrates how the efficiency is related to the selection of the *DPA-Switch*. Devices with lower $R_{DS(ON)}$ dissipate less power where resistive voltage drop dominates the loss. Thus, the efficiency is higher for larger devices at low input voltage. At higher input voltages the RMS current in the *DPA-Switch* decreases and the loss from capacitance on the drain increases, so the lower $R_{DS(ON)}$ has virtually no effect on efficiency.

Clamp Circuit

All applications must protect the *DPA-Switch* from excessive drain voltage. Figure 1 shows a simple and effective solution. A Zener diode from the drain to source provides a hard clamp. The 30 W prototype example (Table 1), uses a 150 V Zener to guarantee substantial margin from the breakdown voltage of 220 V. A small capacitor across the primary of the transformer may be necessary in conjunction with the Zener clamp (see Figure 4).

The designer should put a placeholder for this capacitor on the initial prototype. In some designs there is sufficient stray capacitance on the primary of the transformer to remove the need for this clamp capacitor. Bench tests will determine whether the capacitor is required to maintain safe drain-to-source voltages. In normal steady-state operation, the capacitor C_{CP} across the primary of the transformer absorbs energy from leakage inductance to keep the drain-to-source voltage below the Zener voltage. There is an optimum value for C_{CP} that typically ranges between 10 pF and 100 pF for converters in the range of 10 W to 40 W.

The value of C_{CP} depends on the leakage inductance and the peak current. The proper value of capacitance will allow most of the energy in the leakage inductance to be recovered during the next switching cycle. Too little capacitance will cause the Zener diode to conduct. Dissipation in the Zener will reduce efficiency. Too much capacitance will also reduce efficiency because it will increase turn-on losses in the *DPA-Switch* and may also interfere with the reset of the transformer.

The Zener diode does not conduct during normal steady-state operation, but it is required to limit the drain voltage during start-up, transient loading and overload conditions.

At higher powers, the clamp capacitor value (C_{CP}), becomes a limiting factor on the efficiency of the power supply. Different techniques can be used for these higher power applications

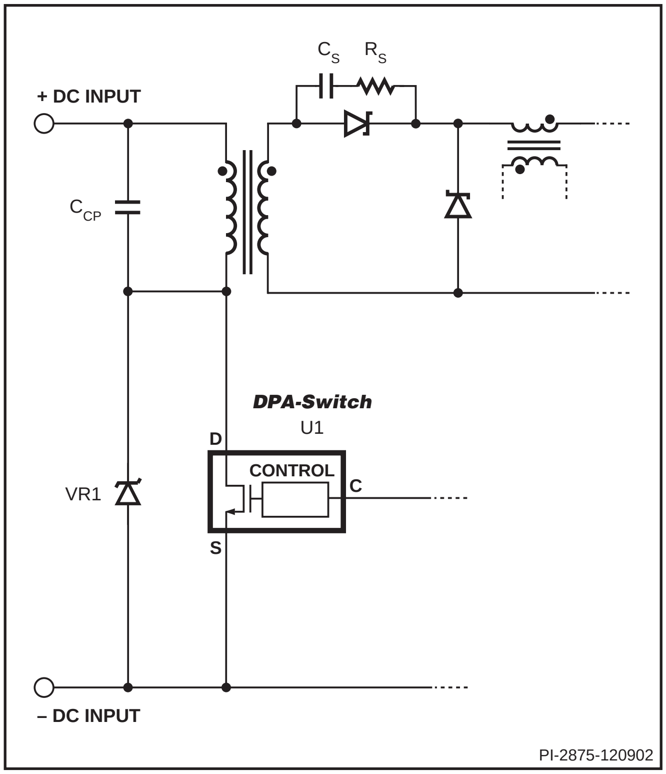

Figure 4. Components of the Transformer Clamp and Reset Circuit.

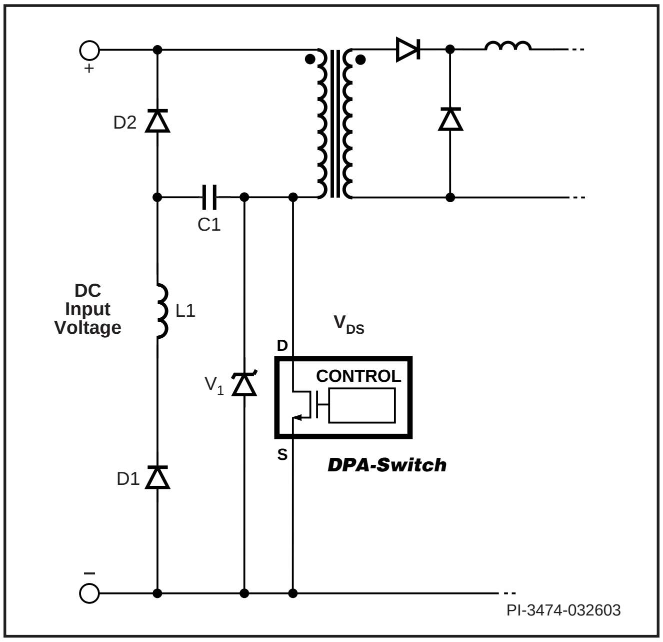

Figure 5. LC (Inductor Capacitor) Reset and Clamp.

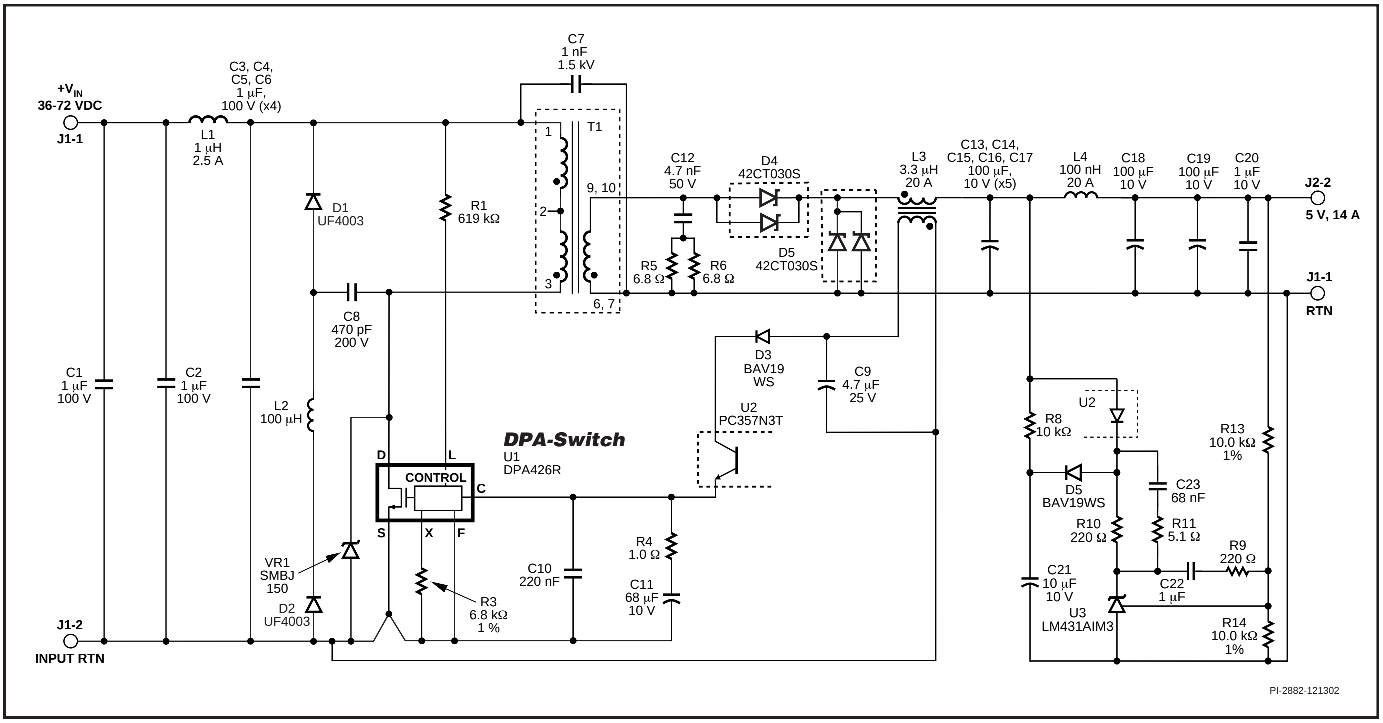

Figure 6. A 70 W DC-DC Converter that uses an Alternative Circuit to Reset the Transformer.

(above approximately 40 W). Figures 5 and 6 show a non-dissipative clamp technique that also resets the transformer. See references [4] and [5] for a description of this technique.

Transformer Reset Circuit

The flux in the magnetizing inductance of the transformer must be reset in each switching cycle to maintain volt-seconds balance and prevent saturation. Since real transformers have finite inductance, they store parasitic energy that is represented as a magnetizing current.

The magnetizing inductance cannot store very much energy before it saturates. Since a saturated transformer behaves like a short circuit, external circuitry must manage the removal of the energy from the magnetization inductance (reset the transformer) on each switching cycle.

This transformer reset will require the voltage on the DRAIN pin to rise above the input voltage. The designer needs to be sure that the transformer reset does not cause voltage overstress on the DRAIN pin of the *DPA-Switch.*

Figure 4 shows the components for the circuit that resets the magnetizing energy in the transformer to a safe value at the end of each switching cycle. The heart of the circuit is the series RC network (R_S and C_S) that is connected across the output rectifier.

When the *DPA-Switch* turns off, current in the magnetizing inductance leaves the transformer through the secondary winding. The capacitor charges as the magnetizing current reduces to zero. The capacitor must be small enough to allow the magnetizing current to go to zero within the minimum offtime. An additional restriction on the size of the capacitor is that it must be large enough to keep the drain-to-source voltage below the voltage of the Zener clamp under normal operating conditions. The resistor in the reset network damps oscillations from the interaction of the capacitor with parasitic inductance. The value of the resistor is typically between one and five ohms.

A different reset circuit is required for applications higher than about 40 W. Figure 6 shows an example of a 70 W converter that uses the circuit of Figure 5 to reset the transformer and to limit the voltage on the *DPA-Switch*.

Verification of Transformer Reset

Users should confirm that the transformer resets under worst case conditions at the lowest and highest input voltages with measurements on the bench. Figure 7 illustrates three situations that show proper transformer reset with the reset circuit in Figure 4. Three examples of improper transformer reset are shown in Figure 8.

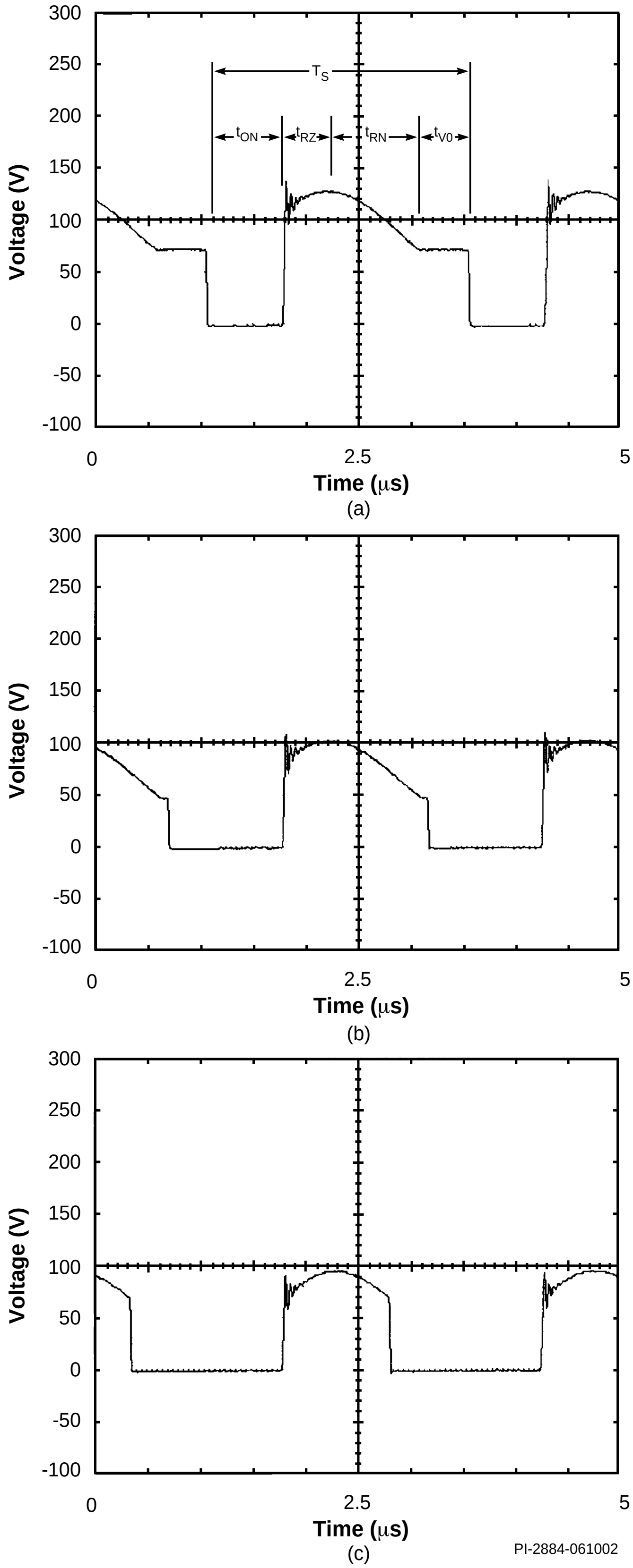

Figure 7. Normal DPA-Switch Drain Waveforms Showing Correct Transformer Reset. a) V_{IN} = 72 V, b) V_{IN} = 48 V, c) V_{IN} = 36 V.

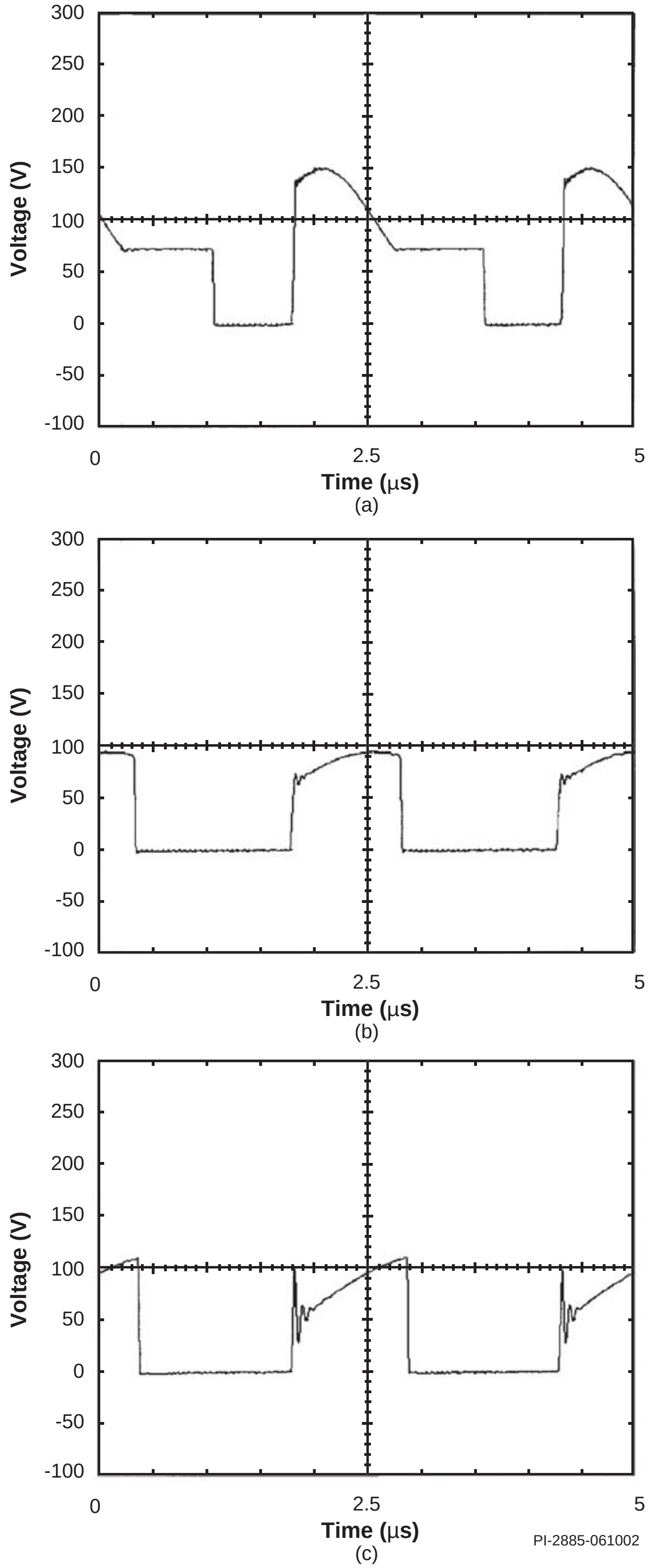

Figure 8. Illustration of Three Situations with Improper Transformer Reset. a) V_{IN} = 72 V, b) V_{IN} = 36 V, c) V_{IN} = 36 V.

The best way to assess the reset characteristics is to observe the drain-to-source voltage on the *DPA-Switch*. Figure 7 (a) shows the voltage on the prototype example when it operates from an input of 72 VDC. It is operating at full load with a reset capacitor (C_S) of 2.2 nF across the output rectifier. The clamp capacitor on the primary is 47 pF. See Design Idea DI-24 (available on www.powerint.com) for a circuit example.

The figure shows the important intervals of the waveform within one switching period T_S. *DPA-Switch* is conducting during the time $t_{ON} = D\ T_S$, where D is the duty ratio. Flux in the transformer increases in the positive direction during t_{ON}, and resets to zero during the interval t_{RZ}. All the energy stored in the magnetizing inductance is removed during t_{RZ} to charge the reset capacitor and the clamp capacitor to maximum voltage. The flux increases in the negative direction during the interval t_{RN} as the reset capacitor and the clamp capacitor discharge into the magnetizing inductance. The flux remains a constant negative value during the interval t_{V0}, where the voltage on the transformer windings is zero. It is easy to see that the primary voltage is zero during t_{V0} because the drain voltage is the same as the input of 72 V. The negative magnetizing current circulates in the secondary winding during t_{V0}.

Figure 7(b) shows the drain voltage on the same circuit when it operates at the nominal input of 48 VDC. The larger duty ratio is consistent with the lower input voltage. Note that the intervals t_{RZ} and tRN are the same as at 72 V input, but now t_{V0} is nearly zero.

Figure 7(c) shows the situation at input voltage of 36 VDC, with a corresponding larger duty ratio. The transformer has reset to zero flux because the drain voltage has reached its peak during the interval t_{RZ}. The drain voltage is in the region of negative flux when the *DPA-Switch* turns on.

Peak drain voltage under normal operating conditions should be less than 150 V. This includes peaks in the drain voltage from the reset of both leakage inductance and magnetizing inductance.

Figure 8 shows three cases of improper transformer reset. The prototype example has been modified to create these illustrations. The RC network has been removed from the output rectifier to obtain the waveform in Figure 8(a). The clamp capacitor C_{CP} on the primary is 47 pF. The magnetizing energy resets into only the clamp capacitor and other stray capacitance. Consequently, at 72 V input the drain voltage goes higher than desired. The figure shows the maximum drain voltage at 152 V, in contrast to 140 V in Figure 7(a) with a proper reset network. The Zener clamp voltage of 150 V is specified at a current of 1 mA. Although the Zener clamp just barely conducts at 152 V, there is not sufficient margin in this design to tolerate a transformer with lower primary inductance.

Figure 8(b) illustrates the situation of too much capacitance. The RC reset network has been restored with a proper capacitance of 2.2 nF, but C_{CP} is increased to 470 pF, ten times the original value. The waveform shows operation at 36 VDC input and full load. The flux in the transformer has just barely reset to zero, as the *DPA-Switch* turns on at the end of the t_{RZ} interval. A larger magnetizing inductance or a lower input voltage would not allow the transformer to reset.

The final example of an improper transformer reset is Figure 8(c). Primary clamp capacitor CCP is restored to its original value of 47 pF, but the reset capacitor is increased to 47 nF. The converter is operating at 36 VDC. The drain voltage shows clearly that the transformer is not resetting completely. The *DPA-Switch* turns on within the interval t_{RZ}. The flux in the transformer has not returned to zero. A small change in operating conditions could cause the transformer to saturate on every cycle or to run so close to saturation that it could not accommodate change in duty ratio from a load step.

Output Capacitors

The ripple current in the output inductor generates a voltage ripple on the output capacitors. Part of the ripple voltage comes from the integration of the current by the capacitance, and part comes from the voltage that appears across the capacitor's equivalent series resistance (ESR). The capacitor must be selected such that the capacitance is high enough and the ESR is low enough to give acceptable voltage ripple with the chosen output inductor. Usually most of the ripple voltage comes from the ESR. Ripple voltage that is dominated by ESR has a triangular waveform like the ripple current in the inductor. Ripple voltage that is dominated by the capacitance has a waveform with segments that are parabolic instead of linear.

Output capacitors in DC-DC converters are typically solid tantalum. They are a good choice because of their low ESR and low impedance at the frequencies used in these converters. The ESR is also an important element in the design of the feedback loop. In this regard, a moderate amount of ESR is desirable. The section on Feedback Design elaborates on the values of the components in the feedback circuit.

It is important for designers to know that the value of ESR may change significantly over the specified temperature range. The output ripple and the stability of the control loop can be affected by the change in ESR. It is necessary to evaluate prototype hardware at the extremes of temperature to confirm satisfactory performance.

The voltage rating for the capacitors is typically 25% higher than the maximum operating voltage for reliability. The derating factor is thus 80%. For example, a 5 V output would have a capacitor that is rated for either 6.3 V or 10 V. The lower voltage capacitor would be smaller, whereas the higher voltage capacitor would have a lower failure rate in the application.

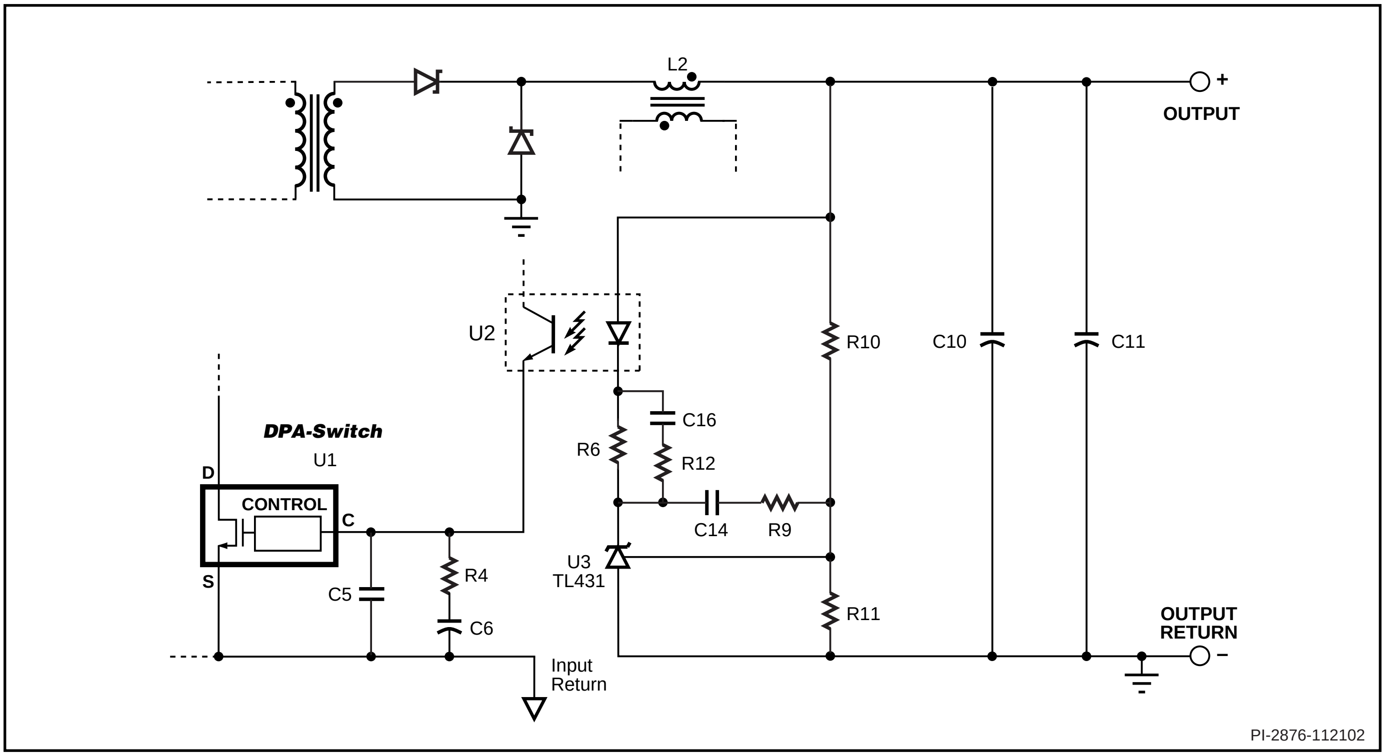

Figure 9. Essential Components of the Feedback Circuit. The Schematic Does Not Show ESR of the Output Capacitors (Component Designators are the Same as in the EP-21 Prototype).

Feedback Design

Stability is an important consideration for a switching power supply. Three parameters that describe the characteristics of the control loop are crossover frequency, phase margin and gain margin. The crossover frequency is the frequency where the magnitude of the loop gain passes through 0 dB. It is a measure of the system's bandwidth.

The phase margin is specified at the crossover frequency. It is the difference between the phase of the loop gain and 180 degrees. A stringent specification will call for a phase margin of at least 60 degrees under worst case conditions. In no case should the phase margin be less than 45 degrees. This means the phase would have to decrease by that amount for the system to become unstable. Phase margin is also related to the dynamic characteristics of the system. A low phase margin suggests an oscillatory response to a load step or other disturbance.

It is also important that the loop gain decrease in magnitude beyond the crossover frequency. This requirement is generally specified as gain margin. Gain margin is the difference between 0 dB and the magnitude of the loop gain at the frequency where the phase is 180 degrees. An acceptable gain margin is greater than 10 dB. This means the magnitude would have to increase by that amount for the system to become unstable. Loop gain should be measured at worst case conditions (generally maximum input voltage with maximum load) and at the extremes of the specified ambient temperature, since important component parameters (especially capacitor ESR) can change greatly with temperature.

Stabilizing a high frequency forward DC-DC converter presents some challenges due to the inherently high bandwidth of this topology. Many DC-DC converter designs use cycle-by-cycle current-mode control. The *DPA-Switch* uses classic voltage mode control to allow operation at duty ratios greater than 50% without the need for the stabilizing ramp ("slope compensation") required with current-mode control. The fundamental system characteristics of the forward converter in continuous conduction mode with voltage mode control call for a compensation circuit with multiple poles and zeros to achieve the desired loop response.

The crossover frequency for a control loop that uses *DPA-Switch* in a forward converter with an optocoupler should be limited to 10 kHz or less at maximum input voltage and room temperature. The *DPA-Switch* has one internal pole at approximately 30 kHz to filter switching noise. Other poles at higher frequencies contribute additional phase shift at 30 kHz. The optocoupler has two poles at approximately 100 kHz. The phase shift from these poles, combined with the phase shift introduced by the LC filter at the output of the converter, is difficult to compensate above 10 kHz.

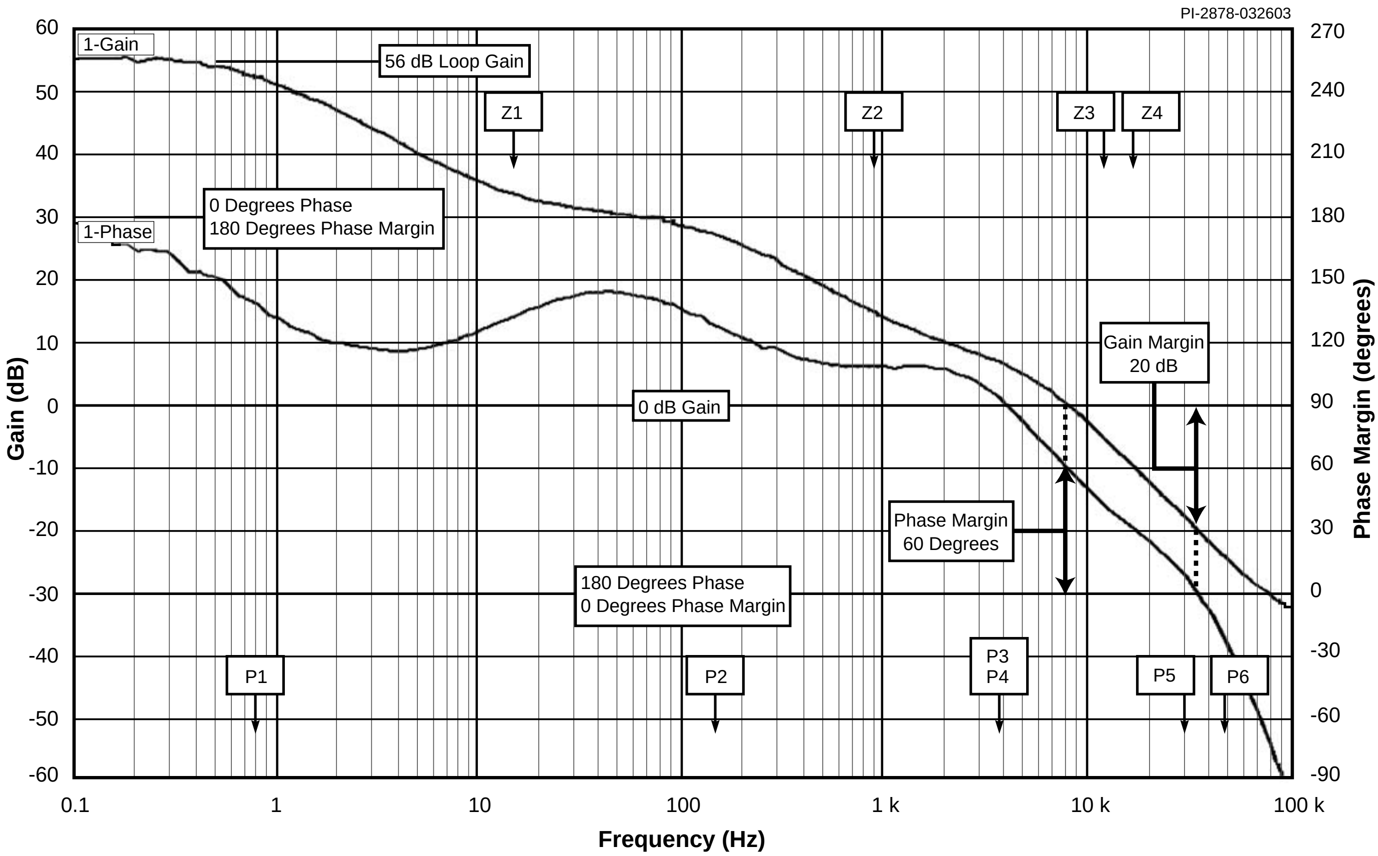

Figure 10. Gain and Phase of a Typical Feedback Loop for DC-DC Forward Converter with DPA-Switch. Markers Show Locations of Major Poles and Zeros.

The objective of the feedback design is to reduce the magnitude of the loop gain to zero dB at a frequency of 10 kHz or less with a phase margin near 60 degrees. Although system requirements and the *DPA-Switch* fix some quantities that determine loop characteristics, the designer can manipulate many components in the feedback circuit to optimize loop stability. Figure 8 shows the essential components of a feedback circuit that uses an ordinary TL431 regulator to achieve the high loop gain required for tight DC voltage regulation. Not shown in the circuit diagram is the ESR of the output capacitors. The ESR is also an important element in the frequency compensation of the feedback loop.

Output LC Filter

The filter formed by the output inductor and the output capacitors contributes two poles to the loop response at the filter's resonant frequency. Since the filter is a resonant circuit with relatively low loss, the gain and phase change rather abruptly near the resonant frequency. Consequently, the poles and zeros for shaping the loop response should either avoid this region or compensate for the resonance.

Proper placement of the resonant frequency of the output filter will avoid complications in the design of the feedback loop. The position of the resonant frequency should allow the designer to shape the desired response with a limited number of compensation components of reasonable size. The recommended resonant frequency for an output filter that uses low ESR tantalum capacitors in a forward converter with *DPA-Switch* and optocoupler feedback is between 4 kHz and 6 kHz. This value is consistent with the inductor and capacitor values for desirable ripple current and ripple voltage.

The output capacitor ESR contributes a zero that compensates for one of the poles from the filter. However, for low ESR tantalum or organic electrolyte capacitors, this zero usually occurs too high in frequency to substantially offset the effects of the filter within the desired loop bandwidth. In the prototype example, the output filter capacitors are 100 μF, with a maximum specified ESR of 100 milliohms. The ESR zero is thus at approximately 16 kHz, well beyond the 4 kHz LC filter resonant frequency. Actual ESR is approximately 80 milliohms, placing the zero typically at 20 kHz. In situations where standard low ESR electrolytic capacitors can be used, the higher ESR may place the ESR zero at a sufficiently low frequency to add significant additional phase margin.

DPA-Switch Compensation

The network of C6 and R4 at the CONTROL pin of *DPA-Switch* provides compensation for the feedback loop in addition to other functions. The capacitance of C6 with R4 and its own ESR plus the impedance of the CONTROL pin impedance provide a pole in the loop gain, followed by a zero from R4 and the ESR of C6.

Suggested values of C6 are between 47 μF and 100 μF. This range of values will generally be sufficient to provide desirable adjustments to the loop gain and to allow the capacitor to perform its other functions in the system.

The zero introduced by R4 and the ESR of C6 should be at approximately 25% of the output filter resonant frequency. This placement allows maximum gain reduction while minimizing the phase lag introduced by this network at the resonant frequency. In the prototype example, C6 is 68 μF with an ESR of about 1.6 ohms. The impedance at the CONTROL pin of *DPA-Switch* is typically 15 ohms. These values put the pole at approximately 130 Hz and the zero at approximately 900 Hz. High frequency bypass capacitor C5 is small enough to have a negligible effect on the loop gain.

Optocoupler Compensation

The current transfer ratio (CTR) of the optocoupler is a major contributor to the magnitude of the loop gain near the crossover frequency. Equally important is the resistor R6 in series with the optocoupler LED. Selection for either of these elements is not arbitrary, as the optocoupler provides power to the *DPA-Switch* during normal operation.

The combination of optocoupler and series resistor must deliver the maximum specified CONTROL pin current for the *DPA-Switch* at minimum specified CTR. In most cases, an optocoupler with a CTR between 100% and 200% will suffice. The designer then selects R6 to provide the LED current required at minimum CTR with a saturated TL431. The network of R12 and C16 in parallel with R6 creates a zero that boosts the gain and phase to compensate one of the poles from the output filter. The position of the zero is generally determined empirically to achieve the desired phase margin. It is typically set at a frequency between one and three times the resonant frequency of the output filter. Resistor R12 limits the boost in gain at high frequencies.

TL431 Compensation

The purpose of the TL431 is to provide high loop gain at low frequencies. Its contribution is not necessary at higher frequencies where the optocoupler provides adequate gain. Therefore, the feedback circuit has compensation around the TL431 to maximize its contribution at very low frequencies and to remove its influence at higher frequencies.

The connection of C14 and R9 between the cathode and the reference terminal of the TL431 allows maximum loop gain at DC for the best voltage regulation. In the prototype example, capacitor C14 forms an integrator that reduces the contribution of the TL431 by 20 dB per decade. Resistor R9 with R10 sets the minimum gain from the TL431 and introduces a zero in the loop gain. The zero in the prototype example is at about 16 Hz.

Another zero, local to the TL431, is formed by C14 and R9 at about 720 Hz. The location of this zero is not critical for normal operation in continuous conduction mode, and does not appear in the loop gain of this example. It becomes important at very light loads where the converter operates in discontinuous conduction mode. The loop gain characteristic for discontinuous conduction mode is fundamentally different from this example of continuous conduction mode. The most significant effect is that the loop gain will generally have a much lower crossover frequency that depends on the load. The crossover frequency could easily fall into the region where the TL431 contributes significantly to the loop gain.

Loop Gain of Prototype Circuit

Figure 10 shows the magnitude and phase of the loop gain of the prototype circuit for an input voltage of 72 V at a load current of 5 amps. The highest input voltage is typically the worst case in forward converters because that is the condition for highest gain, yielding the highest bandwidth and lowest phase margin.

The upper curve in Figure 10 is the magnitude of the loop gain in units of dB. The lower curve is the phase in units of degrees, with the scale shifted by 180 degrees to give the phase margin directly. The markers Z1 through Z4 and P1 through P6 show respectively the frequencies of the significant zeroes and poles.

The integrator formed by C14, R9 and R10 reduces the gain from its DC value such that the TL431 makes essentially no contribution to the gain at frequencies higher than Z1. The asymptotes of the DC value and the 20 dB per decade slope of the integrator create the pole at P1.

Gain is reduced by the pole at P2 that is formed by capacitor C6 with its ESR, resistor R4, and the internal impedance of the CONTROL pin of the *DPA-Switch*. The phase receives a boost from the zero formed by C6 and R4 with the ESR of C6 at Z2. The resistor R4 augments the ESR of the capacitor. Use a tantalum capacitor for C6 so that the total resistance can be adjusted by R4. The ESR of an aluminum capacitor will generally be too large to allow the desired shaping of the frequency response. Capacitor C5 provides a low impedance source for pulses of current into the CONTROL pin. Its effect

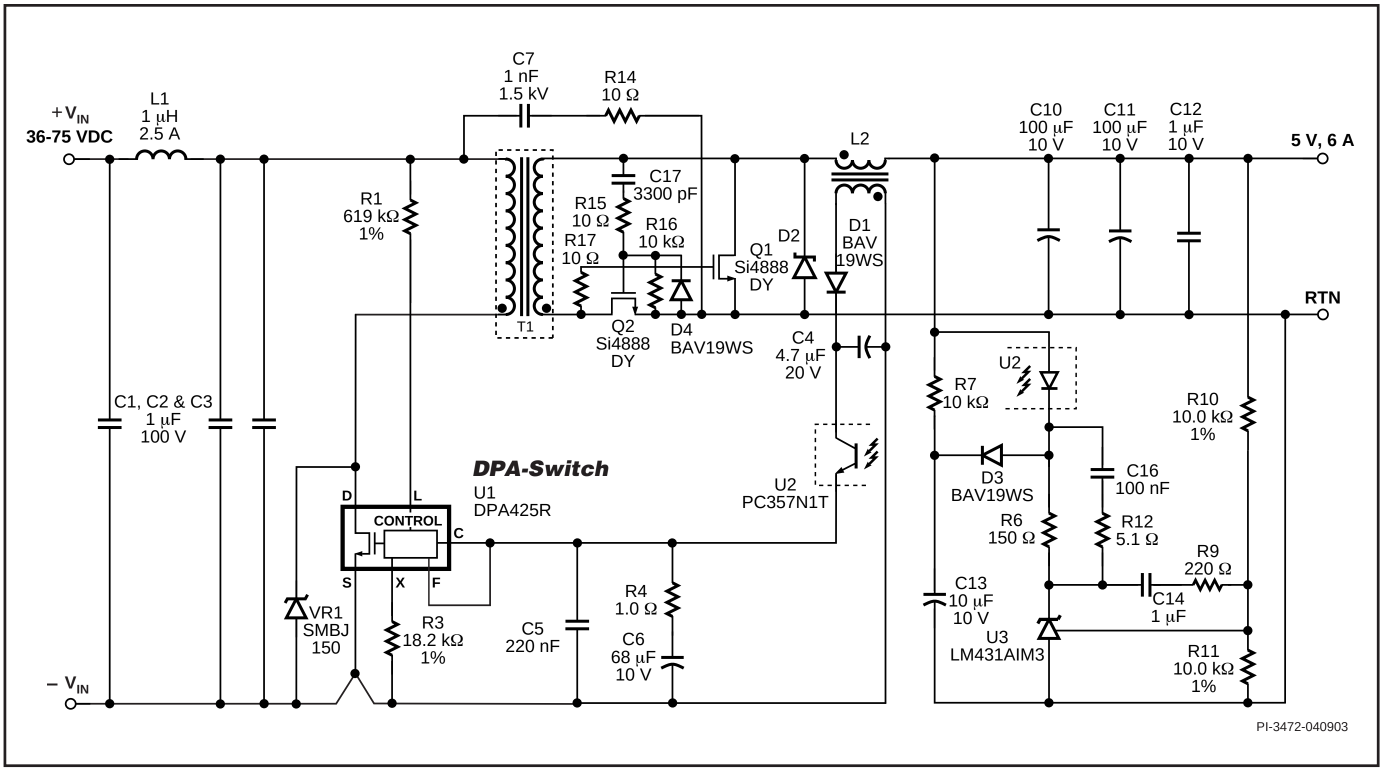

Figure 11. Example of DPA-Switch in a Single-Ended DC-DC Forward Converter with Synchronous Rectification.

on the control loop is minor, appearing at P6, well beyond the 0 dB crossover frequency.

The zero at Z2 provides partial cancellation of the pair of poles P3, P4 that originate from the output inductor and output capacitors of the forward converter. The network of C16, R6 and R12 gives additional cancellation with a zero at Z3. The ESR of the output capacitors gives a final zero at Z4. The internal high frequency filter of the *DPA-Switch* provides the pole at P5.

The magnitude of the gain at frequencies greater than Z1 is related directly to the current transfer ratio (CTR) of the optocoupler. Therefore, the CTR must be controlled to maintain a stable and well-behaved system. Designers should choose an optocoupler that has a CTR in the range of 100% to 200% at the maximum CONTROL pin current of 12 mA. The phototransistor of the optocoupler must also have a breakdown voltage greater than the maximum bias voltage.

Figure 10 shows that this example has a desirable phase margin of 60 degrees and a comfortable gain margin of 20 dB. Sufficient margin is required in the design of the feedback loop to allow for tolerances in the CTR of the optocoupler, changes in ESR of the output capacitor, and the change in gain with operating voltage. The ESR can change significantly with temperature. This should be a primary consideration in the selection of output capacitors. The design must also allow for tolerance variations in all other components.

Operation at No Load

Those who design or specify DC-DC converters should pay particular attention to requirements for minimum load. The control characteristics are different for operation in the continuous conduction mode (moderate to heavy loads) and discontinuous conduction mode (light loads). The boundary between the two modes occurs at the load where $K_{\Delta I} = 2$ (without synchronous rectification).

The two modes have different control characteristics. The converter in discontinuous conduction mode will usually have a slower response to transients and higher ripple voltage at the output than in continuous conduction mode. In extreme cases, a converter that is well-behaved in continuous conduction mode may actually become unstable at light load or with no load unless correctly designed. Many commercial DC-DC converter modules specify a large minimum load to prevent operation in discontinuous conduction mode.

A converter that operates deeply in discontinuous conduction mode requires a very small duty ratio. Operation at very light loads is not a problem for *DPA-Switch* because it automatically reduces the effective switching frequency by skipping cycles to give duty ratios less than about 5%.

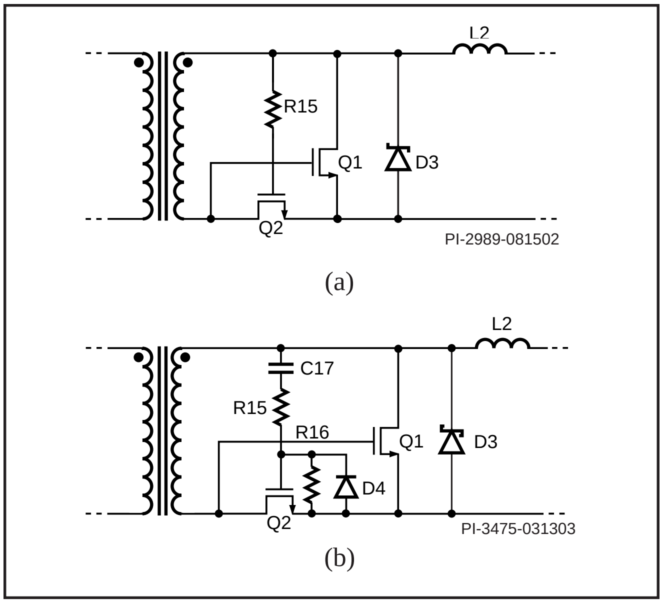

Figure 12. Synchronous Rectification (a) Winding Driven DC Coupled. (b) Winding Driven AC Coupled.

Operation at small duty ratios requires a larger capacitor to keep the bias voltage above its minimum required value of 8 V. In a trade-off with size, cost and efficiency, the best solution to a requirement to operate with no load is to include a small preload in parallel with the output capacitors. The amount of the load is determined empirically to supplement the natural loading from the other small-signal circuits that get their power from the output.

Synchronous Rectification

The use of synchronous rectification can yield a substantial increase in efficiency over passive Schottky rectifiers on the output. For a 5 V output, an efficiency of 85% with Schottky rectifiers would typically go to 90% or higher with synchronous rectifiers. Synchronous rectification gives the benefit of greater efficiency at lower output voltages as shown in Table 3.

Output Voltage	Efficiency Gain Over Diode Rectification
5 V	+3%
3.3 V	+6%
2.5 V	+8%

Table 3. Efficiency Gain vs. Output Voltage for Synchronous Rectification.

DPA-Switch has features that can simplify the design of synchronous rectifier circuits that are in common use. Circuits for synchronous rectification with *DPA-Switch* fall into three categories of increasing complexity.

a) Winding Driven DC Coupled
b) Winding Driven AC Coupled
c) Actively Driven

The first two are shown in Figures 11 and 12. MOSFETs Q1 and Q2 conduct at appropriate times to reduce the voltage drops associated with the output rectifiers of a forward converter. Q2 performs the function of the forward rectifier. Q1 operates as the catch rectifier with a parallel Schottky diode. The voltage drop of each synchronous rectifier is dominated by the on-resistance of the MOSFETs multiplied by the RMS load current, rather than by the average current times the minimum voltage of a Schottky barrier.

Winding Driven DC Coupled Synchronous Rectifier

The simplest way to drive synchronous rectifiers with *DPA-Switch* is shown in Figure 12 (a). The gate-to-source voltage that turns on the MOSFETs is essentially the voltage at the secondary winding of the transformer. The channel of the MOSFET will conduct as long as the gate-to-source voltage exceeds the threshold voltage.

The forward rectifier MOSFET Q2 turns on when the *DPA-Switch* turns on to apply the DC input voltage across the primary winding. The direction of current in Q2 is from source to drain. When the *DPA-Switch* turns off, the reset voltage on the transformer forces a negative gate-to-source voltage on Q2 and a positive gate-to-source voltage on Q1. Schottky diode D3 conducts until the gate-to-source voltage on Q1 rises sufficiently to exceed the threshold voltage.

Suitable MOSFETs for this application have threshold voltages typically between 4 V and 5 V. The permissible maximum gate-to-source voltage is usually 15 V to 20 V. These restrictions limit the range of input voltage for converter operation.

The integrated line overvoltage feature of *DPA-Switch* simplifies the design of winding driven synchronous rectifiers. In most cases it eliminates the need for Zener diodes to protect the gates of the MOSFETs from excessive voltage. Excess voltage will not appear on the secondary of the transformer because the *DPA-Switch* will not operate when the input voltage is too high.

DC coupling of the gates in this configuration permits a mode of operation that may not be desirable in some applications. During shutdown, the voltage across the output inductor will go to zero after its current decays to zero. The remaining output voltage will then appear across Q1 and D3.

If the output voltage is high enough (above the gate threshold of Q2) it will turn on Q2, allowing reverse current to flow through L2 and the transformer secondary. The voltage on the secondary winding will saturate the transformer, abruptly turning off Q2 and generating a voltage spike on the gate of Q1. This

Synchronous Rectifier Type	Efficiency	Complexity and Cost	Comment
Winding Driven DC Coupled	⇑	⇓	Check Gate Voltage at Power Down
Winding Driven AC Coupled	⇑	⇔	Gate Voltage Controlled at Power Down
Active Drive	⇑	⇑⇑⇑	High Complexity

Table 4. Comparison of Synchronous Rectification Techniques.

voltage spike may exceed the rated gate voltage for Q1. This behavior can occur in any design using this form of synchronous rectification with an undervoltage lockout. It is not specific to *DPA-Switch*. A solution to this issue is offered below.

Winding Driven AC Coupled Synchronous Rectifier

The AC coupled circuit of Figure 12 (b) eliminates the high voltage spike by limiting the on-time of Q2 such that significant reverse current cannot flow through L2 and the secondary winding. Capacitor C7 should be chosen to capacitively divide the winding voltage between C7 and the C_{GS} of MOSFET Q2, to provide a voltage on C_{GS} that exceeds the Q2 threshold voltage. The time constant of C17 and R2 should be about 10 μs for 300 kHz operation. R1 is typically about 10 Ω.

Figure 11 shows the *DPA-Switch* in a single-ended DC-DC forward converter that uses winding driven AC coupled synchronous rectification. In this example, the gate of Q1 has enough capacitance to eliminate the need for the discrete capacitor C_S in the transformer reset circuit. Although this is often the case with synchronous rectifiers that are winding driven, designers should follow the guidance in the section on Verification of Transformer Reset to confirm that the transformer resets properly.

Actively Driven Synchronous Rectifiers

The third category of synchronous rectifier circuits uses independent active components that may include discrete devices and integrated circuits to lock onto the switching frequency of the power supply and to drive the MOSFETs. This solution relaxes the restriction on the range of input voltage because the driver can regulate the gate voltage to be independent of the voltage on the secondary winding. Circuits for actively driven synchronous rectifiers are much more complex than the other solutions, and are beyond the scope of this application note. Table 4 gives a comparison of the techniques for synchronous rectification.

In general, *DPA-Switch* with synchronous rectifiers should operate at the lower switching frequency of 300 kHz. The synchronous rectifier catch MOSFETs typically have gate-source capacitance values such that the transformer would have insufficient time to reset at 400 kHz. Connect the F pin to the CONTROL pin to select the lower switching frequency.

Layout Considerations

Figure 13 shows an example of a proper circuit board layout for a forward converter with *DPA-Switch*. Since the *DPA-Switch* can operate with large drain current, designers should follow these guidelines carefully.

Primary Side Connections

The tab of *DPA-Switch* is the intended return connection for the high switching currents. Therefore, the tab should be connected by wide, low impedance traces to the input capacitor. The SOURCE pin should not be used to return the power currents; incorrect operation of the device may result. The SOURCE pin is intended as a signal ground only. The device tab (SOURCE) is the correct connection for power currents.

The bypass capacitor on the CONTROL pin should be located as close as possible to the SOURCE and CONTROL pins. The circuit trace of its connection to SOURCE should not contain any switching current from the primary or bias voltages. All SOURCE pin referenced components connected to the LINE-SENSE (L) or EXTERNAL CURRENT LIMIT (X) pins should also be located closely between their respective pins and SOURCE. Once again, the SOURCE connection trace of these components should not conduct any of the main MOSFET switching currents. It is critical that tab (SOURCE) power switching currents are returned to the negative terminal of the input capacitor through a separate trace that is not shared by the components connected to the SOURCE, CONTROL, L or X pins.

Any traces to the L or X pins should be kept as short as possible and away from the drain trace to prevent noise coupling. Line-sense resistor (R1 in Figure 11) should be located close to the L pin to minimize the trace length on the L pin side. In addition to the CONTROL pin capacitor (C5 in Figure 11), a 220 nF high frequency bypass capacitor in parallel is recommended as close as possible between SOURCE and CONTROL pins for better noise immunity. The feedback optocoupler output should also be located close to the CONTROL and SOURCE pins of *DPA-Switch.*

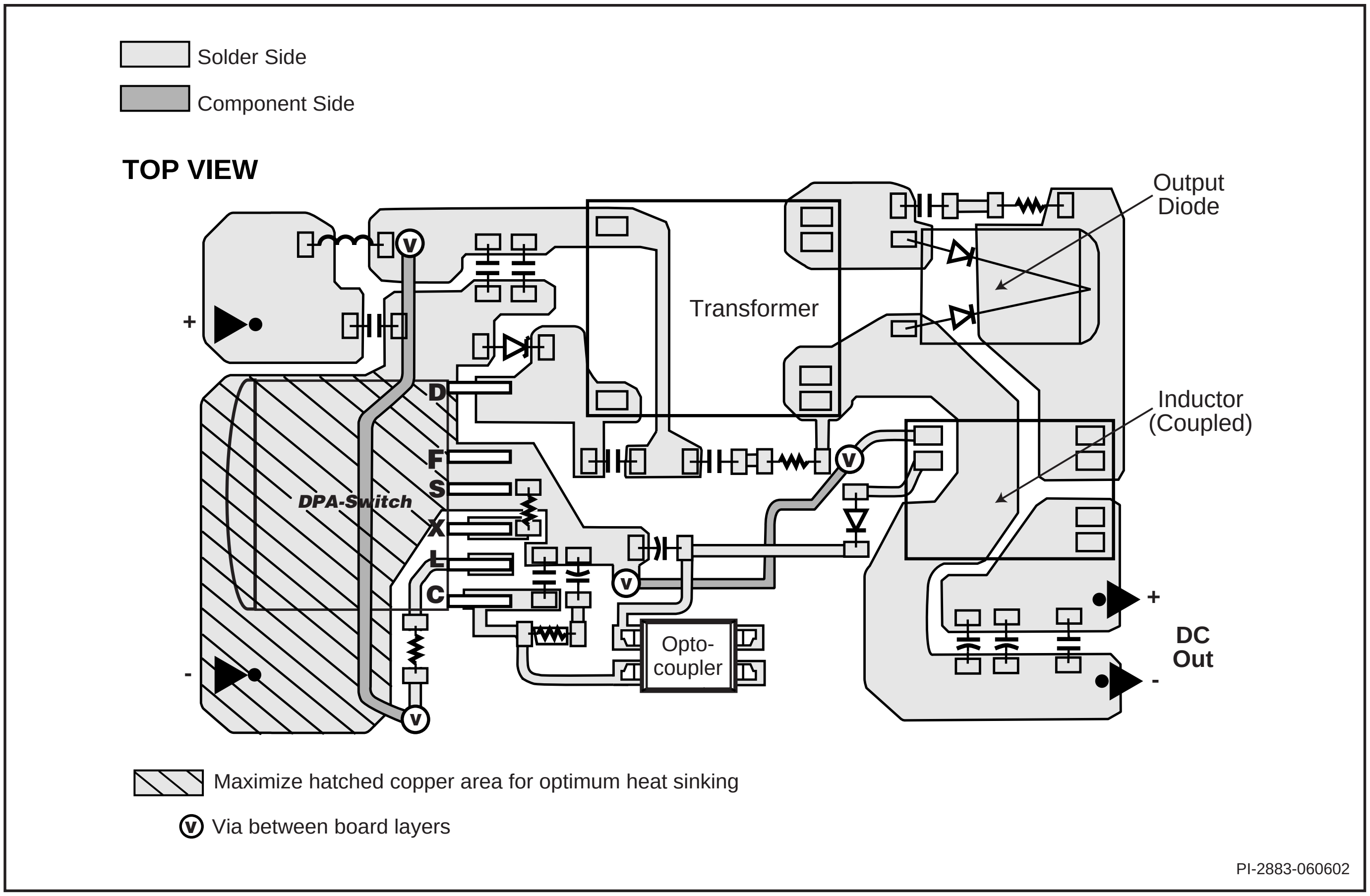

Figure 13. Layout Considerations for DPA-Switch using R Package.

Heat Sinking

To maximize heat sinking of the *DPA-Switch* and the other power components, special thermally conductive PC board material (aluminum clad PC board) is recommended. This has an aluminum sheet bonded to the PC board during the manufacturing process to provide heat sinking directly or to allow the attachment of an external heat sink. If normal PC board material is used (such as FR4), providing copper areas on both sides of the board and using thicker copper will improve heat sinking.

If an aluminum clad board is used, then shielding of switching nodes is recommended. This consists of an area of copper placed directly underneath switching nodes such as the drain node and output diode to provide an electrostatic shield to prevent coupling to the aluminum substrate. These areas are connected to input negative in the case of the primary and output return for secondary. This reduces the amount of capacitive coupling into the insulated aluminum substrate that can then appear on the output as ripple and high frequency noise.

Quick Design Checklist

As with any power supply design, all *DPA-Switch* designs should be verified on the bench to make sure that component specifications limits are not exceeded under worst case conditions. The following minimum set of tests for *DPA-Switch* forward converters is strongly recommended:

1. Maximum drain voltage – Verify that peak drain-to-source voltage does not exceed minimum BV_{DSS} at highest input voltage and maximum overload output power. It is normal, however, to have additional margin of approximately 25 V below BV_{DSS} to allow for other power supply component unit-to-unit variations. Maximum overload output power occurs when the output is loaded to a level just before the power supply goes into auto-restart (loss of regulation).

2. Transformer reset margin – Drain voltage should also be checked at highest input voltage with a severe load step (50% to 100%) to verify adequate transformer reset margin. This test slews the duty cycle at high input voltage, placing the most demand on the transformer reset circuit.

3. Maximum drain current – At maximum ambient temperature, maximum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of transformer or output inductor saturation and excessive leading edge current spikes. *DPA-Switch* has a leading edge blanking time of 100 ns to prevent premature termination of the cycle. Verify that the leading edge current spike does not extend beyond the blanking period.

4. Thermal check – At maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specifications are not exceeded for the transformer, output diodes, output inductors and output capacitors. The *DPA-Switch* is fully protected against overtemperature conditions by its thermal shutdown feature. It is recommended that sufficient heat sinking is provided to keep the tab temperature at or below 115 °C under worst case continuous load conditions (at low input voltage, maximum ambient and full load). This provides adequate margin to minimum thermal shutdown temperature (130 °C) to account for part-to-part $R_{DS(ON)}$ variation. When monitoring tab temperature, note that the junction-to-case thermal resistance should be accounted for when estimating die temperature.

Design Tools

Up-to-date information on design tools is available at the Power Integrations Web site: *www.powerint.com.*

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Revision	Notes	Date
A	1) –	6/02
B	2) Added new information: a) Bias circuits b) Synchronous rectification	4/03

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