

# TLS115x0 Demoboards

Z8F56253795

## Preface

### Scope and purpose

This document provides information about the usage of the Demoboards for the voltage tracking regulators TLS115x0EJ (PG-DSO-8-EP package variant) and the TLS115x0LD (PG-TSON-10 package variant) from Infineon Technologies AG. Please also refer to the corresponding Data Sheets [\[2\]](#) and [\[3\]](#).

### Intended audience

This document is intended for engineers who develop applications.

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**Introduction**

**1 Introduction**

**Table 1** shows an overview of the feature sets and packages in the TLS115x0 voltage tracking regulator family.

**Table 1 Family overview TLS115x0 family**

Type	Package	Output current	Enable	Power Good	Adjustable
TLS115B0EJ	PG-DSO-8-EP	150 mA	✓	–	✓
TLS115D0EJ	PG-DSO-8-EP	150 mA	✓	✓	✓
TLS115B0LD	PG-TSON-10	150 mA	✓	–	✓
TLS115D0LD	PG-TSON-10	150 mA	✓	✓	✓

**1.1 TLS115x0 features**

- 150 mA current capability
- very high accuracy voltage tracking
- output voltage adjustable down to 2.0 V
- very low dropout voltage
- very low current consumption in OFF mode
- Power Good output indicates overvoltage and undervoltage<sup>1)</sup>
- internally controlled soft start
- Green product (RoHS compliant)
- AEC Qualified

Additional benefits of the TLS115x0 voltage tracking regulators:

- fast regulation
- very good stability characteristics
- only a small ceramic capacitor of 1 µF at the output is required
- internal protection features make the devices robust against immediate damage:
  - output current limitation
  - short circuit protected output (to GND and to battery)
  - overtemperature shutdown
  - reverse polarity protected input

These features make the TLS115x0 voltage tracking regulators perfectly suitable as automotive sensor supply and as high precision supply for off-board loads.

<sup>1</sup> valid for TLS115D0

Introduction

### 1.2 Block diagram

Figure 1 shows the block diagram of TLS115D0, which offers the full feature set.

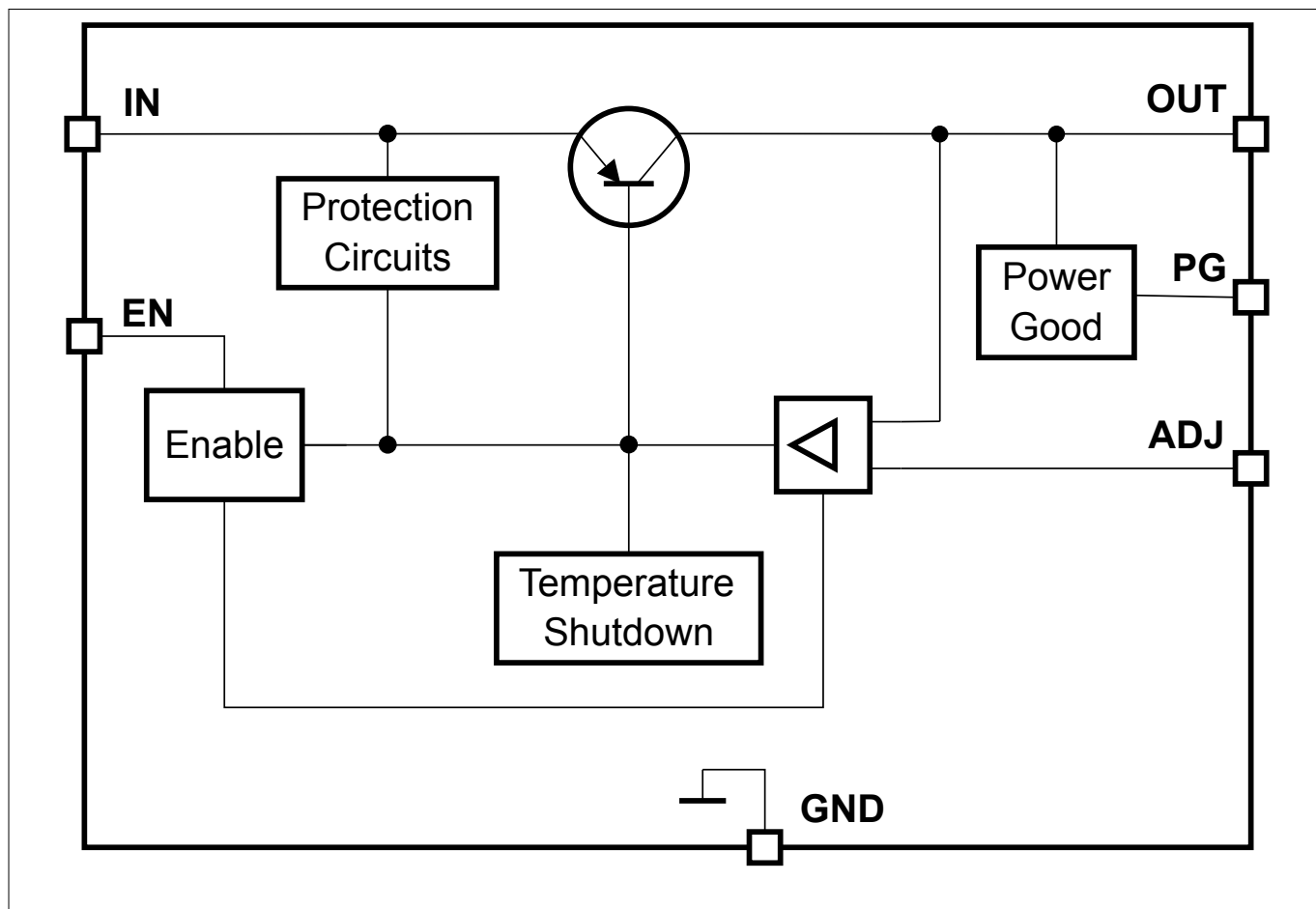


Figure 1 Block diagram of TLS115D0

Demoboard

## 2 Demoboard

The TLS115x0 Demoboards are available for all devices of the TLS115x0 voltage tracking regulator family in a PG-DSO-8-EP or PG-TSON-10 package (see the device list in [Table 1](#)).

[Figure 2](#) shows the TLS115x0EJ Demoboard equipped with TLS115D0EJ (PG-DSO-8-EP package).

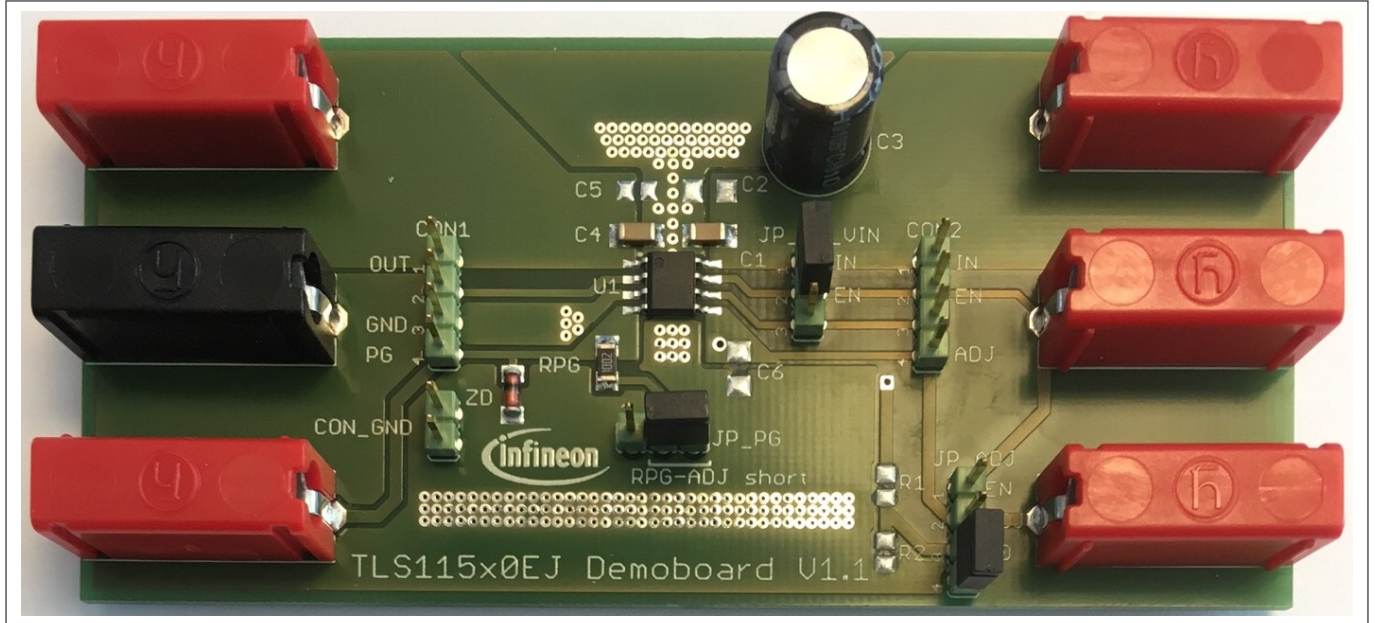


Figure 2 TLS115x0EJ Demoboard

[Figure 3](#) shows the TLS115x0LD Demoboard equipped with TLS115D0LD (PG-TSON-10 package).



Figure 3 TLS115x0LD Demoboard

**Demoboard**

## 2.1 Operating conditions

To avoid electrical damage of the Demoboard, the operating range defined in [Table 2](#) must be followed.

**Table 2 Limit values for operation<sup>1)</sup>**

Parameter	Pin	Maximum Ratings		Unit	Note
		Min.	Max.		
Board supply voltage <sup>2)</sup>	VIN	-16	45	V	power supply
Adjust voltage <sup>3)</sup>	VADJ	-16	45	V	tracked reference voltage
Regulator output voltage	VOUT	-5	45	V	–
Enable input signal	EN	-16	45	V	enables or disables the voltage tracking regulator
Power Good output signal	PG	-0.3	7	V	indicates, whether Power Good conditions are met
Ground	GND	0	0	V	system GND

## 2.2 Demoboard configuration

The jumper pins and solder pads on the Demoboards provide easy to use configuration options.

- jumper connections:
  - EN input pin ↔ supply voltage pin VIN (JP\_EN\_VIN)
  - ADJ pin ↔ EN pin or  
ADJ pin ↔ external voltage divider  
to adjust the reference voltage depending on voltage at VIN pin (JP\_ADJ)
  - ADJ pin ↔ RPG pin  
as pull-up voltage for the Power Good resistor RPG (JP\_PG)
- solder pads for the following components:
  - additional input capacitor C2
  - additional output capacitor C5
  - adjust capacitor C6
  - voltage divider resistor R1
  - voltage divider resistor R2

### 2.2.1 Jumpers

The unlabeled pin of each jumper can take an unused connector to leave the connection open.

#### Jumper JP\_EN\_VIN

The JP\_EN\_VIN jumper can connect the EN input pin to the supply voltage at the VIN pin.

<sup>1</sup> The Demoboard operates at an ambient temperature of 25°C

<sup>2</sup> Functional input voltage range: 4 V to 45 V

<sup>3</sup> Functional ADJ voltage range: 2 V to 14 V

**Demoboard**

**Table 3 Jumper JP\_EN\_VIN options for Enable function**

JP_EN_VIN	Function
EN input pin ↔ VIN pin	the regulator is enabled while it is supplied from the voltage at the VIN pin
open	the EN input pin is supplied from the EN banana jack connector <sup>4)</sup>

**Jumper JP\_ADJ**

The JP\_ADJ jumper can connect the ADJ pin of the device to one of the following:

- the voltage at the EN pin ( $V_{EN}$ ), if the ADJ pin is not supplied from an external voltage
- a reference voltage ( $V_D$ ) adapted by the voltage divider on the demoboard

**Table 4 Jumper JP\_ADJ options for reference voltage**

JP_ADJ	Function
ADJ pin ↔ EN input pin	the ADJ pin is connected to the voltage at the EN pin
ADJ pin ↔ $V_D$	the ADJ pin is connected to the output voltage of the voltage divider ( $V_D$ )
open	the ADJ pin must be supplied from external via ADJ banana jack connector. <sup>5)</sup>

If the ADJ pin is to be supplied from the output voltage of the voltage divider ( $V_D$ ), then the resistors of the voltage divider must be implemented. The value of the resistors can be easily calculated when neglecting the current flowing into the ADJ pin:

$$V_{ADJ} = V_D = \frac{R_2}{R_1 + R_2} \times V_{IN}$$

**Equation 1**

The current flowing into the ADJ pin can be neglected, if  $R_2$  is less than 2.5 kΩ. To benefit from the high accuracy of the TLS115x0, it is highly recommended to supply the ADJ pin from an external voltage source via the banana jack connector.

**PG Jumper**

With jumper JP\_PG, the voltage at the ADJ pin can be used as pull-up voltage for the Power Good resistor RPG. The Power Good signal, which then corresponds to the voltage at the ADJ pin, can then be measured at the PG connector of the Demoboard. To protect the the device from overvoltage, the PG connector is clamped by a Z-diode to typically 6.2 V.

**Table 5 Jumper JP\_PG options for Power Good function**

JP_PG	Function
PG ↔ ADJ pin	The voltage applied at the ADJ pin is used as pull-up voltage for the Power Good resistor RPG. Power Good monitoring is enabled.
open	No pull-up voltage is applied to the Power Good resistor RPG. Power Good monitoring is disabled.

<sup>4</sup> Without supplying a signal to EN, the regulator is disabled because of the internal pull-down resistor

<sup>5</sup> Without supplying a reference voltage to ADJ, the regulator is disabled

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**Demoboard**

### **2.2.2 Signal adaption**

The connectors CON1, CON2 and CON\_GND offer easy signal adaption, for example with probes for an oscilloscope.

**Table 6 Signals on connector**

<b>Connector</b>	<b>Accessible signal</b>
CON1	<ul style="list-style-type: none"><li>• OUT (output voltage)</li><li>• GND (ground)</li><li>• PG (Power Good signal)</li></ul>
CON2	<ul style="list-style-type: none"><li>• IN (input voltage)</li><li>• EN (Enable input signal)</li><li>• ADJ (reference voltage)</li></ul>
CON_GND	<ul style="list-style-type: none"><li>• GND (ground)</li></ul>

### 3 Schematic and layout TLS115x0EJ Demoboard

#### 3.1 Schematic TLS115x0EJ Demoboard

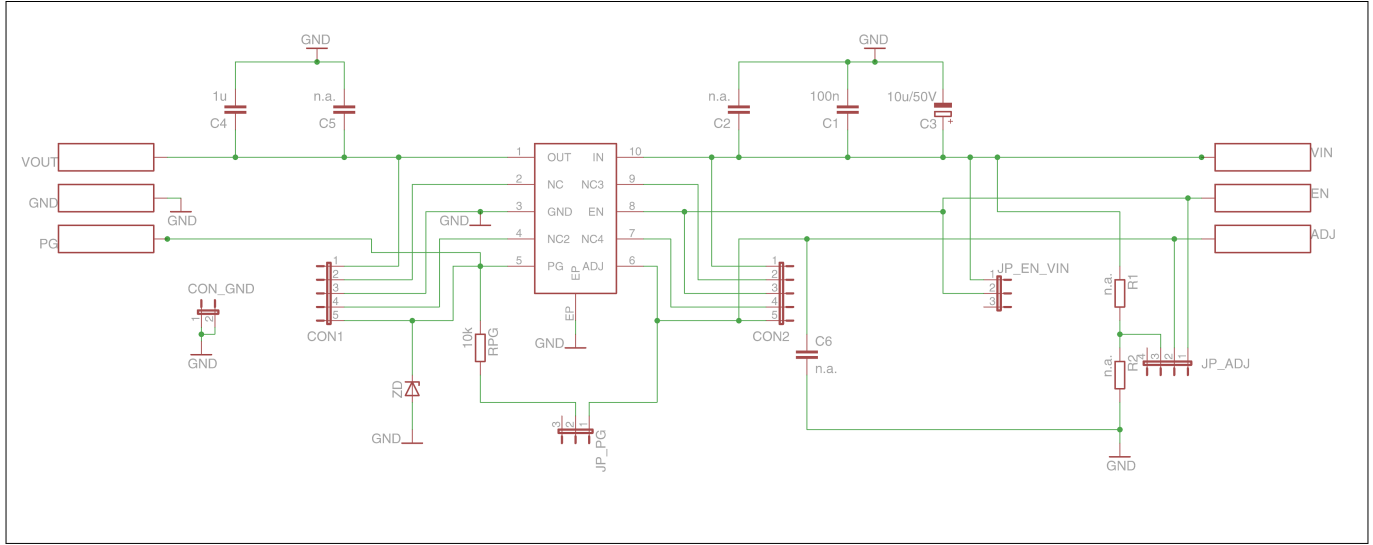


Figure 4 Schematic of TLS115x0EJ Demoboard



Schematic and layout TLS115x0EJ Demoboard

3.2 Layout TLS115x0EJ Demoboard

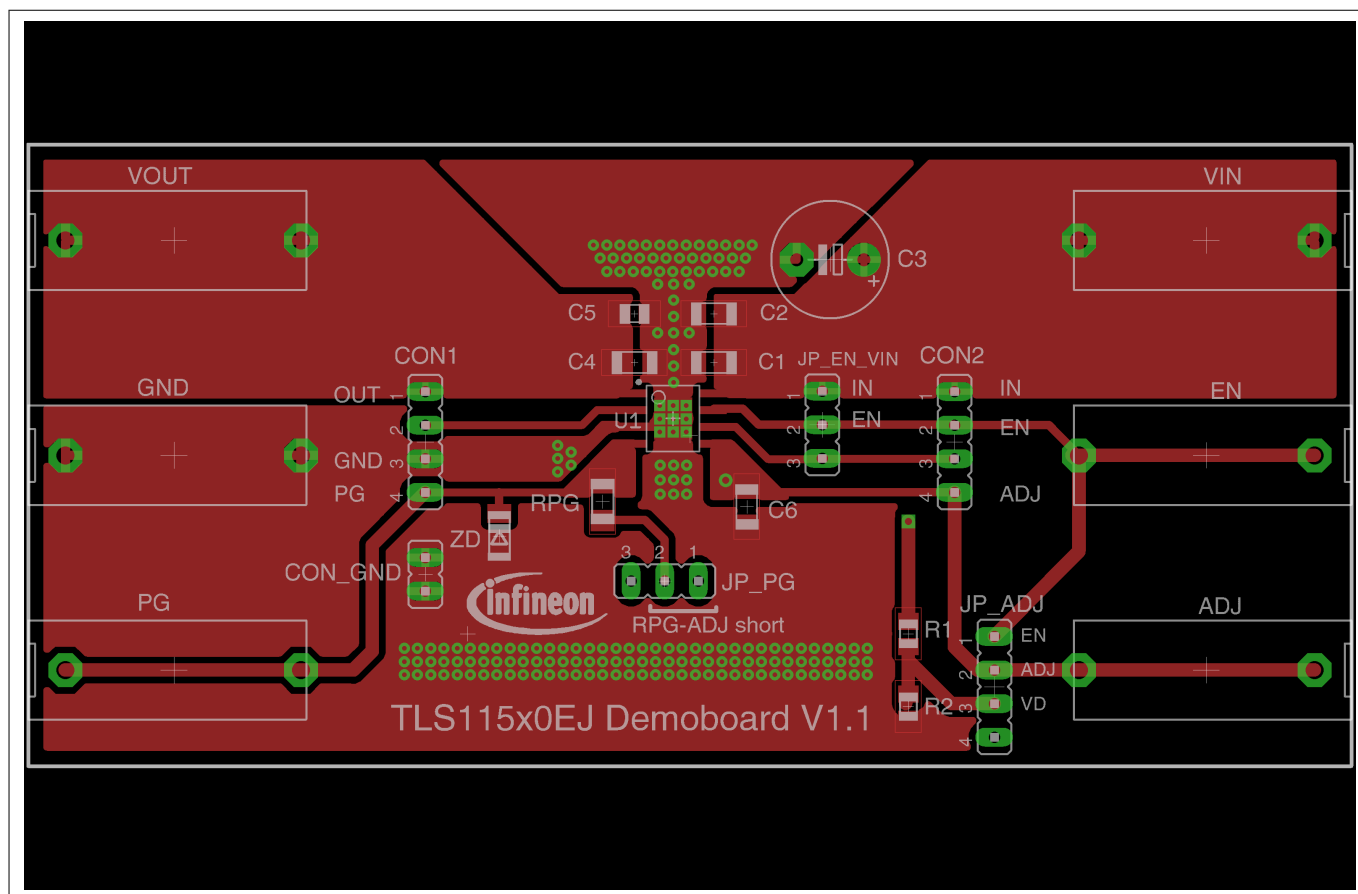


Figure 5 Top layer of TLS115x0EJ Demoboard

Schematic and layout TLS115x0EJ Demoboard

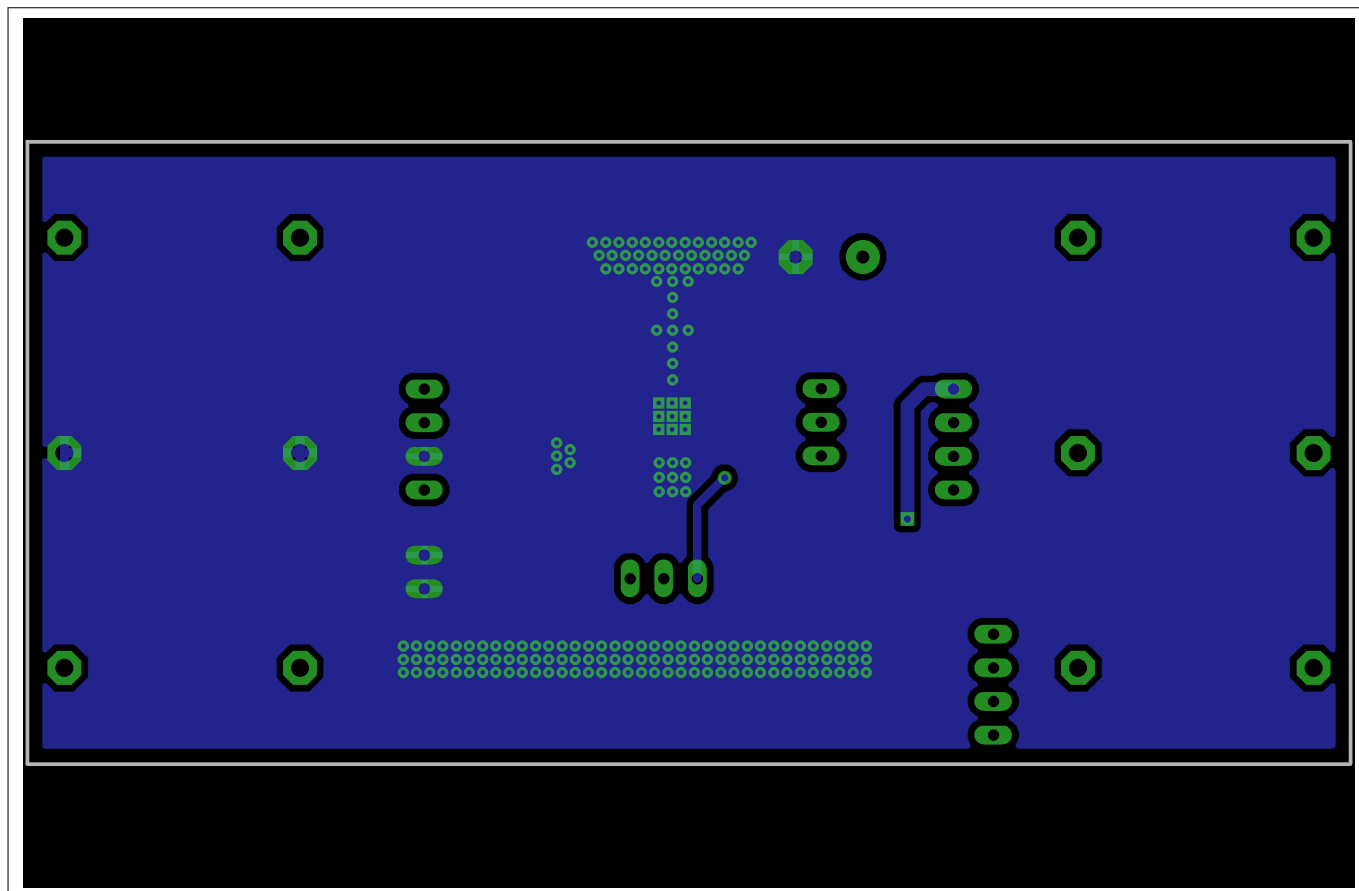


Figure 6 Bottom layer of TLS115x0EJ Demoboard

Schematic and layout TLS115x0LD Demoboard

## 4 Schematic and layout TLS115x0LD Demoboard

### 4.1 Schematic TLS115x0LD Demoboard

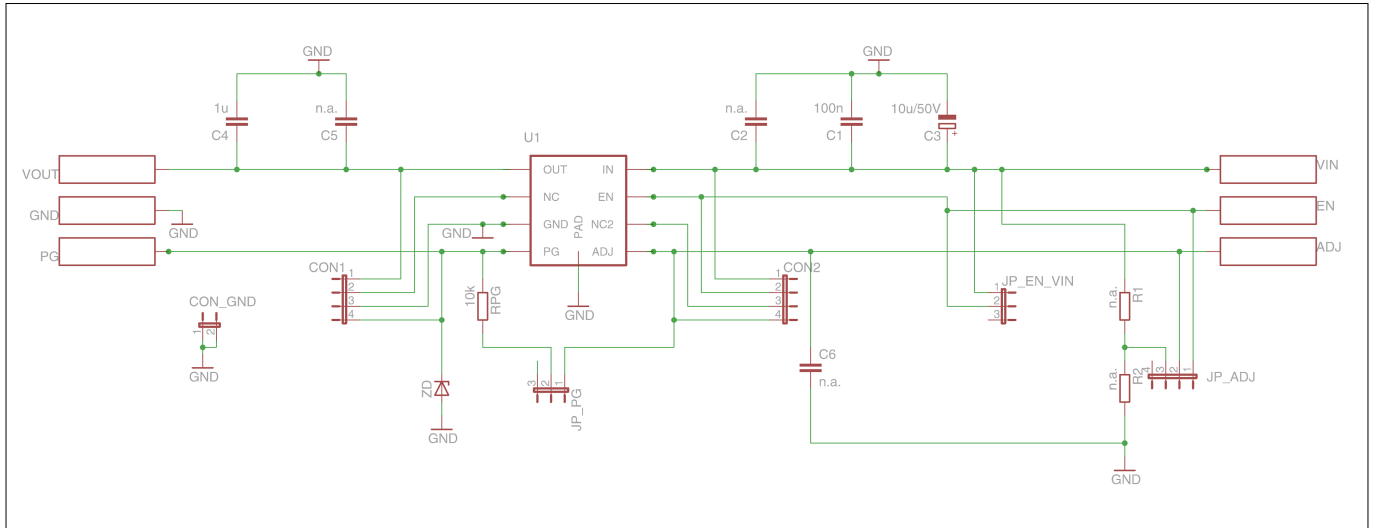


Figure 7 Schematic of TLS115x0LD Demoboard

Schematic and layout TLS115x0LD Demoboard

4.2 Layout TLS115x0LD Demoboard

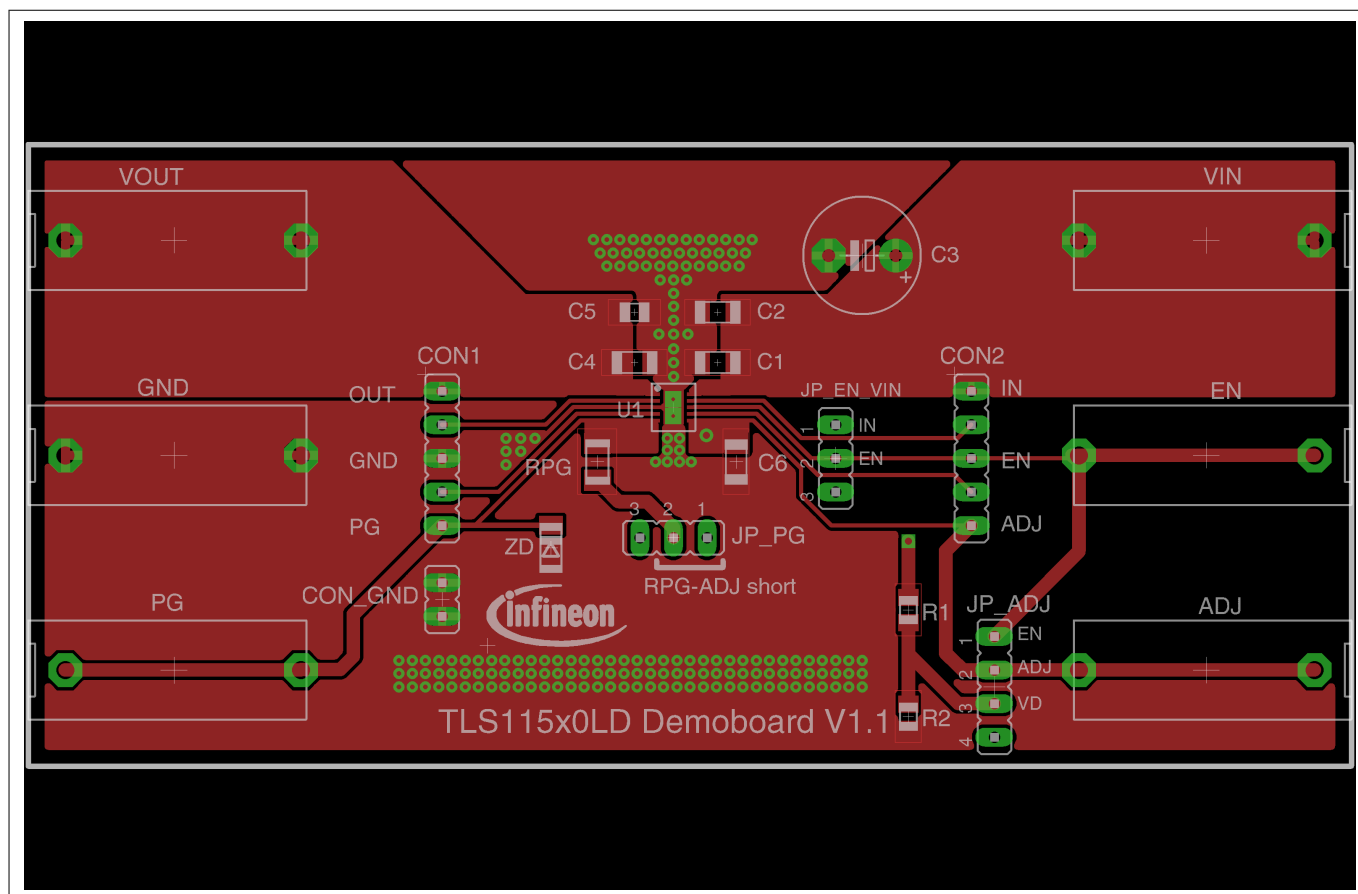


Figure 8 Top layer of TLS115x0LD Demoboard

Schematic and layout TLS115x0LD Demoboard

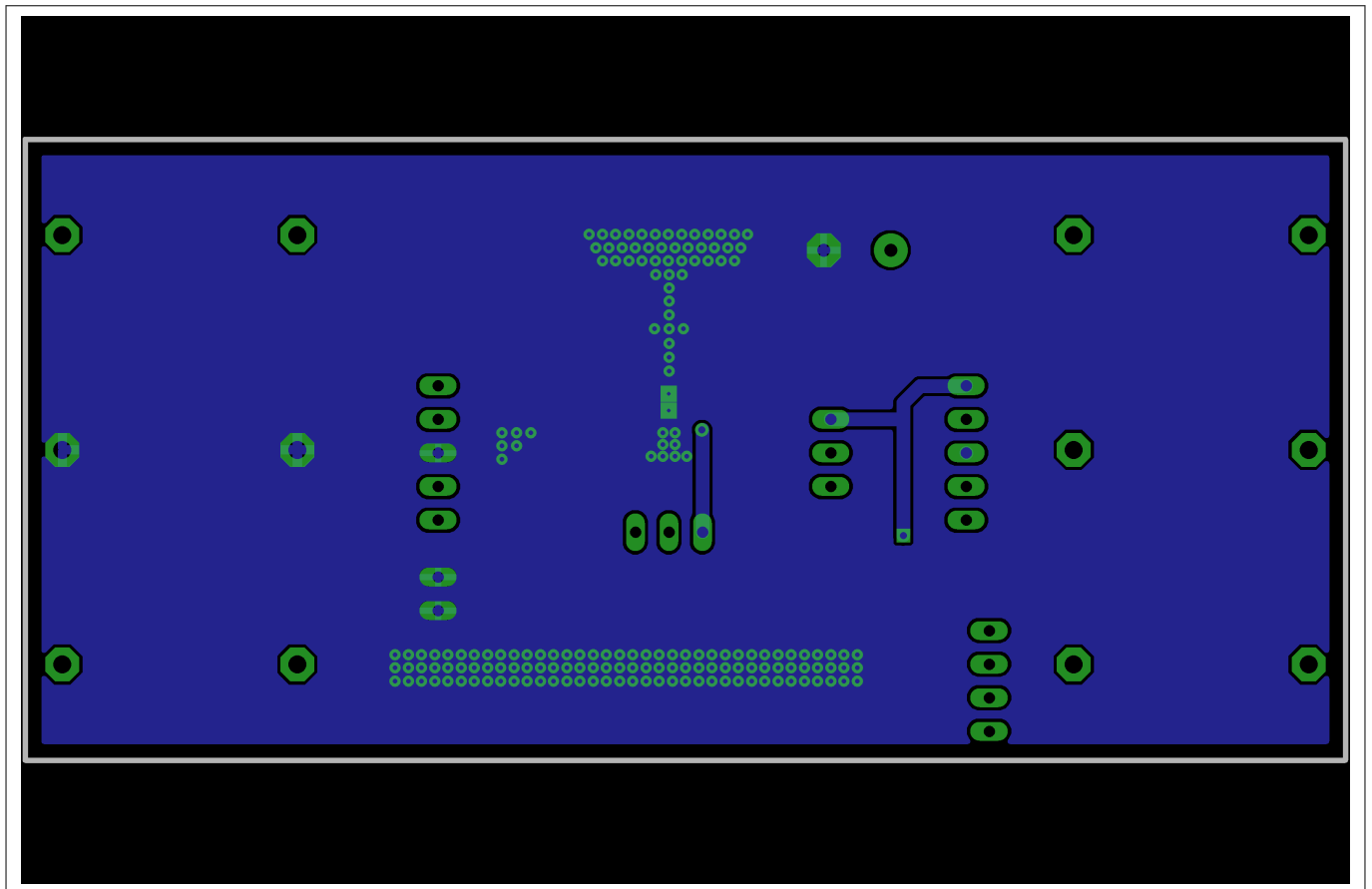


Figure 9 Bottom layer of TLS115x0LD Demoboard

**Bill of material**

**5 Bill of material**

**Table 7 Bill of Material**

<b>Part</b>	<b>Value</b>	<b>Package</b>
U1	one of the following: <ul style="list-style-type: none"> <li>• TLS115B0EJ or TLS115D0EJ</li> <li>• TLS115B0LD or TLS115D0LD</li> </ul>	one of the following: <ul style="list-style-type: none"> <li>• PG-DSO-8-EP</li> <li>• PG-TSON-10</li> </ul>
VIN	banana jack	BABU4MM
VOUT	banana jack	BABU4MM
EN	banana jack	BABU4MM
PG	banana jack	BABU4MM
GND	banana jack	BABU4MM
R1	n.a.	R0805
R2	n.a.	R0805
RPG	10 k $\Omega$	R1206
C1	100 nF / 50 V	C1206
C2	n.a.	C1206
C3	10 $\mu$ F / 50 V	E5-8.5
C4	1 $\mu$ F / 16 V	C1206
C5	n.a.	C0805
C6	n.a.	C1206
CON1	4 pin connector	–
CON2	4 pin connector	–
CON_GND	2 pin connector	–
JP_EN_VIN	–	jumper
JP_ADJ	–	jumper
JP_PG	–	jumper
ZD	Z-diode ZMM6.2 (6.2 V)	SOD80C

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**Restrictions**

## **6 Restrictions**

This Demoboard offers limited features only for evaluation and testing of Infineon products. The Demoboard is not an end product or finished appliance, nor is it intended or authorized by Infineon to be integrated into end products. The Demoboard may not be used in any production system.

For further information please contact [www.infineon.com](http://www.infineon.com).

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References

## 7 References

Table 8

Number	Bibliography
[1]	What The Designer Should Know – Introduction to Automotive Linear Voltage Regulators. Infineon Technologies AG
[2]	TLS115B0 Data Sheet, Infineon Technologies AG
[3]	TLS115D0 Data Sheet, Infineon Technologies AG



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**Revision history**

## **8 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
1.0	2017-02-22	Application Note created

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