General Description

The DA16200 is a highly integrated ultra-low power Wi-Fi system on a chip(SoC), which contains an 802.11b/g/n radio(PHY), a baseband processor, a media access controller(MAC), on-chip memory, and a host networking application processor, all on a single silicon die.

The SoC enables full offload capabilities, running the entire networking stack on chip so that no external network processor, CPU, or microcontroller is required, while many other SoCs optionally use a microcontroller.

DA16200 is a synthesis of breakthrough ultra-low power technologies which enables extremely low power operation in the SoC. DA16200 shuts down every micro element of the chip that is not in use, which allows a near zero level of power consumption when not actively transmitting or receiving data. Such low power operation can extend the battery life as long as a year or more depending on the application. DA16200 also enables ultra-low power transmitting and receiving modes when the SoC needs to be awake to exchange information with other devices. Advanced algorithms enable staying asleep until the exact moment required to wake up to transmit or receive.

The SoC is built from the ground up for the Internet of Things (IoT) and is ideal for door locks, thermostats, sensors, pet trackers, asset trackers, sprinkler systems, connected lighting, video cameras, video door bells, wearables and other IoT devices.

Key Features

- Highly integrated ultra-low power Wi-Fi® system on chip
- Full offload: SoC runs full networking OS and TCP/IP stack
- Wi-Fi processor
  - IEEE 802.11b/g/n, 1×1, 20 MHz channel bandwidth, 2.4 GHz
  - IEEE 802.11s Wi-Fi mesh
  - On-chip PA, LNA, and RF switch
  - Wi-Fi security: WPA/WPA2-Enterprise/Personal, WPA2 SI, WPA3 SAE, and OWE
  - Vendor EAP types: EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1, EAP-FAST, and EAP-TLS
  - Operating modes: Station, SoftAP, and Wi-Fi Direct® Modes (GO, GC, GO fixed)
  - WPS-PIN/PBC for easy Wi-Fi provisioning
  - Connection manager for autonomous and fast Wi-Fi connections
  - Bluetooth coexistence
  - Antenna switching diversity
- Built-in 4-channel auxiliary ADC for sensor interfaces
  - 12-bit SAR ADC: single-ended four channels
  - Provides dynamic auto switching function
- Supports various interfaces
  - eMMC/SD expanded memory
  - SDIO Host/Slave function
  - QSPI for external flash control
  - Three UARTs
  - SPI Master/Slave interface
  - I2C Master/Slave interface
  - I2S for digital audio streaming
  - 4-channel PWM
  - Individually programmable, multiplexed GPIO pins
  - JTAG and SWD
- Wi-Fi Alliance certifications:
  - Wi-Fi CERTIFIED™ b, g, n
  - WPA™ - Enterprise, Personal
  - WPA2™ - Enterprise, Personal
  - WPA3™ - Enterprise, Personal
  - Wi-Fi Direct
  - Wi-Fi Enhanced Open™
  - WMM
  - WMM - Power Save
  - Wi-Fi Protected Setup™

- Direct code execution from the external serial flash memory (XIP)
- Hardware accelerators
  - General HW CRC engine
  - HW zeroing function for fast booting
  - Pseudo random number generator(PRNG)
- Complete software stack
  - Comprehensive networking software stack
  - Provides TCP/IP stack: in the form of network socket APIs
- Advanced security
  - Secure booting
  - Secure debugging using JTAG/SWD and UART ports
  - Secure asset storage
- Built-in hardware crypto engines for advanced security
  - TLS/DTLS security protocol functions
  - Crypto engine for key deliberate generic security functions: AES(128,192,256), DES/3DES, SHA1/224/256, RSA, DH, ECC, CHACHA, and TRNG
- CPU core subsystem
  - Arm® Cortex®-M4F core w/ clock frequency of 30~160 MHz
  - ROM: 256 kB
  - SRAM: 512 kB
  - OTP: 8 kB
- Power management unit
  - On-Chip RTC
  - Wake-up control of fast booting or full booting with minimal initialization time
  - Integrated DC-DC and LDOs
  - Supports three ultra-low power sleep modes
- Clock source
  - 40 MHz crystal (± 20 ppm) for master clock (initial + temp + aging)
  - 32.768 kHz crystal (± 250 ppm) for RTC clock
  - Integrated 32 kHz RC oscillator
- Supply
  - Single operating voltage: 2.1V to 3.6V (typical: 3.3V)
  - Digital I/O Supply Voltage: 1.8V / 3.3V
  - Black-out and brown-out detector
- Package type
  - 6 mm × 6 mm, 0.4 mm pitch, 48-Pin, QFN
  - 3.8 mm × 3.8 mm, 0.4 mm pitch, 72-Pin, fcCSP
- Operating temperature range
  - -40°C to 85°C

Applications

DA16200 is a full offload SoC for IoT Applications, such as:

- Security systems
- Door locks
- Thermostats
- Garage door openers
- Blinds
- Lighting control
- Sprinkler systems
- Video camera security systems
- Smart appliances
- Video door bell
- Asset tracker

System Diagram

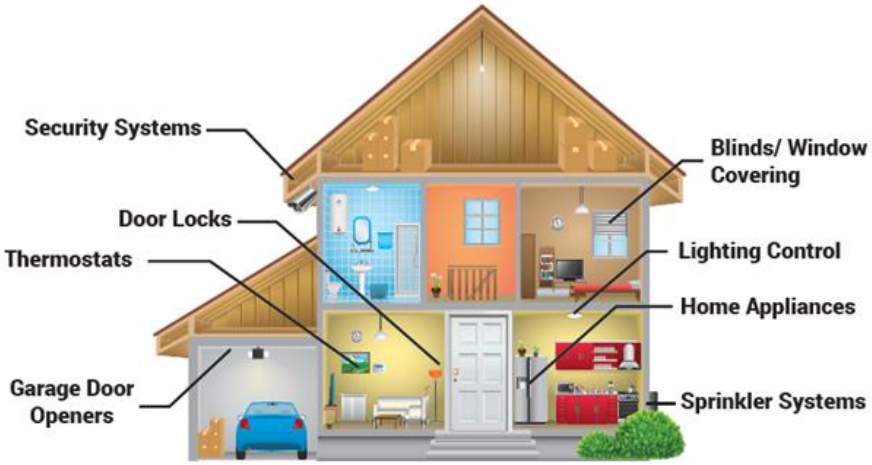


Figure 1: System Diagram

Contents

Figures

Tables

1 Terms and Definitions

API	Application Programming Interface
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
HW	Hardware
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IoT	Internet of Things
JTAG	Joint Test Action Group
LDO	Low-dropout Regulator
LLI	Linked-List Item
NVIC	Nested Vectored Interrupt Controller
NVRAM	Non-Volatile RAM
PLL	Phase-locked Loop
PRNG	Pseudo Random Number Generator
PWM	Pulse Width Modulation
QSPI	Quad-lane SPI
RTC	Real-time Clock
SAR ADC	Successive Approximation Analog-to-Digital Converter
SPI	Serial Peripheral Interface
SW	Software
SWD	Serial Wire Debug
UART	Universal Asynchronous Receivers and Transmitter
XIP	eXecute in Place
TAP	Test Access Port

2 References

[1] Arm Cortex-M4F r0p1 technical reference manual: arm_cortexm4_processor_trm_100166_0001_00_en.pdf

[2] DA16200_Example_Application_Guide.pdf

[3] ITU-T O.150, General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment, 1996

[4] Arm TrustZone® CryptoCell-312, Revision r1p1, Software Integrators Manual

[5] IEEE Standard 1149.1, Test Access Port and Boundary-Scan Architecture

[6] DA16200_SDK_Programmer_Guide.pdf

[7] AMBA AHB bus specification, Rev 3.0

[8] https://static.docs.arm.com/ihi0033/a/IHI0033A_new_eula.pdf?_ga=2.168295970.2050075868.1561605067-2006940633.1551143688

3 Block Diagram

Figure 2 shows the DA16200 hardware (HW) block diagram.

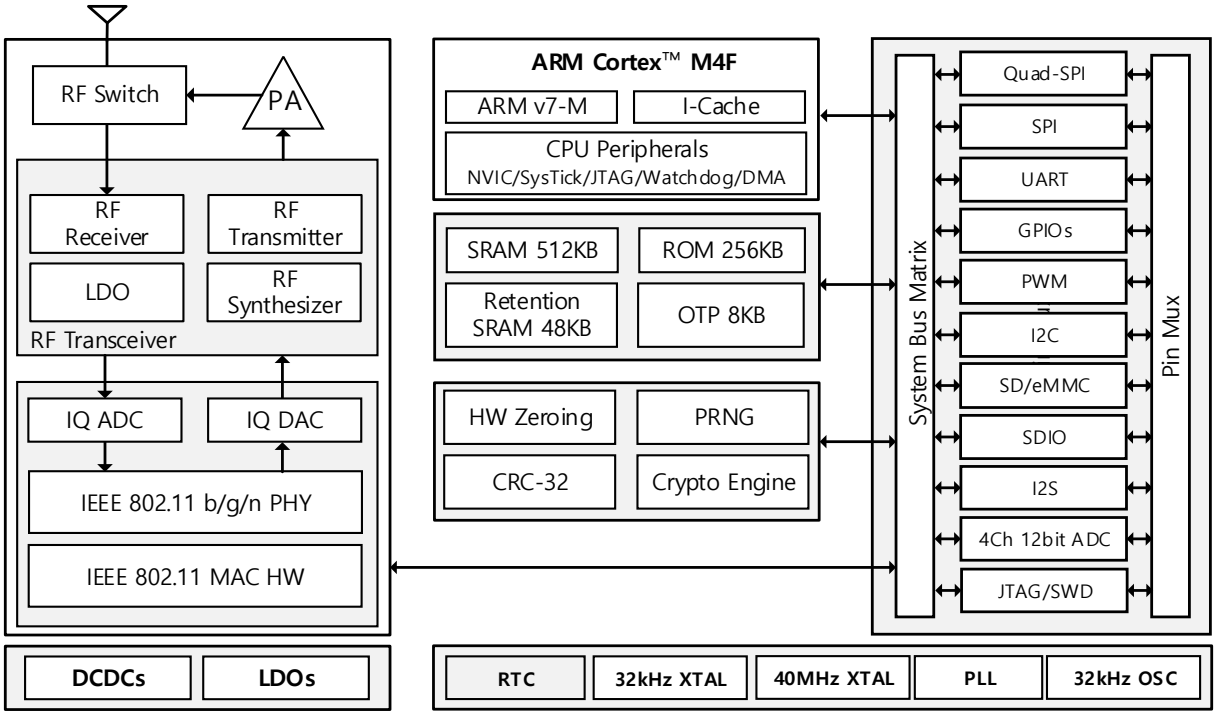


Figure 2: Hardware Block Diagram

Figure 3 shows the DA16200 software (SW) block diagram.

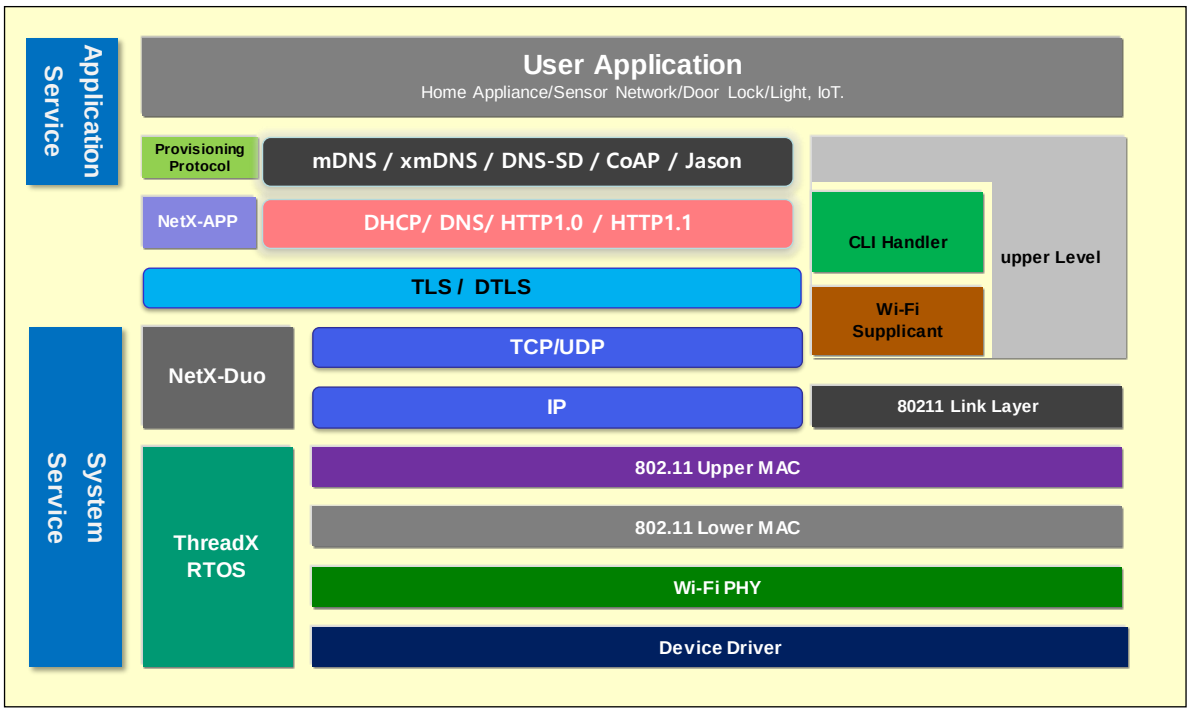


Figure 3: Software Block Diagram

The following descriptions are about the SW block diagrams.

- Kernel layer
  - Real Time Operating System
- The Wi-Fi layer is divided into four layers:
  - Lower MAC
    - SW module to control/handle HW Wi-Fi MAC/PHY and interfaces with Upper MAC layer
  - Upper MAC
    - SW module to control/handle Wi-Fi control/handle to interface with supplicant
    - Wi-Fi Link Layer: Interface layer between Upper MAC and supplicant
    - Supplicant: SW module to control/management to operate Wi-Fi operation
  - Network stack layer
    - Used to control/handle network operation
    - Main protocols are IP, TCP, and UDP
    - Other necessary protocols are supported
  - Security Layer
    - Crypto operation engine is ported to use crypto HW engine
- TLS/TCP and DTLS/UDP APIs are supported to handle security operation:
  - User application layer
    - Variable sample codes are supported in SDK – sample codes use supported APIs
    - TCP Client/Server, UDP Client/Server, TLS Client/Server
    - HTTP/HTTPs download, OTA Update usage, and MQTT usage

Customer applications can be included and implemented easily in SDK

4 Pinout

4.1 48-Pin QFN

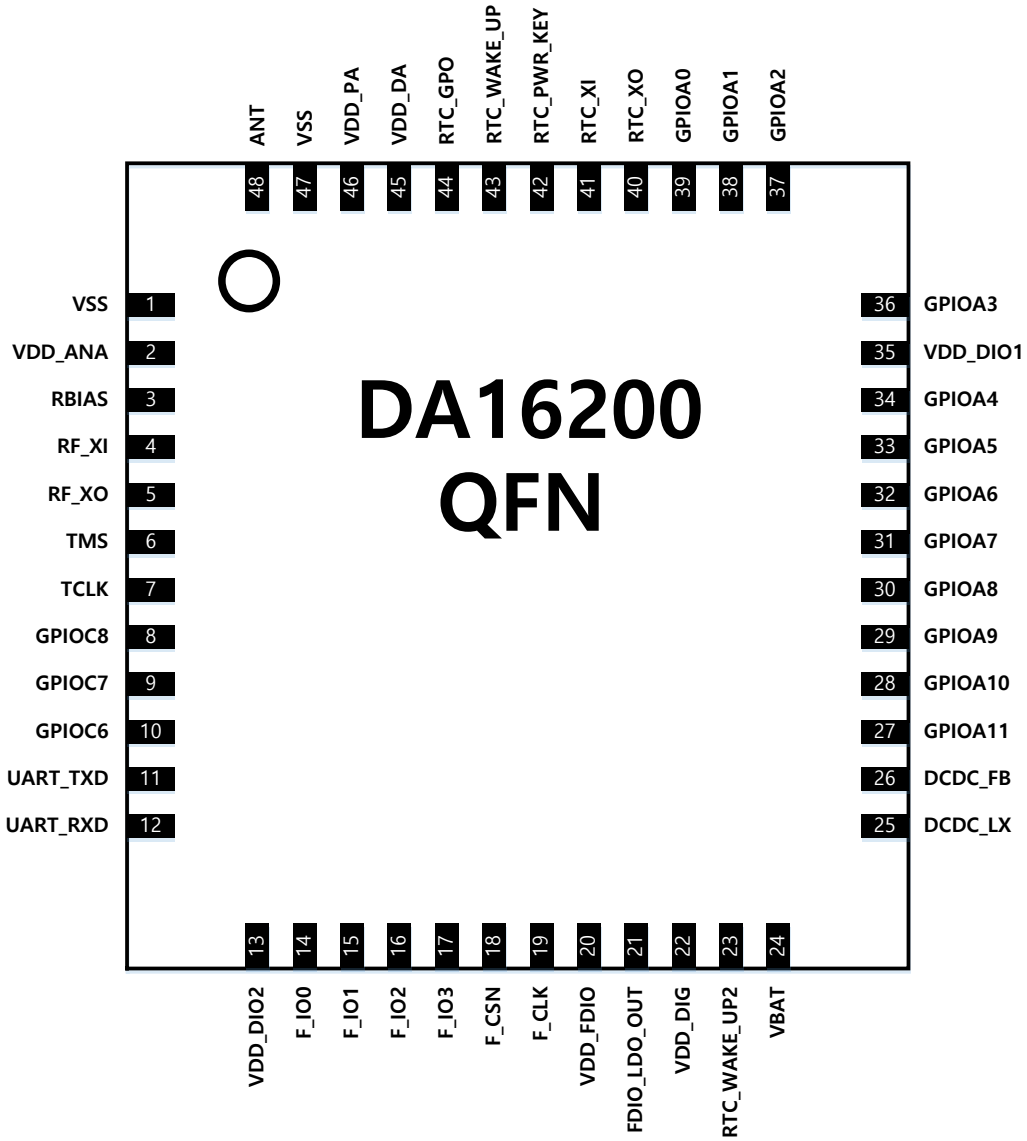


Figure 4: DA16200 QFN48 Pinout Diagram (Top View)

4.2 72-Pin fcCSP

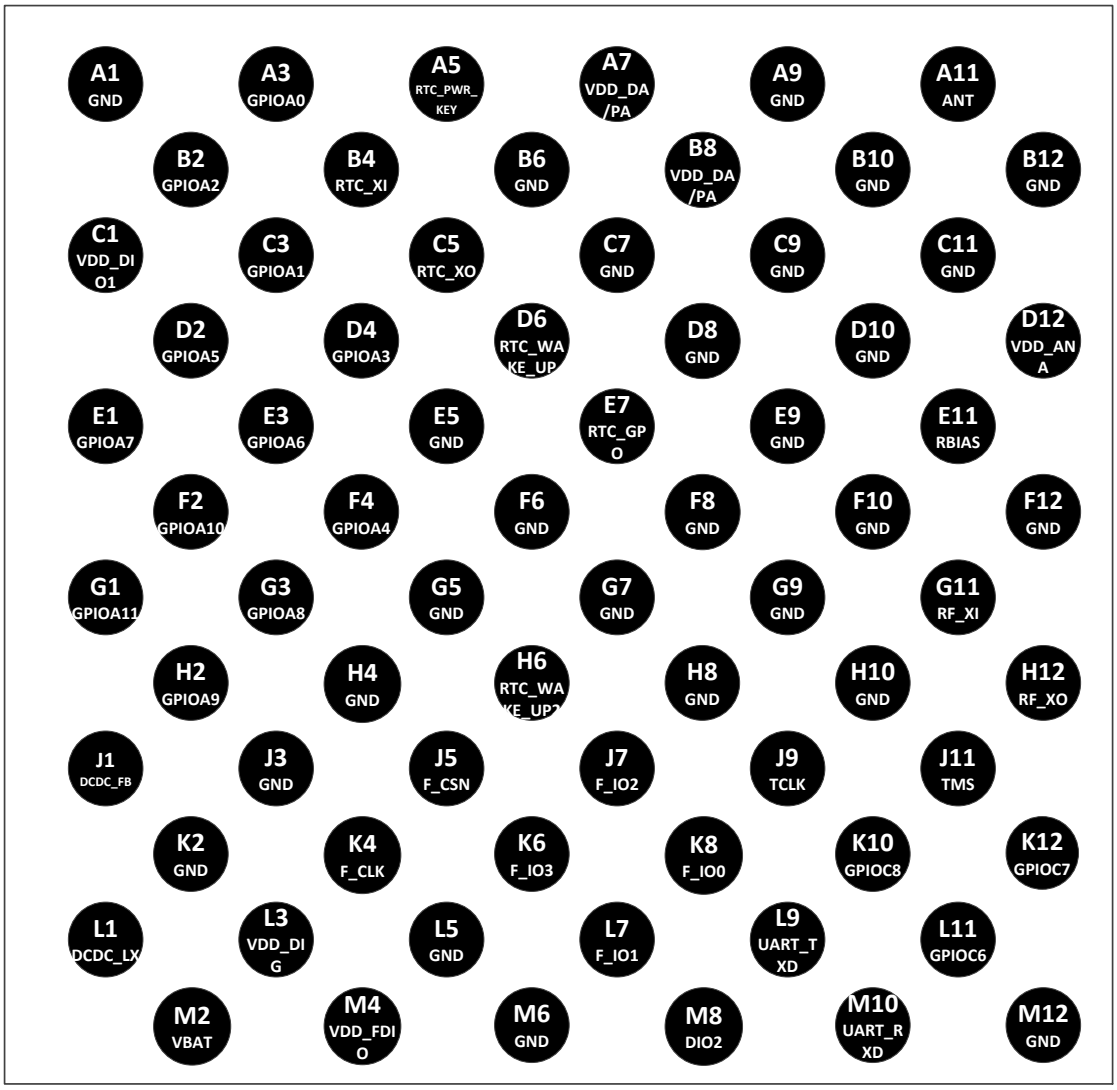


Figure 5: DA16200 fcCSP72 Pinout Diagram (Top View)

Table 1: Pin Description

QFN #Pin	fcCSP #Pin	Pin Name	Type (Table 2)	Drive (mA)	Reset State	Description
1		GND	GND			Ground
2	D12	VDD_ANA	VDD			RF VDD
3	E11	RBIAS	AIO			External reference resistor pin
4	G11	RF_XI	AI			40MHz crystal clock input
5	H12	RF_XO	AO			40MHz crystal clock output
6	J11	TMS	DIO	2/4/8/12	I-PU	JTAG I/F, SWDIO
7	J9	TCLK	DIO	2/4/8/12	I-PD	JTAG I/F, SWCLK, General Purpose I/O
8	K10	GPIOC8	DIO	2/4/8/12	I-PD	General Purpose I/O
9	K12	GPIOC7	DIO	2/4/8/12	I-PD	General Purpose I/O
10	L11	GPIOC6	DIO	2/4/8/12	I-PD	General Purpose I/O
11	L9	UART_TXD	DO	2/4/8/12	O	UART transmit data
12	M10	UART_RXD	DI	2/4/8/12	I	UART receive data
13	M8	VDD_DIO2	VDD			Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD
14	K8	F_IO0	DIO			External Flash Memory I/F
15	L7	F_IO1	DIO			External Flash Memory I/F
16	J7	F_IO2	DIO			External Flash Memory I/F
17	K6	F_IO3	DIO			External Flash Memory I/F
18	J5	F_CSN	DIO			External Flash Memory I/F
19	K4	F_CLK	DIO			External Flash Memory I/F
20	M4	VDD_FDIO	VDD			Flash IO Power
21		FDIO_LDO_OUT	AIO			Flash and IO LDO output and connect to external cap. for flash LDO
22	L3	VDD_DIG	VDD			Digital power and connect to external cap. for DIG LDO
23	H6	RTC_WAKE_UP2	DI			RTC block wake-up signal
24	M2	VBAT	VDD			Supply power for internal DC-DC, DIO_LDO, and analog IP
25	L1	DCDC_LX	AIO			Internal DC-DC feedback input for digital block supply
26	J1	DCDC_FB	AIO			Internal DC-DC feedback output for digital block supply
27	G1	GPIOA11	DIO	2/4/8/12	I-PD	General Purpose I/O
28	F2	GPIOA10	DIO	2/4/8/12	I-PD	General Purpose I/O
29	H2	GPIOA9	DIO	2/4/8/12	I-PD	General Purpose I/O
30	G3	GPIOA8	DIO	2/4/8/12	I-PD	General Purpose I/O
31	E1	GPIOA7	DIO	2/4/8/12	I-PD	General Purpose I/O
32	E3	GPIOA6	DIO	2/4/8/12	I-PD	General Purpose I/O

QFN #Pin	fcCSP #Pin	Pin Name	Type (Table 2)	Drive (mA)	Reset State	Description
33	D2	GPIOA5	DIO	2/4/8/12	I-PD	General Purpose I/O
34	F4	GPIOA4	DIO	2/4/8/12	I-PD	General Purpose I/O
35	C1	VDD_DIO1	VDD			Supply power for digital I/O GPIOA0~GPIOA11
36	D4	GPIOA3	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
37	B2	GPIOA2	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
38	C3	GPIOA1	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
39	A3	GPIOA0	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
40	C5	RTC_XO	AO			32.768kHz crystal clock output
41	B4	RTC_XI	AI			32.768kHz crystal clock input
42	A5	RTC_PWR_KEY	DI			RTC block enable signal
43	D6	RTC_WAKE_UP	DI			RTC block wake-up signal
44	E7	RTC_GPO	DO			Sensor control signal
45	A7,B8	VDD_DA	VDD			Tx DA power and RTC block power
46		VDD_PA	VDD			Supply power for integrated power amplifier
47		GND	GND			Ground
48	A11	ANT	AI			ANT
fcCSP GND Pin A1, A9, B6, B10, B12, C7, C9, C11, D8, D10, F6, F8, F10, F12, G5, G7, G9, H4, H8, H10, J3, K2, L5, M6, M12, E5						

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
DIOD	Digital input/output open drain	BP	Back drive protection
PU	Pull-up resistor (fixed)	SPU	Switchable pull-up resistor
PD	Pull-down resistor (fixed)	SPD	Switchable pull-down resistor
PWR	Power	GND	Ground

4.3 Pin Multiplexing

This device provides various interfaces to support many kinds of applications. It is possible to control each pin according to the required application in reference to the pin multiplexing illustrated in Table 3. Pin control can be realized through register setting. This device can use a maximum of 16 GPIO pins and each of the GPIO pins multiplexes signals of various functions. In particular, four pins from GPIOA0 to GPIOA3 multiplex analog signals, which also can be realized through register setting.

Table 3: DA16200 Pin Multiplexing

Pin	JTAG	Analog	SPI master	SPI slave	I2C master	I2C slave	SDIO slave	SDeMMC	BT coex	I2S	I2S_Clock	UART1	UART2	Muxed w/Analog	Pin State (nRESET=0)	Driving Strength (Note 1)
GPIOA0		CH0		SPI_MISO	I2C_SDA	I2C_SDA				BCLK		TXD		Yes	I-PD	2/4/8/12mA
GPIOA1		CH1		SPI_MOSI	I2C_CLK	I2C_CLK		WRP		MCLK		RXD		Yes	I-PD	2/4/8/12mA
GPIOA2		CH2		SPI_CSB		I2C_SDA				SDO	CLK_IN	TXD		Yes	I-PD	2/4/8/12mA
GPIOA3		CH3		SPI_CLK		I2C_CLK				LRCK		RXD		Yes	I-PD	2/4/8/12mA
GPIOA4					I2C_SDA	I2C_SDA	CMD	CMD		BCLK		TXD/RTS		No	I-PD	2/4/8/12mA
GPIOA5					I2C_CLK	I2C_CLK	CLK	CLK		MCLK		RXD/CTS		No	I-PD	2/4/8/12mA
GPIOA6			SPI_CSB	SPI_CSB		I2C_SDA	D3	D3		SDO		TXD		No	I-PD	2/4/8/12mA
GPIOA7			SPI_CLK	SPI_CLK		I2C_CLK	D2	D2		LRCK		RXD		No	I-PD	2/4/8/12mA
GPIOA8			SPI_DIO0	SPI_MISO	I2C_SDA		D1	D1	BT_SIG0	BCLK				No	I-PD	2/4/8/12mA
GPIOA9			SPI_DIO1	SPI_MOSI	I2C_CLK		D0	D0	BT_SIG1	MCLK				No	I-PD	2/4/8/12mA
GPIOA10			SPI_DIO2	SPI_MISO				WRP	BT_SIG2		CLK_IN		TXD	No	I-PD	2/4/8/12mA
GPIOA11			SPI_DIO3	SPI_MOSI									RXD	No	I-PD	2/4/8/12mA
TCLK/ GPIOA15	TCLK													No	I-PD	2/4/8/12mA
TMS	TMS													No	I-PU	2/4/8/12mA
UART_TXD														No	O	2/4/8/12mA
UART_RXD														No	I	2/4/8/12mA
GPIOC8	TDI													No	I-PD	2/4/8/12mA
GPIOC7	TDO												RXD	No	I-PD	2/4/8/12mA
GPIOC6	NTRST												TXD	No	I-PD	2/4/8/12mA
F_IO1				SPI_MOSI			D0			LRCK				No		2/4/8/12mA
F_IO2				SPI_MISO			D1			SDO			RXD	No		2/4/8/12mA
F_IO3							D2						TXD	No		2/4/8/12mA
F_IO4							D3							No		2/4/8/12mA
F_CSN				SPI_CSB			CMD			BCLK				No		2/4/8/12mA
F_CLK				SPI_CLK			CLK			MCLK				No		2/4/8/12mA

Note 1 Default Value: 8 mA

5 Electrical Specification

5.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Parameter	QFN Pins	fcCSP Pins	Min	Max	Units
VBAT, VDD_DA, VDD_PA	24, 45, 46	M2,A7,B8	VSS	3.9	V
VDD_DIO1	35	C1	VSS	3.9	V
VDD_DIO2	13	M8	VSS	3.9	V
VDD_FDIO	20	M4	VSS	3.9	V
FDIO_LDO_OUT	21	-	VSS	3.9	V
VDD_DIG	22	L3	VSS	1.32	V
VDD_ANA	2	D12	VSS	1.65	V
Operating temperature range (TA)			-40	+85	°C

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	QFN Pins	fcCSP Pins	Min	Typ	Max	Units
VBAT, VDD_DA, VDD_PA	24, 45, 46	M2,A7,B8	2.1		3.6	V
VDD_DIO1	35	C1	1.62		3.6	V
VDD_DIO2	13	M8	1.62		3.6	V
VDD_FDIO	20	M4	1.62		3.6	V
FDIO_LDO_OUT	21	-	1.62		3.6	V
VDD_DIG	22	L3		1.1		V
VDD_ANA	2	D12		1.37		V
Operating temperature range(TA)			-40		+85	°C

5.3 Electrical Characteristics

5.3.1 DC Parameters, 1.8 V IO

Table 6: DC Parameters, 1.8 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.2 × DVDD	V
Input High Voltage	V_{IH}	Guaranteed logic High level	0.8 × DVDD		DVDD	V
Output Low Voltage	V_{OL}	DVDD=Min.	VSS		0.3 × DVDD	V
Output High Voltage	V_{OH}	DVDD=Min.	0.7 × DVDD		DVDD	V
Pull-up Resistor	R_{PU}	$V_{PAD}=V_{IH}$, DIO=Min.			32.4	kΩ
Pull-down Resistor	R_{PD}	V_{PAD}=VIL, DIO=Min.			32.4	

Note 1 DVDD = 1.8 V, VDD_DIO1, VDD_DIO2 Logic Level

5.3.2 DC Parameters, 3.3 V IO

Table 7: DC Parameters, 3.3V IO

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Low Voltage	V_{IL}	Guaranteed logic Low level	VSS		0.8	V
Input High Voltage	V_{IH}	Guaranteed logic High level	2.2		DVDD	V
Output Low Voltage	V_{OL}	DVDD=Min.	VSS		0.4	V
Output High Voltage	V_{OH}	DVDD=Min.	2.4		DVDD	V
Pull-up Resistor	R_{PU}	VPAD=VIH, DIO=Min.			19.4	kΩ
Pull-down Resistor	R_{PD}	$V_{PAD}=V_{IL}$, DIO=Min.			16.0	

Note 1 DVDD= 3.3 V, VDD_DIO1, VDD_DIO2 Logic Level

5.4 Radio Characteristics

5.4.1 WLAN Receiver Characteristics

TA = +25 °C, VBAT = 3.3 V. Parameters are measured at ANT pin on CH1 (2412 MHz).

Table 8: WLAN Receiver Characteristics - QFN

Parameter	Condition	Min	Typ	Max	Units
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)	1 Mbps DSSS	-100.5	-99.5	-97.5	dBm
	2 Mbps DSSS	-96	-95	-93	
	11 Mbps CCK	-91	-90	-88	
	6 Mbps OFDM	-92	-91	-89	
	9 Mbps OFDM	-92	-91	-89	
	18 Mbps OFDM	-90	-89	-87	
	36 Mbps OFDM	-83	-82	-80	
	54 Mbps OFDM	-77	-76	-74	
	MCS0(GF)	-92	-91	-89	
	MCS7(GF)	-94	-73	-71	
Maximum input level (8% PER for 11b rates, 10% PER for 11g/11n rates)	802.11b	-10	-4	-3	
	802.11g	-10	-4	-3	

Table 9: WLAN Receiver Characteristics - fcCSP

Parameter	Condition	Min	Typ	Max	Units
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)	1Mbps DSSS	-100.5	-99.5	-97.5	dBm
	2Mbps DSSS	-96	-95	-93	
	11Mbps CCK	-91	-90	-88	
	6Mbps OFDM	-92	-91	-89	
	9Mbps OFDM	-92	-91	-89	
	18Mbps OFDM	-90	-89	-87	
	36Mbps OFDM	-83	-82	-80	
	54Mbps OFDM	-77	-76	-74	
	MCS0(GF)	-92	-91	-89	
	MCS7(GF)	-74	-73	-71	
Maximum input level (8% PER for 11b rates, 10% PER for 11g/11n rates)	802.11b	-10	-4	-3	
	802.11g	-10	-4	-3	

5.4.2 WLAN Transmitter Characteristics

TA = +25 °C, VBAT = 3.3 V. Parameters are measured at ANT pin on CH1 (2412 MHz).

Table 10: WLAN Transmitter Characteristics - QFN

Parameter	Condition	Min	Typ	Max	Units
Maximum Output Power measured from IEEE spectral mask and EVM	1 Mbps DSSS	17.5	20.0	21	dBm
	2 Mbps DSSS	17.5	20.0	21	
	5.5 Mbps CCK	17.5	20.0	21	
	11 Mbps CCK	17.5	20.0	21	
	6 Mbps OFDM	16.5	19.0	20	
	9 Mbps OFDM	16.5	19.0	20	
	12 Mbps OFDM	16.5	19.0	20	
	18 Mbps OFDM	16.5	19.0	20	
	24 Mbps OFDM	15.5	18.0	19	
	36 Mbps OFDM	15.5	18.0	19	
	48 Mbps OFDM	14	16.5	17.5	
	54 Mbps OFDM	13	15.5	16.5	
	MCS0 OFDM	16.5	19.0	20	
	MCS7 OFDM	13	15.5	16.5	
Transmit center frequency accuracy		-20		+20	ppm

Table 11: WLAN Transmitter Characteristics - fcCSP

Parameter	Condition	Min	Typ	Max	Units
Maximum Output Power measured form IEEE spectral mask and EVM	1 Mbps DSSS		9.5		dBm
	2 Mbps DSSS		9.5		
	5.5 Mbps CCK		9.5		
	11 Mbps CCK		9.5		
	6 Mbps OFDM		8.0		
	9 Mbps OFDM		8.0		
	12 Mbps OFDM		8.0		
	18 Mbps OFDM		8.0		
	24 Mbps OFDM		5.5		
	36 Mbps OFDM		5.5		
	48 Mbps OFDM		2.0		
	54 Mbps OFDM		2.0		
	MCS0 OFDM		8.0		
	MCS7 OFDM		2.0		
Transmit center frequency accuracy		-20		+20	ppm

Note 1 Higher power available in normal Tx power mode: 19 dBm @ 11b.

5.5 Current Consumption

TA = +25 °C, VBAT = 3.3 V, w/ CPU clock 80 MHz.

Table 12: Current Consumption in Active State - QFN

Parameter	Condition			Min	Typ	Max	Units
ACTIVE	TX	1 Mbps DSSS	@ 20.0 dBm	260	280	320	mA
		6 Mbps OFDM	@ 19.0 dBm	240	260	300	
		54 Mbps OFDM	@ 15.5 dBm	180	200	240	
		MCS7	@ 15.5 dBm	180	200	240	
	RX	No signal (Note 2)		25	29	51	
		1 Mbps DSSS (Note 2)		26.5	30.5	53	
		1 Mbps DSSS		27	37.5	54	
		54 Mbps OFDM		29	38.5	54	
		MCS7		29	38.5	54	

Note 2 Low Current Mode & CPU clock 30 MHz.

TA = +25 °C, VBAT = 3.3 V with CPU clock 80 MHz

Table 13: Current Consumption in Active State - fcCSP

Parameter	Condition			Min	Typ	Max	Units
ACTIVE	TX	1 Mbps DSSS	@ 9.5 dBm		85		mA
		6 Mbps OFDM	@ 8.0 dBm		85		
		54 Mbps OFDM	@ 2.0 dBm		70		
		MCS7	@ 2.0 dBm		70		
	RX	No signal (Note 2)			28.5		
		1 Mbps DSSS (Note 2)			30.0		
		1 Mbps DSSS			37.5		
		54 Mbps OFDM			39		
		MCS7			39		

Note 1 Low Current Mode & CPU clock 30 MHz.

TA = +25 °C, VBAT = 3.3 V

Table 14: Current Consumption in Low Power Operation

Parameter	Condition	Min	Typ	Max	Units
Low Power Operation	Sleep 1		0.2		µA
	Sleep 2		1.8		
	Sleep 3		3.5		

5.6 ESD Ratings

Table 15: QFN Package

Reliability Test	Standards	Test Conditions	Result
Human Body Model (HBM)	JEDEC EIA/JESD22-A114	± 2,000 V	Pass
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101	± 500 V	Pass

Table 16: fcCSP Package

Reliability Test	Standards	Test Conditions	Result
Human Body Model (HBM)	JEDEC EIA/JESD22-A114	± 2,000 V	Pass
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101	± 500 V	Pass

5.7 Brown-Out and Black-Out

The device enters a brown-out condition whenever the input voltage dips below V_{BROWN} (see Table 17). This condition must be considered during design of the power supply routing, especially if the SoC is operated from a battery. High-current operations, like TX operation, cause a dip in the supply voltage, potentially triggering a brown-out. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (for example, four contacts for two AA batteries), wiring resistance, and PCB routing resistance.

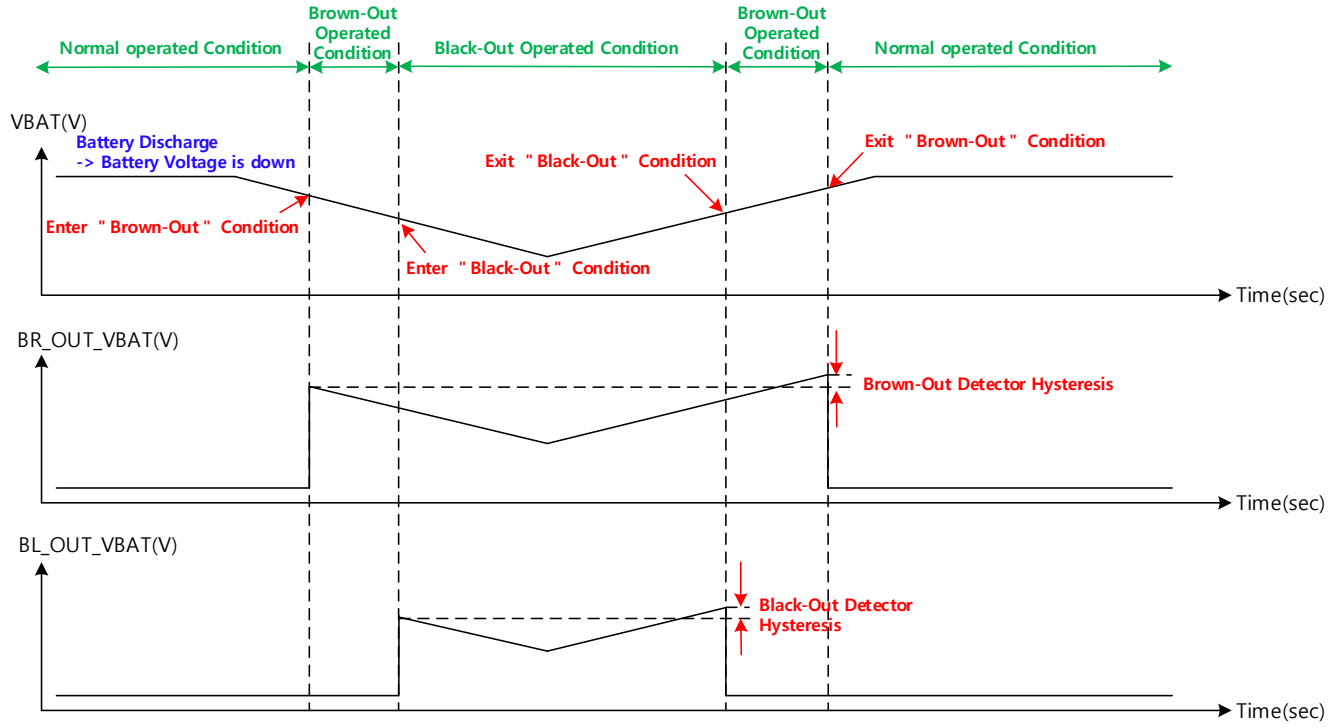


Figure 6: Brown-Out and Black-Out Levels

Brown-out and black-out conditions only operate in normal mode. The black-out condition is equivalent to a hardware reset event in which all states within the device are lost. Table 17 lists the brown-out and black-out voltage levels.

Table 17: Brown-Out and Black-Out Voltage Levels

Condition	Voltage	Hysteresis	Operation
Vbrown-out	2.10 V (Note 1)	90 mV	S/W Control
Vblack-out	1.75 V (Note 1)	90 mV	Full boot

Note 1 Recommended voltage level. Adjustable depending on the application condition.

5.8 Clock Electrical Characteristics

DA16200 needs two clock sources. One is the 32.768 kHz clock used by the RTC block, and the other is the 40 MHz clock for the internal processor and Wi-Fi system. More specifically, the 40 MHz clock is used as a source clock for the internal PLL while the PLL output is used for the internal processor and Wi-Fi system block.

5.8.1 RTC Clock Source

The 32.768 kHz RTC clock source is necessary for the free-running counter in the RTC block. The RTC block of the SoC contains an internal 32.768 kHz RC oscillator as well, which is used as a clock for chip initialization before the external 32.768 kHz crystal reaches the stable time in the initial stage. It is necessary to convert it into an external clock for accurate clock counting after the initialization stage. This process is executed through the register setting. Table 18 shows the suitable loading capacitor value and required tolerance. Figure 7and Figure 8 show connections for the RTC crystal clock.

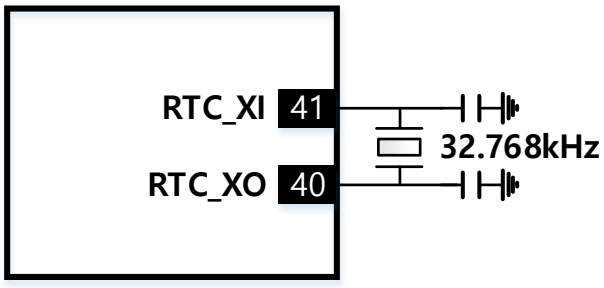


Figure 7: DA16200 6×6 QFN RTC Crystal Connections

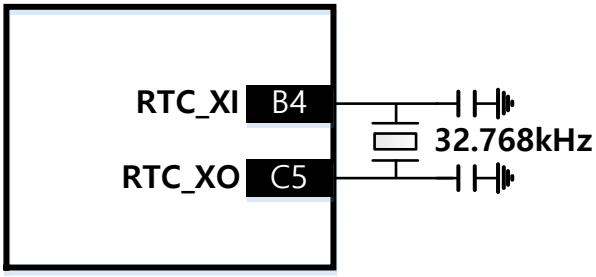


Figure 8: DA16200 3.8 × 3.8 fcCSP RTC Crystal Connections

Table 18 lists the RTC crystal requirements.

Table 18: RTC Crystal Requirements

Parameter	Condition	Min	Typ	Max	Units
Frequency			32.768		kHz
Frequency accuracy	Initial + temp + aging	-250		+250	ppm
Crystal ESR	32.768 kHz,C1 = C2 = 9 pF			90	Ω

5.8.2 Main Clock Source

DA16200 contains a crystal oscillator for the main clock source which supports the external crystal clock. Basically, the external clock is 40 MHz. Table 19 shows the load capacitor value and required clock tolerance for 40 MHz. Figure 9 and Figure 10 show the crystal clock connections.

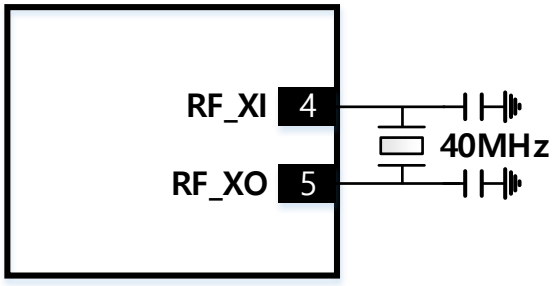


Figure 9: DA16200 6×6 QFN Crystal Clock Connections

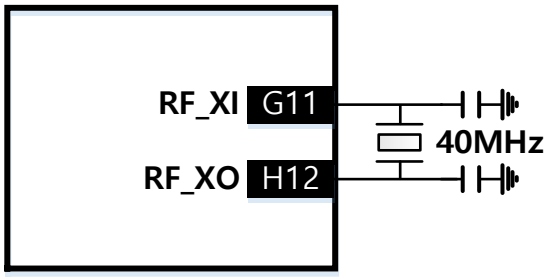


Figure 10: DA16200 3.8 × 3.8fcCSP Crystal Clock Connections

Table 19 lists the WLAN crystal requirements.

Table 19: WLAN Crystal Clock Requirements

Parameter	Condition	Min	Typ	Max	Units
Frequency			40		MHz
Frequency accuracy	Initial + temp + aging	-20		+20	ppm
Crystal ESR	40 MHz, C1 = C2 = 6 pF			60	Ω

6 Power Management

DA16200 has an RTC block which provides power management and function control for low power operation. In normal operation, the RTC block is always powered on when RTC_PWR_KEY is enabled. RTC block also has a control function for DA16200's internal power supplying components, like LDOs, DC-DCs, and power switches.

6.1 Power On Sequence

The sequence after the initial switching from power-off to power-on is shown in Figure 11. The RTC_PWR_KEY of DA16200 is a pin that enables the RTC block. Once RTC_PWR_KEY is enabled after VBAT power is supplied, all the internal regulators are turned on automatically in the sequence pre-defined by the RTC block.

Once RTC_PWR_KEY is turned on, LDOs for both XTAL and digital I/O are turned on shortly and then the DC-DC regulator is turned on according to the pre-defined interval. The enabling intervals are also modifiable by register setting after initial power-up.

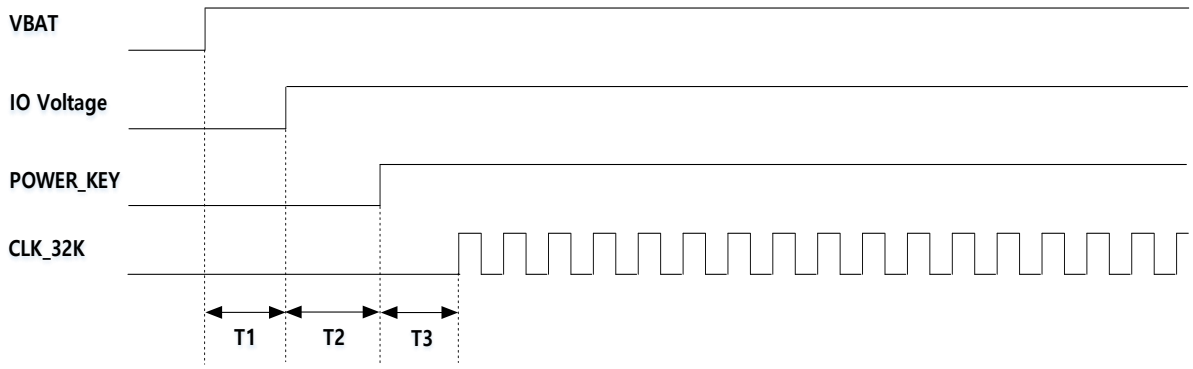


Figure 11: Power on Sequence

Table 20: Power on Sequence Timing Requirements

Name	Description	Min	Typ	Max	Unit
T1	IO voltage and VCC supply		0		µs
T2	RTC_PWR_KEY turn-on time after VBAT supply		100		µs
T3	Internal RC oscillator wake-up time		217		µs

6.2 Power Management Unit

DA16200 has one internal DC-DC converter and several LDOs for supplying power to all internal sub-blocks. Power management does the on-off control of these regulators and it is implemented through the register setting inside the RTC block.

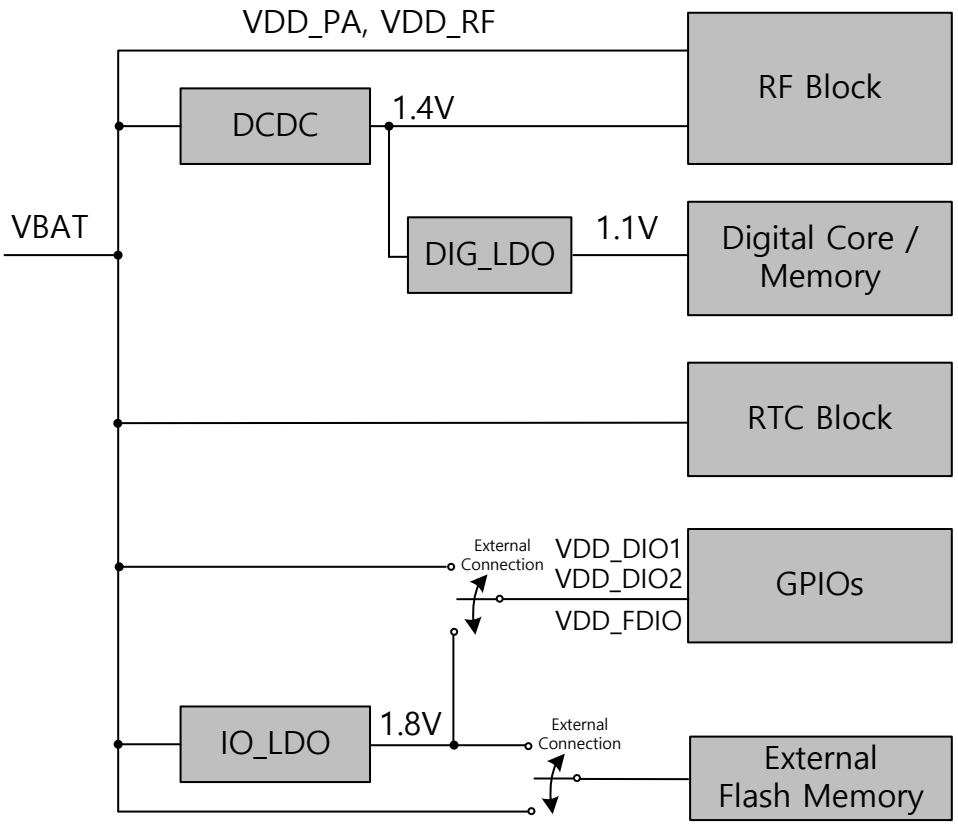


Figure 12: Power Management Block Diagram

Details of the internal DC-DC converters and LDOs are explained below:

- DC-DC converter: from the power supply of external VBAT input, it generates 1.4 V power for the digital LDO and RF block
- LDO for digital Blocks: from the DC-DC output, it generates 1.1 V power which is used for digital blocks
- LDO for I/O and external flash memory:
  - This LDO output is used only for 1.8 V digital I/O applications
  - From external VBAT power input, it generates 1.8 V output voltage which is used for digital I/O power domain in 1.8 V digital I/O applications
  - It is also used for external flash memory
  - For 3.3 V digital I/O applications, external power (3.3 V) is directly supplied for digital I/O power

With the internal DC-DC converters and LDOs, all the power necessary for DA16200's internal sub-blocks are sufficiently generated.

6.3 Low Power Operation Mode

DA16200 provides three sleep modes as low power operation modes.

6.3.1 Sleep Mode 1

Sleep mode 1 is an operation mode in which RTC_PWR_KEY is not enabled yet. In other words, RTC_PWR_KEY is in the disabled (zero) state and DA16200 is only supplied with external VBAT. With all the internal blocks off, only the leakage current from minimal number of internal blocks connected to VBAT remains.

6.3.2 Sleep Mode 2

Sleep mode 2 is an operation mode in which RTC_PWR_KEY is enabled and only the RTC block is running. Only the 32-kHz clock is active. Sleep mode 2 can be activated by a command from the CPU. In other words, by setting the registers of the RTC block, power management unit can be controlled and DA16200 can enter sleep mode 2.

Since only the RTC block operates in sleep mode 2, minimal power consumption can be realized in this mode.

To turn sleep mode 2 back to the idle state, the count value that has been set by the CPU prior to entering the sleep mode should be reached or an external wake-up event should occur via the RTC_WAKE_UP pin.

6.3.3 Sleep Mode 3

Compared to sleep mode 2, sleep mode 3 is an operation mode where the Wi-Fi connection is continuously alive. DA16200 can enter either of the sleep modes, sleep mode 2 or sleep mode 3, by application’s selection which is activated by a CPU command.

7 Core System

7.1 Arm Cortex-M4F Processor

The Cortex-M4F processor is a low-power processor that features low gate count, low interrupt latency, low-cost debug, and includes floating point arithmetic functionality. The processor is intended for deeply embedded applications that require fast interrupt response features.

The features of the Cortex-M4F processor in DA16200 are summarized below:

- Operation clock frequency is up to 160 MHz
- 32-bit Arm Cortex-M4F architecture optimized for embedded applications
- Thumb-2 mixed 16/32-bit instruction set
- Hardware division and fast multiplication
- Includes Nested Vectored Interrupt Controller(NVIC)
- SysTick timer provided by Cortex-M4F processor
- Supports both standard JTAG (5-wire) and the low-pin-count Arm SWD (2-wire, TCLK/TMS) debug interfaces
- Cortex-M4F is binary compatible with Cortex-M3

For more information on the Arm Cortex-M4F, see the *Arm Cortex-M4F r0p1 technical reference manual* [1].

7.2 Wi-Fi Processor

DA16200 includes an internal MCU(Arm Cortex-M4F) to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast and secure WLAN and Internet connections with 256-bit encryption. It supports the station, SoftAP, and Wi-Fi Direct modes. It also supports WPA/WPA2 personal and enterprise security, WPA2 SI, WPA3 SAE, OWE, and WPS 2.0. It includes an embedded IPv4 and IPv6 TCP/IP stack.

7.3 Memory

7.3.1 Internal Memory

DA16200 contains four types of internal memories and also supports an external serial flash memory interface. The roles and functions of each memory are described in the following sub-sections.

7.3.1.1 ROM

This memory contains boot loader, system kernel, network stack, and various kinds of drivers for interfaces and peripherals.

7.3.1.2 SRAM

This memory is used as data space for all codes running on the internal CPU. All codes run on serial flash memory via I-Cache (XIP mode). All the contents in this memory disappear in the low-power sleep mode.

7.3.1.3 OTP

DA16200 includes one-time electrically field programmable non-volatile CMOS memory. The array can be programmed by 1 bit and read by 32 bits. Since the OTP controller is designed internally, it is possible to execute read/write by commands through register setting.

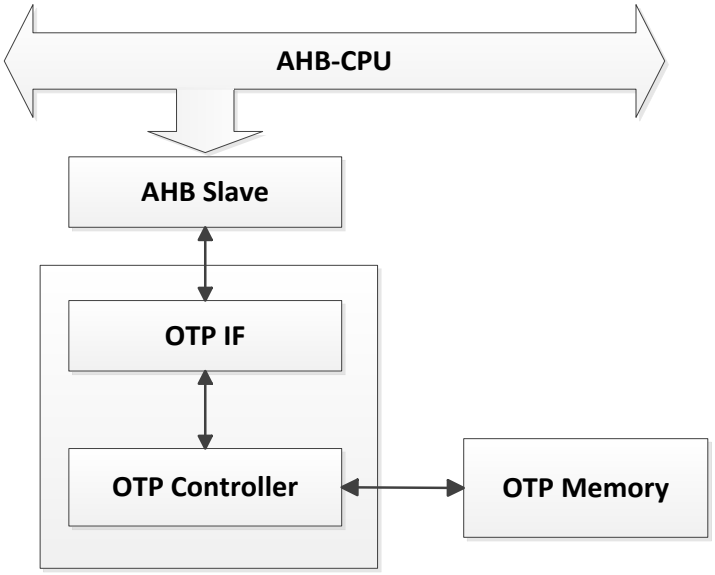


Figure 13:OTP Block Diagram

This memory is to protect and manage major information essential for mass production and management of products, such as booting information, MAC address, serial number, and others.

The OTP is also used for storing secret information which is used for the advanced security functions like secure booting, secure debugging, and secure asset storage. But this secret information cannot be accessed in a normal way of CPU read or write access so that it is protected from the external access.

The OTP controller translates a request into the corresponding control sequence for the OTP cell to be in one of the following modes:

- **Standby mode**: it is used to reduce the power consumption when the OTP is not used
- The OTP cell is powered but is less than the power consumption in active mode
- **Operation mode**: for the OTP to operate correctly, OTP must be operation mode
- Programming, reading, and test mode can be operated after operation mode is set
- **Program mode**: when OTP is instantiated, the SoC has all bits in "0"s and "1"s are loaded into the SoC through programming
- The program mode provides the functionality for programming a 1-bit into an OTP position
- Immediately after programming the bit at the selected memory cell(program operation), a verification operation follows to check for successful programming results with sufficient margin
- **Read mode**: in this mode, the contents of the OTP cell are read at reactive AHB address space
- **Test mode**: tests can be performed during wafer sort, final test, or in-system/in-field, depending on the test plan used by end users

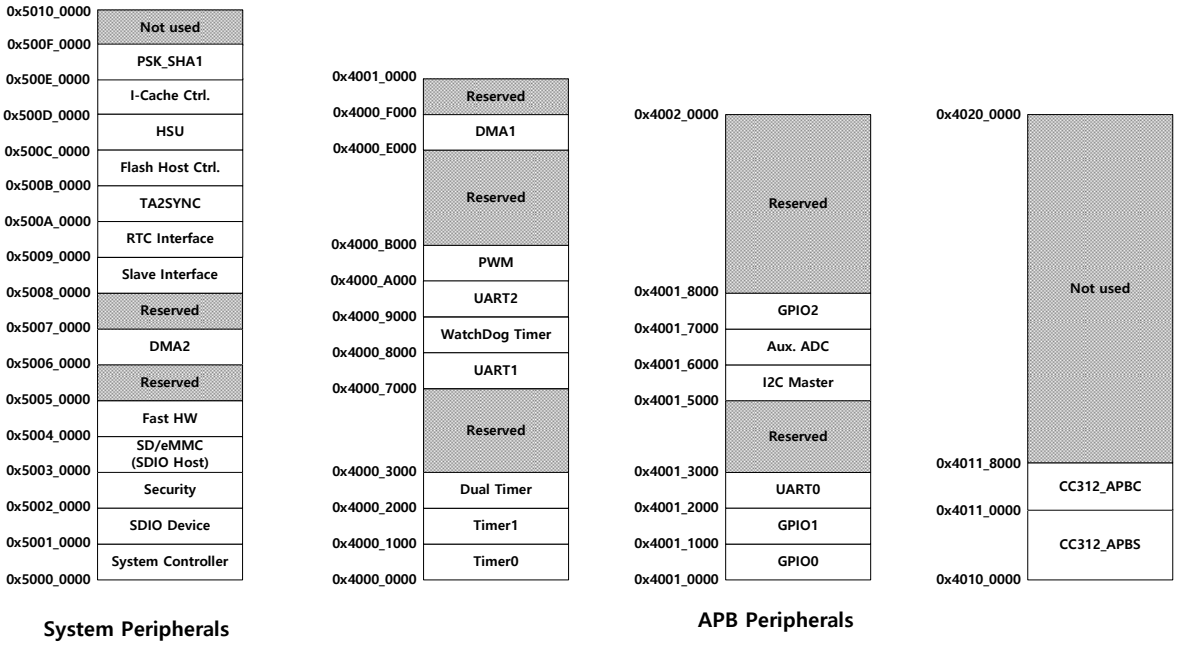
Table 21: OTP Map

Offset	Field	Size (Bytes)
0x000	Dialog Reserved	1024
0x100	MAC Address #0 Low	4
0x101	MAC Address #0 High	4
0x102	MAC Address #1 Low	4
0x103	MAC Address #1 High	4
0x104	MAC Address #2 Low	4
0x105	MAC Address #2 High	4

Offset	Field	Size (Bytes)
0x106	MAC Address #3 Low	4
0x107	MAC Address #3 High	4
0x10A	XTAL Offset #0	4
0x10B	XTAL Offset #1	4
0x10C to 0x7FF	User Area	7128

7.3.1.4 Serial Flash Interface

DA16200 supports an external serial memory interface, QSPI, explained in section 9.1. This memory is used for storing DA16200's software code, including user application code, its pre-defined data, and various configuration data in the form of NVRAM(Non-Volatile RAM).



7.4 RTC

Among the pins in DA16200, four special pins are directly connected to the RTC block, which are RTC_PWR_KEY, RTC_GPO, RTC_WAKE_UP, and RTC_WAKE_UP2.

Table 22: RTC Pin Description

Pin Name	Pin Number		Description
	QFN	fcCSP	
RTC_PWR_KEY	42	A5	RTC_PWR_KEY represents a power key for the RTC block. When this pin is enabled, the RTC starts to work by following a pre-defined power-up sequence and eventually all the necessary power is supplied to all the sub-blocks including the main digital block in DA16200. When disabled, all blocks are powered off and this mode is defined as sleep mode 1. DA16200 consumes minimum leakage current in sleep mode 1. This pin also operates as a RESET pin of the whole chip.
RTC_GPO	44	E7	This pin is an output pin. It has three different functions. ● GPO function: its output value can be set as ′1′ or ′0′ via register setting. It can keep the value even in sleep mode. ● Flash control function: when in sleep mode, it becomes ′0′; when in active mode, it is ′1′.
RTC_WAKE_UP	43	D6	This pin is an input pin for receiving an external event signal from an external device like a sensor. The RTC block detects an external event signal via this pin and wakes up DA16200 from sleep mode 2 or sleep mode 3.
RTC_WAKE_UP2	23	H6	

DA16200contains not only an on-chip oscillator that uses 32.768 kHz external crystal but also an internal 32.768 kHz RC oscillator for faster initialization, which leads to prompt clock generation after power-up and is used until the external crystal becomes stable. Afterwards, the input source can be switched to the external crystal via register setting.

RTC block has a 36-bit real time counter. Its resolution is equal to one clock period of 32.768 kHz. The count value can be read via the register read command.

7.4.1 Wake-up Controller

The wake-up controller is designed to wake up DA16200 from a sleep mode by an external signal. It detects an edge trigger of the wake-up signal and selects either the rising edge or the falling edge. Also, the wake-up signal must be maintained for at least 200 µs upon occurrence of transition on one side.

When it comes to the source of wake-up, 11 digital I/Os in addition to the two pins directly connected to the RTC block can be used. Although up to 11 digital I/Os are available for use, the maximum number of digital I/Os that are simultaneously available is eight. Table 23 describes the digital I/Os that are available for simultaneous use.

Table 23: Wake-up Sources

QFN & fcCSP Package	
Input Selection = 0	**Input Selection = 1**
GPIOA4	X
GPIOA5	X
GPIOA6	X
GPIOA7	X
GPIOA8	X
GPIOA9	GPIOC6
GPIOA10	GPIOC7
GPIOA11	GPIOC8

For more on wake-up source selection, refer to input selection register: 0x50091008[25:16].

The wake-up controller is located in the RTC block. Several parameters can be set by RTC registers and they identify which pin is used to wake up the SoC by checking the status register after wake-up.

DA16200 has another wake-up function using analog sources, which is described in section 9.8.4. Using the Aux-ADC, DA16200 detects whether it exceeds the pre-defined threshold value. If it detects the wanted condition, it will wake up from a sleep mode. Four ports (GPIOA[3:0]) are used for this function.

7.4.2 Retention I/O Function

DA16200 I/O has an retention mode. During this mode, I/O cells retain the previous state values at the core side inputs. When it is required to maintain the value of a specific GPIO in sleep mode, this function will be used. For example, in order to maintain HIGH value on GPIOA4 in sleep mode, it is required to set the value of GPIOA4 to HIGH and set the register bit of RTC block (0x5009_1018:BIT[27:24]) to enable retention to the proper value described in Table 24 before going to the sleep mode. For GPIOA4, BIT[25] should be set to HIGH, then GPIOA4 can keep the value HIGH during the sleep mode.

The retention enable register is comprised of three bits in total, and the I/O power domains covered by each of the bits are described in Table 24.

Table 24: I/O Power Domain

[25] DIO1	[26] DIO2	[27] FDIO
GPIOA[11:4]	GPIOC[8:6]	F_CLK
	TCLK/TMS	F_CSN
	UART0_RXD/UART0_TXD	F_IO0 to F_IO3

7.5 Pulse Counter

7.5.1 Introduction

The pulse counter is a module which counts the number of rising or falling edges of input signals. And this counter module can run even in sleep mode. It includes one 32-bit up-counter. The input channel can be chosen by register setting among the 11 digital I/Os. It also has a glitch filter which is designed to remove the unwanted trigger of an input signal.

7.5.2 Functional Description

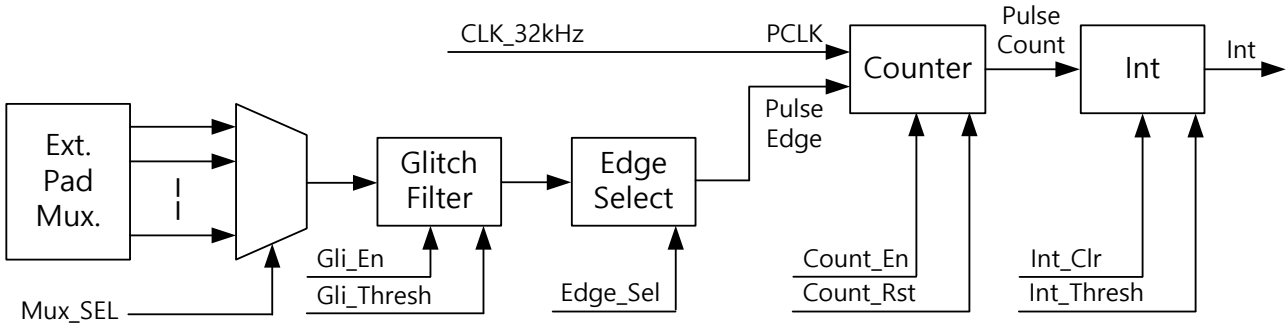


Figure 14: Pulse Counter Block Diagram

7.5.2.1 Input

Available input channels are described in Table 23. It uses the same input sources with the wake-up controller. By register setting, input channels can be selected among 11 digital I/Os.

7.5.2.2 Clock

The operation clock of the pulse counter is 32 kHz.

7.5.2.3 Counter

As described in Figure 14, the pulse counter is activated by several counter control signals. By register setting, input signals can be selected on either the rising edges or falling edges. In order to enable the glitch filter module, Gli_En and Gli_Thresh register values need to be set. The pulses whose cycles are shorter than the Gli_Thresh value are removed. The counter is a 32-bit up-counter and the counter value can be reset to zero by Count_Rst.

7.5.2.4 Interrupts

An interrupt occurs when the counter values reaches the Interrupt Threshold value(Int_Thresh). In sleep mode, this interrupt can be used as a wake-up source.

7.6 HW Accelerators

7.6.1 Zeroing of SRAM

DA16200 provides a function to quickly set a constant value for the set SRAM area. This function is mainly used to initialize the set SRAM area to zero, and it can be used even when SRAM is used.

For example, assuming that the entire 512 KB SRAM is being initialized, the processing time is 8192 cycles based on the CPU clock, that is, the maximum processing time is 8192 cycles irrespective of the SRAM size to be initialized.

For more information to use this function, refer to [2].

7.6.2 CRC Calculation

The CRC algorithm detects the corruption of data during transmission and detects a higher percentage of errors than a simple checksum. The CRC calculation consists of an iterative algorithm involving XOR and shifts operations that is executed much faster in hardware than in software. The CRC calculator is mainly used to check the flash image and the features of CRC calculator in DA16200 are summarized below:

- Operation clock frequency is up to 160 MHz, the same as CPU clock
- Supports 8-bit, 16-bit, and 32-bit data paths
- Performs CRC operation simultaneously in real time during data transfer on the selected AHB bus
- Operation type of CRC calculation
  - CRC-32: generator polynomial is G(x) = x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 +x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1
  - CRC-16 CCITT: generator polynomial is G(x) = x^16 + x^12 + x^5 +1
  - CRC-16 IBM: generator polynomial is G(x) = x^16 + x^15 + x^2 +1

For more information to use this function, refer to the DA16200_Example_Application_Guide [2].

7.6.3 Pseudo Random Number Generator (PRNG)

DA16200 provides a function, PRNG, to generate a pseudo random number. The features of PRNG in DA16200 are summarized as follows:

- Operation clock frequency is up to 160 MHz, the same as CPU clock
- Supports partial parallel processing of 8-bit, 16-bit, and 32-bit unit
- Generator polynomial is G(x) = x^31 + x^28 + 1 (reference standard: [3])

7.7 DMA Operation

7.7.1 DMA1

DA16200 includes a DMA controller of its own, with single AHB master. The DMA1 has sixteen channels for fast data transfers from/to I2S, I2C, UARTs, and ADC to/from any on-chip RAM. The DMA requests of each module are directly connected to the dedicated DMA channels. Each DMA channel has a priority level, a smaller channel number standing for a higher priority.

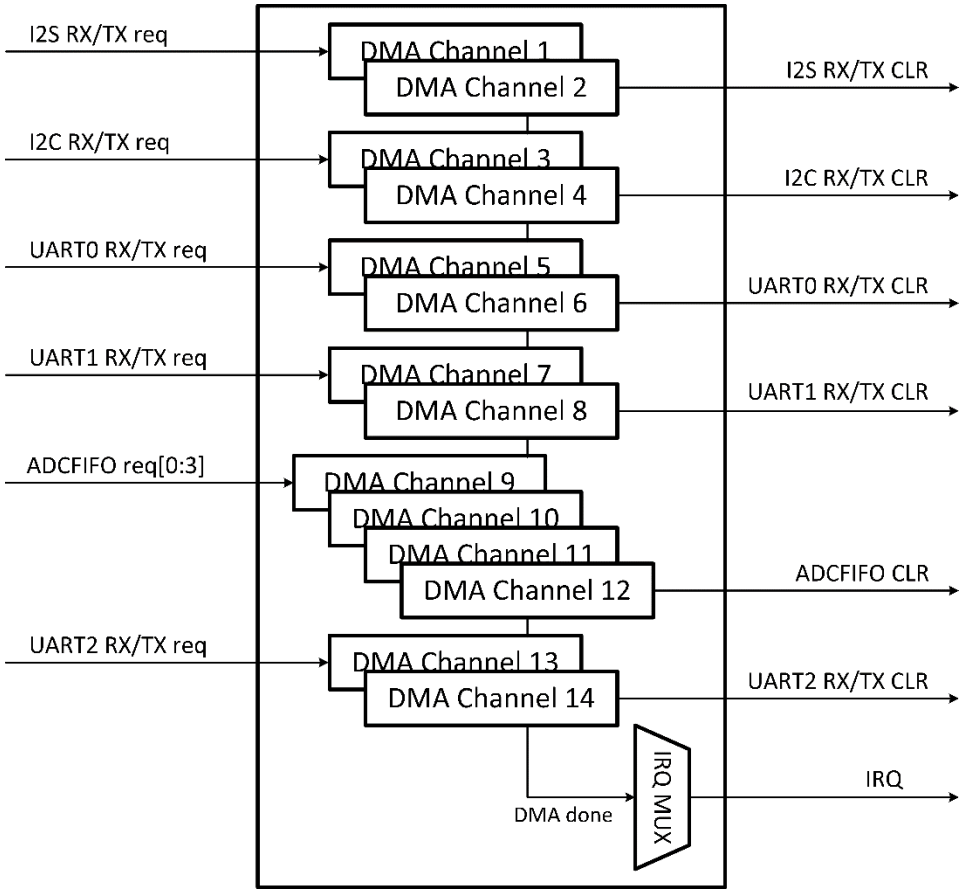


Figure 15: DMA1 Controller Block Diagram

Table 25: DMA1 Served Peripherals

DMA Channel	Module Name	Direction	Transfer Size
Channel 0	Mem-to-mem	T/RX	Word
Channel 1	I2S	RX	Word
Channel 2	I2S	TX	Word
Channel 3	I2C	RX	Byte
Channel 4	I2C	TX	Byte
Channel 5	UART0	RX	Byte
Channel 6	UART0	TX	Byte
Channel 7	UART1	RX	Byte
Channel 8	UART1	TX	Byte
Channel 9	ADCFIFO[0]	READ	Halfword
Channel 10	ADCFIFO[1]	READ	Halfword
Channel 11	ADCFIFO[2]	READ	Halfword
Channel 12	ADCFIFO[3]	READ	Halfword
Channel 13	UART2	RX	Byte
Channel 14	UART2	TX	Byte
Channel 15	Mem-to-mem	T/RX	Word

DA16200's DMA1 controller supports Linked-List Item (LLI) function which can sequentially operate multiple DMA tasks. It is possible to reduce the SW burden and process delay with this function.

Figure 16 shows the DMA1 state machine.

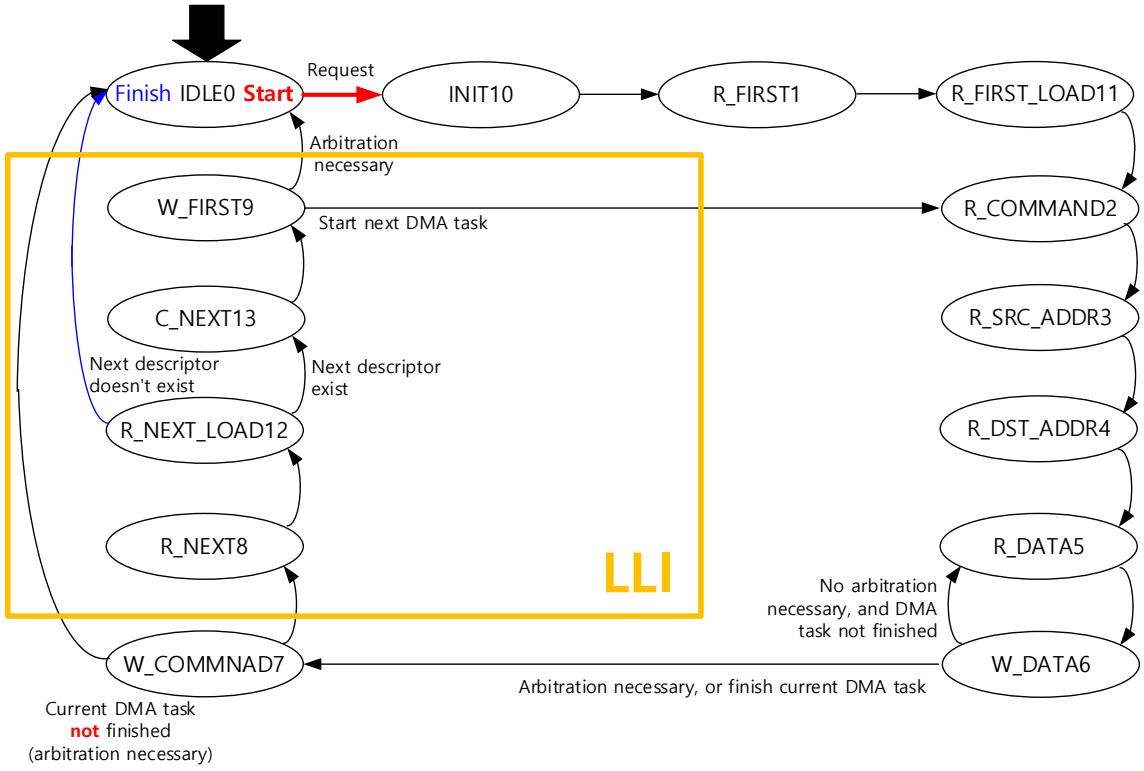


Figure 16: DMA1 State Machine

- **IDLE**: this is the state to wait for the DMA request. When the DMA request appears, the state moves to R_FIRST
- **R_FIRST**: this is the state to read the address of the first DMA descriptor (head node of the linked list)
- **R_COMMAND**: this is the state to read the Command Field of the DMA descriptor
- **R_SRC_ADDR**: this is the state to read the Src_start_addr Field of the DMA descriptor
- **R_DST_ADDR**: this is the state to read the Dst_start_addr Field of the DMA descriptor
- **R_DATA**: this is the state to read the data from the source address
- **W_DATA**: this is the state to write the data read in the R_DATA state to the destination address. By the information written in the DMA descriptor, if data read/write has been required, the state moves to R_DATA. If the DMA task is required to be suspended or stopped, the state moves to W_COMMAND
- **R_NEXT**: this is the state to read the next_descriptor field to check whether the next DMA task exists or not, before stopping the current DMA task
- **W_FIRST**: this is the state to write the address of the next DMA descriptor read in R_NEXT to the memory region where the first address of the DMA descriptor is stored. If arbitration is required, the state moves to IDLE state. If the current DMA channel is required to be operated, the state moves to R_FIRST state
- **INIT**, **R_FIRST_LOAD**, **R_NEXT_LOAD**, and **C_NEXT**: these are the states for reducing the critical path delay in the DMA block. These states generate one clock delay

7.7.2 DMA2 (Fast DMA)

DMA2 (Fast DMA) controller consists of a master read port, a master write port, and a slave port for configuration register setting. Fast DMA performs bulk data transfers, data reading from the source address range, and data writing to the destination address range. Fast DMA is mainly used for fast data transfer from memory to memory.

The features of Fast DMA in DA16200 are summarized as follows.

- Transfer size is programmable from 1 to 1 Megabytes
- Up to four channels can be set at the same time
- LLI function of ring type is supported by using configuration registers of four channels
- Interrupt enable can be set for each channel
- Provides a hold function to pause data transfer for each channel

The basic unit of bus transmission is 32-bit, and it has a function to automatically correct address align, even if the source and destination addresses are not in word units.

For example, assuming that the transfer size is 23 bytes, the source base address is 0x001 for read access, and the destination base address is 0x102 for write access, the number of bytes per transaction is performed as follows:

- Source base address [1:0] = 0x1: the master read port of fast DMA performs read access with the following sequences:
- 1 -> 2 -> 4 -> 4 -> 4 -> 4 -> 4 bytes
- Destination base address [1:0] = 0x2: the master write port of fast DMA performs write access with the following sequences:
- 2 -> 4 -> 4 -> 4 -> 4 -> 4 -> 1 bytes

Figure 17 shows the DMA2 block diagram.

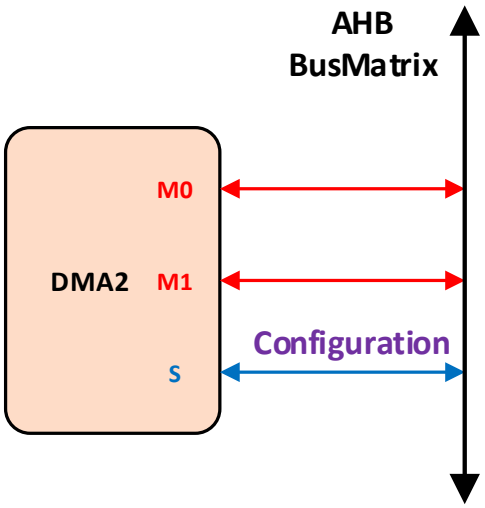


Figure 17: DMA2 Block Diagram

7.8 Bus Protection of Serial Slave Interfaces

DA16200 supports a variety of serial slave interfaces, including SPI, I2C, and SDIO slaves.

When DA16200 interfaces with an external host, it is necessary to provide the access to the authorized area. Therefore, DA16200 provides bus protection for serial slave interfaces.

The features of bus protection in DA16200 are summarized as follows:

- Up to two accessible areas can be set and the setting unit is 4-byte.
- The bus protection provides the write/read protection function outside the set area.

For more information to use this function, refer to the DA16200_Example_Application_Guide [2].

7.9 Watchdog Timer

The watchdog timer in DA16200 is based on a 32-bit down-counter that is initialized from the reload register, WDOGLOAD. The watchdog timer generates a regular interrupt, WDOGINT, depending on the programmed value. The counter decrements by one on each positive clock edge of WDOGCLK when the clock enable, WDOGCLKEN, is HIGH.

The watchdog monitors the interrupt and asserts a reset request signal, WDOGRES, when the counter reaches 0, and the counter is stopped. On the next enabled WDOGCLK clock edge, the counter is reloaded from the WDOGLOAD register and the countdown sequence continues. If the interrupt is not cleared by the time the counter reaches 0 for a second time, the watchdog timer reasserts the reset signal.

The watchdog timer applies a reset to the system in the event of a software failure, providing a way to recover from software crashes. The watchdog unit can be enabled or disabled as required.

Figure 18 shows the watchdog timer block diagram.

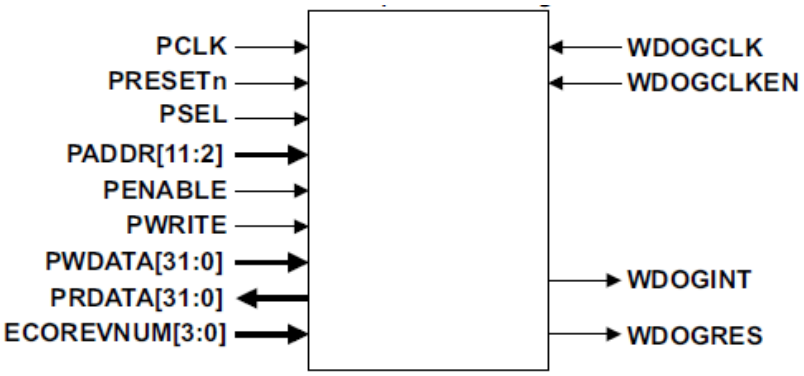


Figure 18: Watchdog Timer Block Diagram

Figure 19 shows the flow diagram for the watchdog operation.

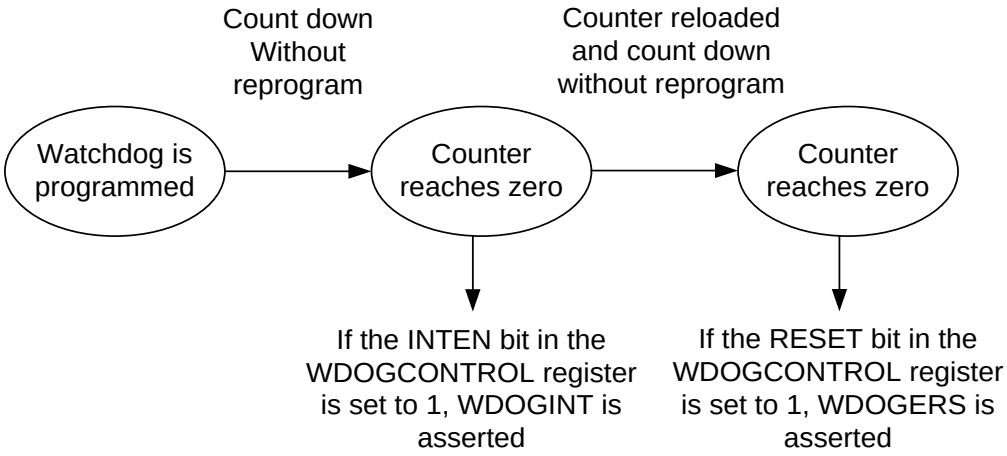


Figure 19: Watchdog Operation Flow Diagram

7.10 Clock Generator

The generation of the system's clocks is described in detail in Figure 20.

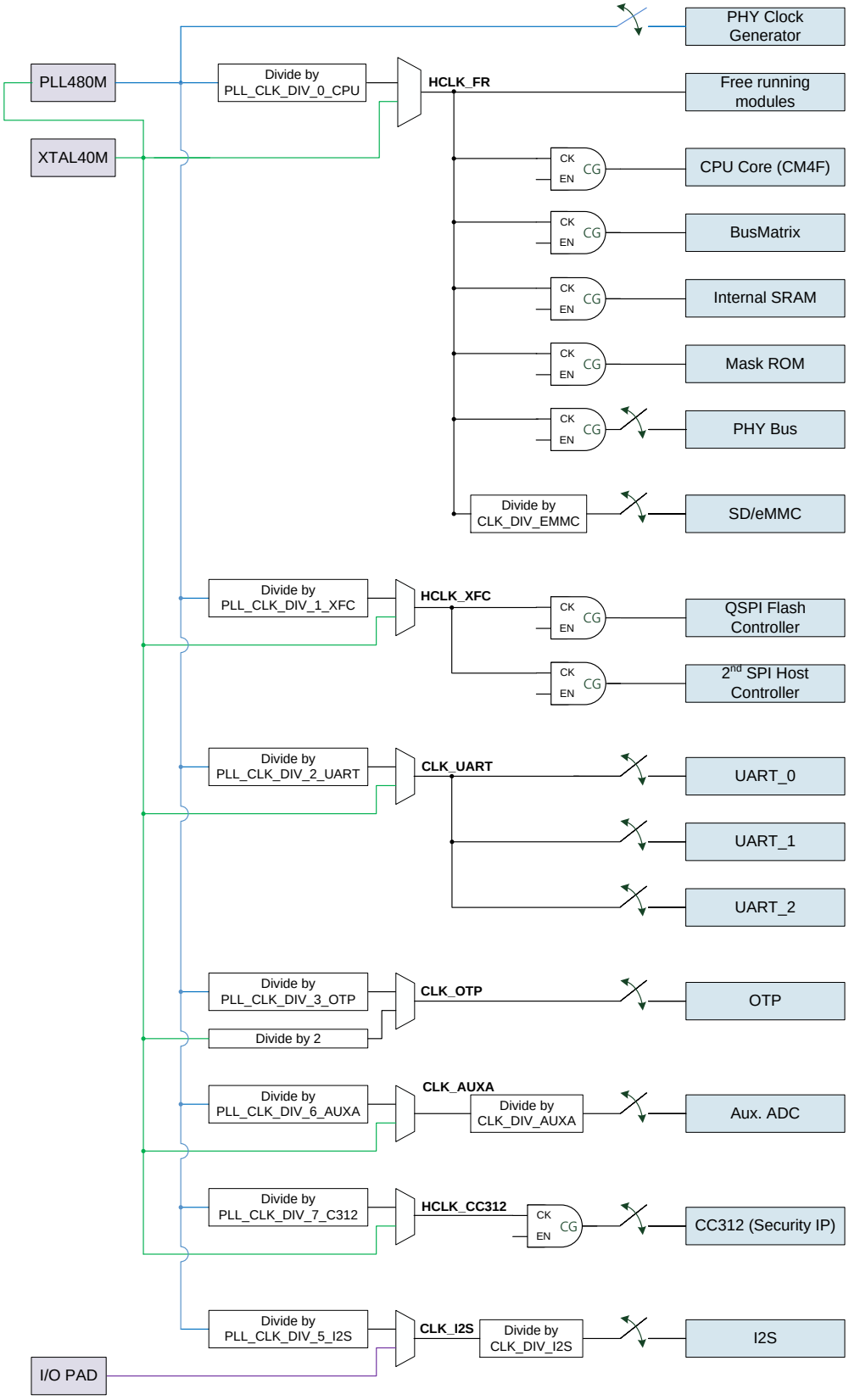


Figure 20: Clock Tree Diagram

8 Crypto Engine

HW crypto engine can be used for accelerating many crypto algorithms, such as hashing, secret key generation, and others.

Table 26 shows the supported HW acceleration crypto algorithms in DA16200. This table is cited from [4]. How to use these crypto functions is explained in [2].

Table 26: HW Acceleration Crypto Algorithms in DA16200

Algorithm	Mode	Key Sizes
AES	ECB, CBC, CTR, OFB, CMAC, CBC-MAC, AESCCM, AES-CCM*, AES-GCM	128 bits, 192 bits and 256 bits.
AES key wrapping	N/A	All
Chacha and Chacha-Poly1305	N/A	N/A
Diffie-hellman ● *ANSI X9.42-2003: Public Key Cryptography for the Financial Services Industry: Agreement of Symmetric Keys Using Discrete Logarithm Cryptography.* ● *Public-Key Cryptography Standards (PKCS) #3: Diffie Hellman Key Agreement Standard.*	N/A	1024 bits, 2048 bits and 3072 bits.
ECC key generation	N/A	NIST curves and 25519 curves.
ECIES	N/A	NIST curves and 25519 curves.
ECDSA	N/A	NIST curves and ED25519.
ECDH	N/A	NIST curves and 25519 curves.
Hash	SHA1, SHA224 and SHA256.	N/A
HKDF	N/A	N/A
HMAC	SHA1, SHA224 and SHA256.	N/A
KDF *NIST SP 800-108: Recommendation for Key Derivation Using Pseudorandom Functions*	CMAC or HMAC.	N/A
RSA PKCS#1 operations ● *Public-Key Cryptography Standards (PKCS) #1 v2.1: RSA Cryptography Specifications.* ● *Public-Key Cryptography Standards (PKCS) #1 v1.5: RSA Encryption.*	Encryption and signature schemes.	2048 bits, 3072 bits and 4096 bits.
RSA key generation	N/A	2048 bits and 3072 bits.

9 Peripherals

This section describes the peripherals that are supported by the DA16200 device.

9.1 QSPI: Master with XIP Feature

QSPI master supports 4-line SPI communication with commercial flash memory devices and uses Motorola SPI-compatible interface among SPI communication modes. The highest communication speed is the same as the AMBA bus clock, and the speed is adjustable in integer multiples. The designed QSPI supports 4-/2-/1-line types depending on the purpose. These types should be combined. Especially when the 1-line communication mode is used, it can be used as the SPI master.

QSPI master is an IP for communication between the flash memory and AMBA AHB bus and is designed to support XIP. The features of the QSPI master are summarized as follows:

Serial flash interface:

- SPI compatible serial bus interface
  - Configurable SPI I/O modes:
    - Single I/O mode
    - Dual I/O mode
    - Quad I/O mode
  - JEDEC Standard : JESD216B
  - 24-bit and 32-bit addressing
  - Supports to access flash with XIP mode
    - Read access without command
    - Read access without address and command
  - Programmable SPI clock phase and polarity
  - Maximum number of SPI CS is four that can be operated
- Compatible with serial NOR flash devices, such as Macronix, Micron, Spansion, ESMT, and ISSI

AMBA slave interface

- Compliance to the *AMBA AHB bus specification*, *Rev 3.0* [7]
- Direct code execution: directly addressable access without additional driver software
- Supports single and incrementing burst transfer (SINGLE, INCR, INCR4, INCR8, INCR16)
- Supports byte, half-word, and word transaction
- AMBA slave interface is optional to access configuration and status registers
- Simple timer is used to check the completion time of flash operation
- XIP path of QSPI master supports HW remapping function to execute selected boot image for over-the-air programming(OTA)

AMBA master interface

- Compliance to the *AMBA AHB bus specification*, *Rev 3.0* [7]
- Supports DMA operation to access serial flash devices
  - Automatic copy of code image from serial flash to system RAM
  - Automatic programming of code image from system RAM to serial flash
- Performs a mem-to-mem copy in units of 32 bits, regardless of the address and length
- Supports single and incrementing burst transfer (SINGLE, INCR, INCR4, INCR8, INCR16)
- Supports byte, half-word, and word transaction

Figure 21 shows the QSPI Master Block Diagram.

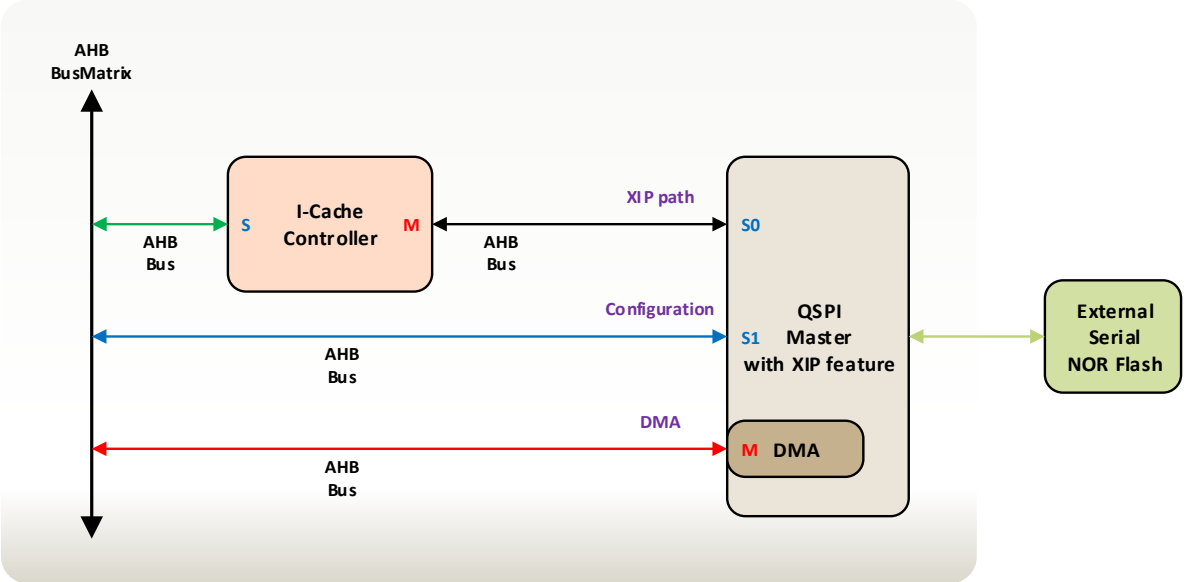


Figure 21: QSPI Master Block Diagram

Table 27 shows the pin definition of the external QSPI master interface.

Table 27: External QSPI Master Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
F_CSN	18	J5	O	QSPI_CSB1
F_CLK	19	K4	O	QSPI_CLK
F_IO0	14	K8	I/O	QSPI_SO (TXD0)
F_IO1	15	L7	I/O	QSPI_SI (TXD1)
F_IO2	16	J7	I/O	QSPI_WP (TXD2)
F_IO3	17	K6	I/O	QSPI_HOLD (TXD3)

Figure 22 shows the timing diagram for the QSPI master.

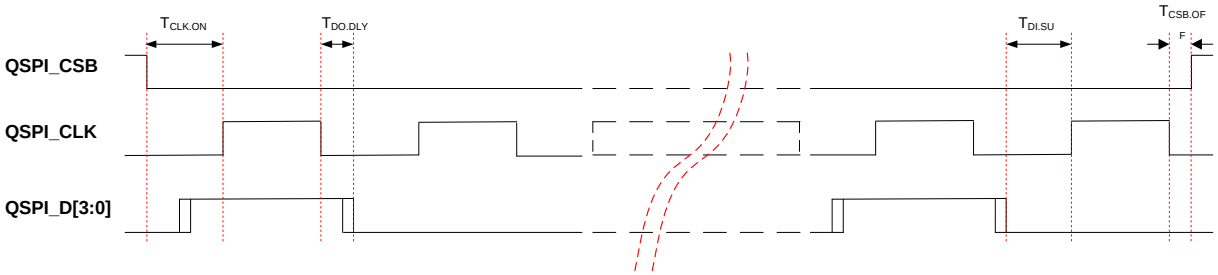


Figure 22: QSPI Master Timing Diagram (Mode 0)

Table 28 lists the timing parameters for the QSPI master.

Table 28: QSPI Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
QSPI_CLK frequency	F_{CLK}	10		120	MHz
QSPI_CLK clock duty			50		%
1st CLK active rising transition time	$T_{CLK.ON}$	0.5 ×T_{CLK}		T_{CLK} (Note 1)	ns
QSPI_CSB non-active rising transition time	$T_{CSB.OFF}$	0		TCLK	ns
QSPI_D[3:0] input setup time	$T_{DI.SU}$	6			ns
QSPI_D[3:0] output delay time	$T_{DO.DLY}$			2	ns

Note 1 $T_{CLK} = (F_{CLK} \times 10^6)^{-1}$ seconds

9.2 SPI Master

QSPI can use the SPI master, using single line interface. Table 29 shows the pin definition of the SPI master interface. SPI signal timing is the same as QSPI.

To use DA16200 as an SPI master, the CSB signal can be used with any of the GPIO pins. CSB [3:1] can be selected from GPIO special function by setting the registers in the GPIO.

Table 29: SPI Master Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOx			O	E_SPI_CSB[3:1]
GPIOA6	32	E3	O	E_SPI_CSB[0]
GPIOA7	31	E1	O	E_SPI_CLK
GPIOA8	30	G3	I/O	E_SPI_MOSI or E_SPI_D[0]
GPIOA9	29	H2	I/O	E_SPI_MISO or E_SPI_D[1]
GPIOA10	28	F2	I/O	E_SPI_D[2]
GPIOA11	27	G1	I/O	E_SPI_D[3]

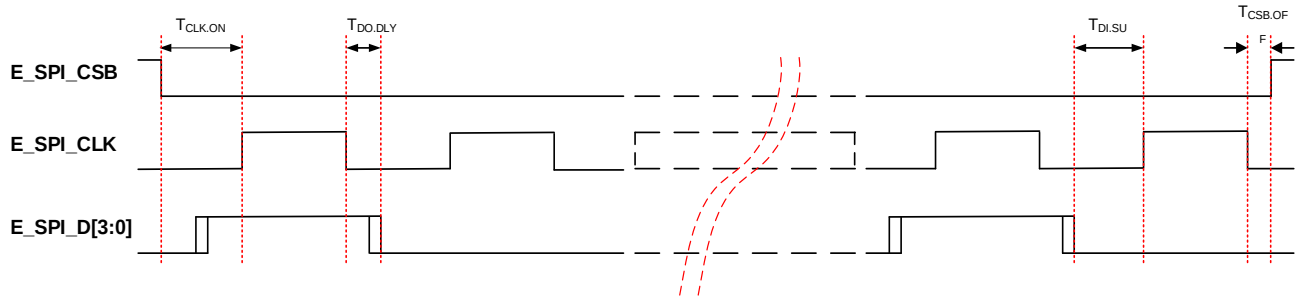


Figure 23: SPI Master Timing Diagram (Mode 0)

Table 30: SPI Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
QSPI_CLK frequency	F_{CLK}	5		60	MHz
QSPI_CLK clock duty			50		%
1st CLK active rising transition time	$T_{CLK.ON}$	0.5 × T_{CLK}		T_{CLK} (Note 1)	ns
QSPI_CSB non-active rising transition time	$T_{CSB.OFF}$	0		T_{CLK}	ns
QSPI_D[3:0] input setup time	$T_{DI.SU}$	6			ns
QSPI_D[3:0] output delay time	$T_{DO.DLY}$			2	ns

Note 1 $T_{CLK} = (F_{CLK} \times 10^6)^{-1}$ seconds

9.3 SPI Slave

SPI slave interface supports the control of DA16200 by an external host. The range of SPI clock speed is the same as that of internal bus clock speed. The SPI slave supports both the burst mode and non-burst mode. In the burst mode, SPI_CSB remains active from the start to the end of communication. In the non-burst mode, SPI_CLK remains active at every eight bits.

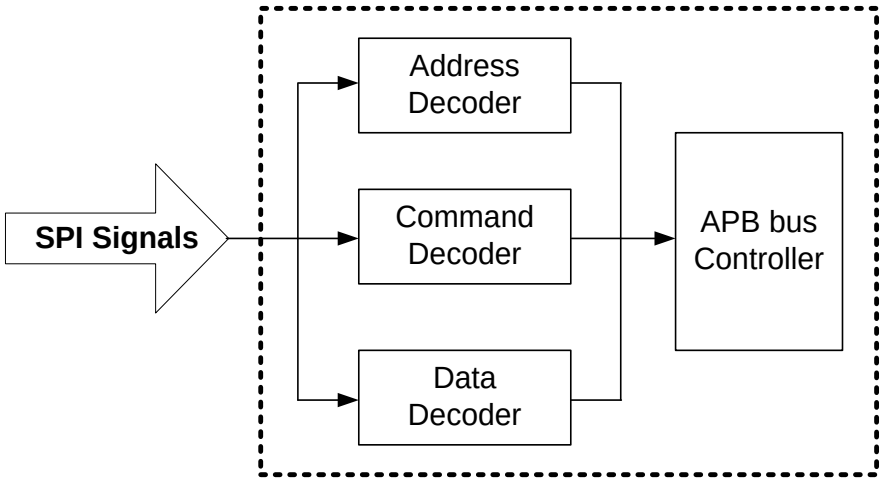


Figure 24: SPI Slave Block Diagram

Communication protocols of the SPI slave interface use either 4-byte or 8-byte control signals. Between the two available communication protocols, the CPU chooses one before initiating the control.

Figure 25 and Figure 26 shows the 8-byte and 4-byte control types.

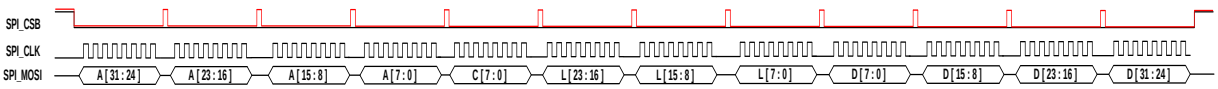


Figure 25: 8-byte Control Type

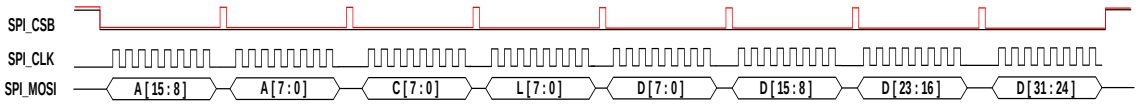


Figure 26: 4-byte Control Type

The 8-byte control type uses 4-byte address, 1-byte control, and 3-byte length. The 4-byte address displays the address of registers subject to internal access. The 1-byte control is for communication control and 3-byte length shows the length of data subject to continuous access in bytes. Hence, when the 8-byte control type is applied, the maximal length of data subject to continuous access is 16 MB.

The 4-byte control type uses 2-byte address, 1-byte control, and 1-byte length. The 2-byte address displays the address of registers subject to internal access. The 1-byte control is for communication control and 1-byte length shows the length of data subject to continuous access in bytes. Since the 32-bit address map is used internally, the 2-byte address is not enough to express everything. Thus, the upper 2-byte base address is designated, and then the lower 2-byte address is used.

Table 31 and Table 32 shows the meaning of each bit in the 1-byte control in the 8-byte control type and the 4-byte control type, respectively.

Table 31: Control Field of the 8-byte Control Type

Control Bit	Abr.	Description	
7	Auto Inc.	1 = Internal Address auto-increment	0 = Address fixed
6	Read/Write	1 = Read	0 = Write
5:0		Not used. Set all bits to '0'	

Table 32: Control Field of the 4-byte Control Type

Control Bit	Abr.	Description	
7	Auto Inc.	1 = Internal address auto-increment	0 = Address fixed
6	Read/Write	1 = Read	0 = Write
5	Common	1 = Refer base address as common area	0 = Refer base address
4	Length section	1 = Refer to register value	0 = Refer to length field
3:0	Length[12:8]	Length field upper	

Table 33 shows the pin definition of the SPI slave interface.

Table 33: SPI Slave Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA2	37	B2	I	SPI_CSB
GPIOA6	32	E3	I	
F_CSN	18	J5	I	
GPIOA3	36	D4	I	SPI_CLK
GPIOA7	31	E1	I	
F_CLK	19	K4	I	
GPIOA1	38	C3	I	SPI_MOSI
GPIOA9	29	H2	I	
GPIOA11	27	G1	I	
F_IO0	14	K8	I	
GPIOA0	39	A3	O	SPI_MISO
GPIOA8	30	G3	O	
GPIOA10	28	F2	O	
F_IO1	15	L7	O	

Figure 27 shows the timing diagram for the SPI slave.

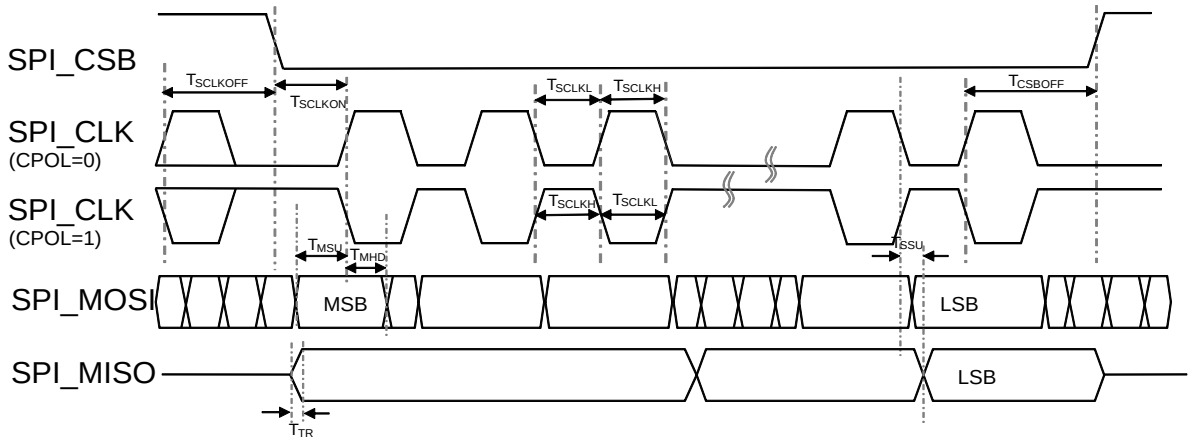


Figure 27: SPI Slave Timing Diagram

Table 34 lists the timing parameters for the SPI slave.

Table 34: SPI Slave Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	F_{SCLK}	-	-	50	MHz
SCLK clock duty		40			%
Non active duration	$T_{SCLKOFF}$	400	-	-	ns
1st CLK active rising transition time	T_{SCLKON}	T_{SCLKL}(CPOL=0) T_{SCLKH} (CPOL=1)	-	-	ns
CSB non active rising transition time	T_{CSBOFF}	T_{SCLKH} (CPOL=0) T_{SCLKL} (CPOL=1)	-	-	ns
MOSI setup time	T_{MSU}	8	-	T_{SCLK} (Note 1)	ns
MOSI hold time	T_{MHD}	8	-	T_{SCLK}	ns
MISO delay time	T_{SSU}	-	-	8	ns
MISO transition time(10% to 90% transition)	T_{TR}	-	4	5	ns

Note 1 $T_{SCLK} = 0.5 \times (F_{SCLK} \times 10^{6})^{-1}$ second

9.4 SDIO

SDIO is a full/high speed card suitable for memory card and I/O card applications with low power consumption. The full/high speed card supports SPI, 1-bit SD, and 4-bit SD transfer modes at the full clock range of 0 to 50 MHz. To be compatible with the serviceable SDIO clock, the internal BUS clock needs to be set to minimum 50 MHz. The CIS and CSA area is located inside the internal memory and the SDIO registers(CCCR and FBR) are programmed by the SD host.

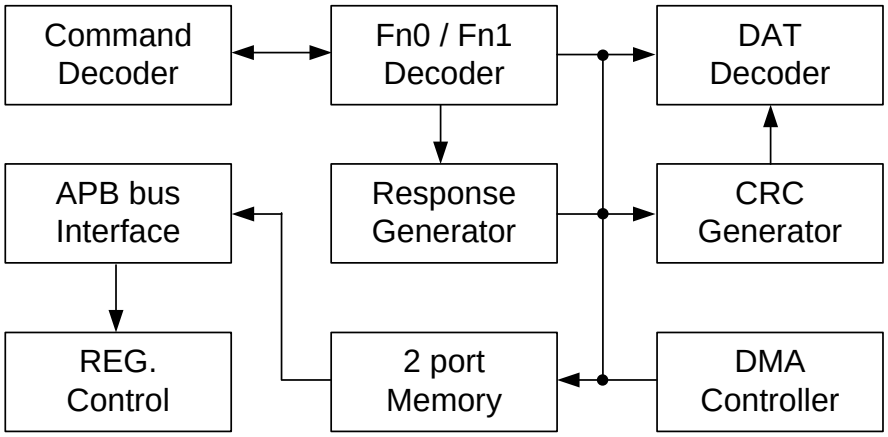


Figure 28: SDIO Slave Block Diagram

Table 35 shows the pin definition of the SDIO interface.

The GPIOA4 and GPIOA5 pins are set to SDIO CMD and CLK by default. If SDIO initialization is performed and SDIO communication is enabled, SDIO data pin setting is performed automatically. In other words, when the SDIO communication is detected, the pin used as the SDIO data among the GPIO pins is automatically activated in the SDIO use mode. However, the auto setting function is not supported for the F_xxx pin used as the flash function.

Table 35: SDIO Slave Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA4	34	F4	I/O	SDIO_CMD
F_CSN	18	J5	I/O	
GPIOA5	33	D2	I	SDIO_CLK
F_CLK	19	K4	I	
GPIOA9	29	H2	I/O	SDIO_D0
F_IO0	14	K8	I/O	
GPIOA8	30	G3	I/O	SDIO_D1
F_IO1	15	L7	I/O	
GPIOA7	31	E1	I/O	SDIO_D2
F_IO2	16	J7	I/O	
GPIOA6	32	E3	I/O	SDIO_D3
F_IO3	17	K6	I/O	

Figure 29 shows the timing diagram for the SDIO slave.

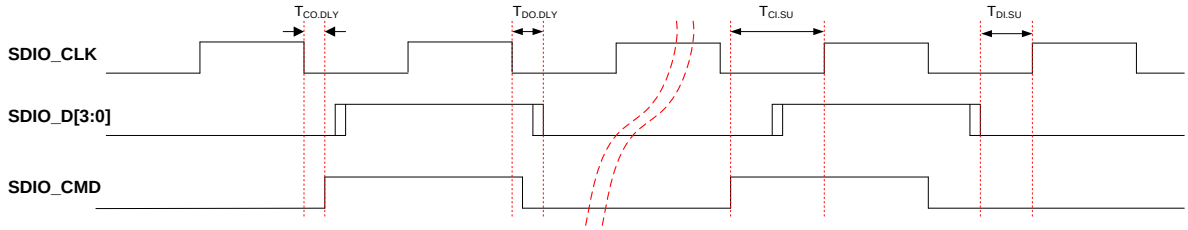


Figure 29: SDIO Slave Timing Diagram

Table 36 lists the timing parameters for the SDIO slave.

Table 36: SDIO Slave Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SDIO_CLK frequency	F_{SCLK}	-	-	50	MHz
SDIO_CLK clock duty			50		%
SDIO_CMD input setup time	$T_{CI.SU}$	3			ns
SDIO_CMD output delay time	$T_{CO.DLY}$			11 (Note 1)	ns
SDIO_D[3:0] input setup time	$T_{DI.SU}$	3			ns
SDIO_D[3:0] output delay time	$T_{DO.DLY}$			11 (Note 1)	ns

Note 1 SDIO signals can set previous output from half cycle.

9.5 I2C Interface

9.5.1 I2C Master

DA16200 includes an I2C master module. Three ranges of clock speeds are supported: standard (100 kHz), fast (400 kHz), and high (3.4 MHz) speed mode. Table 37 shows the pin definition of the I2C master interface.

Table 37: I2C Master Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA1	38	C3	O	
GPIOA5	33	D2	O	I2C_CLK
GPIOA9	29	H2	O	
GPIOA0	39	A3	I/O	
GPIOA4	34	F4	I/O	I2C_SDA
GPIOA8	32	G3	I/O	

Figure 30 shows the I2C timing diagram. The timing diagram is the same as that of I2C slave timing diagram.

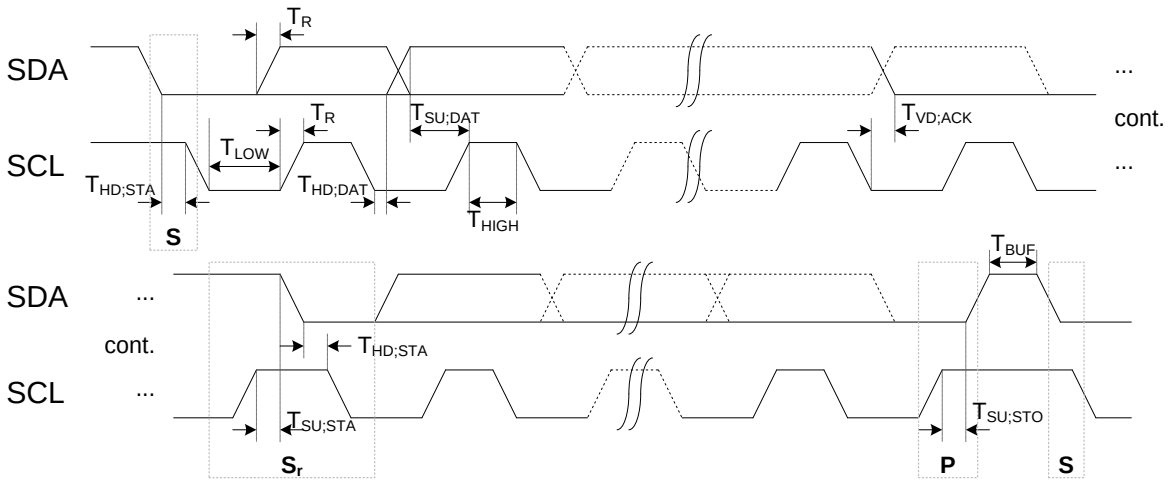


Figure 30: I2C Master Timing Diagram

Table 38 lists the I2C master timing parameters.

Table 38: I2C Master Timing Parameters

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	FSCLK	100	400	100	3400 (Note 2)	kHz
Hold time of START	THD;STA	0.2	-	0.2	-	µs
Low period of the SCL clock	TLOW	1.27	-	0.15	-	µs
High period of the SCL clock	THIGH	1.23	-	0.14	-	µs
Setup time for START condition	TSU;STA	1.1	-	0.37	-	µs
Data hold time	THD;DAT	0.07	-	0.07	-	µs

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
Data setup time	TSU;DAT	0.08	-	0.08	-	µs
Rise time of both SDA and SCL	TR (Note 3)	0.02	0.3	-	0.05	µs
Setup time for STOP condition	TSU;STO	0.36	-	0.36	-	µs
Data valid acknowledge time	TVD;ACK	0.04	-	0.04	-	µs
Buffer free time between START and STOP condition	TBUF	0.5	-	0.5	-	µs

Note 1 Clock duty ratio = (THIGH /TSCLK) × 100[%], TSCLK = 1/FSCLK

Note 2 Max. clock = 3.4 MHz (clock period = 295 ns)

Note 3 TR depends on a pull-up resistor value.

9.5.2 I2C Slave

I2C slave interface supports the control of DA16200 by an external host. Pin mux condition is defined in Table 39. Three ranges of clock speed are supported: standard(100 kHz), fast (400 kHz), and high(1.0 MHz) speed mode.

Table 39: I2C Slave Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA1	38	C3	I	I2C_CLK
GPIOA3	36	D4	I	
GPIOA5	33	D2	I	
GPIOA7	31	E1	I	
GPIOA0	39	A3	I/O	I2C_SDA
GPIOA2	37	B2	I/O	
GPIOA4	34	F4	I/O	
GPIOA6	32	E3	I/O	

Figure 31 shows the I2C slave timing diagram.

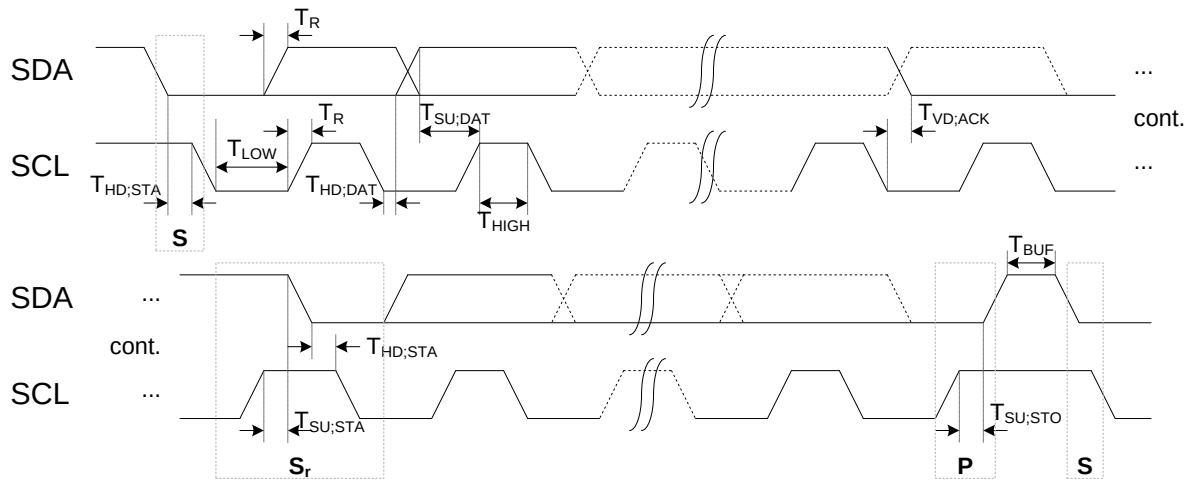


Figure 31: I2C Slave Timing Diagram

Table 40 lists the I2C slave timing parameters.

Table 40: I2C Slave Timing Parameters

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	F_{SCLK}	0	400	0	1000 (Note 2)	kHz
Hold time of START	$T_{HD;STA}$	0.6	-	0.26	-	µs
Low period of the SCL clock	T_{LOW}	1.3	-	0.5	-	µs
High period of the SCL clock	T_{HIGH}	0.6	-	0.26	-	µs
Setup time for START condition	$T_{SU;STA}$	0.6	-	0.26	-	µs
Data hold time	$T_{HD;DAT}$	0	-	0	-	µs
Data setup time	$T_{SU;DAT}$	100	-	50	-	ns
Rise time of both SDA and SCL	T_R	20	300	-	120	ns
Setup time for STOP condition	$T_{SU;STO}$	0.6	-	0.26	-	µs
Data valid acknowledge time	$T_{VD;ACK}$	-	-	-	-	µs
Buffer free time between START and STOP condition	T_{BUF}	1.3	-	0.5	-	µs

Note 1 Clock duty ratio = (THIGH/TSCLK) × 100[%], TSCLK = 1/FSCLK

Note 2 Max. clock = 1.0 MHz (clock period = 1000 ns)

9.6 SD/SDeMMC

The SD/eMMC host IP provides the function for DA16200 to access SD or eMMC cards. This SD/eMMC host IP only supports a 4-bit data bus and the maximum clock rate is 50 MHz. The maximum data rate is 25 MB/s(200 Mbps) under the 4-bit data bus and 50 MHz clock.

SD/eMMC pin mux condition is defined in Table 41.

Table 41: SD/eMMC Master Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA4	34	F4	I/O	SD/eMMC_CMD
GPIOA5	33	D2	O	SD/eMMC_CLK
GPIOA9	29	H2	I/O	SD/eMMC_D0
GPIOA8	30	G3	I/O	SD/eMMC_D1
GPIOA7	31	E1	I/O	SD/eMMC_D2
GPIOA6	32	E3	I/O	SD/eMMC_D3
GPIOA10	28	F2	I	SD/eMMC_WRP
GPIOA1	38	C3	I	

9.6.1 Block Diagram

Figure 32 shows the block diagram of SD/eMMC host IP and it includes the control register, clock control, command/response pipe, data pipe, and AHB master interface blocks.

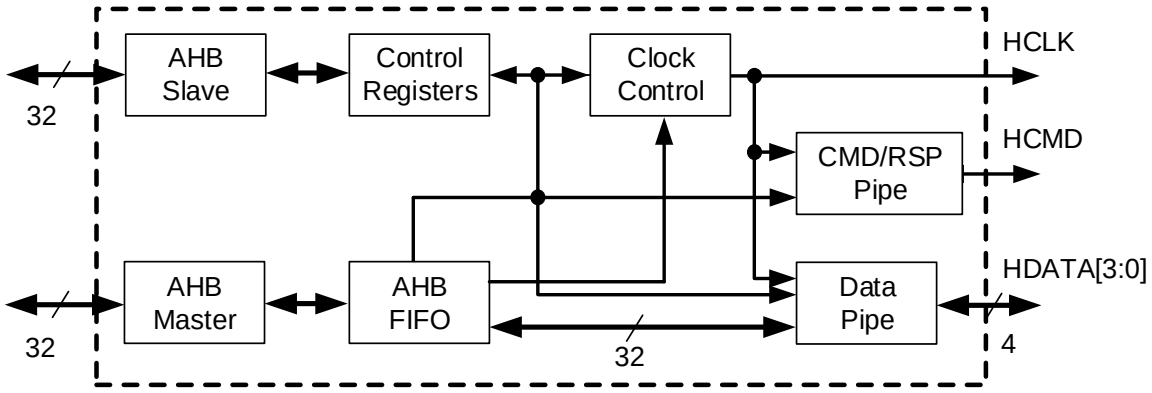


Figure 32: SD/eMMC Block Diagram

Figure 33 shows the timing diagram for the SD/eMMC master.

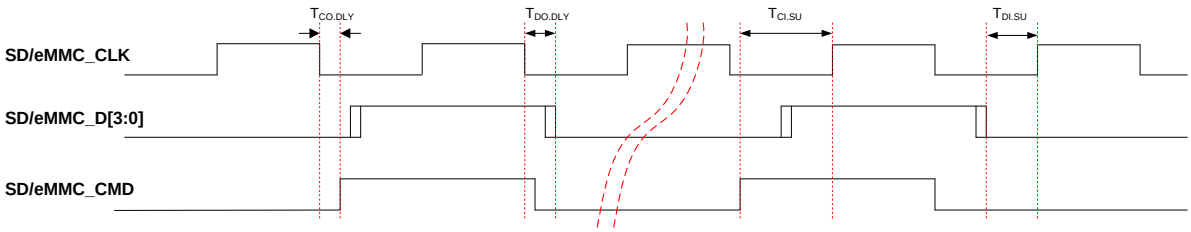


Figure 33: SD/eMMC Master Timing Diagram

Table 42 lists the timing parameters for the SD/eMMC master.

Table 42: SD/eMMC Master Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
SD/eMMC_CLK frequency	F_{SCLK}	-	-	50	MHz
SD/eMMC_CLK clock duty			50		%
SD/eMMC_CMD input setup time	$T_{CI.SU}$	8			ns
SD/eMMC_CMD output delay time	$T_{CO.DLY}$			3	ns
SD/eMMC_D[3:0] input setup time	$T_{DI.SU}$	8			ns
SD/eMMC_D[3:0] output delay time	$T_{DO.DLY}$			8	ns

9.7 I2S

DA16200 provides an I2S interface. Once an I2S block receives audio data through the DMA, it sends audio data to the external port according to the I2S standard. To use the external DAC, output through the GPIO port is possible through the register setting according to the pin configuration (Table 43).

The I2S also provides a receive function. However, I2S transmission and reception functions cannot be used at the same time. The transmit and receive functions can be selected by register setting. If the I2S signal is input from outside after the reception function is set, the audio signal can be decoded, stored in the FIFO, and read out through the DMA. The decodable reception function provides 8/16/24/32-bit modes and can receive either mono or stereo.

Using the I2S clock divider register, the internal PLL clock can be variably applied to the I2S clock source. The available I2S clock source is 24/48 MHz. There is also a way to apply the I2S clock source directly from outside using the GPIO pin. For accurate I2S audio sampling, I2S clock source can be input to external GPIO pins. It needs to select the GPIO pin setting as the I2S clock input and apply appropriate clock source. The available I2S clock pins are shown in Table 43.

Table 43: I2S Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA1	38	C3	O	I2S_MCLK
GPIOA5	33	D2	O	
GPIOA9	29	H2	O	
F_CLK	19	K4	O	
GPIOA0	39	A3	O	I2S_BCLK
GPIOA4	34	F4	O	
GPIOA8	30	G3	O	
F_CSN	18	J5	O	
GPIOA3	36	D4	O	I2S_LRCK
GPIOA7	31	E1	O	
F_IO0	14	K8	O	
GPIOA2	37	B2	I/O	I2S_SDO
GPIOA6	32	E3	I/O	
F_IO1	15	L7	I/O	
GPIOA3	36	D4	I	I2S_CLK_IN
GPIOA10	28	F2	I	

9.7.1 I2S Transmit and Receive Timing Diagram

I2S output is possible in the following three modes. The main clock(MCLK) always outputs in 512×fs.

- I2C Mode

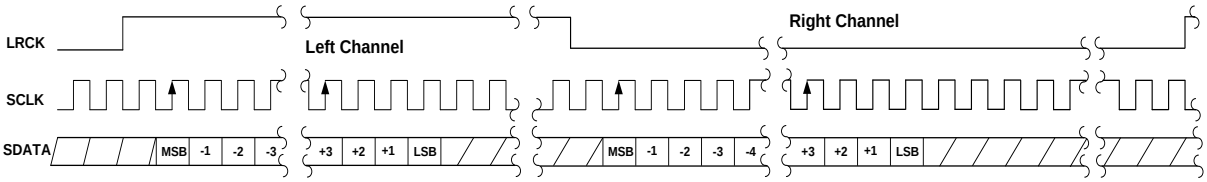


Figure 34: I2S Timing Diagram

- Left Justified Mode

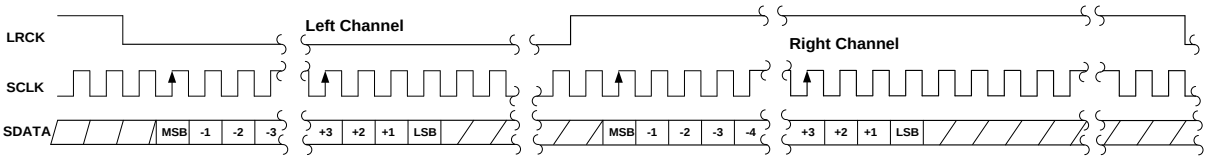


Figure 35: Left Justified Mode Timing Diagram

- Right Justified Mode

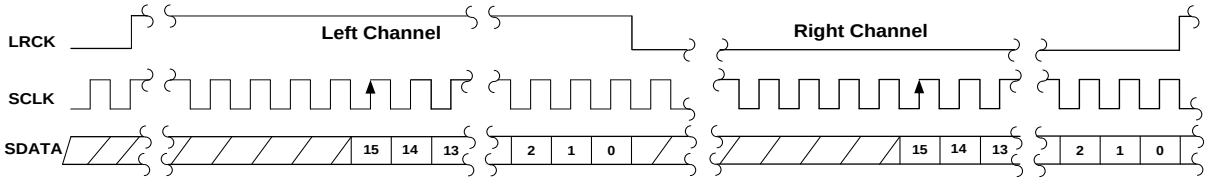


Figure 36: Right Justified Mode Timing Diagram

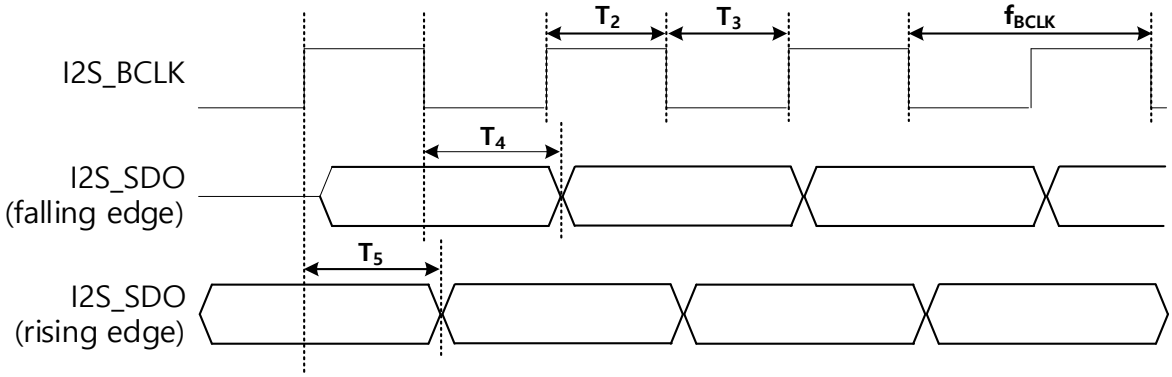


Figure 37: I2S Transmit Timing Diagram

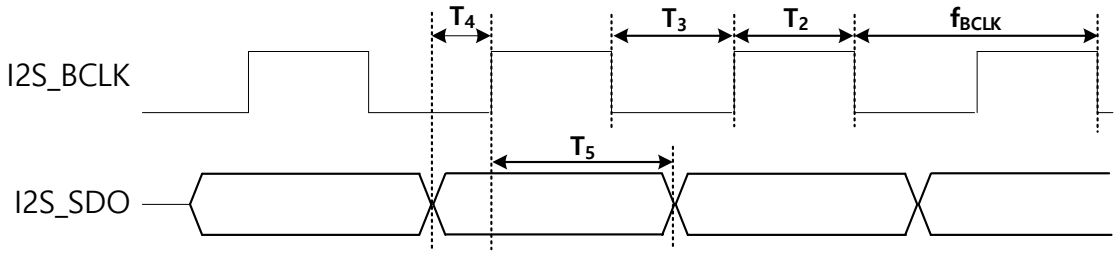


Figure 38: I2S Receive Timing Diagram

Table 44: I2S Transmit Timing Parameters

Description	Timing	Min	Typ	Max	Unit
I2S_BCLK frequency	f_{BCLK}	-		3.072	MHz
High period of the BCLK clock	T_2	-		½ f_{BCLK}	ns
Low period of the BCLK clock	T_3	-		½ f_{BCLK}	ns
I2S_SDO output hold (falling edge)	T_4	160		-	ns
I2S_SDO output hold (rising edge)	T_5	160		-	ns

Table 45: I2S Receive Timing Parameters

Description	Timing	Min	Typ	Max	Unit
I2S_BCLK frequency	f_{BCLK}	-		3.072	MHz
High period of the BCLK clock	T_2	-		½ f_{BCLK}	ns
Low period of the BCLK clock	T_3	-		½ f_{BCLK}	ns
I2S_SDO input setup time	T_4	15		-	ns
I2S_SDO input hold time	T_5	60		-	ns

9.8 ADC(Aux 12-bit)

9.8.1 Overview

DA16200 includes a high precision, ultra low power, and wide dynamic range SAR ADC with a 12-bit resolution. It has a 4-channel single-end ADC.

Analog input is measured by four pins from GPIOA0 to GPIOA3, and pin selection is changed through the register setting.

Figure 39 shows the control block diagram.

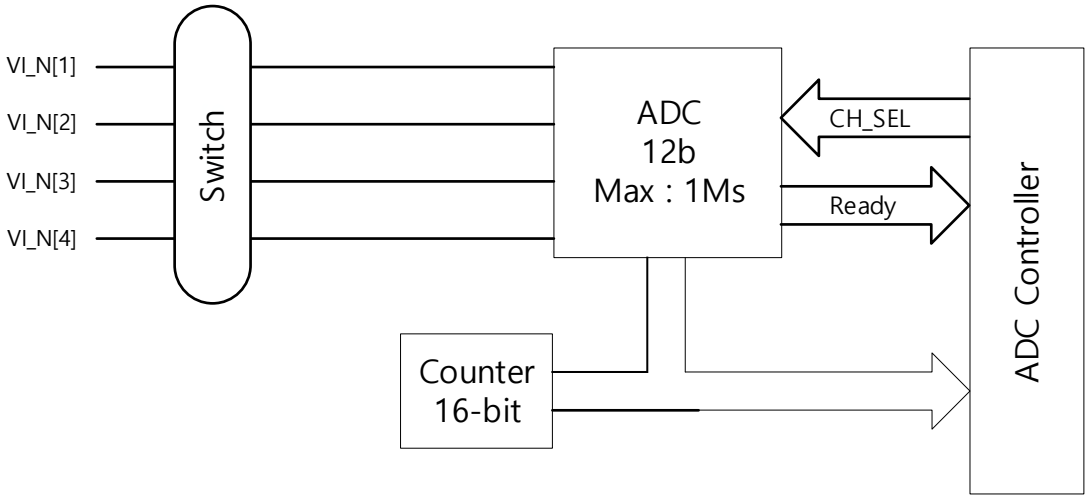


Figure 39: ADC Control Block Diagram

9.8.2 Timing Diagram

The input is digitized at a maximum of 1.0 Msps throughput rate. And maximum input clock rate is 15 MHz.

Figure 40 shows the conversion timing, and Table 46 describes DC specifications.

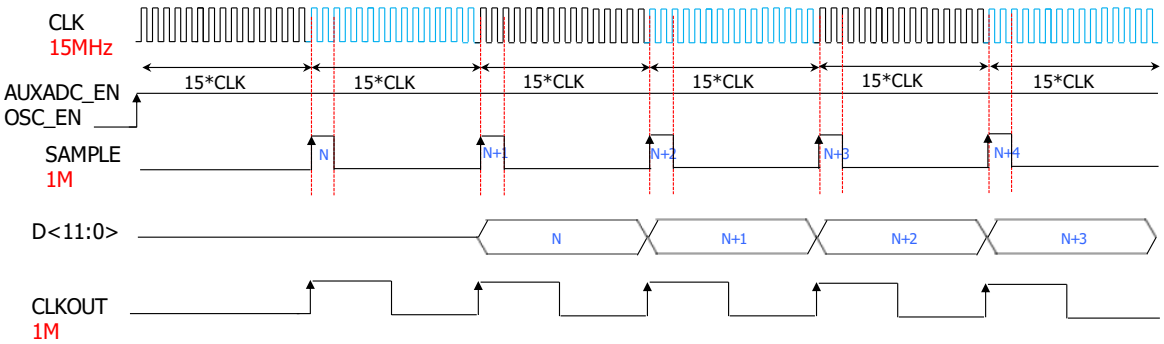


Figure 40: 12-bit ADC Timing Diagram

Table 46: DC Specification

Description	Min	Typ	Max	Unit
Resolution	4	12	12	Bits
Max clock input			15	MHz
Conversion frequency			1	MHz
Accuracy:				
• SNR • SNDR		• 61.7 • 67.2		• dB • dB
Analog input range	0		1.4	V

9.8.3 DMA Transfer

There are four ADC channel settings available. Once the input data of each channel reaches the FIFO level, it is possible to read the data through the DMA path.

9.8.4 ADC Ports

Table 47 shows the pin definition of the ADC.

Table 47: ADC Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOA3	36	D4	A	Analog signal
GPIOA2	37	B2	A	Analog signal
GPIOA1	38	C3	A	Analog signal
GPIOA0	39	A3	A	Analog signal

9.9 GPIO

All digital pads can be used as GPIO, and each GPIO port is muxed with a multi-functional interface. The GPIO features of DA16200 are listed below:

- Input or output lines in a programmable direction
- Word and half word read/write access
- Address-masked byte writes to facilitate quick bit set and clear operations
- Address-based byte reads to facilitate quick bit test operations
- Maskable interrupt generation based on input value change
- Possible to be output signal of PWM[3:0], external interrupt, QSPI_CSB[3:1], RF_SW[1:0], and UART_TXDOE[2:0] on the GPIO pins:
  - It provides special functions for GPIO pin use. PWM [3:0], external interrupt, QSPI_CSB [3:1], RF_SW [1:0], and UART_TXDOE [2:0] signals can be output by selecting unused pins among the GPIO pins. It is possible to select the function to be output from the GPIO register setting and select the remaining GPIO pin without using it to output the specific function to the desired GPIO pins

9.9.1 Antenna Switching Diversity

DA16200 provides the antenna switching diversity function for performance improvement in multi-path environment. Phy block measures the RSSI of each antenna and selects the antenna with the largest RSSI. The selected antenna is also used for transmission. To use this function, an external switching element is required, and switching control is performed through the GPIO. Two GPIOs can be used for switching control, and any unused pins among the GPIO pins can be selected for this purpose. The control signal can be changed by register setting to suit the external switching device.

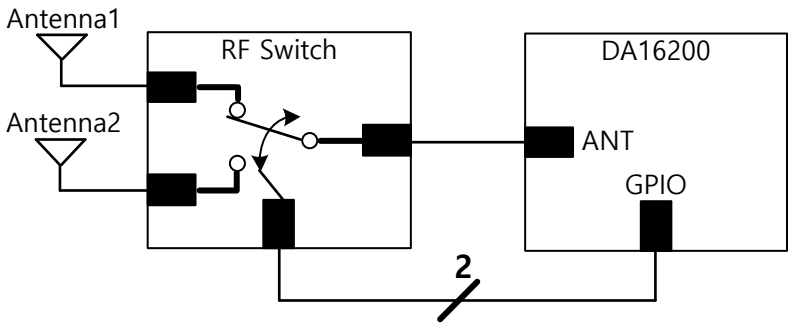


Figure 41: Antenna Switching Internal Block Diagram

9.10 UART

DA16200 provides three UARTs, features of which are described below:

- Programmable use of UART (UART1 and UART2)
- Compliance to the *AMBA AHB bus specification* [7] for easy integration into SoC implementation
- Supports both byte and word access for reduction of bus burden
- Supports both RS-232 and RS-485
- Separate 32×8 bit transmit and 32×12 bit receive FIFO memory buffers to reduce CPU interrupts
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator
- Standard asynchronous communication bits (start, stop and parity), which are added prior to transmission and removed on reception
- Independent masking of transmit FIFO, receive FIFO, and receive timeout
- Supports for DMA
- False start bit detection
- Programmable flow control (CTS/RTS, UART1 and UART2)
- Fully programmable serial interface characteristics:
  - Data can be of 5,6,7, or 8 bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1- or 2- stop bit generation
  - Baud rate generation

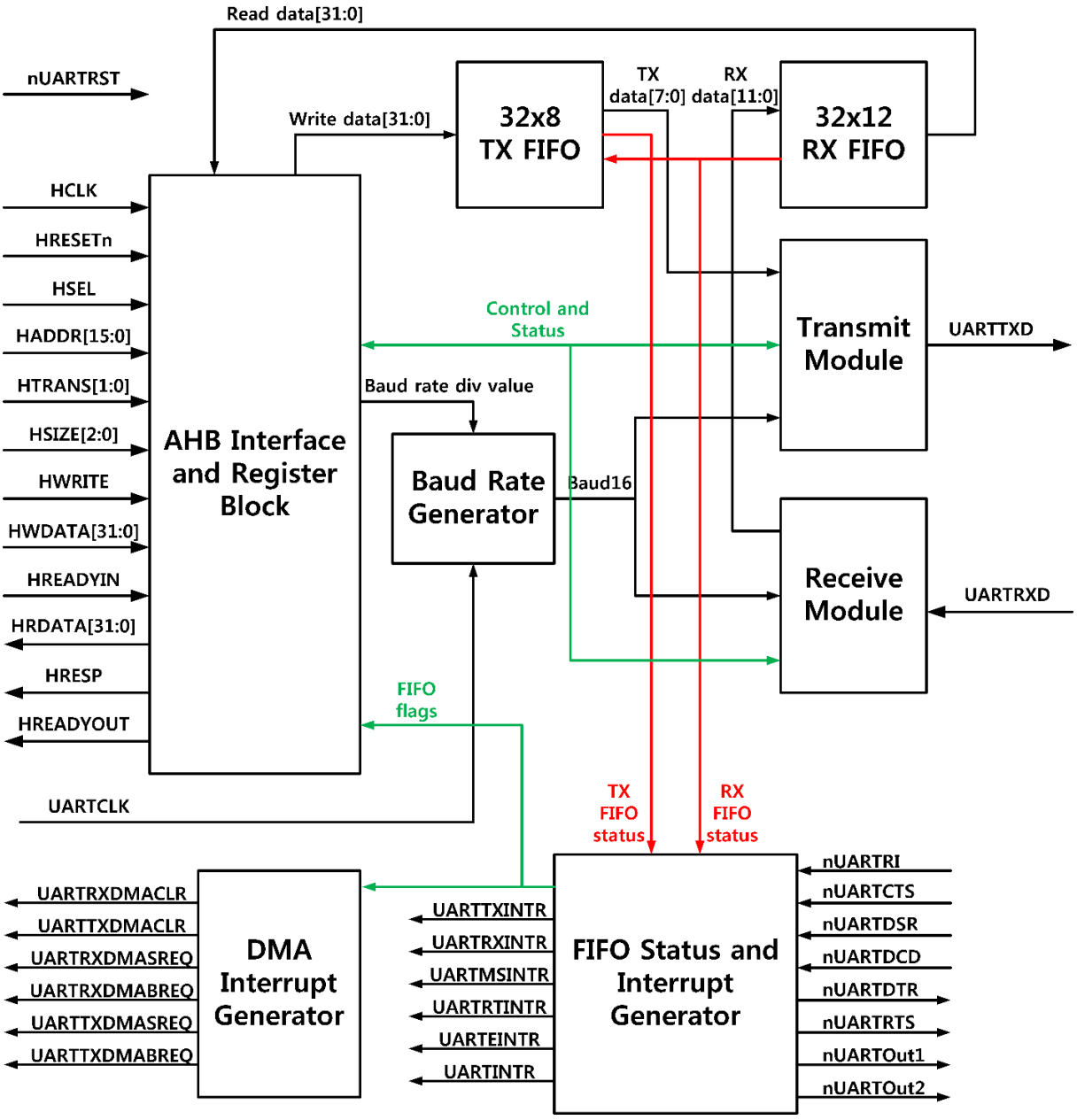


Figure 42: DA16200 UART Block Diagram

9.10.1 RS-232

As the serial communication between the UART and the selected device is asynchronous, additional bits (start and stop) are inserted to the data line to indicate the beginning and end. By these bits, two devices can be synchronized. This structure of serial data accompanied by start and stop bits is referred to as a character, as shown in Figure 43.

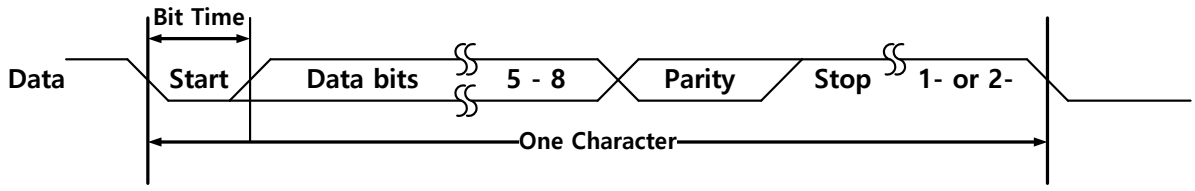


Figure 43: Serial Data Format

An additional parity bit may be added to the serial character. This bit appears between the last data bit and the stop bit(s) in the character structure. It provides the UART with the ability to perform simple error checking on the received data.

The UART Line Control Register is used to control the serial character characteristics. The individual bits of the data word are sent after the start bit, starting with the least significant bit (LSB). These are followed by the optional parity bit, followed by the stop bit(s), which can be 1 or 2.

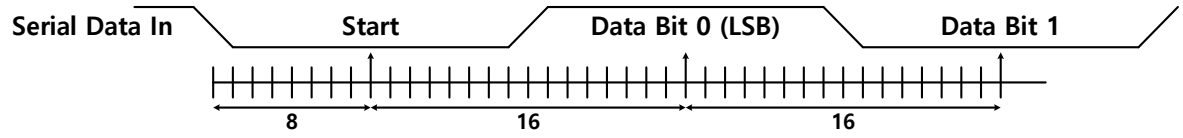


Figure 44: Receiver Serial Data Sampling Points

All the bits in the transmission are transmitted for exactly the same time duration. This is referred to as a Bit Period or Bit Time. One Bit Time equals 16 baud clocks. To ensure stability on the line, the receiver samples the serial input data at approximately the mid-point of the Bit Time, once the start bit has been detected. As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit. Figure 44 shows the sampling points of the first couple of bits in a serial character.

9.10.2 RS-485

DA16200 UART supports RS-485. UART485EN register (0x054) is required to be assigned to one, to enable the RS-485. In order to use RS-485, additional signal (UARTTXDOE) is required to notice TXD intervals. This signal can be an output by selecting any unused pins among the GPIO pins.

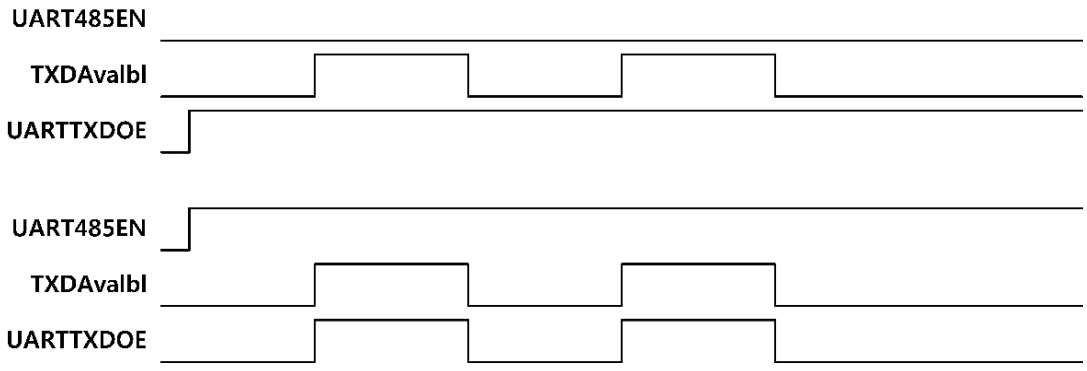


Figure 45: UARTTXDOE Output Signal for UART RS-485

9.10.3 Hardware Flow Control

Hardware flow control feature is fully selectable, and serial data flow is controlled by using nUARTRTS output and nUARTCTS input signals. Figure 46 shows how two different UART can communicate using hardware flow control.

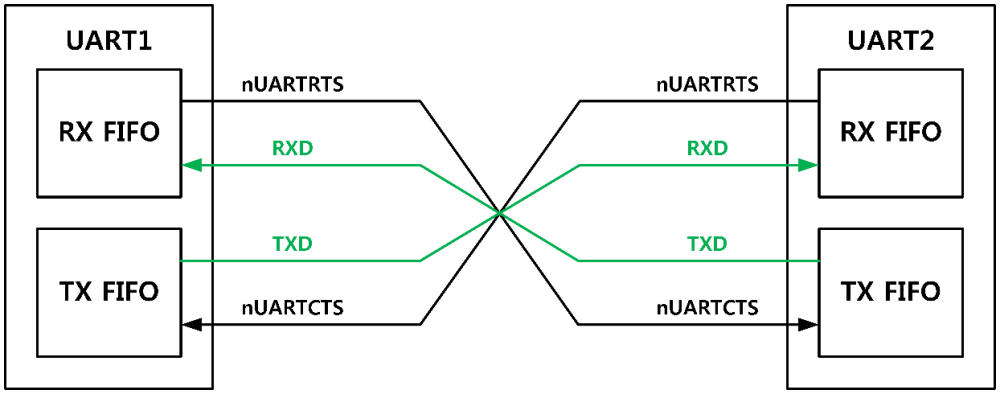


Figure 46: UART Hardware Flow Control

When RTS flow control is enabled, nUARTRTS signal is asserted until the receive FIFO is filled up to programmed level. When CTS flow control is enabled, transmitter can transmit the data when nUARTCTS signal is asserted. CTSEn (CTS enable) and RTSEn (RTS enable) bits are determined by 14th (RTS) and 15th bit (CTS) of UARTCR register.

Table 48: Control bits to enable and disable hardware flow control

CTSEn	RTSEn	Description
1	1	Both RTS and CTS flow control are enabled
1	0	Only CTS flow control is enabled
0	1	Only RTS flow control is enabled
0	0	Both RTS and CTS flow control are disabled

9.10.4 Interrupts

DA16200 UART block provides five interrupt signals by separate interrupt lines. Each interrupt conditons are Modem Status, Receive FIFO Request, Transmit FIFO Request, Receive Timeout and Reception Error. These conditions are logically OR'ed to provide a single combined interrupt, UARTINTR. Table 49 shows the interrupt signals.

Table 49: UART Interrupt Signals

Signal Name	Description
UARTMSINTR	UART Modem Status Interrupt
UARTRXINTR	UART Receive FIFO Interrupt
UARTTXINTR	UART Transmit FIFO Interrupt
UARTRTINTR	UART Receive Timeout Interrupt
UARTEINTR	UART Error Interrupt
UARTINTR	UART Interrupt. Five Interrupt signals are combined by OR function

9.10.5 DMA Interface

DA16200 UART block can generate DMA request signals with register settings by using DMA interrupt generator module to connect to DA16200 DMA Controller (DMA1). DMA operation of the UART is controlled using DMA Control Register.

DA16200 UART provides four DMA signals and receives two DMA signals, two signals to transmit (TXDMASREQ, TXDMABREQ) which are cleared by TX clear signal (TXDMACLR) and two signals to receive (RXDMASREQ, RXDMABREQ), which are cleared by RX clear signal (RXDMACLR).

When the DMA interface is not used, the TXDMACLR and RXDMACLR lines should be connected to a logic '0'.

Table 50 shows the pin definition of the UART interface.

Table 50: UART Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
UART0_RXD	12	M10	I	UART0_RXD
UART0_TXD	11	L9	O	UART0_TXD
GPIOA7	31	E1	I	UART1_RXD
GPIOA5	33	D2	I	
GPIOA3	36	D4	I	
GPIOA1	38	C3	I	
GPIOA6	32	E3	O	UART1_TXD
GPIOA4	34	F4	O	
GPIOA2	37	B2	O	
GPIOA0	39	A3	O	
GPIOA5	33	D2	I	UART1_CTS
GPIOA4	34	F4	O	UART1_RTS
GPIOA11	27	G1	I	UART2_RXD
GPIOC7	9	K12	I	
F_IO2	16	J7	I	
GPIOA10	28	F2	O	UART2_TXD
GPIOC6	10	L11	O	
F_IO3	17	K6	O	

9.11 PWM

Pulse width modulation(PWM) is a modulation technique used to encode a message into a pulse signal. The blocks are designed to adjust output pulse duration by the CPU bus clock (HCLK).

Figure 47 shows the structure of the PWM block.

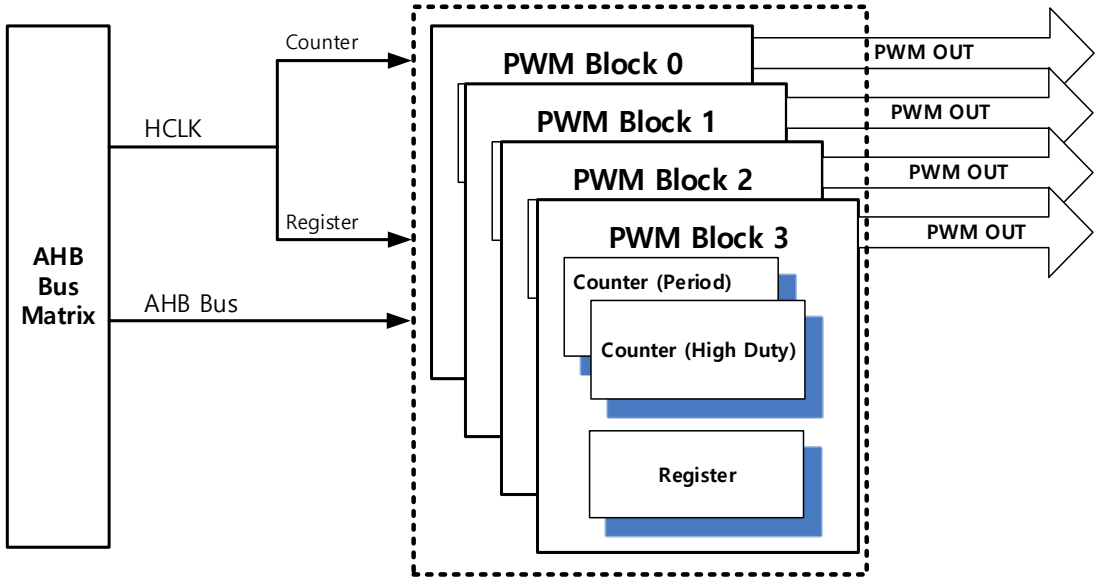


Figure 47: PWM Block Diagram

Table 51 shows the pin definition of the PWM interface. GPIOx means that PWM signals can go out through any GPIO pins via register setting.

Table 51: PWM Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
GPIOx				PWM[3:0] output

9.11.1 Timing Diagram

Table 52 shows the relation between the internal bus clock and PWM output wave patterns. Figure 48 show the conversion timing diagram. '**a**' and '**b**' can be adjusted through the register setting, and PWM wave patterns vary depending on the ratio. '**a**' controls the high width of pulses(nCycle High), while '**b**' controls the general cycle (nCycle Period).

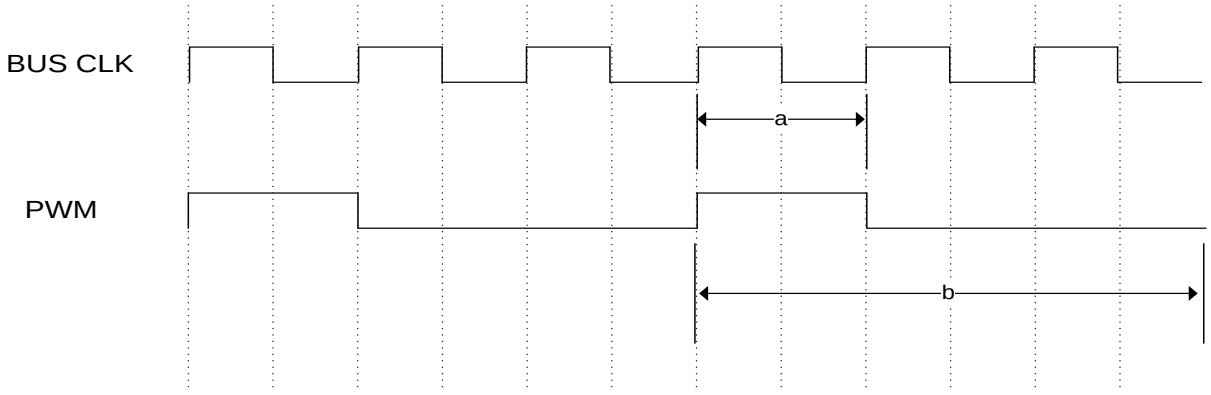


Figure 48: PWM Timing Diagram

Table 52: PWM Timing Diagram Description

Time	Description
a	Bus Clock Period × (nCycle High + 1)
b	Bus Clock Period × (nCycle Period + 1)

9.12 Debug Interface

DA16200 supports both IEEE Standard 1149.1 JTAG (5-wire) and the low-pin-count Arm SWD (2-wire, TCLK/TMS) debug interfaces. The SWD protocol can handle the same debug features as the JTAG.

The JTAG port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see [5].

Figure 49 shows the JTAG timing diagram.

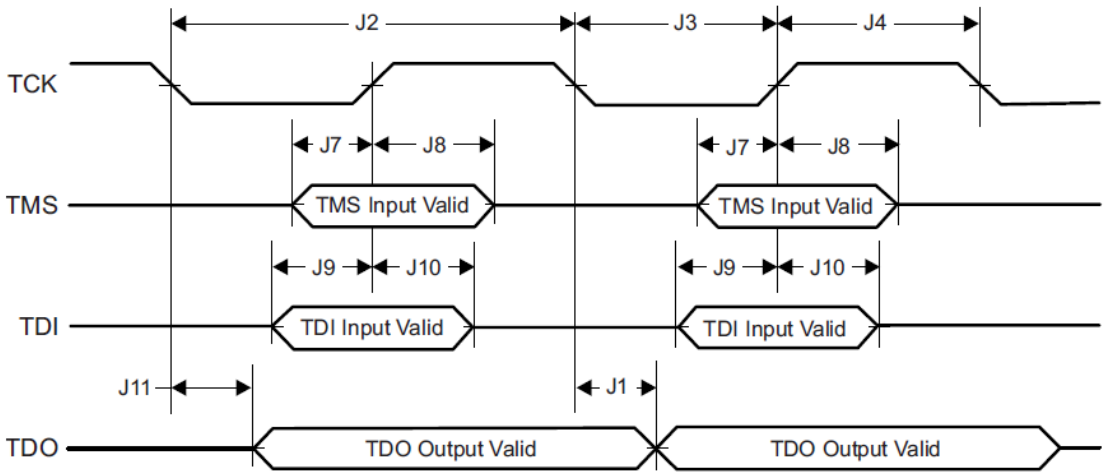


Figure 49: JTAG Timing Diagram

Table 53 shows the JTAG timing parameters.

Table 53: JTAG Timing Parameters

Parameter Number	Parameter	Parameter Name	Min	Max	Unit
J1	f_{TCK}	Clock Frequency		15	MHz
J2	t_{TCK}	Clock Period		$1/f_{TCK}$	ns
J3	t_{CL}	Clock Low Period		$t_{TCK}/2$	ns
J4	t_{CH}	Clock High Period		$t_{TCK}/2$	ns
J7	t_{TMS_SU}	TMS Setup Time	1		
J8	t_{TMS_HO}	TMS Hold Time	16		
J9	t_{TDI_SU}	TDI Setup Time	1		
J10	t_{TDI_HO}	TDI Hold Time	16		
J11	t_{TDO_HO}	TDO Hold Time		15	

Table 54 shows the pin definition of the JTAG interface.

Table 54: JTAG Pin Configuration

Pin Name	Pin Number		I/O	Function Name
	QFN	fcCSP		
TMS	6	J11	I/O	Data
TCLK	7	J9	I	Clock
GPIOC8	8	K10	I	TDI: Data Input
GPIOC7	9	K12	O	TDO: Data Output
GPIOC6	10	L11	I	nTRST: Reset

9.13 Bluetooth Coexistence

DA16200 provides the bluetooth coexistence function to be properly aligned with external devices activated at 2.4 GHz.

9.13.1 Interface Configuration

The following three pins can be set in pin multiplexing:

- BT_sig0 (oWlanAct)
  - It indicates that Output, WLAN is currently active
- BT_sig1 (iBtAct)
  - It indicates that Input, BT/BLE is currently active
- BT_sig2 (iBTPri)
  - It indicates that Input (Optional), BT/BLE has a higher priority

A variety of configurable settings are available, including active high/low, manual force mode, use status of the optional iBTPri function, and whether or not to switch oWlanAct to active in the event of TX/RX/TRX.

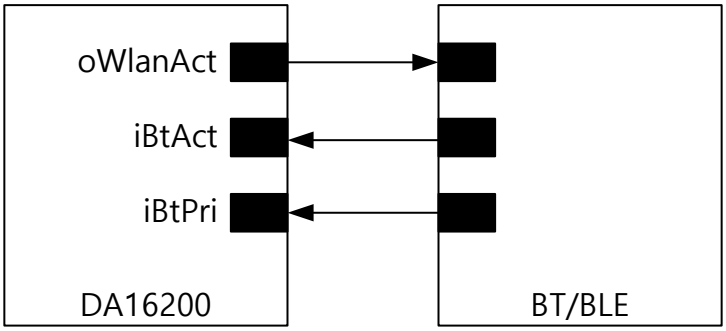


Figure 50: Bluetooth Coexistence Interface

9.13.2 Operation Scenario

The bluetooth coexistence can be turned on/off by the configurable register, and the activation scenarios based on the status of each pin are described below:

- BT_sig0 (oWlanAct)
  - When asserted, external BT/BLE is expected to stop occupying RF
- BT_sig1 (iBtAct)
  - When asserted, DA16200 stops occupying RF
- BT_sig2 (iBTPri)
  - It is optional and thus may not be used
  - If it is used and DA16200's iBtAct = Active while iBTPri = Non-Active, DA16200 may ignore iBtAct

10 Applications Schematic

10.1 Typical Application: QFN, 3.3 V Flash

Figure 51 shows the schematics for an application using the DA16200 in 3.3 V flash mode.

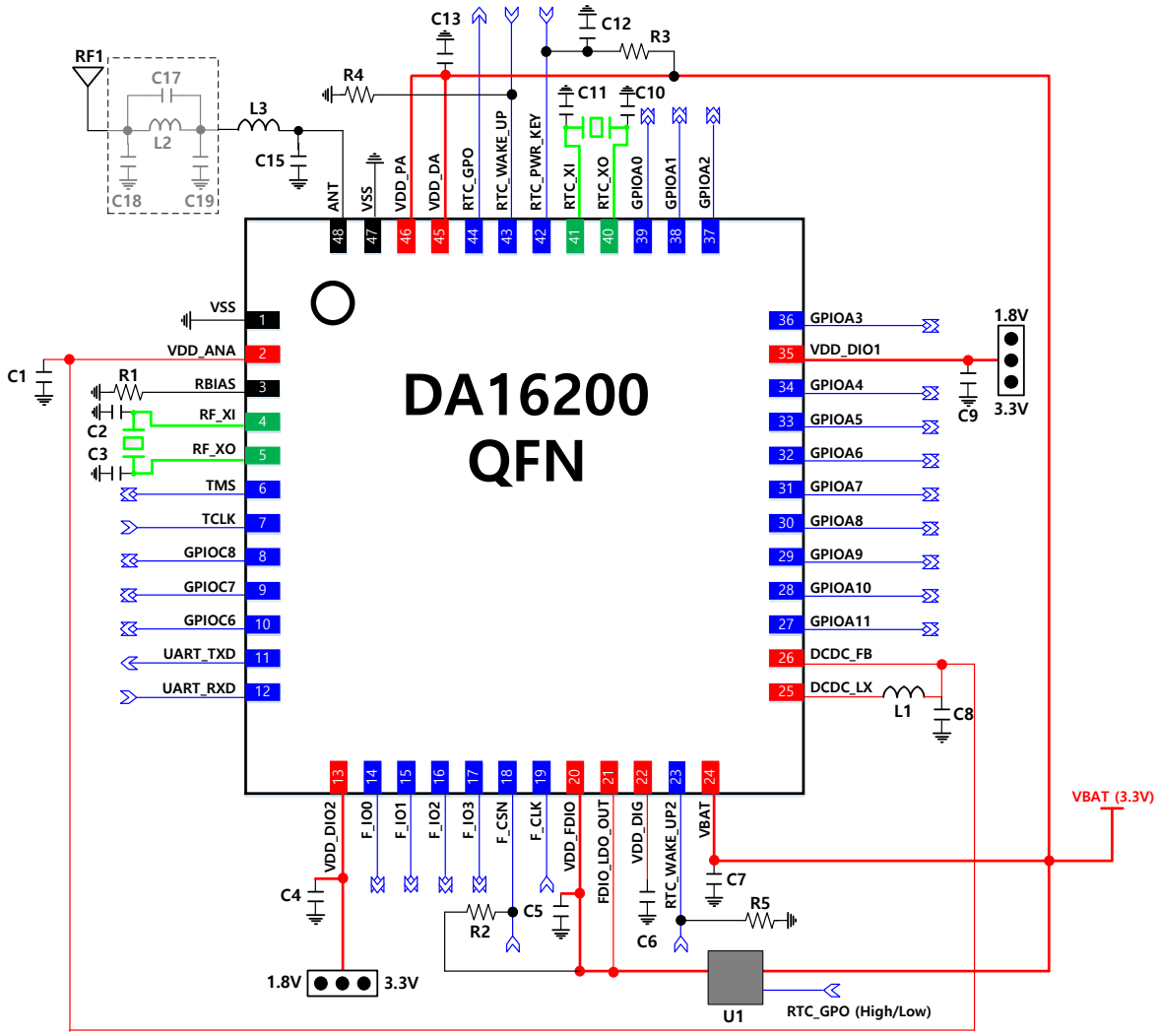


Figure 51: Typical Application – QFN, 3.3 V Flash

Table 55 lists the components for an application using the DA16200 QFN in 3.3 V flash mode.

Table 55: Components for DA16200 QFN, 3.3 V Flash Mode

Quantity	Part Reference	Value	Description
1	R1	30 kΩ(1%)	
2	C2, C3	1.2pF	These values may be changed by crystal component characteristics and board condition Part: FCX-07L
5	C1, C4, C5, C7, C9	1µF	
1	C6	470nF	
1	R2	10 kΩ	
1	L1	4.7µH	LQM21PN4R7MGH(Murata)
1	C8	10µF	
2	C10, C11	15pF	These values may be changed by crystal component characteristics and board condition Part: TFX-03
1	R3	4.7 kΩ	
1	C12	100nF	
2	R4, R5	4.7 kΩ	
1	C13	4.7µF	
1	C15	DNI	Optional
1	L3	2.2 nH	
1	C17	0.5pF	Optional
2	C18, C19	1pF	Optional
1	L2	1.8nH	Optional
1	U1		Optional, load switch for disconnecting VBAT for VDD_FDIO

Note 1 Use any 5% tolerance.

Table 56: IO Power Domain

IO Power Domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO	F_IO[3:0], F_CSN, F_CLK

10.2 Typical Application: QFN,1.8 V Flash

Figure 52 shows the schematics for an application using the DA16200 QFN in 1.8 V flash mode.

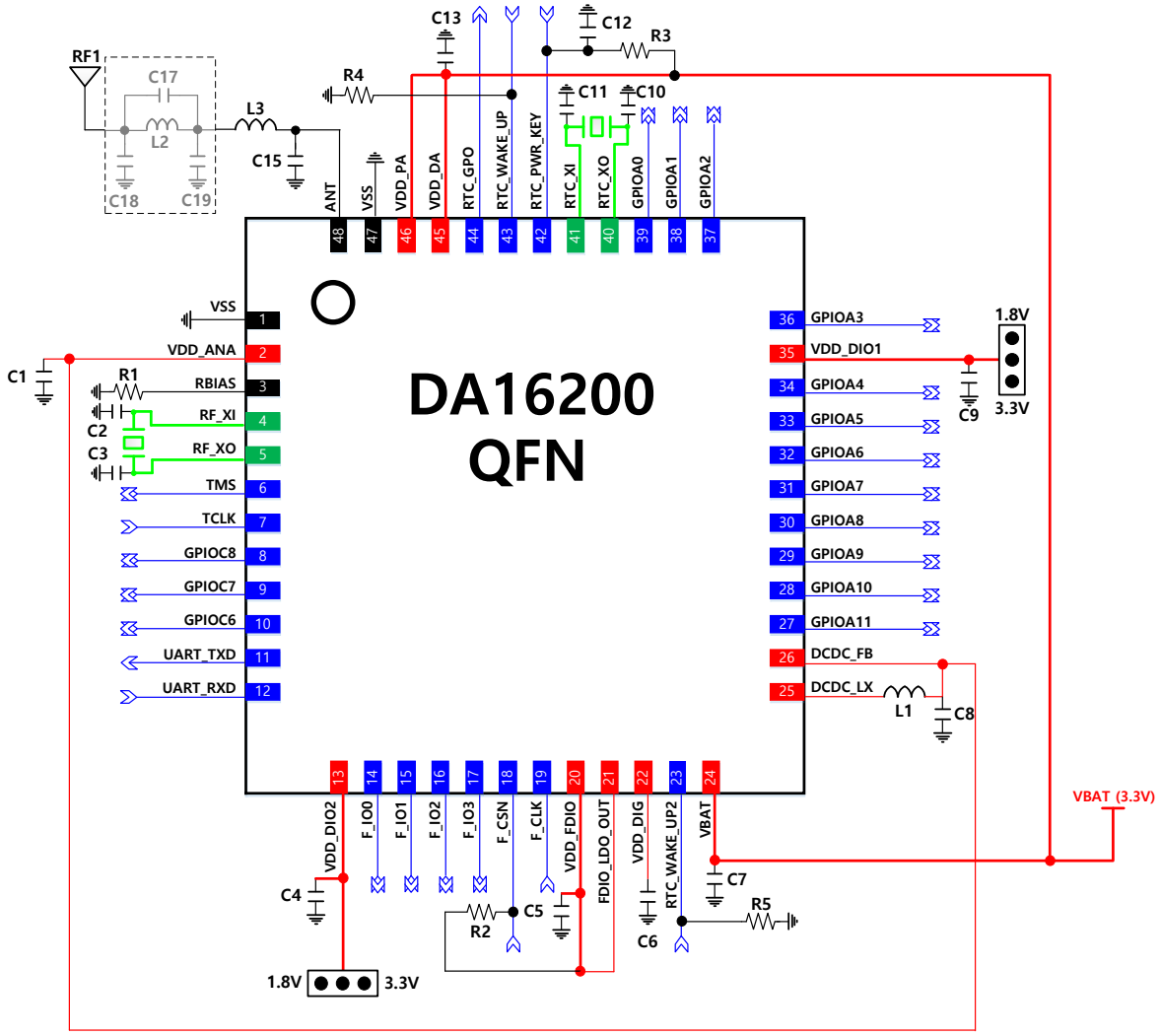


Figure 52: Typical Application – QFN, 1.8 V Flash

Table 57 lists the components for an application using the DA16200 QFN in 1.8 V flash mode.

Table 57: Component for DA16200 QFN, 1.8 V Flash Mode

Quantity	Part Reference	Value	Description
1	R1	30 kΩ(1%)	
2	C2, C3	1.2 pF	These values may be changed by crystal component characteristics and board condition Part: FCX-07L
5	C1, C4, C5, C7, C9	1 µF	
1	C6	470 nF	
1	R2	10 kΩ	
1	L1	4.7 µH	LQM21PN4R7MGH(Murata)
1	C8	10 µF	
2	C10, C11	15 pF	These values may be changed by crystal component characteristics and board condition Part: TFX-03
1	R3	4.7 kΩ	
1	C12	100 nF	
2	R4, R5	4.7 kΩ	
1	C13	4.7 µF	
1	C15	DNI	Optional
1	L3	2.2 nH	
1	C17	0.5 pF	Optional
2	C18, C19	1 pF	Optional
1	L2	1.8 nH	Optional

Note 1 Use any 5% tolerance.

Table 58: IO Power Domain

IO Power Domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO	F_IO[3:0], F_CSN, F_CLK

10.3 Typical Application: fcCSP,1.8 V Flash

Figure 53 shows the schematics for an application using the DA16200 fcCSP in 1.8 V flash mode.

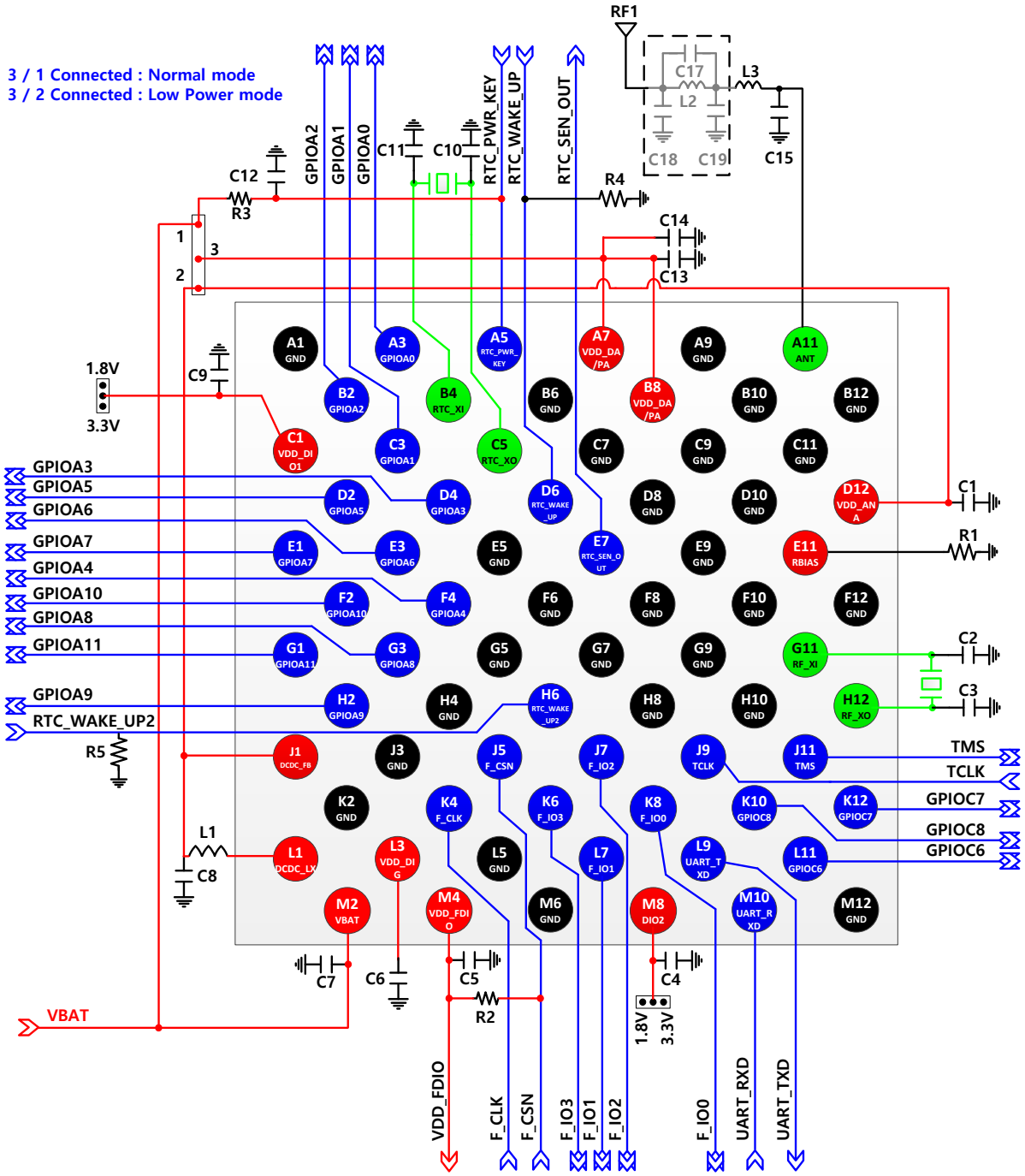


Figure 53: Typical Application – fcCSP, 1.8 V Flash

Table 59 lists the components for an application using the DA16200 fcCSP in 1.8 V flash mode.

Table 59: Component for DA16200 fcCSP, 1.8 V Flash Mode

Quantity	Part Reference	Value	Description
1	R1	30 kΩ(1%)	
2	C2, C3	1.2 pF	These values may be changed by crystal component characteristics and board condition Part: FCX-07L
1	C6	470 nF	
4	C1, C4, C5, C9	1 µF	
1	C7	2.2 uF	
1	R2	10 kΩ	
1	L1	4.7 µH	LQM21PN4R7MGH (Murata)
1	C8	10 µF	
2	C10, C11	15 pF	These values may be changed by crystal component characteristics and board condition Part: TFX-03
1	R3	4.7 kΩ	
1	C12	100 nF	
1	R4, R5	4.7 kΩ	
1	C13	4.7 µF	
1	C15	0.5 pF	Normal power mode
1	L3	2.7 nH	Normal power mode
1	C15	DNI	Low power mode
1	L3	2.2 nH	Low power mode
1	C17	0.5 pF	Optional
2	C18, C19	1 pF	Optional
1	L2	1.8 nH	Optional

Note 1 Use any 5% tolerance.

Table 60: IO Power Domain

IO Power Domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO	F_IO[3:0], F_CSN, F_CLK

11 Package Information

11.1 Moisture Sensitivity Level (MSL)

The MSL is an indicator for the maximum allowable time period (floor life time) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60 % RH before the solder reflow process.

QFN and fcCSP packages are qualified for MSL 3.

MSL Level	Floor Life Time
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30°C/85%RH

11.2 Top View: QFN and fcCSP

Figure 54: DA16200 48-Pin QFN Package

Figure 55: DA16200 72-Pin fcCSP Package

11.3 Dimension: 48-pin QFN

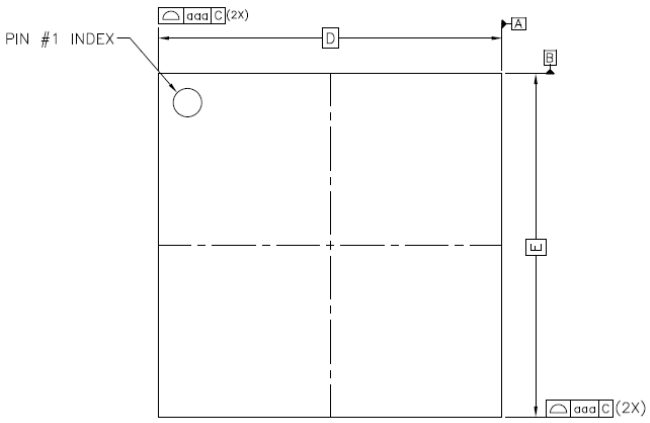


Figure 56: Top View

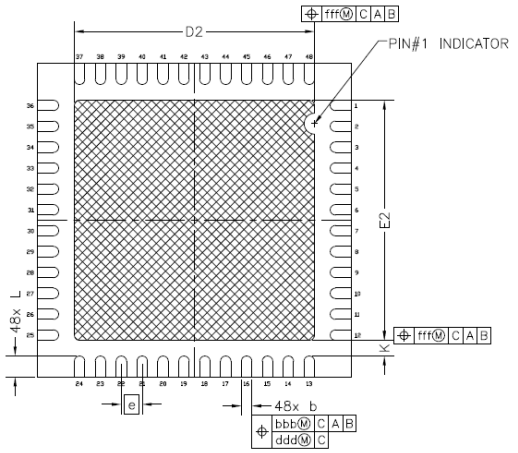


Figure 57: Bottom View

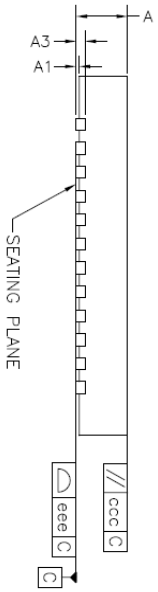


Figure 58: Side View

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D		6.00 BSC	
E		6.00 BSC	
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20		
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 59: DA16200 48-Pin QFN Package Dimensions

11.4 Dimension: 72-pin fcCSP

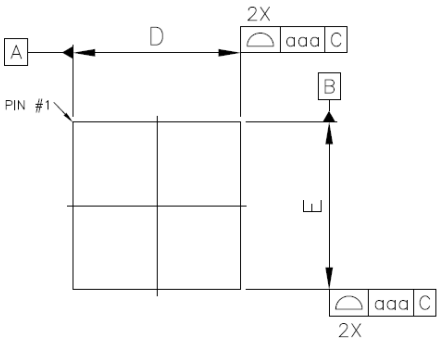


Figure 60: Top View

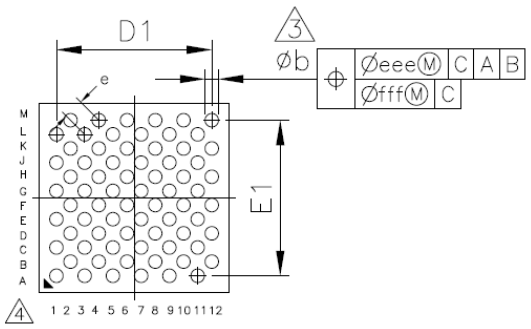


Figure 61: Bottom View

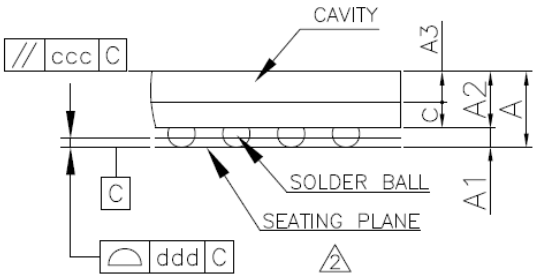


Figure 62: Side View

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.54	0.61	0.68
A1	0.11	0.16	0.21
A2	0.40	0.45	0.50
A3	0.25	0.28	0.31
c	0.14	0.17	0.20
D	3.73	3.80	3.87
E	3.73	3.80	3.87
D1	---	3.11	---
E1	---	3.11	---
e	---	0.40	---
b	0.22	0.27	0.32
aaa	0.07		
ccc	0.10		
ddd	0.08		
eee	0.10		
fff	0.05		
MD/ME	12/12		

Figure 63: DA16200 72-Pin fcCSP Package Dimensions

11.5 Land Pattern: 48-pin QFN

Unit: mm

Pad:Metal mask = 1:1

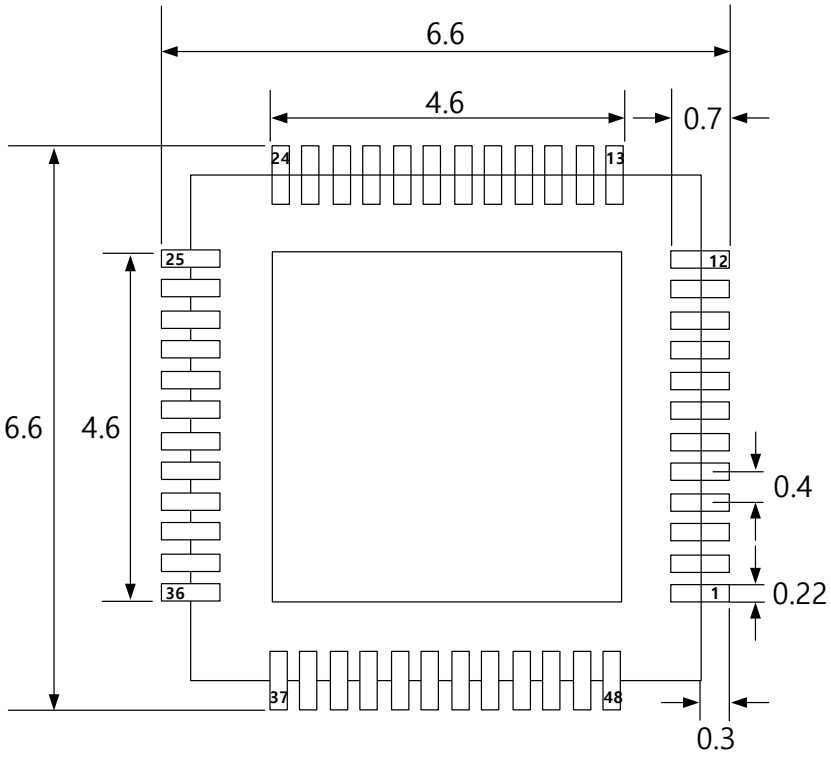


Figure 64: DA16200 48-Pin QFN Land Pattern

11.6 Land Pattern: 72-pin fcCSP

Unit: mm

Pad:Metal mask = 1:1

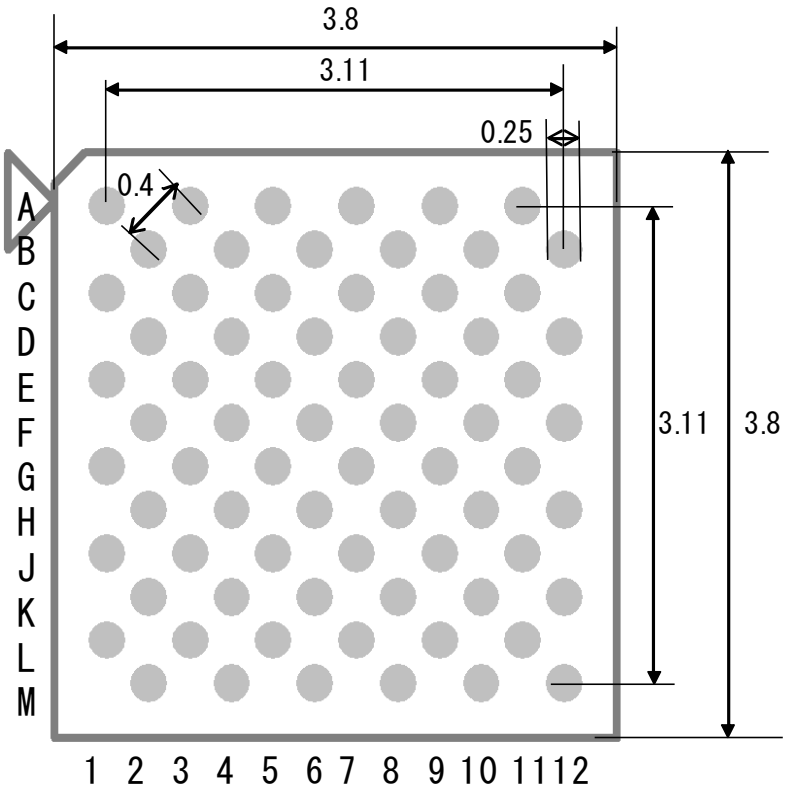


Figure 65: DA16200 72-Pin FcCSP Land Pattern

11.7 Soldering Information

11.7.1 Recommended Condition for Reflow Soldering

Figure 66 shows the typical process flow for mounting surface mount packages to PCB.

The reflow profile depends on the solder paste being used and the recommendations from the paste manufacture should be followed to determine the proper reflow profile. Figure 66 shows a typical reflow profile when a no-clean paste is used. Oven time above liquidus (260 °C for lead-free solder) is 30 to 60 seconds.

Since solder joints are not exposed in QFN packages, any retouch is not possible and the whole package has to be removed if the surface mount process results in shorts or opens. Furthermore, rework of QFN packages can be a challenge due to their small size. In most applications, QFNs will be mounted on smaller, thinner, and denser PCBs, and it introduces further challenges due to handling and heating issues. Since reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent complexities, the following steps only provides a guideline and a starting point for the development of a successful rework process for the QFN packages.

The rework process involves the following steps:

1. Component removal
2. Site redress
3. Solder paste application
4. Component placement
5. Component attachment

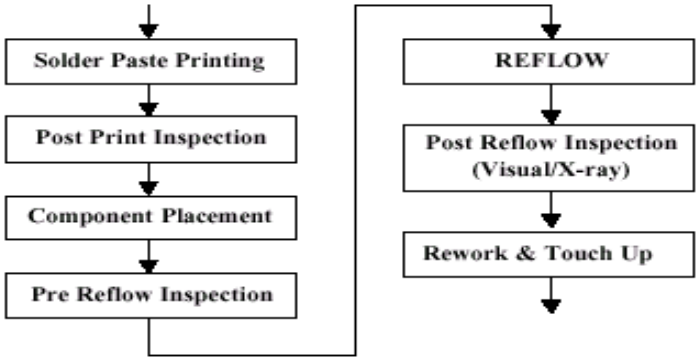


Figure 66: Typical PCB Mounting Process Flow

Table 61: Typical Reflow Profile(Lead Free): J-STD-020C

Profile Feature	Lead Free SMD
Average ramp up rate(Ts_{max} to T_p)	3°C/s Max.
Preheat	
• Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (Ts_{max} to Ts_{min})	• 150°C • 200°C • 60 to 180 seconds
Time maintained above	
• Temperature(T_L) • Time(t_L)	• 217°C • 60 to 150 seconds
Peak/Classification temperature (T_p)	260°C
Time within 5°C of peak temperature(tp)	20 to 40 seconds
Ramp down rate	6°C/s Max.
Time from 25°C to peak temperature	8 minutes Max.

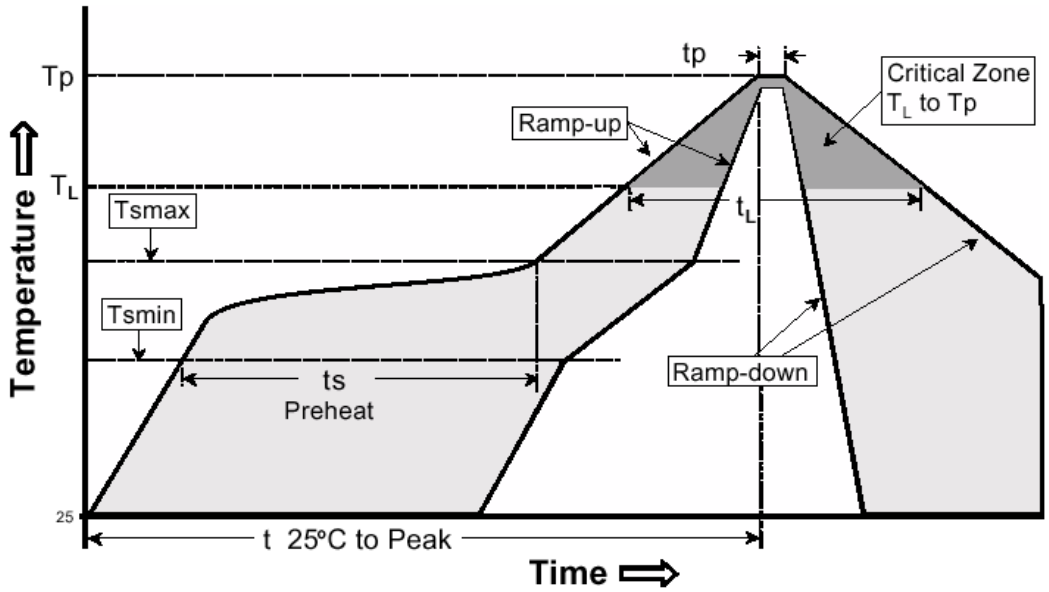


Figure 67: Reflow Condition

12 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's Customer Support at https://support.dialog-semiconductor.com/wifi or your local sales representative.

Table 62: Ordering Information (Samples)

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA16200-00000A32	QFN48	6 × 6	Reel	100/500
DA16200-00000F22	fcCSP72	3.8 × 3.8	Reel	100/500

Table 63: Ordering Information (Production)

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA16200-00000A32	QFN48	6 × 6	Reel	3000
DA16200-00000F22	fcCSP72	3.8 × 3.8	Reel	4000

Part Number Legend:3

DA16200-RRXXXYYZ

RR: Chip revision number

XXX: variant (000: No Flash)

YY: package code (A3: QFN48, F2: fcCSP72)

Z: packing method (1: Tray, 2: Reel, A: Mini-Reel)

Revision History

Revision	Date	Description
3.1	15-May-2020	Non NDA version
3.0	26-Mar-2020	Final release
2.9	11-Feb-2020	[9] Feature, Wi-Fi Alliance certification: Detailed added [10] Chaptor 5.4.1 and 5.4.2 measurement condition CH1 added [11] Chaptor 9.10.1 RS-232 added [12] Chaptor 9.10.3 Hardware Flow Control added [13] Chaptor 9.10.4 Interrupts added [14] Table 3 Pin Multiplexing changed [15] Chaptor 11.1 MSL added [16] Figure 54. DA16200 fcCSP Package Top view added [17] Application circuit (QFN, fcCSP) BOM changed [18] Feature deleted : DPD function support [19] Rx and Tx min/max value added for the QFN package (Table 8 and Table 10) [20] Rx and Tx min/max value added for the fcCSP package (Table 9 and Table 11) [21] **Table 12** and **Table 14** updated [22] ESD ratings added for the QFN and fcCSP packages in Table 15 and Table 16
2.3	5-Sep-2019	[23] Pin name "RTC_SEN_OUT" changed to "RTC_GPO" [24] Pull-down resistor added in Figure50, Figure51, Figure52 [25] QFN48 package "RTC_WAKE_UP" & "RTC_WAKE_UP2" [26] fcCSP72 package "RTC_WAKE_UP" [27] Ordering information sample and production pack quantity updated [28] Application circuit revised in QFN & fcCSP package [29] RTC_WAKE_UP pull down resistor added
2.2	12-Aug-2019	[30] Added Figure 65: DA16200 72-Pin fcCSP Land Pattern [31] AC characteristics and current consumption of fcCSP data updated in Table 9, Table 11, and **Table 13** [32] Ordering information added
2.1	30-Jul-2019	[33] Added "3.8 mm × 3.8 mm, 0.4 mm pitch, 72-Pin, fcCSP" in package type in key features [34] Added Figure 5, Figure 8, and Figure 10 [35] Added pin numbers for fcCSP package in Table 1, Table 22, Table 27, Table 29, Table 33, Table 35, Table 37, Table 39, Table 41, Table 43, Table 47, Table 50, and Table 54 [36] Added "GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD" in the description of Pin13/M8 in Table 1 [37] Added "GPIOA0~GPIOA11" in the description of Pin35/C1 in Table 1 [38] Added "fcCSP GND Pin A1,A9,B6,B10,B12,C7,C9,C11,D8,D10,F6,F8,F10,F12,G5,G7,G9,H4,H8,H10,J3,K2,L5,M6,M12,E5" in Table 1 [39] In Table 3 SPI master contents updated [40] Added information on fcCSP pins in section 5.1 and 5.2 [41] Added Table 9, Table 11, and **Table 13** [42] Added section 10.3 [43] Updated section 11.1 to include information on fcCSP [44] Added section 11.4 [45] Changed the caption of Table 21 to "OTP Map"

Revision	Date	Description
2.0	03-Jul-2019	Preliminary datasheet

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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