Voltage mode SEPIC evaluation kit

TLD5099EP

About this document

Product description

The TLD5099EP is an AEC qualified DC/DC boost controller.

- Built in diagnosis and protection features
- ENABLE control pin available
- Spread spectrum modulator to improve the EMI performance

Scope and purpose

Scope of this user manual is to provide to the audience instructions on usage of TLD5099EP voltage-mode SEPIC evaluation board.

Intended audience

This document is intended for engineers who need to perform measurements and check performance with TLD5099EP voltage-mode SEPIC evaluation board.

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1 Description

Evaluation board for medium power application with TLD5099EP configured in voltage-mode SEPIC topology. It can be implemented as a DC/DC power supply with constant voltage output.

Default configuration of the board is voltage-mode SEPIC topology without any additional features enabled. In this configuration, it can deliver up to 12 W to the load with an efficiency above 85%. Auxiliary circuits to protect the DC/DC and the load during short to ground, forcing the current to zero, are not present. The short to ground current is limited to about 3.6 A because of the SWCS pin connected to the current-mode shunt that acts as a rough limiter.

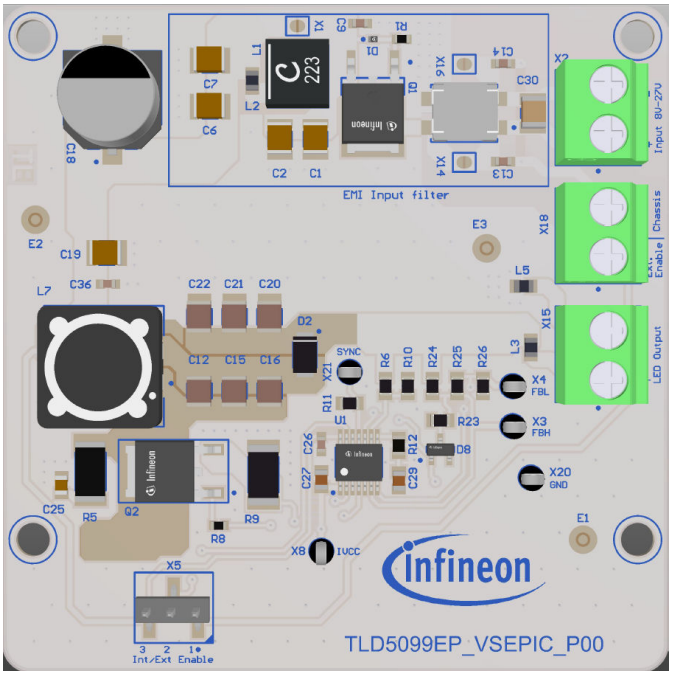

Figure 1 Board picture

1 Description

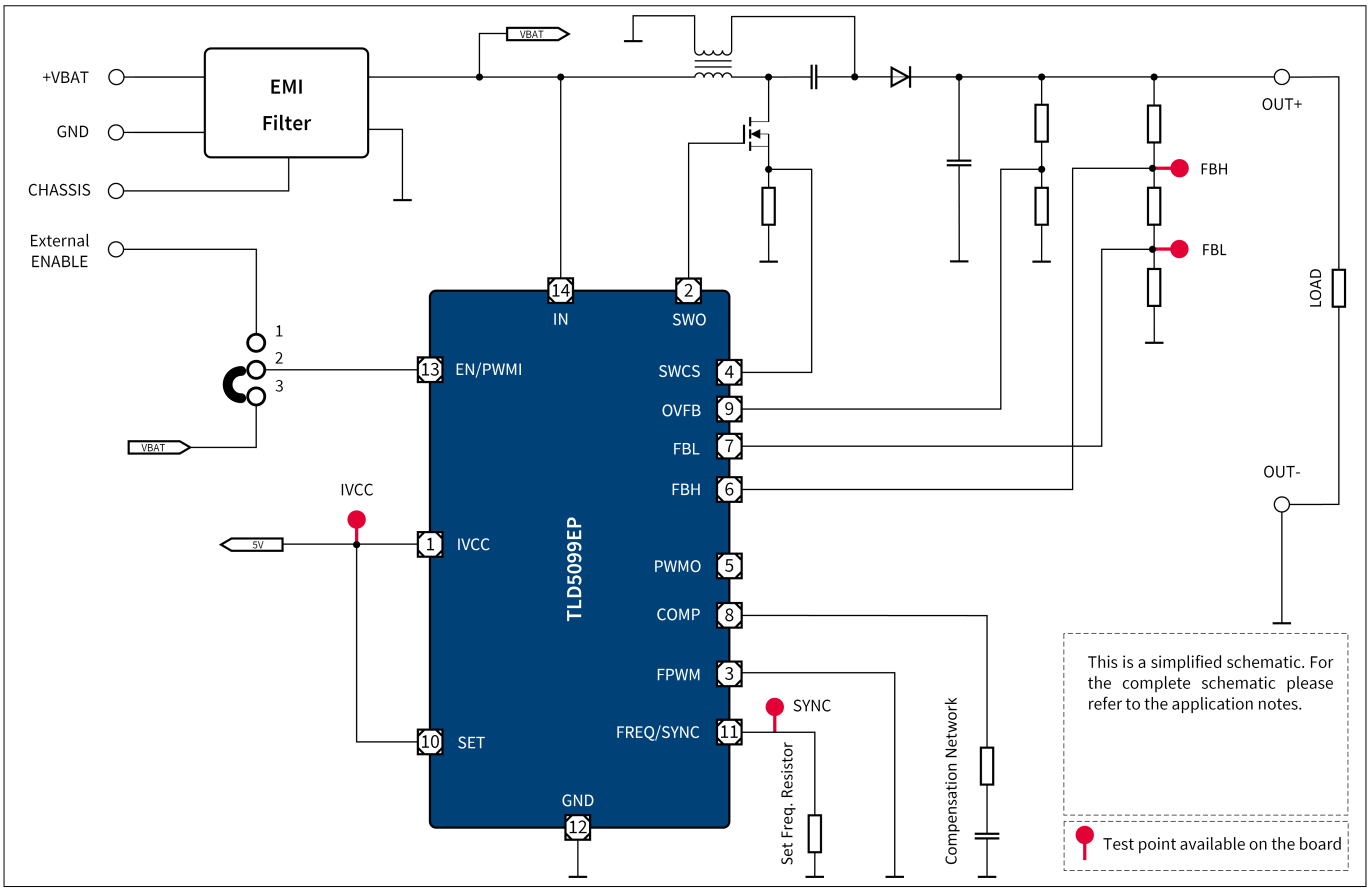

Figure 2 Simplified schematic

Table 1 Performance summary

Parameter	Conditions	Value
Input supply voltage	Parameter degradation below 6.5 V	8 V to 27 V Down to 6.5 V for less than 2 s
Maximum output current	Resistive load	1 A
Switching frequency	V_{IN} = 13.2 V; spread spectrum "on"	400 kHz
Efficiency	Measured with a 12 Ω power resistor as load	> 85%
Output voltage range	Output voltage related to ground	12 V
Output overvoltage protection	Output voltage related to ground	16 V

2 Quick start procedure

The default configuration of the board has all additional features disabled. Jumper is positioned in 1-2 position.

In this configuration, ENABLE signal has to be applied on X18 (max 45 V). If another output voltage is required, the voltage divider composed of R24, R25, R26 must be changed according to the rule that a 300 mV dropout should be present across R25 when the desired voltage is present in the output.

The default configuration is depicted below:

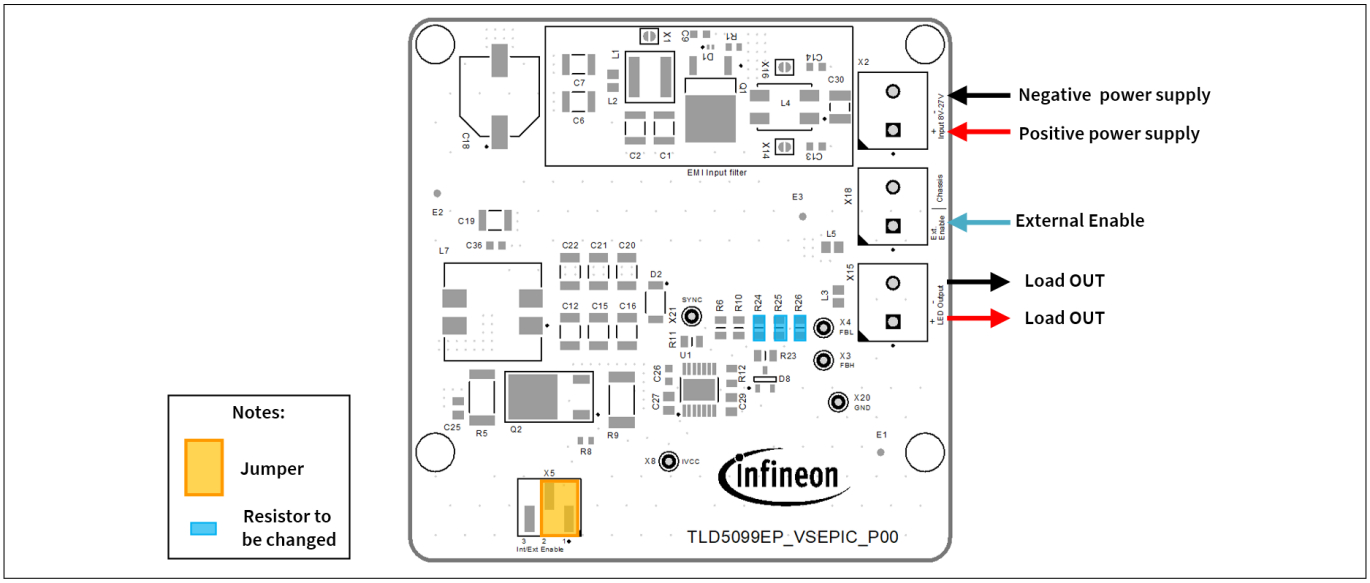

Figure 3 Default configuration of the board

3 Auto-enable configuration

By positioning the jumper on the position 2-3, an external enable signal to turn-on the device is no longer needed.

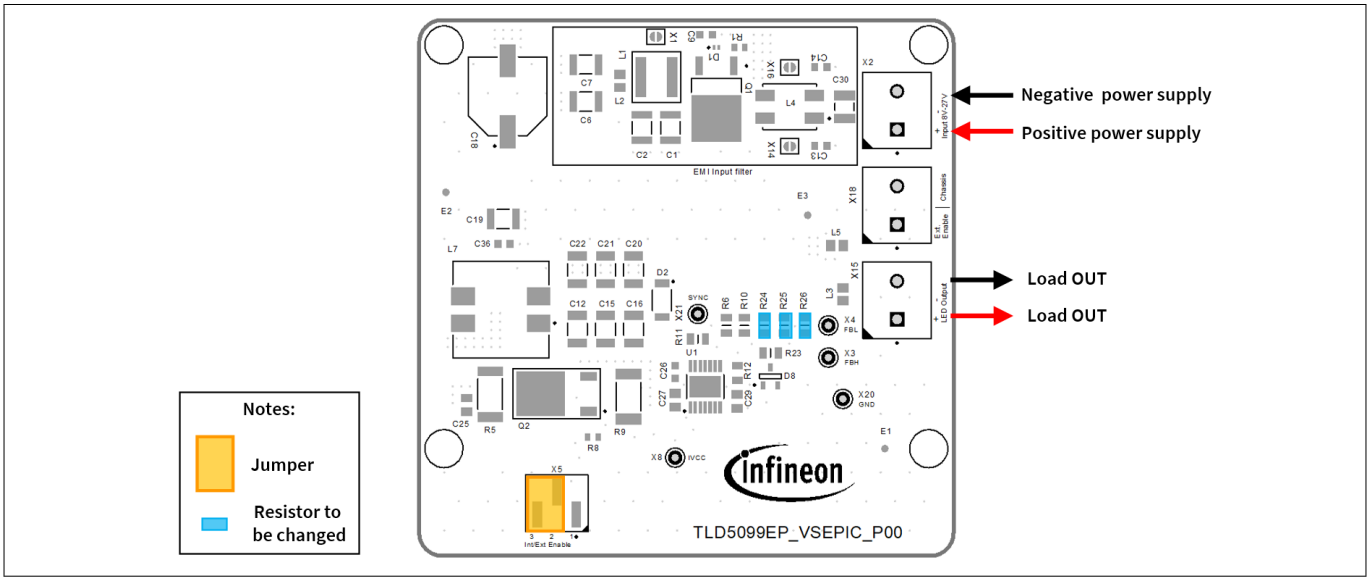

Figure 4 Current adjustment

4 Schematics

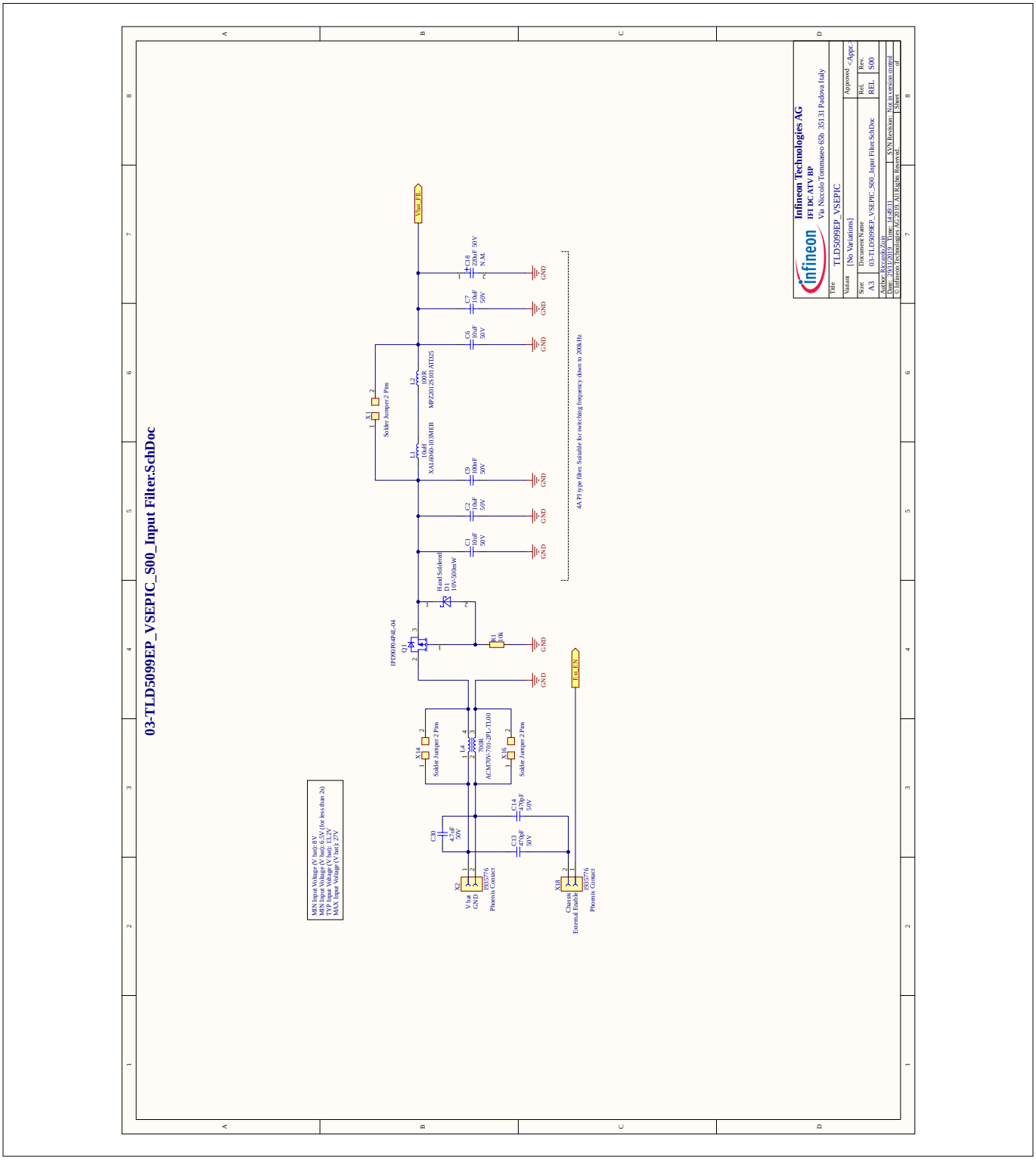

Figure 5 Input filter

4 Schematics

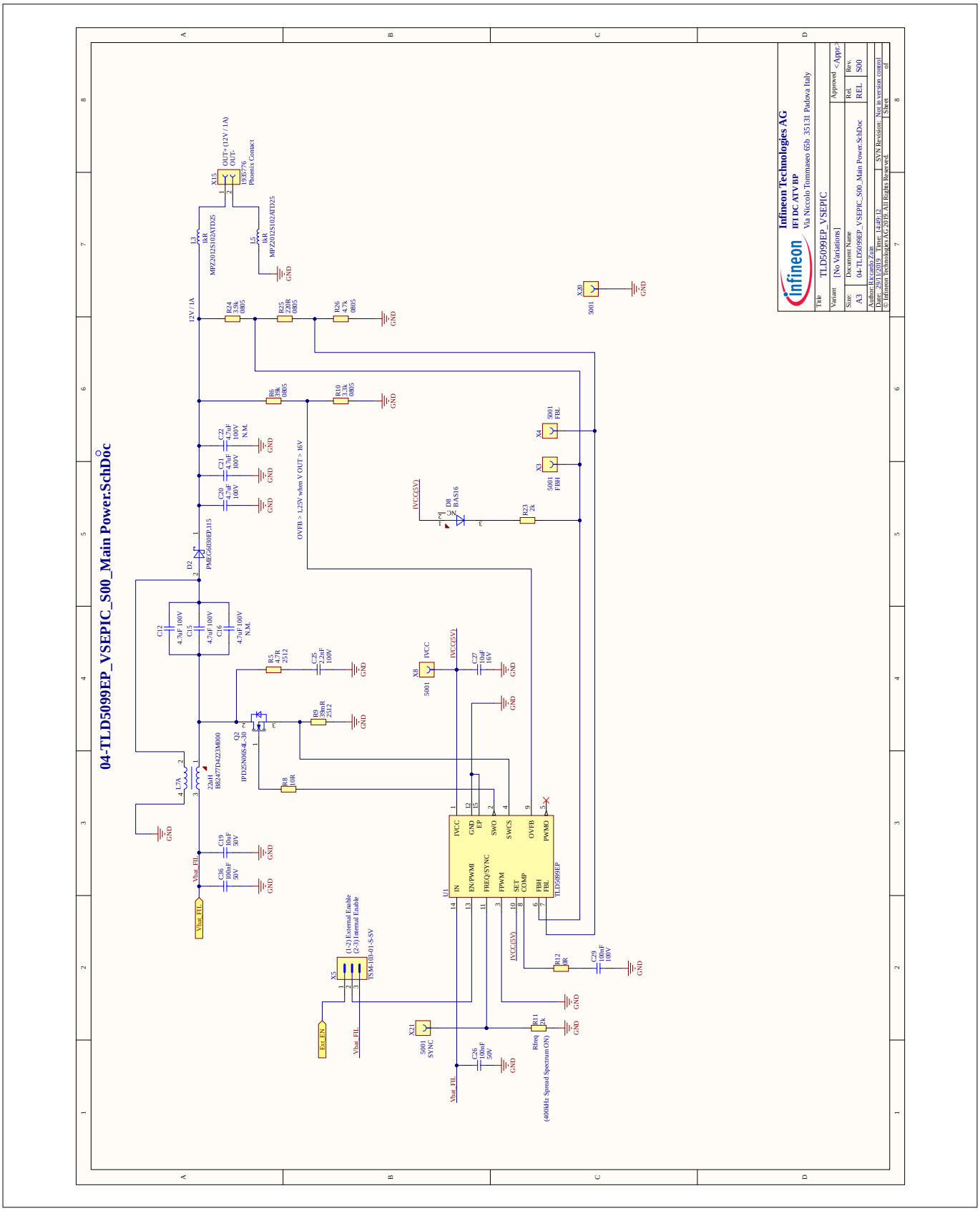

Figure 6 Main power

5 PCB layout

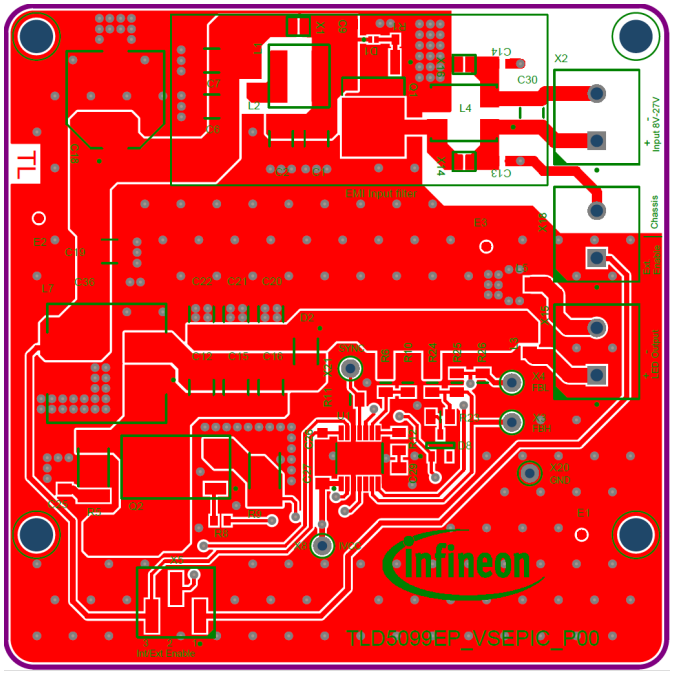

Figure 7 PCB layout top view

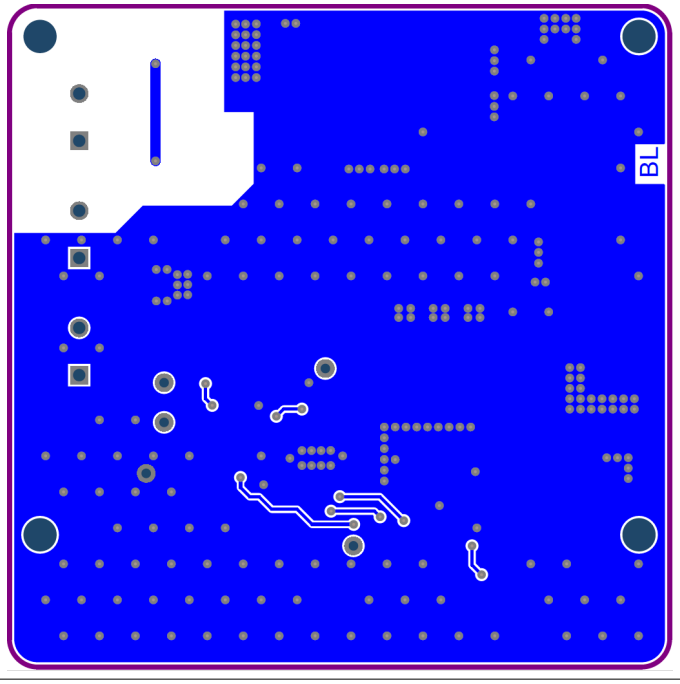

Figure 8 PCB layout bottom view

6 Bill of material

Table 2 Bill of material

Designator	Value	Manufacturer	Manufacturer order number
C1, C2, C6, C7, C19	10uF	muRata	GCM32EC71H106KA03
C9, C26, C36	100nF	AVX	06035C104K4Z2A
C12, C15, C20, C21	4.7uF	TDK	CGA6M3X7S2A475K200AE
C13, C14	470pF	muRata	GCM1885C1H471JA16
C16, C22	4.7uF	TDK	CGA6M3X7S2A475K200AE
C18	220uF	Panasonic	EEEFK1H221P
C25	2.2nF	MuRata	GCM2165C2A222FA16
C27	10uF	TDK	CGA4J1X7S1C106K125AC
C29	100nF	TDK	CGA4J2X7R2A104M125AE
C30	4.7uF	Kemet	C1210C475K5RACAUTO
D1	Zener 10V-500mW		
D2	PMEG6030EP,115	Nexperia	PMEG6030EP,115
D8	BAS16	Infineon Technologies	BAS16
L1	10uH	Coilcraft	XAL6060-103MEB
L2	100H	TDK Corporation	MPZ2012S101ATD25
L3, L5	1kH	TDK	MPZ2012S102ATD25
L4		TDK	ACM70V-701-2PL-TL00
L7	22uH	TDK Corporation	B82477D4223M000
Q1	IPD90P04P4L-04	Infineon Technologies	IPD90P04P4L-04
Q2	IPD25N06S4L-30	Infineon Technologies	IPD25N06S4L-30
R1	10kΩ	Vishay	CRCW060310K0FK
R5	4.7Ω	Vishay	CRCW25124R70FK
R6	39kΩ	Vishay	CRCW080539K0FK
R8	10Ω	Vishay	CRCW060310R0FK
R9	39mΩ	Vishay	WSL2512R0390FEA
R10	3.3kΩ	Vishay	CRCW08053K30FK
R11	2kΩ	Vishay	CRCW08052K00FK
R12	0Ω	Yageo	AC0805JR-070RL
R23	2kΩ	Vishay	CRCW08052K00FK
R24	3.9kΩ	Vishay	CRCW08053K90FK
R25	220Ω	Vishay	CRCW0805220RFK
R26	4.7kΩ	Vishay	CRCW08054K70FK
U1	TLD5099EP	Infineon Technologies	TLD5099EP
X1, X14, X16	Solder Jumper 2 Pins	Infineon Technologies AG	Solder Jumper 2 Pins

6 Bill of material

Table 2 Bill of material (continued)

Designator	Value	Manufacturer	Manufacturer order number
X2, X15, X18	1935776	Phoenix Contact	1935776
X3, X4, X8, X20, X21	5001	Keystone	5001
X5	TSM-103-01-S-SV	Samtec	TSM-103-01-S-SV

7 Efficiency measurements

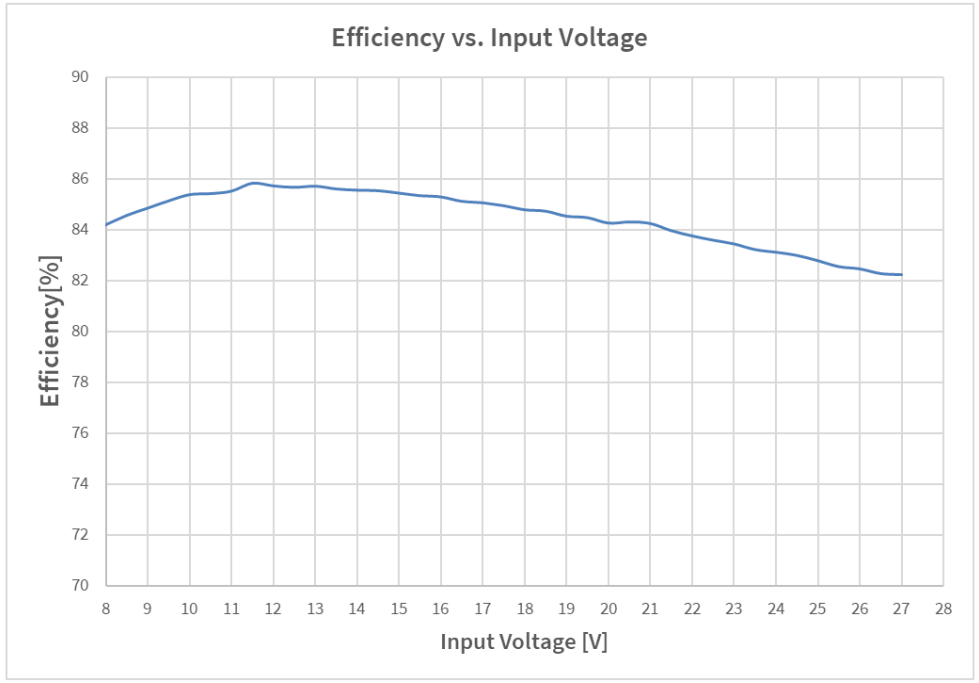

Figure 9 Efficiency vs. input voltage

This efficiency performance has been obtained with:

Table 3 Parameters influencing efficiency

Output load:	12 Ω power resistor
EMI filter:	Totally bypassed by closing the jumpers X1, X14 and X16

Efficiency performances can be increased: refer to ***Chapter 8***.

8 Maximizing efficiency

This evaluation board has been designed to reach a fair compromise between efficiency performance and EMI emissions compliance.

Nevertheless, if the maximum efficiency is needed, the following actions should be considered:

1. Remove the snubber circuit R5, C25 or choose a lower value for the capacitor C25 (for example 1 nF)
2. Bypass the whole EMI filter, by bridging the jumpers X1, X14 and X16
3. Bypass the output ferrite beads L3 and L5
4. Replace the main inductor L6 with one that boasts a lower parasitic DC resistance, for example
   - TDK model B82477C6223M603
   - TDK model B82477D6223M603
5. Bypass gate resistor R8

9 Minimizing EMI emissions

This evaluation board has been designed to reach a fair compromise between efficiency performance and EMI emissions compliance. Furthermore, this evaluation board can fulfill the class V of the CISPR25 in conducted emissions from 150 kHz to 108 MHz.

Nevertheless, if the minimum EMI emission is required, the following actions should be considered:

1. Choose a higher value for the capacitor C25 (for example 3.3 nF)
2. Include the whole EMI filter by removing bridges from the jumpers X1, X14 and X16
3. Replace the 10 Ω resistor R8 with a higher value such as 22 Ω or 33 Ω
4. With a short piece of wire connect the CHASSIS TERMINAL to the test ground plane as close as possible to where the board is placed

10 Revision history

Table 4 Revision history

Document version	Date of release	Description of changes
Rev. 1.00	2020-01-29	First release related to evalboard S00_P00.

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