



Product Change Notification - SYST-19IGCU330

Date:

22 Jun 2020

Product Category:

P-Channel Enhancement Mode MOSFETs

Affected CPNs:**Notification subject:**

Data Sheet - TP2540 P-Channel Enhancement-Mode Vertical DMOS FET Data Sheet

Notification text:

SYST-19IGCU330

Microchip has released a new Product Documents for the TP2540 P-Channel Enhancement-Mode Vertical DMOS FET Data Sheet of devices. If you are using one of these devices please read the document located at [TP2540 P-Channel Enhancement-Mode Vertical DMOS FET Data Sheet](#).

Notification Status: Final**Description of Change:**

- 1) Converted Supertex Doc# DSFP-TP2540 to Microchip DS20006371A
- 2) Added a pin function tables
- 3) Changed the package marking format
- 4) Removed the 3-Lead TO-92 N3 P003, P005, P013, and P014 media types
- 5) Made minor text changes throughout the document.

Impacts to Data Sheet: None**Reason for Change:** To Improve Manufacturability**Change Implementation Status:** Complete**Date Document Changes Effective:** 22 Jun 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A**Attachment(s):**

[TP2540 P-Channel Enhancement-Mode Vertical DMOS FET Data Sheet](#)

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Affected Catalog Part Numbers (CPN)

TP2540N3-G

TP2540N3-G-P002

TP2540N8-G

TP2540N8-L-G

SYST-19IGCU330 - Data Sheet - TP2540 P-Channel Enhancement-
Mode Vertical DMOS FET Data Sheet

Affected Catalog Part Numbers(CPN)

TP2540N3-G

TP2540N3-G-P002

TP2540N8-G

TP2540N8-L-G

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- -2.4V Maximum Low Threshold
- High Input Impedance
- 60 pF Low Input Capacitance
- Fast Switching Speeds
- Low On-Resistance
- Free from Secondary Breakdown
- Low Input and Output Leakage

Applications

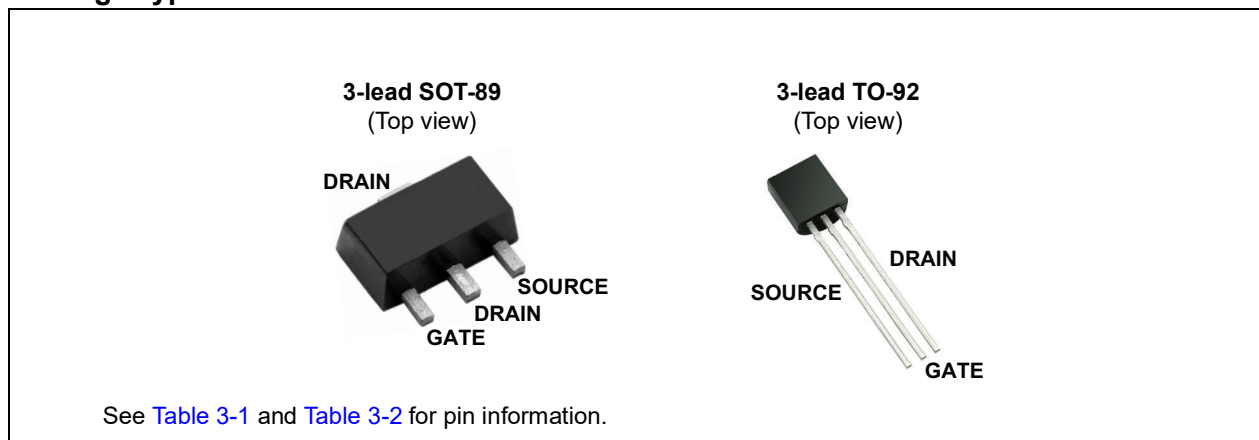
- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Battery-Operated Systems
- Photovoltaic Drives
- Analog Switches
- General Purpose Line Drivers
- Telecommunication Switches

General Description

The TP2540 low-threshold, Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type



TP2540

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	$\pm 20V$
Operating Ambient Temperature, T_A	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature, T_S	$-55^{\circ}C$ to $+150^{\circ}C$

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^{\circ}C$ unless otherwise specified. All DC parameters are 100% tested at $25^{\circ}C$ unless otherwise stated. Pulse test: 300 μs pulse, 2% duty cycle.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	-400	—	—	V	$V_{GS} = 0V, I_D = -2 \text{ mA}$
Gate Threshold Voltage	$V_{GS(th)}$	-1	—	-2.4	V	$V_{GS} = V_{DS}, I_D = -1 \text{ mA}$
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	4.8	mV/ $^{\circ}C$	$V_{GS} = V_{DS}, I_D = -1 \text{ mA}$ (Note 1)
Gate Body Leakage Current	I_{GSS}	—	—	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	-10	μA	$V_{GS} = 0V,$ $V_{DS} = \text{Maximum rating}$
		—	—	-1	mA	$V_{DS} = 0.8 \text{ Maximum rating},$ $V_{GS} = 0V, T_A = 125^{\circ}C$ (Note 1)
On-State Drain Current	$I_{D(ON)}$	-0.2	-0.3	—	A	$V_{GS} = -4.5V, V_{DS} = -25V$
		-0.4	-1.1	—	A	$V_{GS} = -10V, V_{DS} = -25V$
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	20	30	Ω	$V_{GS} = -4.5V, I_D = -100 \text{ mA}$
		—	19	25	Ω	$V_{GS} = -10V, I_D = -100 \text{ mA}$
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	0.75	%/ $^{\circ}C$	$V_{GS} = -10V, I_D = -100 \text{ mA}$ (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: $T_A = 25^\circ\text{C}$ unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	100	175	—	mmho	$V_{DS} = -25\text{V}$, $I_D = -100\text{ mA}$
Input Capacitance	C_{ISS}	—	60	125	pF	$V_{GS} = 0\text{V}$, $V_{DS} = -25\text{V}$, $f = 1\text{ MHz}$
Common-Source Output Capacitance	C_{OSS}	—	20	70	pF	
Reverse Transfer Capacitance	C_{RSS}	—	10	25	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	—	10	ns	$V_{DD} = -25\text{V}$, $I_D = -0.4\text{A}$, $R_{GEN} = 25\Omega$
Rise Time	t_r	—	—	10	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	—	20	ns	
Fall Time	t_f	—	—	13	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	-1.8	V	$V_{GS} = 0\text{V}$, $I_{SD} = -100\text{ mA}$ (Note 1)
Reverse Recovery Time	t_{rr}	—	300	—	ns	$V_{GS} = 0\text{V}$, $I_{SD} = -100\text{ mA}$

Note 1: Unless otherwise stated, all DC parameters are 100% tested at 25°C . Pulse test: 300 μs pulse, 2% duty cycle.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-55	—	+150	$^\circ\text{C}$	
Storage Temperature	T_S	-55	—	+150	$^\circ\text{C}$	
PACKAGE THERMAL RESISTANCE						
3-lead TO-92	θ_{JA}	—	132	—	$^\circ\text{C/W}$	
3-lead SOT-89	θ_{JA}	—	133	—	$^\circ\text{C/W}$	

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (mA)	Power Dissipation at $T_A = 25^\circ\text{C}$ (W)	I_{DR} (Note 1) (mA)	I_{DRM} (mA)
3-lead TO-92	-86	-600	0.74	-86	-600
3-lead SOT-89	-125	-1200	1.6 (Note 2)	-125	-1200

Note 1: I_D (continuous) is limited by maximum rated T_J .

2: Mounted on an FR5 board, 25 mm x 25 mm x 1.57 mm

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

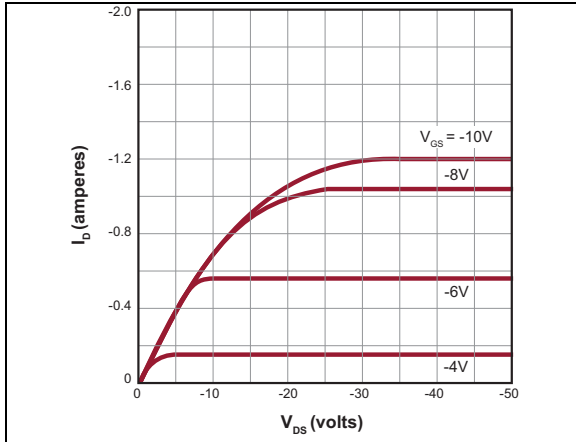


FIGURE 2-1: Output Characteristics.

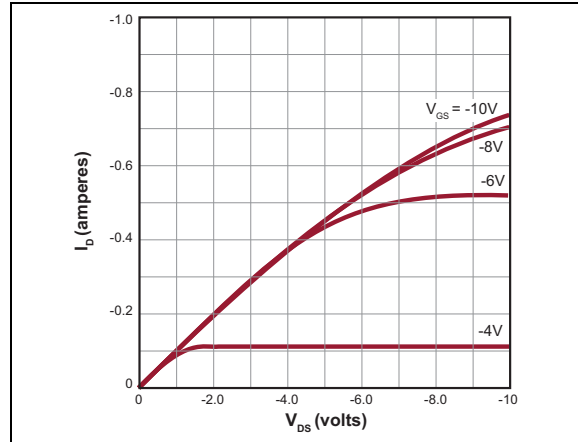


FIGURE 2-4: Saturation Characteristics.

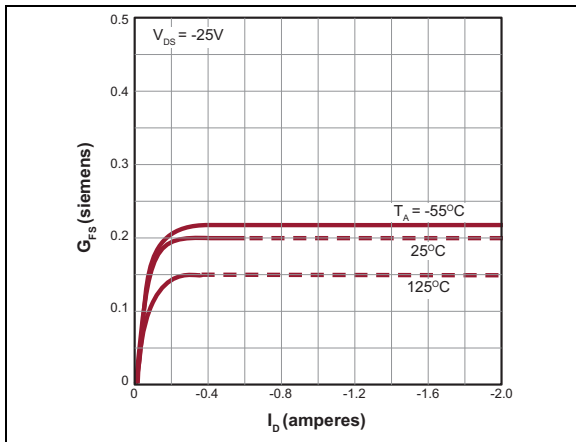


FIGURE 2-2: Transconductance vs. Drain Current.

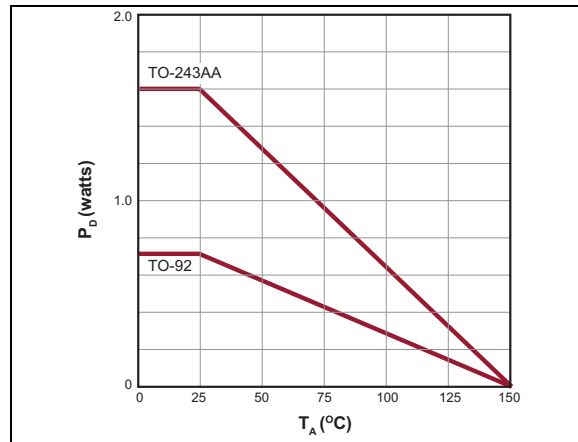


FIGURE 2-5: Power Dissipation vs. Ambient Temperature.

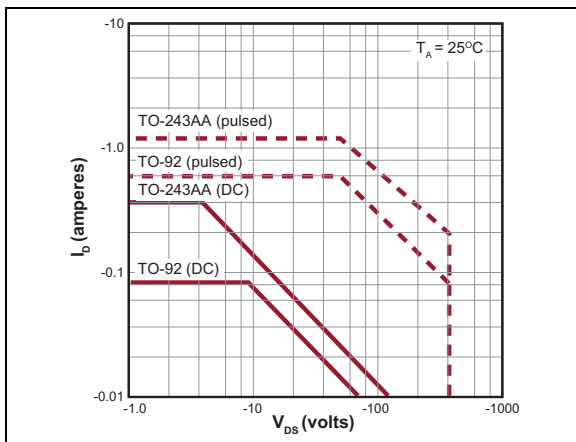


FIGURE 2-3: Maximum Rated Safe Operating Area.

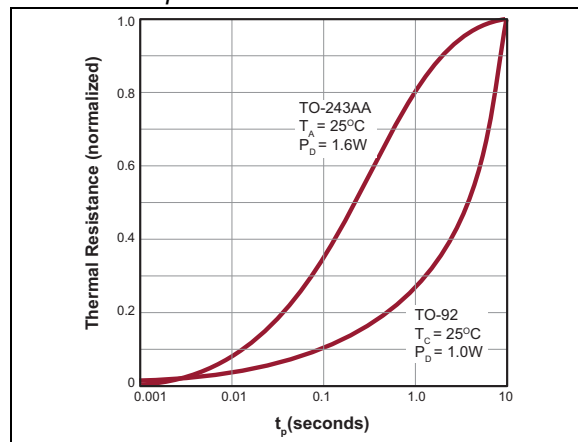


FIGURE 2-6: Thermal Response Characteristics.

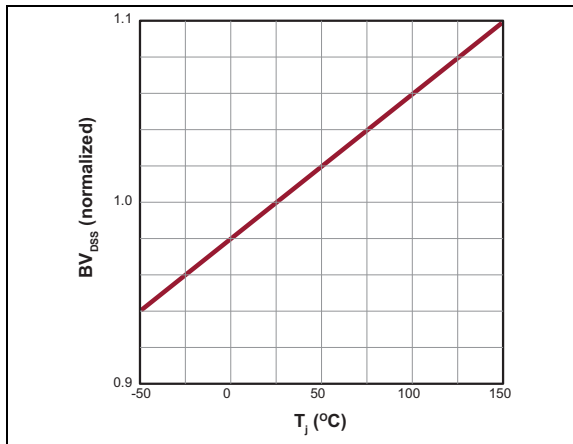


FIGURE 2-7: BV_{DSS} Variation with Temperature.

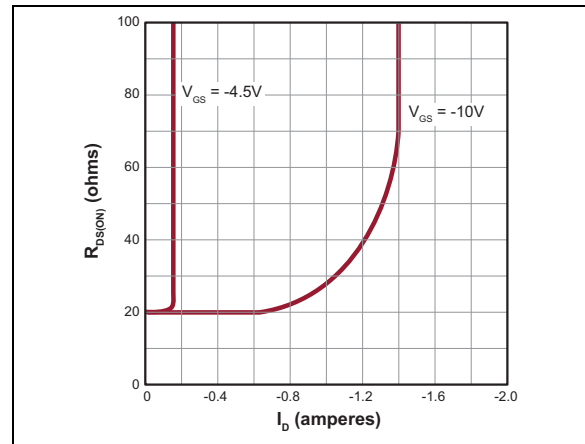


FIGURE 2-10: On-Resistance vs. Drain Current.

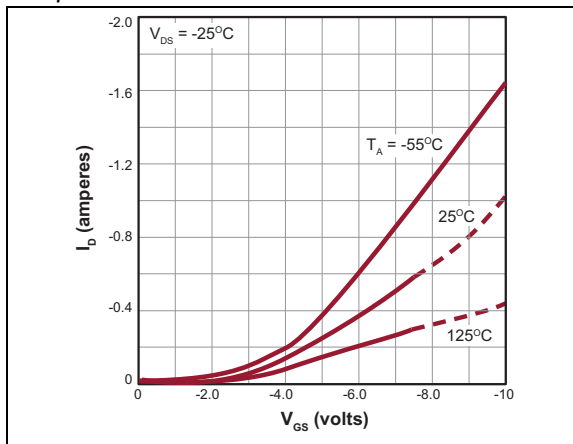


FIGURE 2-8: Transfer Characteristics.

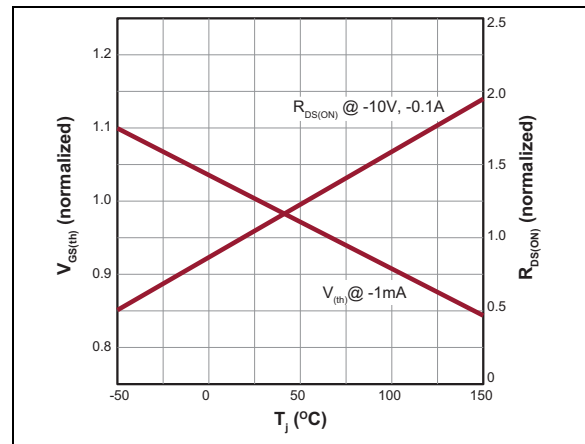


FIGURE 2-11: $V_{GS(th)}$ and R_{DS} Variation with Temperature.

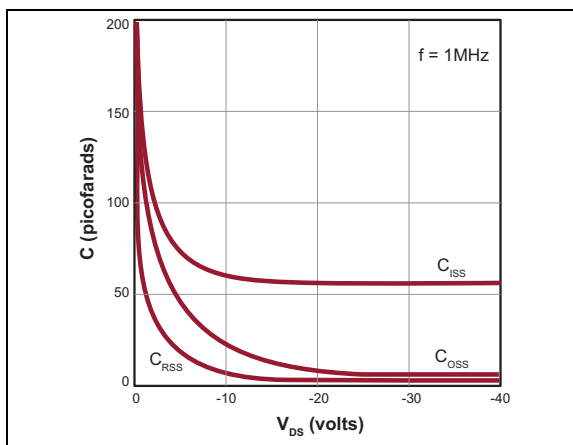


FIGURE 2-9: Capacitance vs. Drain-to-Source Voltage.

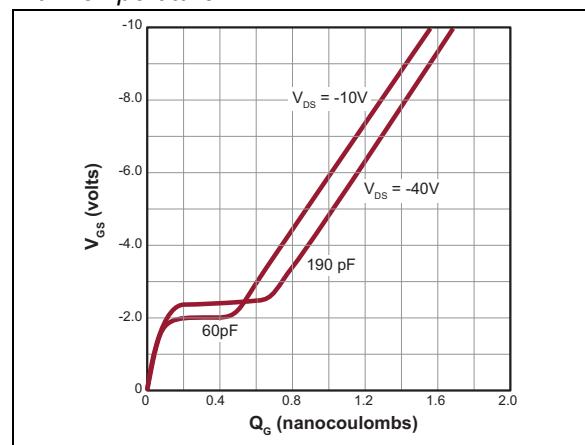


FIGURE 2-12: Gate Drive Dynamic Characteristics.

TP2540

3.0 PIN DESCRIPTION

The details on the pins of TP2540 TO-92 and SOT-89 packages are listed in [Table 3-1](#) and [Table 3-2](#), respectively. Refer to [Package Type](#) for the location of pins.

TABLE 3-1: TO-92 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Source	Source
2	Gate	Gate
3	Drain	Drain

TABLE 3-2: SOT-89 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2,4	Drain	Drain
3	Source	Source

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for the TP2540.

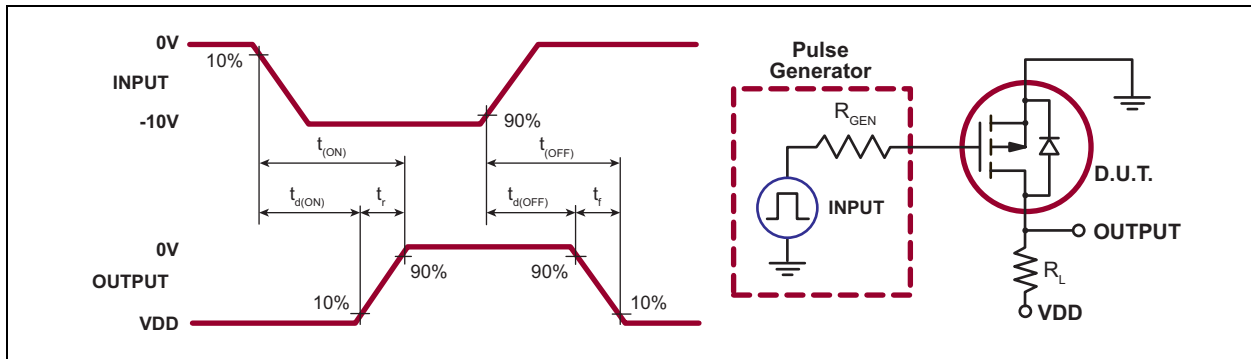


FIGURE 4-1: Switching Waveforms and Test Circuit.

TABLE 4-1: PRODUCT SUMMARY

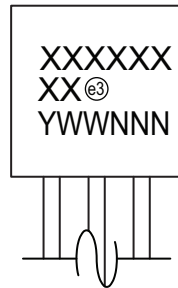
BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$V_{GS(TH)}$ (Maximum) (V)	$I_{D(ON)}$ (Minimum) (A)
-400	25	-0.4	-2.4

TP2540

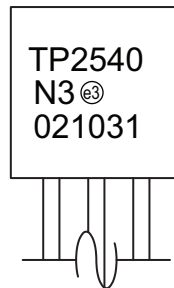
5.0 PACKAGE MARKING INFORMATION

5.1 Package Marking Information

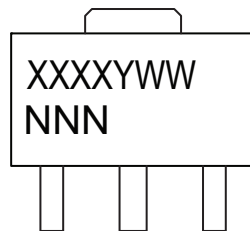
3-lead TO-92



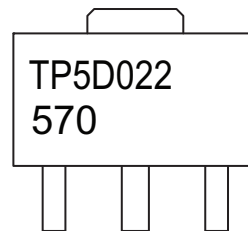
Example



3-lead SOT-89

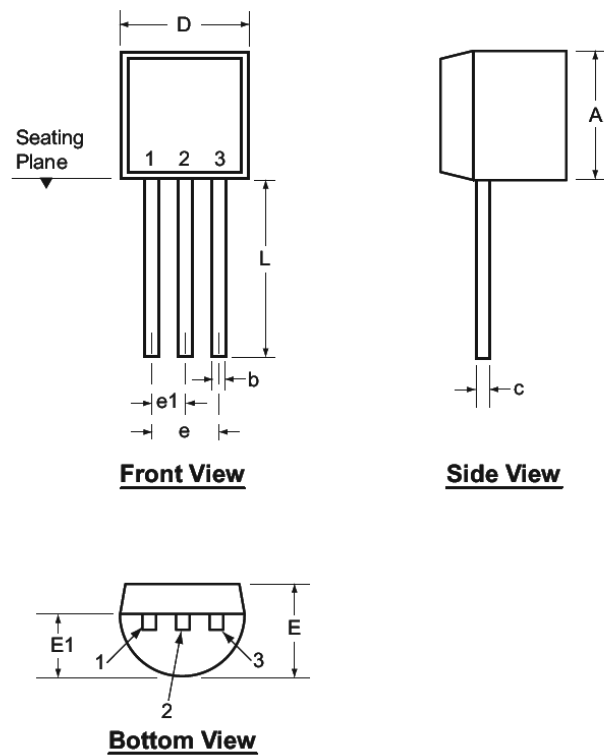


Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

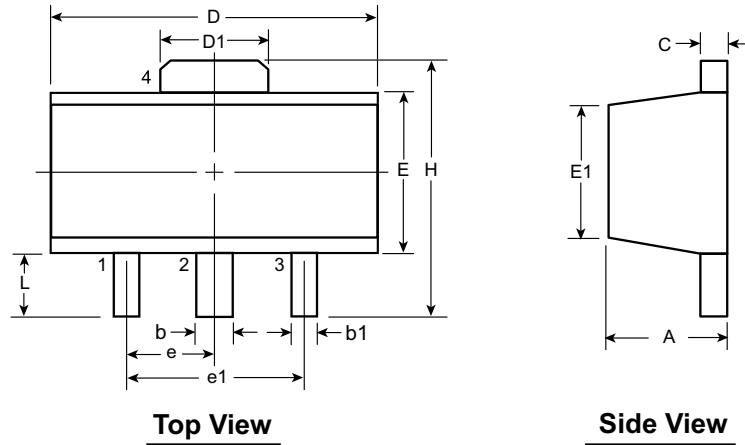
* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

TP2540

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol	A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 [†]	1.50 BSC	3.00 BSC	3.94	0.73 [†]	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

[†] This dimension differs from the JEDEC drawing

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (June 2020)

- Converted Supertex Doc# DSFP-TP2540 to Microchip DS20006371A
- Added a pin function tables
- Changed the package marking format
- Removed the 3-Lead TO-92 N3 P003, P005, P013, and P014 media types
- Made minor text changes throughout the document

TP2540

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>		<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device		Package Options		Environmental		Media Type
Device:	TP2540	=		P-Channel Enhancement-Mode Vertical DMOS FET		
Packages:	N3	=		3-lead TO-92		
	N8	=		3-lead SOT-89		
Environmental:	G	=		Lead (Pb)-free/RoHS-compliant Package		
Media Types:	(blank)	=		1000/Bag for an N3 Package		
	(blank)	=		2000/Reel for an N8 Package		
	P002	=		2000/Reel (Reverse T/R) for an N8 Package		

Examples:	
a) TP2540N3-G:	P-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead TO-92, 1000/Bag
b) TP2540N8-G:	P-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead SOT-89, 2000/Reel
c) TP2540N8-G-P002:	P-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead SOT-89, 2000/Reel (Reverse T/R)

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