Innovative Service Around the Globe YAGEO

DATA SHEET

SURFACE-MOUNT CERAMIC MULTILAYER CAPACITORS

C-Array: Class 1, NP0

50 V

size 0612 (4 × 0603)

Phycomp

Product Specification – Jul 18, 2003 V.7

Surface-mount ceramic multilayer capacitors

C Array: Class 1, NP0 50 V size 0612 (4 × 0603)

FEATURES

- 4 × 0603 capacitors (of the same capacitance value) per array
- Less than 50% board space of an equivalent discrete component
- High volumetric efficiency
- Dense dielectric layers
- Supplied in tape on reel
- Increased throughput by time saved in mounting
- Cost savings on manufacturing time.

APPLICATIONS

- Professional electronics
- High density consumer electronics
- Automotive.

DESCRIPTION

Each capacitor element consists of a rectangular block of ceramic dielectric in which a number of interleaved precious metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two terminations, silver dipped with a barrier layer of plated nickel and finally covered with a layer of plated tin (NiSn). An outline of the structure is shown in Fig.1.

QUICK REFERENCE DATA

DESCRIPTION	VALUE
Rated voltage U_R (DC)	50 V (IEC)
Capacitance range (E12 series)	10 pF to 1 nF
Tolerance on capacitance	±5%, ±10%
Test voltage (DC) for 1 minute	2.5 × U_R
Sectional specifications	IEC 60384-10, second edition 1989-04; also based on CECC 32 100
Detailed specification	based on CECC 32 101-801
Climatic category (IEC 60068)	55/125/56

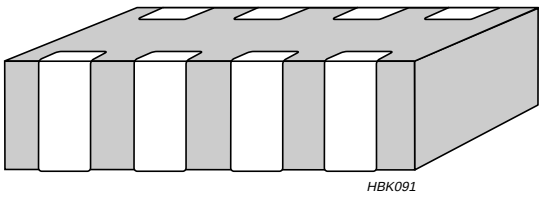
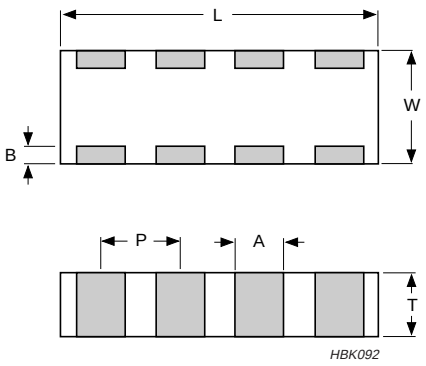


Fig.1 Simplified outline.

Surface-mount ceramic multilayer capacitors

C Array: Class 1, NP0 50 V size 0612 (4 × 0603)

MECHANICAL DATA



For dimensions see Table 1.

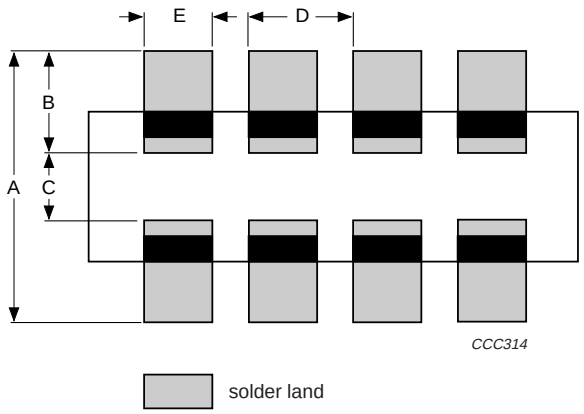
Fig.2. Dimensional outline.

Physical dimensions

Table 1 Capacitor dimensions; see Fig.2

CASE SIZE	L	W	T	A	B	P
Dimensions in millimetres						
0612 (4 × 0603)	3.2 ±0.15	1.60 ±0.15	0.80 ±0.10	0.40 ±0.10	0.30 ±0.20	0.80 ±0.10
Dimensions in inches						
0612 (4 × 0603)	0.126 ±0.006	0.063 ±0.006	0.032 ±0.004	0.016 ±0.004	0.012 ±0.008	0.031 ±0.004

DIMENSIONS OF SOLDER LANDS



For dimensions see Table 2.

Fig.3 Recommended dimensions of solder lands.

Table 2 Solder land dimensions; see Fig.3

CASE SIZE	FOOTPRINT DIMENSIONS (mm)				
	A	B	C	D	E
0612 (4 × 0603)	2.54 ±0.15	0.89 ±0.10	0.76 ±0.10	0.80 ±0.10	0.45 ±0.10

SELECTION CHART FOR 50 V

C (pF)	LAST TWO DIGITS OF 12NC	50 V
		0612 (4 × 0603)
10	23	
12	24	
15	25	
18	26	
22	27	
27	28	
33	29	
39	31	
47	32	
56	33	
68	34	
82	35	
100	36	0.8 ±0.1
120	37	
150	38	
180	39	
220	41	
270	42	
330	43	
390	44	
470	45	
560	46	
680	47	
820	48	
1 000	49	

Note

1. Values in shaded cells indicate thickness class.

Thickness classification and packing quantities

THICKNESS CLASSIFICATION (mm)	8 mm TAPE WIDTH QUANTITY PER REEL
	∅180 mm; 7"
	PAPER
0.8 ±0.1	4 000

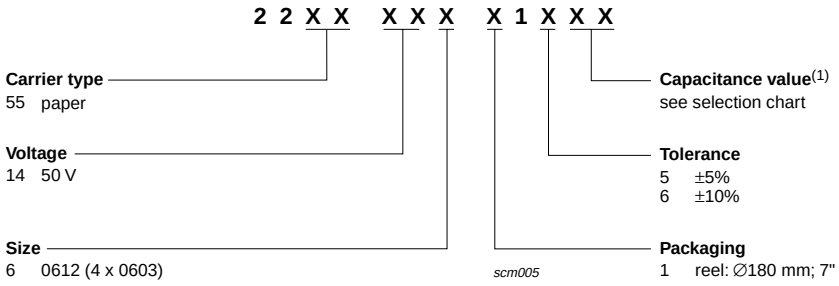
Surface-mount ceramic multilayer capacitors

C Array: Class 1, NP0 50 V size 0612 (4 × 0603)

ORDERING INFORMATION

Components may be ordered by using either a Phycomp's unique 12NC or simple 15-digit clear text code.

Ordering code 12NC (preferred)



(1) Quantity on reel depends on thickness classification, see section "Thickness classification and packing quantities".

Clear text code

Example: 0612CG102J9B200

Size Code	Temp. Char.	Capacitance	Tol.	Vol.	Termination	Packing	Marking	Series
0612 (4 × 0603)	CG = NP0	102 = 1000 pF; the third digit signifies the multiplying factor: 0 = × 1 1 = × 10 2 = × 100	J = ±5% K = ±10%	9 = 50 V	B = NiSn	2 = 180 mm; 7" paper	0 = no marking	0 = conv. ceramic

ELECTRICAL CHARACTERISTICS

Class 1 capacitors; NP0 dielectric; NiSn terminations

Unless otherwise stated all electrical values apply at an ambient temperature of 20 ±1 °C, an atmospheric pressure of 86 to 106 kPa, and a relative humidity of 63 to 67%.

DESCRIPTION	VALUE
Capacitance range (E12 series); note 1	10 pF to 1 nF
Tolerance on capacitance after 1000 hours	±5%; 10%
Test voltage (DC) for 1 minute	$2.5 \times U_R$
Tan δ; note 1	$\leq$ 0.1%
Insulation resistance after 1 minute at U_R (DC):	$R_{ins} \geq 100$ GΩ
Temperature coefficient	$(0 \pm 30) \times 10^{-6}$/K

Note

1. Measured at 1 V, 1 MHz for C ≤ 1000 pF and at 1 V, 1 kHz for C > 1000 pF, using a four-gauge method.

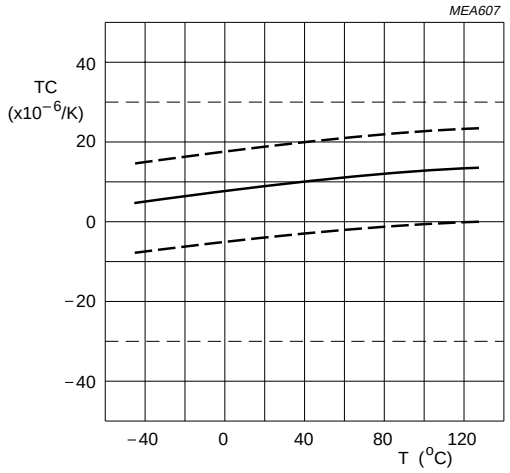


Fig.4 Typical temperature coefficient as a function of temperature.

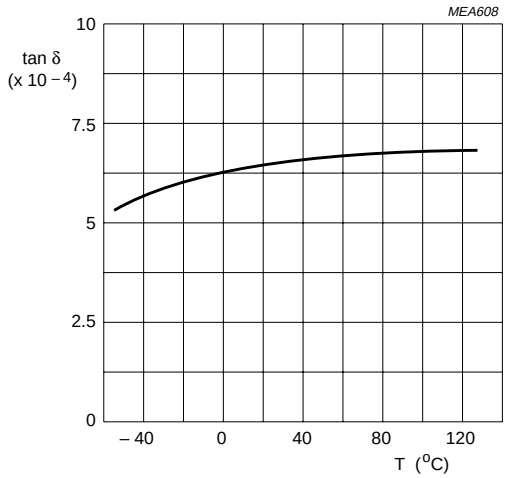


Fig.5 Typical tan δ as a function of temperature.

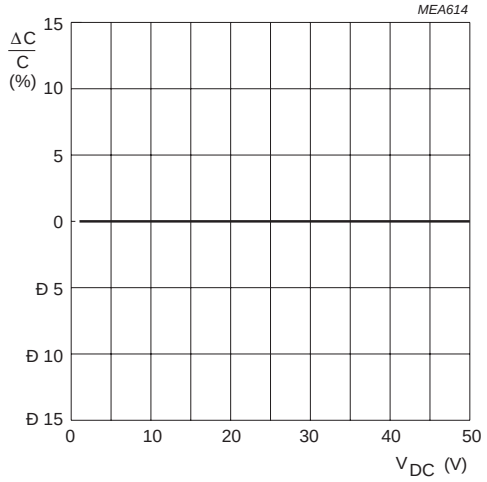


Fig.6 Typical capacitance change with respect to the capacitance at 1 V as a function of DC voltage.

TESTS AND REQUIREMENTS

Table 3 Test procedures and requirements

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.4		mounting	the capacitors may be mounted on printed-circuit boards or ceramic substrates by applying wave soldering, reflow soldering (including vapour phase soldering) or conductive adhesive	no visible damage
4.5		visual inspection and dimension check	any applicable method using ×10 magnification	in accordance with specification
4.6.1		capacitance (measured 1000 hours after date of manufacture)	f = 1 kHz; measuring voltage 1 V_{rms} at 20 °C	within specified tolerance
4.6.2		tan δ	f = 1 kHz; measuring voltage 1 V_{rms} at 20 °C	in accordance with specification
4.6.3		insulation resistance	at U_R (DC) for 1 minute	in accordance with specification
4.6.4		voltage proof	2.5 × U_R for 1 minute	no breakdown or flashover
4.7.1		temperature coefficient	between minimum and maximum temperature	in accordance with specification
4.8		adhesion	a force of 5 N applied for 10 s to the line joining the terminations and in a plane parallel to the substrate	no visible damage
4.9		bond strength of plating on end face	mounted in accordance with IEC 60384 10, paragraph 4.4 conditions: bending 1 mm at a rate of 1 mm/s, radius jig 340 mm	no visible damage $\Delta C/C$: ≤10%
4.10	Tb	resistance to soldering heat; jig clamps to the second component in the longitudinal line	260 ±5 °C for 10 ±0.5 s in a static solder bath	the terminations shall be well tinned after recovery $\Delta C/C$: ±10%
		resistance to leaching; jig clamps to the second component in the longitudinal line	260 ±5 °C for 30 ±1 s in a static solder bath	using visual enlargement of ×10, dissolution of the terminations shall not exceed 10%

IEC 60384-10/ CECC 32 100 CLAUSE	IEC 60068-2 TEST METHOD	TEST	PROCEDURE	REQUIREMENTS
4.11	Ta	solderability; jig clamps to the second component along the longitudinal line	zero hour test, and test after storage (20 to 24 months) in original packing in normal atmosphere; unmounted chips completely immersed for 2 ±0.5 s in a solder bath at 235 ±5 °C	the terminations shall be well tinned
4.12	Na	rapid change of temperature	Preconditioning: between minimum and maximum temperature, 5 cycles	no visible damage after 24 hours recovery; Δ°C/C: ≤15%
4.14	Ca	damp heat	Preconditioning: 56 days at 40 °C; 90 to 95% RH; U_R applied	after 48 hours recovery: Δ°C/C: ±15% tan δ: 7% R_{ins}: 1000 MΩ or $R_iC_R \geq 25$ s, whichever is less
4.15		endurance	Preconditioning: (thermal treatment) 2 × U_R at 125 °C for 1000 hours, recovery 48 ±4 hours at room temperature	after 48 hours recovery: Δ°C/C: ±20% tan δ: 7% R_{ins}: 2000 MΩ or $R_iC_R \geq 25$ s, whichever is less

REVISION HISTORY

Revision	Date	Change Notification	Description
Rev.5	2001 May 30	-	- Converted to Phycomp brand
Rev.6	2003 Mar 04	-	- Updated company logo
Rev.7	2003 Jul 18	-	- Cover page revised