CIPOS™ Nano

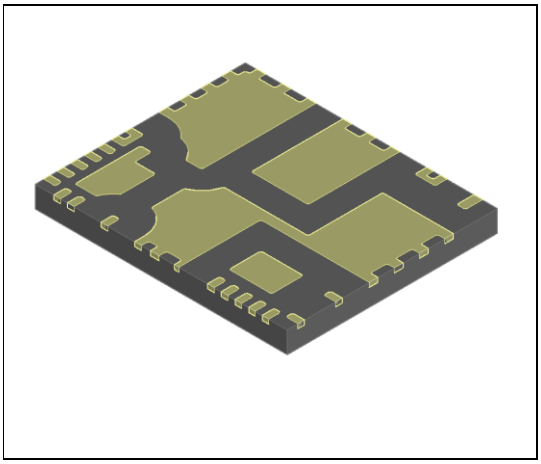
IM111-X3Q1B

Description

IM111-X3Q1B is an H-bridge integrated power module (IPM) designed for advanced appliance motor drive applications. This advanced low profile IPM offers a combination of Infineon's low $R_{DS(ON)}$ OptiMOS ™ technology and the industry benchmark high voltage, rugged driver in a small 12x10mm QFN package.

Features

- Integrated gate drivers and bootstrap functionality
- Overcurrent protection & fault reporting
- Low 0.063Ω $R_{DS(on)}$, 250V OptiMOS™
- Under-voltage lockout for both channels
- Shoot through protection
- Matched propagation delay for all channels
- Optimized dv/dt for loss and EMI trade offs
- Advanced input filter
- 3.3V input logic compatible
- Motor power range 80-200W
- 1500V_{RMS} min isolation



Potential Applications

- Linear refrigerator compressors
- High efficiency single-phase motor drives
- DC-AC inverters

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table 1 Part Ordering Table

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IM111-X3Q1B	QFN 12x10mm	Tape and Reel	2000	IM111-X3Q1BAUMA1

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1 Internal Electrical Schematic

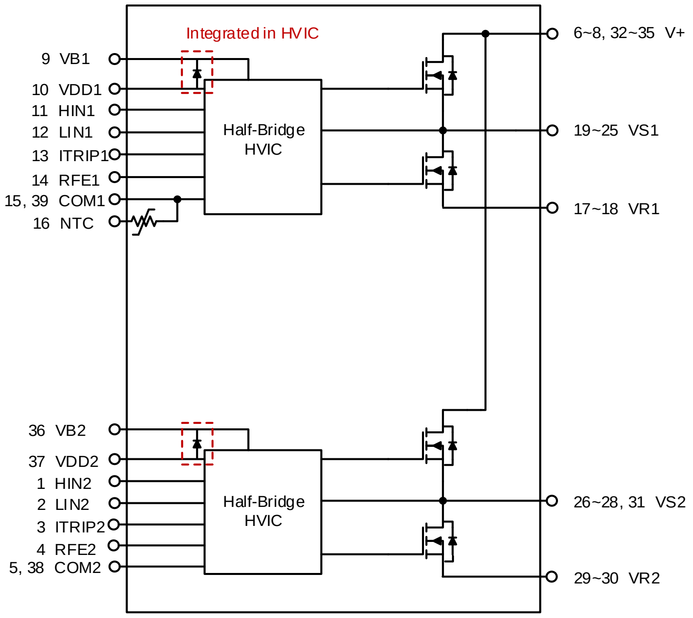


Figure 1 Internal electrical schematic.

2 Pin Configuration

2.1 Pin Assignment

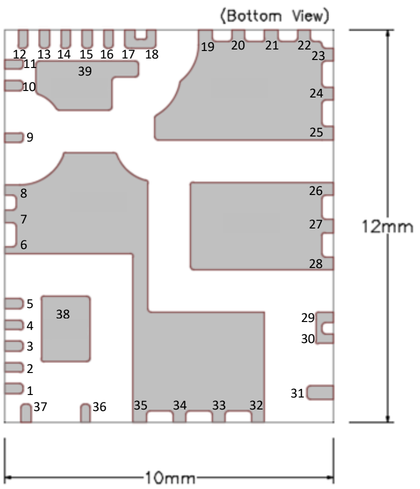


Figure 2 Module pinout

Table 2 Pin Assignment

Pin	Name	Description
1	HIN_2	Logic Input for High Side Gate Driver (Active High)
2	LIN_2	Logic Input for Low Side Gate Driver (Active High)
3	I_{TRIP2}	Over Current Protection
4	RFE_2	Fault Clear, Fault Reporting & Enable
5	COM_2	Logic Ground
6-8	V+	DC Bus Voltage Positive
9	V_{B1}	High Side Floating Supply (Bootstrap Cap Connection +)
10	V_{DD1}	Low Side Control Supply
11	HIN_1	Logic Input for High Side Gate Driver (Active High)
12	LIN_1	Logic Input for Low Side Gate Driver (Active High)
13	I_{TRIP1}	Over Current Protection
14	RFE_1	Fault Clear, Fault Reporting & Enable
15	COM_1	Logic Ground
16	NTC	Negative Temperature Coeffient Thermistor
17-18	V_{R1}	Low Side Source
19-25	V_{S1}	Phase Output
26-28	V_{S2}	Phase Output
29-30	V_{R2}	Low Side Source
31	V_{S2}	Phase Output (Bootstrap Cap Connection -)
32-35	V+	DC Bus Voltage Positive
36	V_{B2}	High Side Floating Supply (Bootstrap Cap Connection +)
37	V_{DD2}	Low Side Control Supply
38	COM_2	Logic Ground
39	COM_1	Logic Ground

2.2 Pin Descriptions

LIN and HIN (Low side and high side control pins)

These pins are positive logic and they are responsible for the control of the integrated OptiMOS. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-down resistor of about 800kΩ is internally provided to pre-bias inputs during supply start-up and an ESD diode is provided for pin protection purposes. Input Schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time t_{FILIN}. The filter acts according to Figure 4.

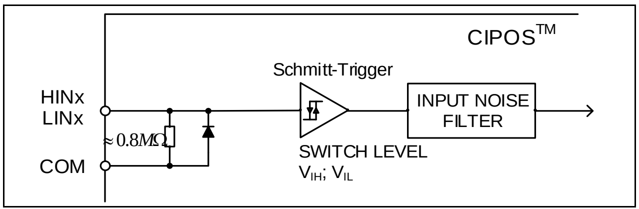


Figure 3 Input pin structure

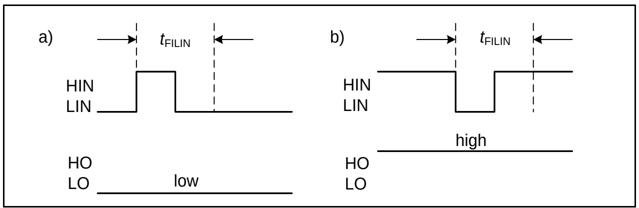


Figure 4 Input filter timing diagram

The integrated gate drive provides additionally a shoot through prevention capability which avoids the simultaneous on-state of the high-side and low-side switch of the same inverter phase. A minimum deadtime insertion of typically 300ns is also provided by driver IC, in order to reduce cross-conduction of the external power switches.

V_{DD}, COM (Low side control supply and reference)

V_{DD} is the control supply and it provides power both to input logic and to output power stage. Input logic is referenced to COM ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 8.9V is present.

The IC shuts down all the gate drivers power outputs, when the V_{DD} supply voltage is below V_{DDUV-} = 7.7V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

V_B and V_S (High side supplies)

V_B to V_S is the high side supply voltage. The high side circuit can float with respect to COM following the external high side power device source voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical V_{BSUV+} = 8.9V and a falling threshold of V_{BSUV-} = 7.7V.

V_S provide a high robustness against negative voltage in respect of COM. This ensures very stable designs even under rough conditions.

V_R (Low side source)

The low side source is available for current measurements of each phase leg. It is recommended to keep the connection to pin COM as short as possible in order to avoid unnecessary inductive voltage drops.

V_S (High side source and low side drain)

This pin is motor input pin.

V+ (Positive bus input voltage)

The high side OptiMOS devices are connected to the bus voltage. It is noted that the bus voltage does not exceed 200V.

I_{TRIP} (Over current protection)

Analog input for over-current shutdown. When active, I_{TRIP} shuts down outputs and activates RFE low.

RFE (Fault clear, fault reporting and enable)

Integrated fault reporting function, fault clear timer and external enable pin. This pin has negative logic and an open-drain output.

3 Absolute Maximum Ratings

3.1 Module

Table 3

Parameter	Symbol	Condition		Units
Storage temperature	T_{STG}		-40 ~ 150	°C
Operating case temperature	T_C		-40 ~ 125	°C
Operating junction temperature	T_J		-40 ~ 150	°C
Isolation voltage[1]	V_{ISO}	1min, RMS, f = 60Hz	1500	V

1. Characterized, not tested at production

3.2 Inverter

Table 4

Parameter	Symbol	Condition		Units
Max. blocking voltage	V_{DSS}/V_{RRM}		250	V
Output current based on $R_{TH(J-C)B}$ [1]	I_O	T_C = 25°C, DC	12	A
Peak output current	I_{OP}	T_C = 25°C, pulsed current	38	A
Output current based on $R_{TH(J-A)}$	I_{OA}	T_A = 25°C, DC	4	A
Peak power dissipation per MOSFET	P	T_C = 25°C	150	W

1. Limited by wire bonding current capability inside the package

3.3 Control

Table 5

Parameter	Symbol	Condition		Units
Low side control supply voltage	V_{DD}		-0.3 ~ 20	V
Input voltage LIN, HIN	V_{IN}		-0.3 ~ V_{DD}	V
High side floating supply voltage (V_B reference to V_S)	V_{BS}		-0.3 ~ 20	V

4 Thermal Characteristics

Table 6

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Single MOSFET thermal resistance, junction-case (bottom)	$R_{TH(J-C)B}$	Measures either high side or low side device	-	0.7	-	°C/W
Thermal resistance, junction-ambient[(1)]	$R_{TH(J-A)}$		-	12	-	°C/W

(1) The junction to ambient thermal resistance is simulated based on standard JESD51-5/7 using a FR4 2s2p board with device mounted and power evenly distributed to four power MOSFETs.

5 Recommended Operating Conditions

Table 7

Parameter	Symbol	Min.	Typ.	Max.	Units
Positive DC bus input voltage	V+	-	-	200	V
Low side control supply voltage	V_{DD}	13.5	-	16.5	V
High side floating supply voltage	V_{BS}	12.5	-	17.5	V
Input voltage	V_{IN}	0	-	5	V
PWM carrier frequency	F_{PWM}	-	6	-	kHz
External dead time between HIN & LIN	DT	1	-	-	µs
Voltage between COM and V_R	V_{COMR}	-5	-	5	V
Minimum input pulse width	$PW_{IN(ON)}$, $PW_{IN(OFF)}$	0.5	-	-	µs

6 Static Parameters

6.1 Inverter

(V_{DD}-COM) = (V_B - V_S) = 15 V. T_C = 25°C unless otherwise specified.

Table 8

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Drain to Source ON Resistance	$R_{DS(on)}$	I_D = 1A	-	0.063	0.073	Ω
		I_D= 1A, T_J = 150°C	-	0.12	-	Ω
Drain source leakage current	I_{DSS}	V_{IN} = 0V, V+ = 250V	-	15	-	µA
		V_{IN} = 0V, V+ = 250V, T_J = 150°C	-	40	-	µA
Diode forward voltage	V_F	I_F = 1A	-	0.71	-	V
		I_F = 1A, T_J = 150°C	-	0.48	-	V

6.2 Control

(V_{DD}-COM) = (V_B - V_S) = 15 V. T_C = 25°C unless otherwise specified. The V_{IN} and I_{IN} are referenced to COM and are applicable to all six channels. The V_{DDUV} is referenced to COM. The V_{BSUV} is referenced to V_S.

Table 9

Parameter	Symbol	Min.	Typ.	Max.	Units
Logic "1" input voltage (LIN, HIN)	$V_{IN,TH+}$	2.2	-	-	V
Logic "0" input voltage (LIN, HIN)	$V_{IN,TH-}$	-	-	0.8	V
RFE positive going threshold	V_{RFE+}	-	-	2.5	V
RFE negative going threshold	V_{RFE-}	0.8	-	-	V
V_{DD}/V_{BS} supply undervoltage, positive going threshold	$V_{DD,UV+}$, $V_{BS,UV+}$	8	8.9	9.8	V
V_{DD}/V_{BS} supply undervoltage, negative going threshold	$V_{DD,UV-}$, $V_{BS,UV-}$	6.9	7.7	8.5	V
V_{DD}/V_{BS} supply undervoltage lock-out hysteresis	V_{DDUVH}, V_{BSUVH}	-	1.2	-	V
Quiescent V_{BS} supply current	I_{QBS}	-	45	70	µA
Quiescent V_{DD} supply current	I_{QCC}	1.0	1.7	3.0	mA
Input bias current V_{IN}=4V for LIN,HIN	I_{IN+}	-	5	20	µA
Input bias current V_{IN}=0V for LIN, HIN	I_{IN-}	-	-	2	µA
Input bias current V_{IN} = 4V for RFE	$I_{IN,RFE+}$	-	0	1	µA
Input bias current V_{IN} = 4V for I_{TRIP}	I_{TRIP+}	-	5	20	µA
I_{TRIP} positive going threshold	$V_{IT,TH+}$	0.475	0.500	0.525	V
I_{TRIP} negative going threshold	$V_{IT,TH-}$	-	0.43	-	V
I_{TRIP} input hysteresis	$V_{IT,HYS}$	-	0.07	-	V
Bootstrap resistance	R_{BS}	-	200	-	Ω
RFE low on resistance	R_{RFE}	-	50	100	Ω

7 Dynamic Parameters

7.1 Inverter

(V_{DD}-COM) = (V_B - V_S) = 15 V. T_C = 25°C unless otherwise specified.

Table 10

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input to output turn-on propagation delay	T_{ON}	I_D = 1A, V+ = 150V	-	0.6	-	µs
Turn-on rise time	T_R		-	11	-	ns
Turn-on switching time	$T_{C(on)}$		-	42	-	ns
Input to output turn-off propagation delay	T_{OFF}	I_D = 1A, V+ = 150V	-	0.7	-	µs
Turn-off fall time	T_F		-	106	-	ns
Turn-off switching time	$T_{C(off)}$		-	96	-	ns
RFE low to six switch turn-off propagation delay	T_{EN}	V_{IN} = 0 or V_{IN} = 5V, V_{EN} = 5V	-	0.44	-	µs
I_{TRIP} to six switch turn-off propagation delay	T_{ITRIP}		-	920	-	ns
Turn-on switching energy	E_{ON}	I_D = 1A, V+ = 150V, V_{DD} = 15V, L = 9mH	-	12	-	µJ
Turn-off switching energy	E_{OFF}		-	5	-	
Diode reverse recovery energy	E_{REC}		-	10	-	
Diode reverse recovery time	T_{RR}		-	35	-	ns
Turn-on switching energy	E_{ON}	I_D = 1A, V+ = 150V, V_{DD} = 15V, L = 9mH, T_J = 150°C	-	24	-	µJ
Turn-off switching energy	E_{OFF}		-	5	-	
Diode reverse recovery energy	E_{REC}		-	13	-	
Diode reverse recovery time	T_{RR}		-	55	-	ns

7.2 Control

(V_{DD}-COM) = (V_B - V_S) = 15V. T_C = 25°C unless otherwise specified.

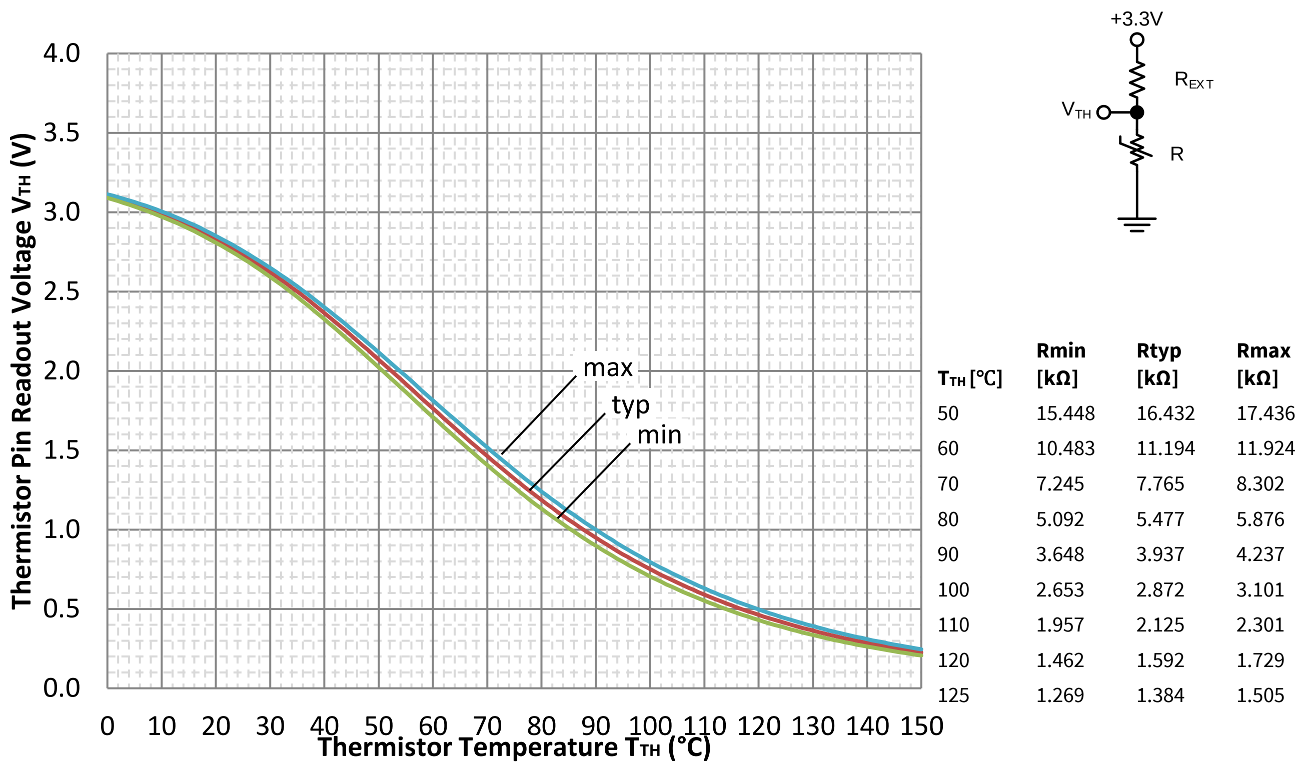
Table 11

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input filter time (HIN, LIN, I_{TRIP})	$T_{FIL,IN}$	V_{IN} = 0 or V_{IN} = 5V	-	300	-	ns
Input filter time (RFE)	$T_{FIL,EN}$	V_{RFE} = 0 or V_{RFE} = 5V	-	500	-	ns
ITRIP to Fault propagation delay	T_{FLT}	V_{IN} = 0 or V_{IN} = 5V, V_{ITRIP} = 5V	-	660	-	ns
Internal injected dead time	$T_{DT,GD}$	V_{IN} = 0 or V_{IN} = 5V	-	300	-	ns
Matching propagation delay time (on and off) for same phase high-side and low-side	M_T	External dead time > 1µs	-	-	50	ns

8 Thermistor Characteristics

Table 12

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Resistance	R_{25}	T_C = 25°C, ±5% tolerance	44.65	47	49.35	kΩ
Resistance	R_{125}	T_C = 125°C	1.27	1.39	1.51	kΩ
B-constant (25/100)	B	±1% tolerance	-	4006	-	K
Temperature Range			-20	-	150	°C



T_{TH} [°C]	Rmin [kΩ]	Rtyp [kΩ]	Rmax [kΩ]
50	15.448	16.432	17.436
60	10.483	11.194	11.924
70	7.245	7.765	8.302
80	5.092	5.477	5.876
90	3.648	3.937	4.237
100	2.653	2.872	3.101
110	1.957	2.125	2.301
120	1.462	1.592	1.729
125	1.269	1.384	1.505

Figure 5 **Thermistor resistance – temperature curve, for R_{EXT}=9.76kΩ, and thermistor resistance variation with temperature.**

9 Qualification Information

Table 13

Moisture sensitivity level	MSL3	
RoHS Compliant	Yes	
ESD	CDM	±2kV, Class C3, per ANSI/ESDA/JEDEC JS-002 standard
	HBM	±2kV, Class 2, per ANSI/ESDA/JEDEC JESD22-A114F standard

10 Diagrams & Tables

10.1 Input-Output Logic Table

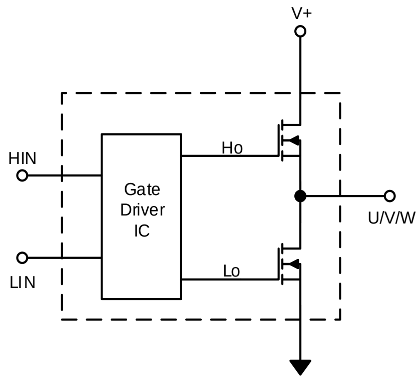


Figure 6 Module block diagram

Table 14

RFE	I_{TRIP}	HIN	LIN	U,V,W
1	0	1	0	V+
1	0	0	1	0
1	0	0	0	‡
1	0	1	1	‡
1	1	x	x	‡
0	x	x	x	‡

‡ Voltage depends on direction of phase current

10.2 Switching Time Definitions

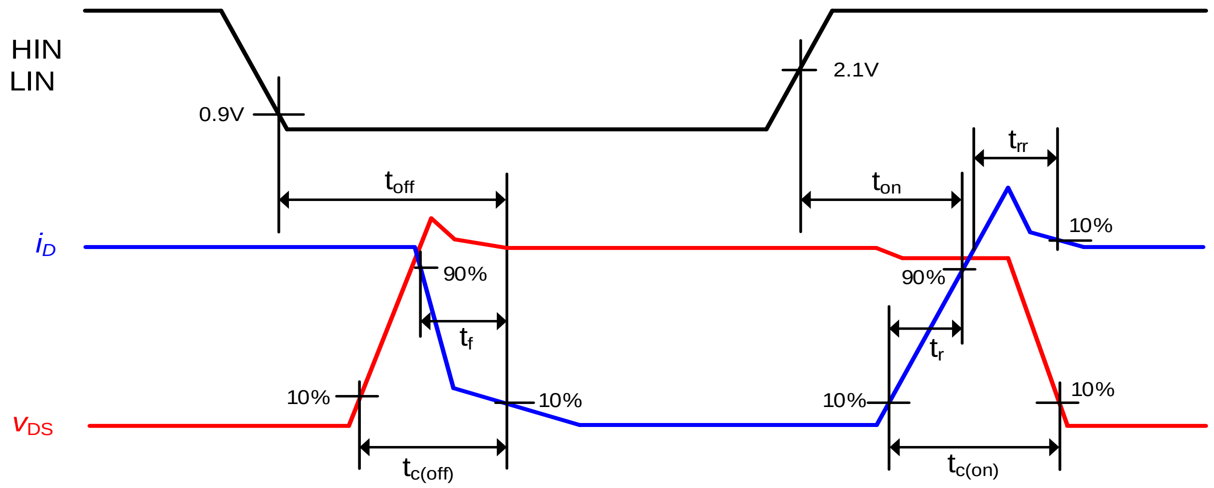


Figure 7 Switching times definition

11 Application Guide

11.1 Typical Application Schematic

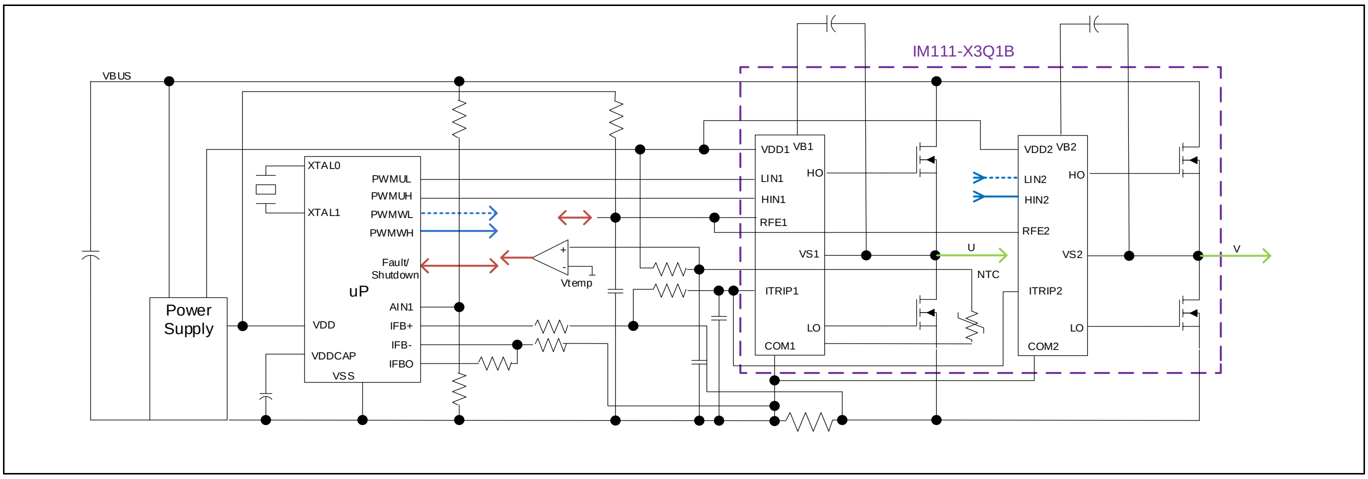


Figure 8 Application schematic

11.2 Performance Charts

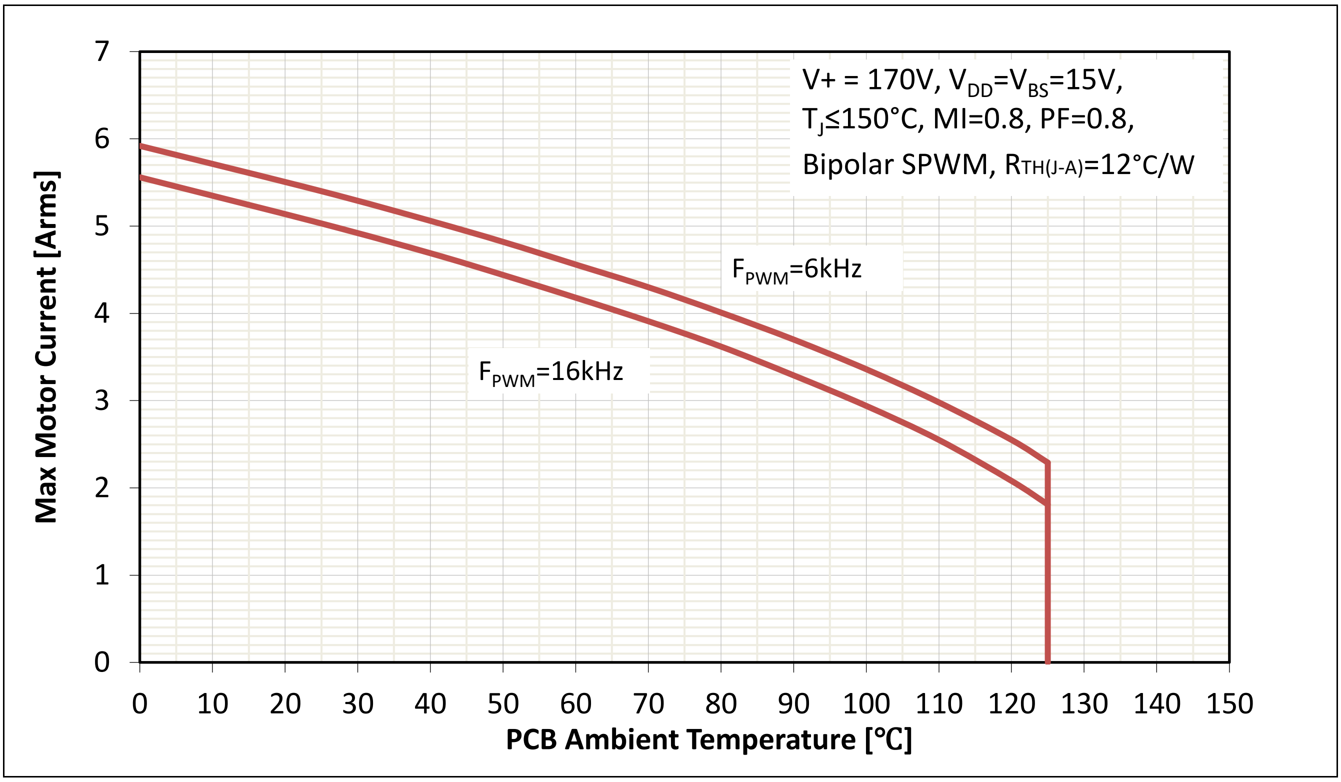


Figure 9 Max current SOA

11.3 –Vs Immunity

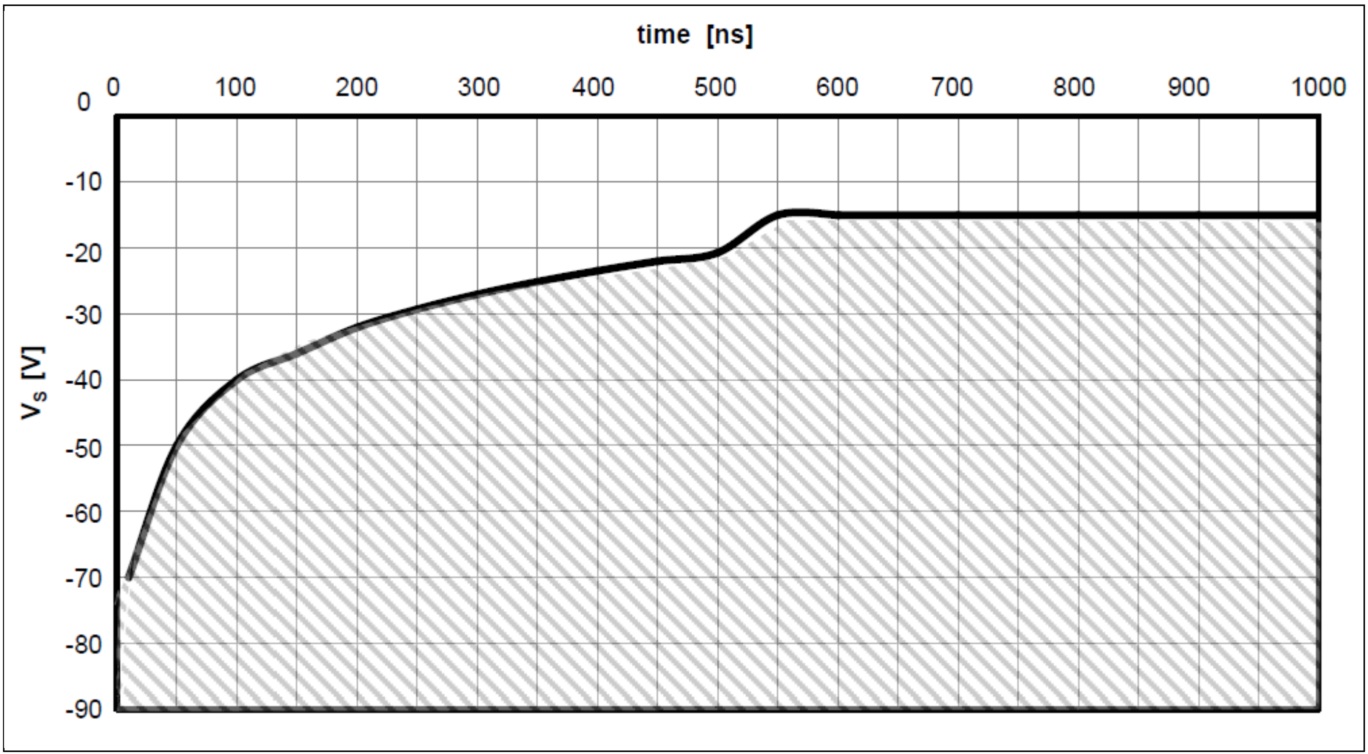
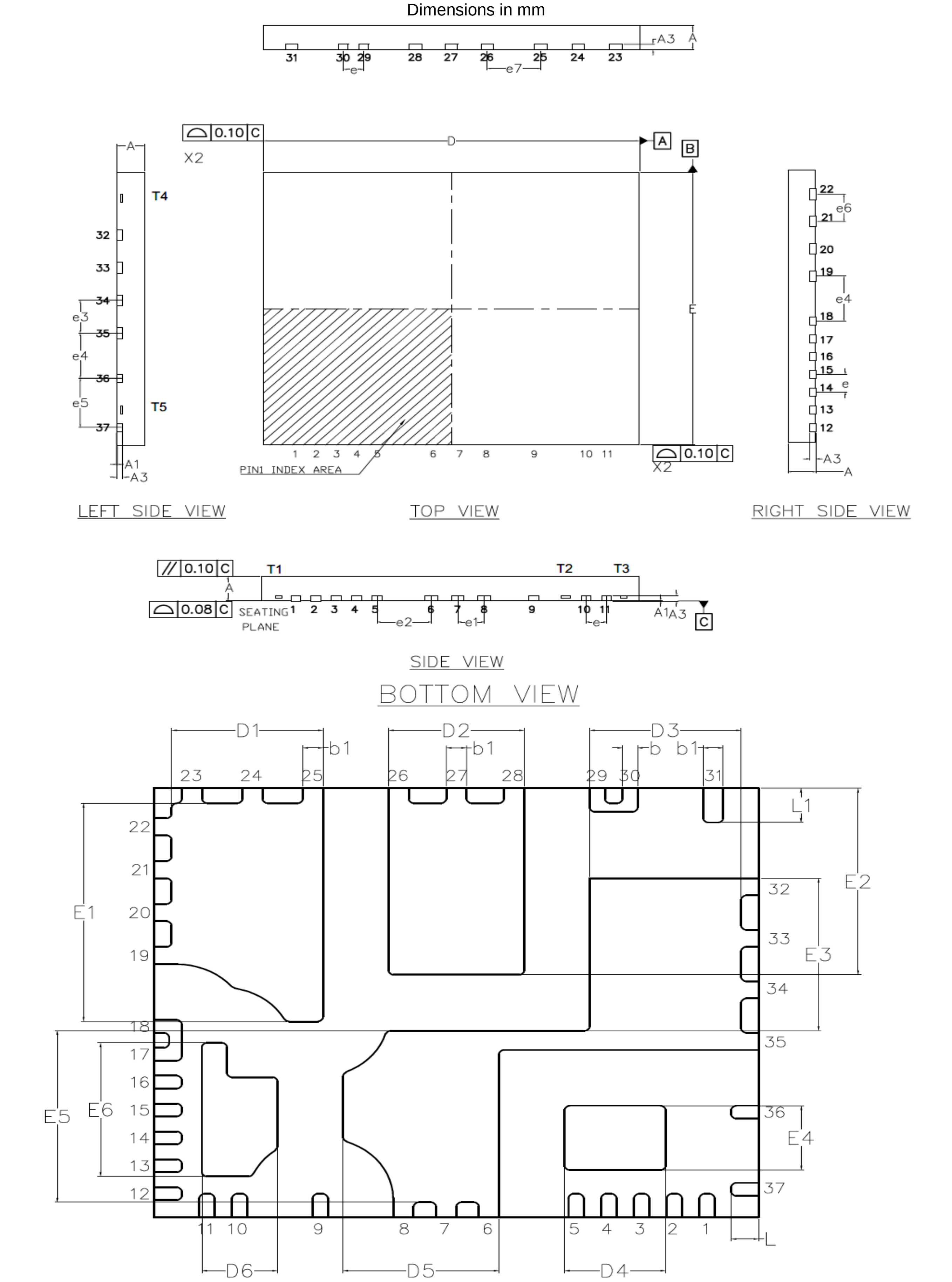


Figure 10 –Vs immunity

12 Package Outline



SYMBOL	Common					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.033	0.035	0.037
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.203 REF			0.008 REF		
b	0.250	0.300	0.350	0.010	0.012	0.014
b1	0.350	0.400	0.450	0.014	0.016	0.018
D	11.90	12.00	12.10	0.469	0.472	0.476
E	9.95	10.00	10.10	0.392	0.394	0.398
D1	2.955	3.005	3.055	0.116	0.118	0.120
E1	5.035	5.085	5.135	0.198	0.200	0.202
D2	2.640	2.690	2.740	0.104	0.106	0.108
E2	4.300	4.350	4.400	0.169	0.171	0.173
D3	2.955	3.005	3.055	0.116	0.118	0.120
E3	3.500	3.550	3.600	0.138	0.140	0.142

SYMBOL	Common					
	DIMENSIONS mm			DIMENSIONS Inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
D4	1.905	2.005	2.105	0.075	0.079	0.083
E4	3.350	3.400	3.450	0.132	0.134	0.136
D5	3.045	3.095	3.145	0.120	0.122	0.124
E5	3.950	4.000	4.050	0.156	0.157	0.159
D6	1.450	1.500	1.550	0.057	0.059	0.061
E6	3.065	3.115	3.165	0.121	0.123	0.125
L	0.500	0.550	0.600	0.020	0.022	0.024
L1	0.750	0.800	0.850	0.030	0.031	0.033
e	0.650 BSC.			0.026 BSC.		
e1	0.848 BSC.			0.033 BSC.		
e2	1.730 BSC.			0.068 BSC.		
e3	1.200 BSC.			0.047 BSC.		
e4	1.650 BSC.			0.065 BSC.		
e5	1.800 BSC.			0.071 BSC.		
e6	1.000 BSC.			0.040 BSC.		
e7	1.700 BSC.			0.067 BSC.		

Note: Exposed tie bars on side of the module.
T1 is internally connected to pin 37
T2 is internally connected to pin 15
T3 is internally connected to pin 12
T4 is internally connected to pin 31
T5 is internally connected to pin 5

Revision History

Major changes since the last revision

Page or Reference	Description of change

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Edition 2019-12-12

Published by

Infineon Technologies AG
81726 München, Germany

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Document reference