HF500-40

Fixed-Frequency, Flyback Regulator with Multi-Mode Control and Over-Power Line Compensation

DESCRIPTION

The HF500-40 is a fixed-frequency, current-mode regulator with built-in slope compensation. The HF500-40 combines a 700V MOSFET and a full-featured controller into one chip for a low-power, offline, flyback, switch-mode power supply.

At medium and heavy loads, the regulator works in a fixed frequency with frequency jittering. Jittering helps reduce EMI energy on the switching frequency and its harmonics. During light-load condition, the regulator freezes the peak current and reduces its switching frequency to 25kHz to offer excellent efficiency. At very light loads, the regulator enters burst mode to achieve low standby power consumption.

Full protection features include brown-in and brown-out, VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), input over-voltage protection (OVP), VCC over-voltage protection (OVP), and over-temperature protection (OTP).

The HF500-40 features over-power line compensation to ensure that the overload protection point is independent of the input voltage.

The HF500-40 is available in a PDIP8-7B package.

	Maximum Output Power (1)			
	$230V_{AC}$ ± 15%		$85V_{AC}$ ~ $265V_{AC}$	
	Adapter (2)	Open Frame (3)	Adapter (2)	Open Frame (3)
P_{OUT} (W)	30	45	25	35

NOTES:

1) The junction temperature can limit the maximum output power.
2) Maximum continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
3) Maximum continuous power in an open-frame design at 50°C ambient temperature.

FEATURES

- 700V/1Ω Integrated MOSFET
- Fixed-Frequency, Current-Mode Control Operation with Built-In Slope Compensation
- Frequency Foldback Down to 25kHz at Light Load
- Burst Mode for Low Standby Power Consumption
- Frequency Jittering for a Reduced EMI Signature
- Over-Power Compensation
- Internal High-Voltage Current Source
- VCC Under-Voltage Lockout (UVLO) with Hysteresis
- Programmable Input B/O and Over-Voltage Protection (OVP)
- VCC Over-Voltage Protection (OVP)
- Overload Protection (OLP) with Programmable Delay
- Latch-Off Protection on TIMER
- Over-Temperature Protection (OTP) (Auto-Restart with Hysteresis)
- Short-Circuit Protection (SCP)
- Programmable Soft Start (SS)
- Available in a PDIP8-7B Package

APPLICATIONS

- Power Supplies for Home Appliances
- Set-Top Boxes
- Standby and Auxiliary Power
- Adapters

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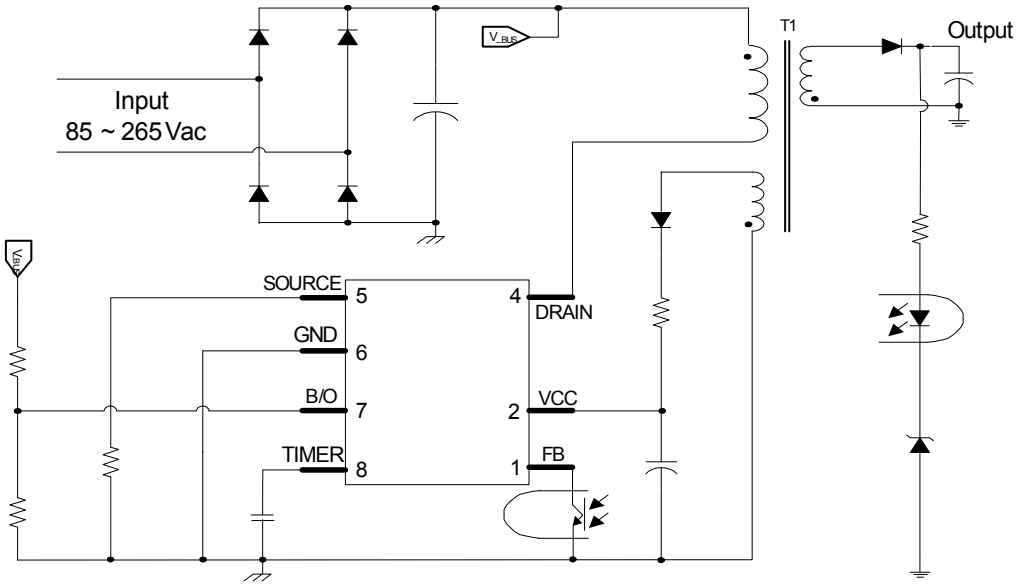
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
HF500GP-40	PDIP8-7B	*See Below*

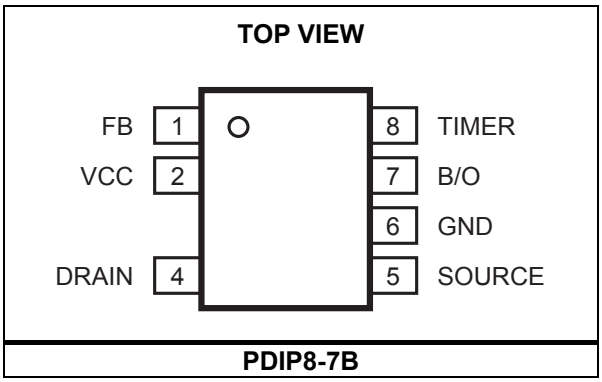
* For Tape & Reel, add suffix –Z (e.g.: HF500GP-40–Z).

TOP MARKING

MPS YYWW
HF500-40
LLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
HF500-40: Product code of HF500GP-40
LLLLLLLL: Lot number

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1	FB	**Feedback.** A pull-down optocoupler controls the output regulation.
2	VCC	**Power supply of the IC.** VCC enters over-voltage protection (OVP) if the voltage on VCC rises above V_{OVP}.
4	DRAIN	**Drain of the internal MOSFET.** DRAIN is the input for the start-up, high-voltage current source.
5	SOURCE	**Source of the internal MOSFET.** SOURCE is the input of the primary current-sense signal.
6	GND	**Ground.**
7	B/O	**Brown-in/out, input OVP, and over-power compensation detection.** Brown-in/out, input OVP, and over-power compensation are achieved by detecting the voltage on B/O. All functions are disabled when B/O is pulled above V_{DIS}.
8	TIMER	**Combined soft start, frequency jittering, and timer functions for over-load protection (OLP) and brown-out protection.** The IC is latched by pulling TIMER down. TIMER allows for external OVP and over-temperature protection (OTP) detection.

ABSOLUTE MAXIMUM RATINGS (4)

DRAIN breakdown voltage ..... -0.3V to 700V
VCC to GND..... -0.3V to 30V
FB, TIMER, SOURCE, B/O to GND ..... -0.3V to 7V
Continuous power dissipation (T_A = +25°C) (5) 1.19W
Junction temperature ..... 150°C
Lead temperature..... 260°C
Storage temperature .....-60°C to +150°C
ESD capability human body model (all pins except DRAIN) 4.0kV
ESD capability machine model..... 200V

Recommended Operating Conditions (6)

Operating junction temp. (T_J)....-40°C to +125°C
Operating VCC range ..... 9V to 24V

Thermal Resistance (7)

	θ_{JA}	θ_{JC}	
PDIP8-7B	105	45 ...	°C/W

NOTES:

4) Exceeding these ratings may damage the device.
5) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
6) The device is not guaranteed to function outside of its operating conditions.
7) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VCC = 16V, T_J = -40°C to 125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start-Up Current Source (DRAIN)						
Supply current from DRAIN	I_{Drain_0}	VCC = 0V, V_{DRAIN} = 120V/400V	1.4	3.6	6.2	mA
	I_{Drain_11}	VCC = 11V, V_{DRAIN} = 120V/400V	1.4	5	7.9	
Leakage current from DRAIN	I_{LK}	VCC = 10V, V_{DRAIN} = 400V		5	12	µA
Breakdown voltage	V_{BR}	T_J = 25°C	700			V
Internal MOSFET (DRAIN)						
On state resistance	R_{DS_ON}	VCC = 10.5V, I_D = 0.1A, T_J = 25°C		1	1.15	Ω
Supply Voltage Management (VCC)						
VCC level (increasing) where the internal regulator stops	VCC_{OFF}		11	12	13	V
VCC level (decreasing) where the IC shuts down and the internal regulator turns on	VCC_{UVLO}		6	7	8	V
VCC UVLO hysteresis	VCC_{OFF} - VCC_{UVLO}		4	4.8		V
VCC recharge level when protection occurs	VCC_{PRO}		4.7	5.3	5.9	V
VCC decreasing level where the latch-off phase ends	VCC_{LATCH}			2.5		V
Internal IC consumption	I_{CC}	V_{FB} = 3V, VCC = 12V		0.9	1.2	mA
Internal IC consumption, latch-off phase	$I_{CCLATCH}$	VCC = 12V, T_J = 25°C		700	900	µA
Voltage on VCC (upper limit) where the regulator latches off (OVP)	V_{OVP}		25	27	29	V
Blanking duration on the OVP comparator	T_{OVP}			60		µs
Oscillator						
Oscillator frequency	f_{OSC}	V_{FB} > 1.85V, T_J = 25°C	62	65	68	kHz
Frequency jittering amplitude in percentage of f_{OSC}	A_{jitter}	V_{FB} > 1.85V, T_J = 25°C	±4.5	±6.5	±8	%
Frequency jittering entry level	V_{FB_JITTER}				1.95	V
Frequency jittering modulation period	T_{jitter}	C_{TIMER} = 47nF		3.7		ms

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ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 16V, T_J = -40°C to 125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Protections (B/O)						
Brown-in threshold voltage on B/O	V_{B/O_IN}	$V_{B/O}$ increasing	0.94	1	1.06	V
Brown-out threshold voltage on B/O	V_{B/O_OUT}	$V_{B/O}$ decreasing	0.85	0.9	0.95	V
Brown-in/out hysteresis	$\Delta V_{B/O}$		0.065	0.1	0.14	V
Timer duration for line cycle dropout	$T_{B/O}$	C_{TIMER} = 47nF	34	55		ms
Input OVP threshold on B/O	$OVP_{B/O}$		4.2	4.5	4.8	V
Input OVP delay time	$T_{OVPB/O}$			90		µs
Voltage on B/O to disable B/O and input OVP function	V_{DIS}		5.4	6	6.6	V
Clamp voltage on B/O	V_{B/O_Cla}		7			V
Input impedance	$R_{B/O}$		1.2			MΩ
Current Sense (SOURCE)						
Current-limit point	V_{ILIM}		0.93	1	1.07	V
Short-circuit protection point	V_{SCP}		1.3	1.5	1.7	V
Current limitation during frequency foldback	V_{FOLD}	V_{FB} = 1.85V	0.63	0.68	0.73	V
Current limitation when entering burst	V_{IBURL}	V_{FB} = 0.7V		0.1		V
Current limitation when exiting burst	V_{IBURH}	V_{FB} = 0.8V		0.13		V
Leading-edge blanking for V_{ILIM}	T_{LEB1}			300		ns
Leading-edge blanking for V_{SCP}	T_{LEB2}			250		ns
Slope of the compensation ramp	S_{RAMP}		18	25	31	mV/µs
Feedback (FB)						
Internal pull-up resistor	R_{FB}	T_J = 25°C	12	13.5	15	kΩ
Internal pull-up voltage	V_{DD}			4.3		V
V_{FB} to internal current-set point division ratio	K_{FB1}	V_{FB} = 2V	2.5	2.8	3.1	
V_{FB} to current-set point division ratio	K_{FB2}	V_{FB} = 3V	2.8	3.1	3.4	
FB level (decreasing) where the regulator enters burst mode	V_{BURL}		0.63	0.7	0.77	V
FB level (increasing) where the regulator exits burst mode	V_{BURH}		0.72	0.8	0.88	V

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ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 16V, T_J = -40°C to 125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Overload Protection (FB)						
FB level where the regulator enters OLP after a dedicated time	V_{OLP}			3.7		V
Time duration before OLP when FB reaches the protection point	T_{OLP}	C_{TIMER} = 47nF	32			ms
Over-Power Compensation (B/O)						
Compensation voltage	V_{OPC}	$V_{B/O}$ = 1.1V, V_{FB} = 2.5V, T_J = 25°C		0		mV
		$V_{B/O}$ = 1.3V, V_{FB} = 2.5V, T_J = 25°C		19		
		$V_{B/O}$ = 2.9V, V_{FB} = 2.5V, T_J = 25°C	153	200	247	
		$V_{B/O}$ = 3.5V, V_{FB} = 2.5V, T_J = 25°C	205	270	335	
		$V_{B/O}$ > V_{DIS}, T_J = 25°C		0		
FB voltage (lower limit) when compensation is removed	$V_{OPC(OFF)}$		0.55			V
FB voltage (upper limit) when compensation is fully applied	$V_{OPC(ON)}$				2.5	V
Frequency Foldback						
FB voltage (lower threshold) when frequency foldback starts	$V_{FB(FOLD)}$			1.8		V
Minimum switching frequency	$f_{OSC(min)}$	T_J = 25°C	20.5	25	30	kHz
FB voltage (lower threshold) when frequency foldback ends	$V_{FB(FOLDE)}$			1		V
Latch-Off Input (Integration in TIMER)						
Lower threshold when the regulator is latched	$V_{TIMER(LATCH)}$		0.7	1	1.5	V
Blanking duration on latch detection	T_{LATCH}			42		µs
Over-Temperature Protection (OTP)						
Thermal shutdown threshold	T_{OTP}			150		°C
Thermal shutdown hysteresis	$T_{OTP(HYS)}$			25		°C

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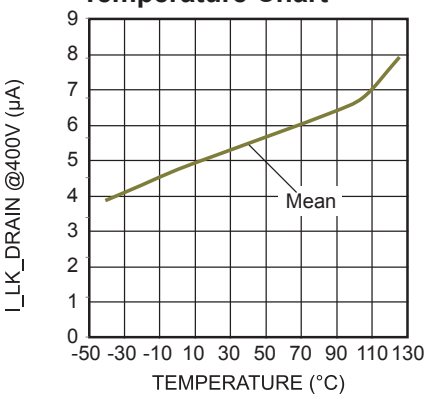
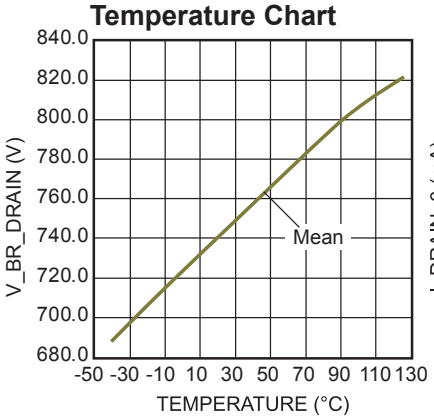
TYPICAL CHARACTERISTICS

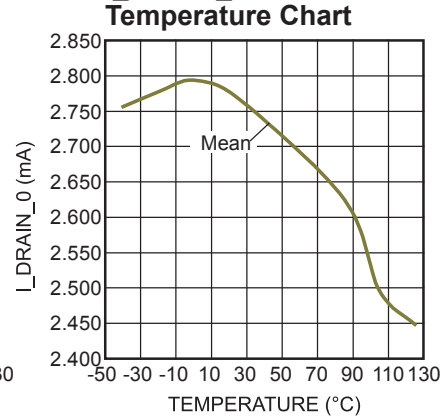
I_LK_DRAIN @400V vs . Temperature Chart



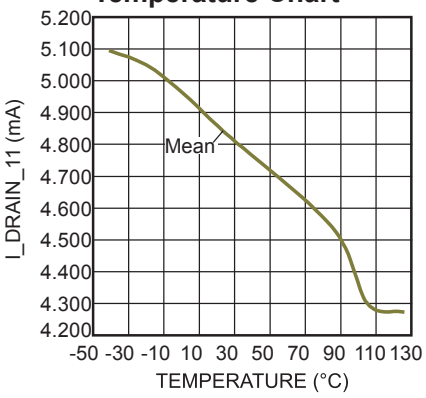
V_BR_DRAIN vs. Temperature Chart



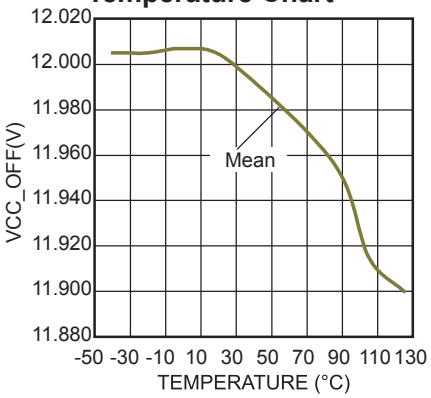
I_DRAIN_0 vs. Temperature Chart



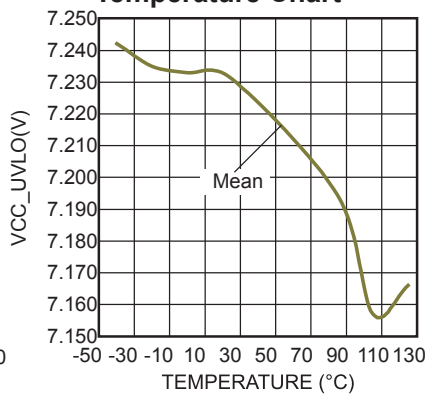
I_DRAIN_11 vs. Temperature Chart



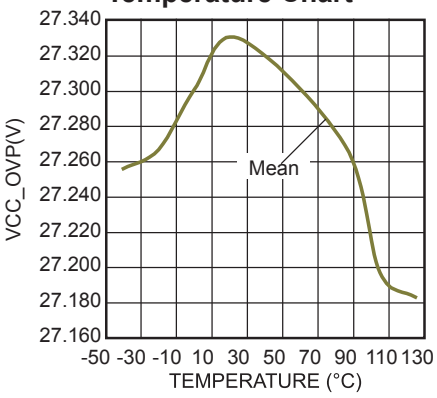
VCC_OFF vs. Temperature Chart



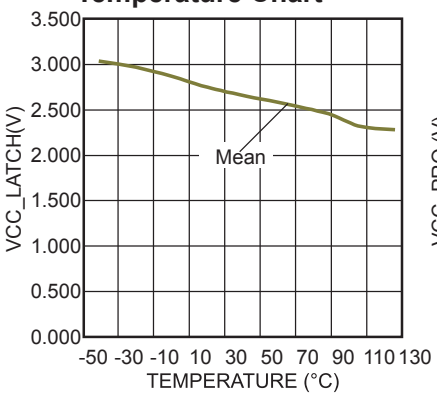
VCC_UVLO vs. Temperature Chart



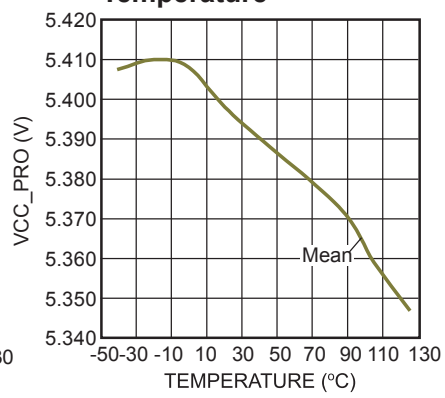
VCC_OVP vs. Temperature Chart



VCC_Latch vs. Temperature Chart



VCC_PRO vs. Temperature



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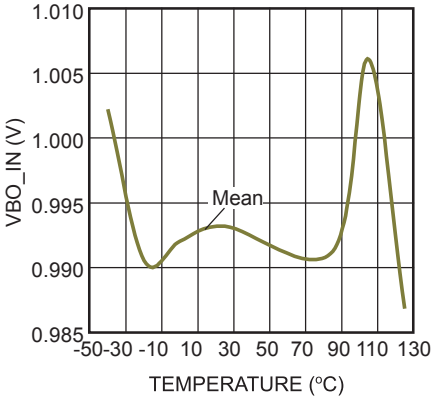
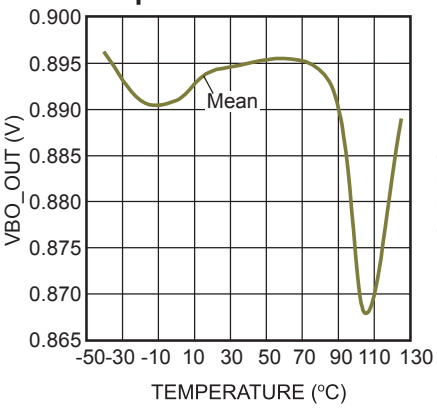
TYPICAL CHARACTERISTICS *(continued)*

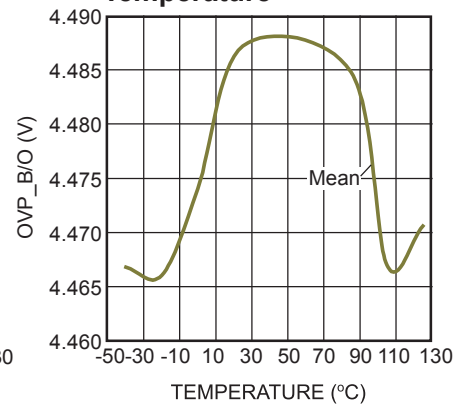
VBO_IN vs. Temperature



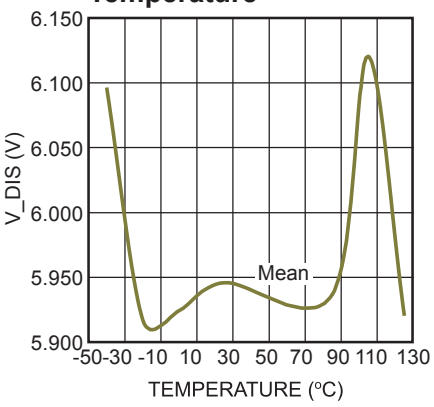
VBO_OUT vs. Temperature



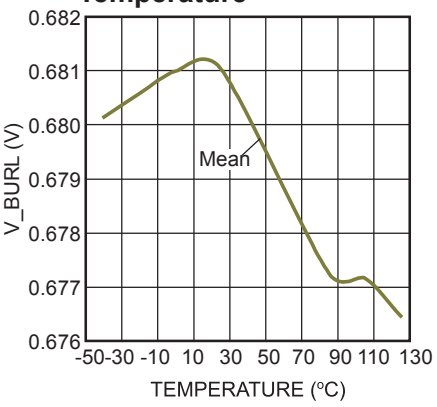
OVP_B/O vs. Temperature



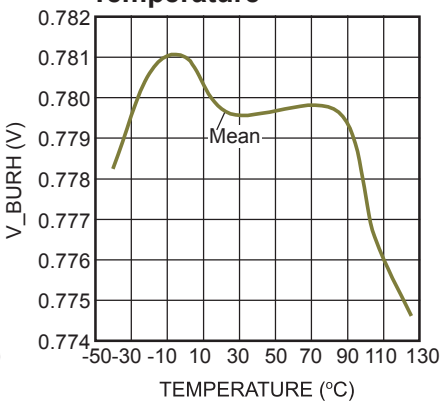
V_DIS vs. Temperature



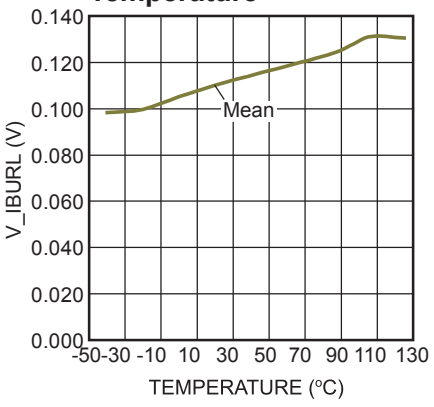
V_BURL vs. Temperature



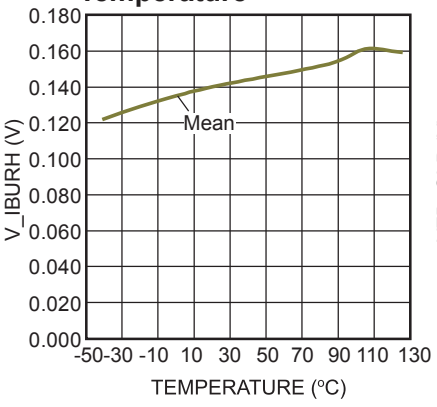
V_BURH vs. Temperature



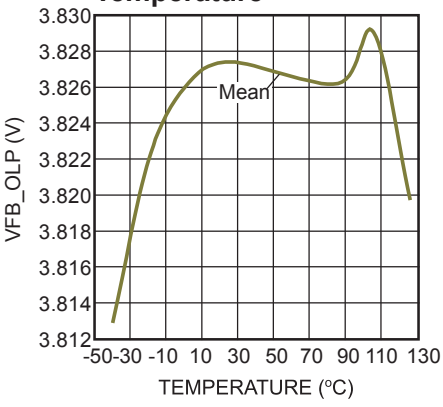
V_IBURL vs. Temperature



V_IBURH vs. Temperature



VFB_OLP vs. Temperature



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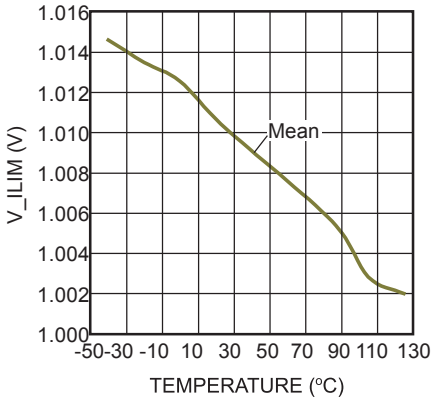
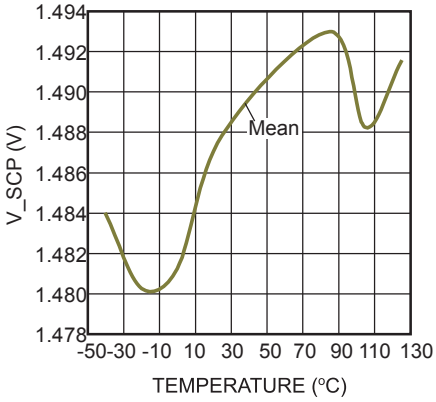
TYPICAL CHARACTERISTICS *(continued)*

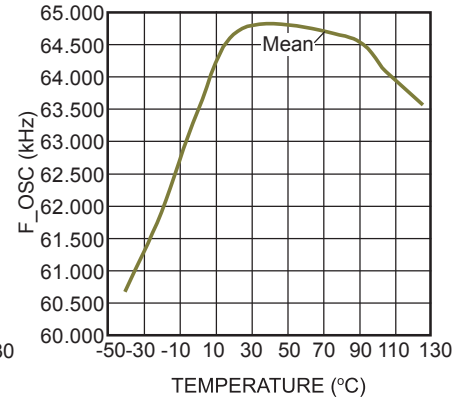
V_ILIM vs. Temperature



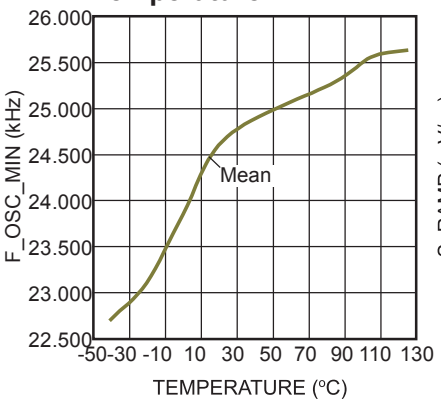
V_SCP vs. Temperature



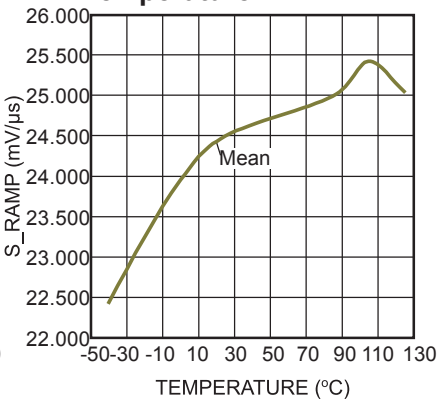
F_OSC vs. Temperature



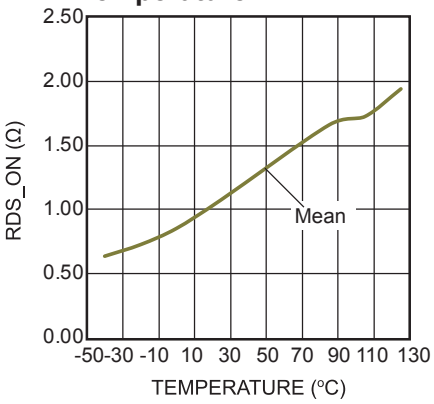
F_OSC_MIN vs. Temperature



S_RAMP vs. Temperature



RDS_ON vs. Temperature



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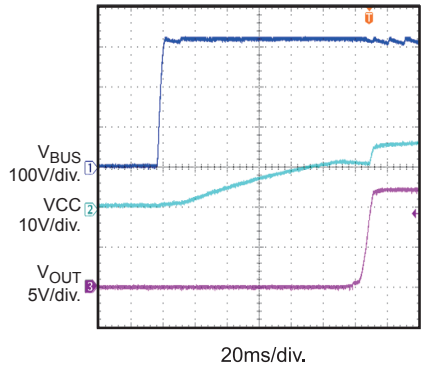
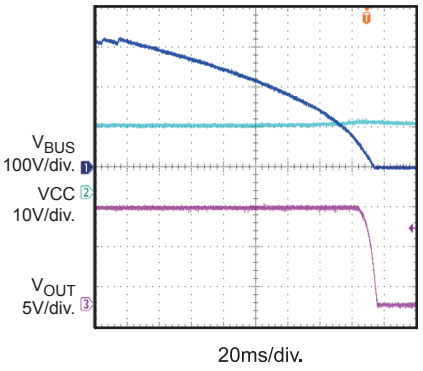
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 230V_{AC}, V_{OUT} = 12V, I_{OUT} = 2.5A, unless otherwise noted.

Input Power On

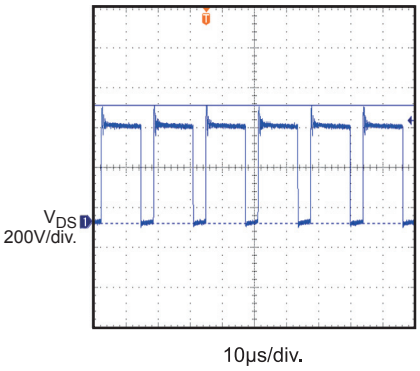


Input Power Off

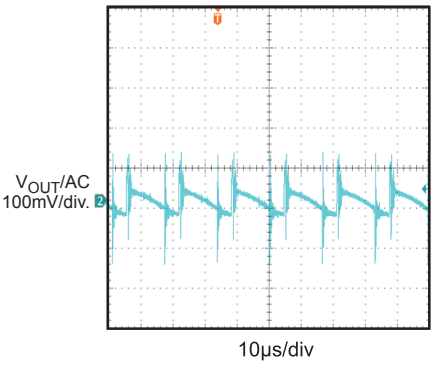


Stress

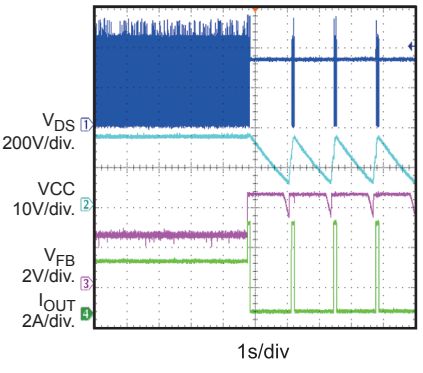
V_{IN}=265VAC



Output Ripple

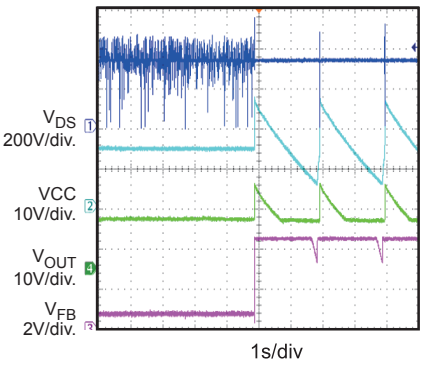


OLP Entry

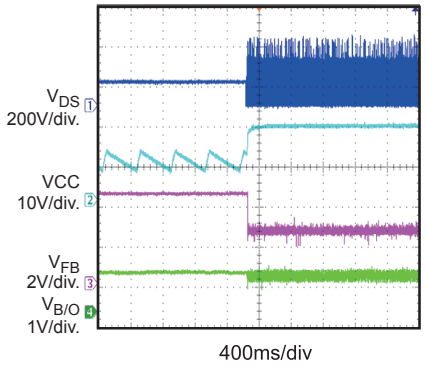


OVP Entry

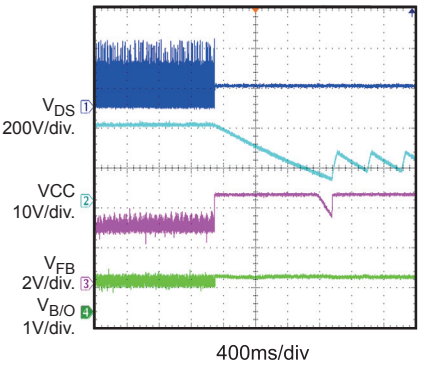
No Load



Brown-In

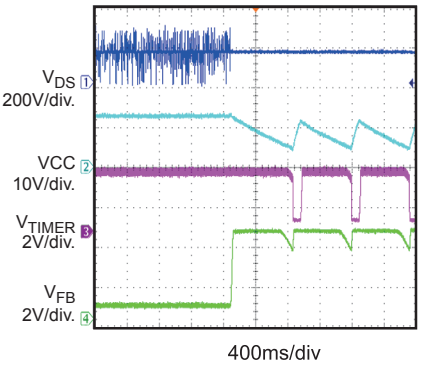


Brown-Out



OTP Entry

V_{IN}=115VAC, No Load



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BLOCK DIAGRAM

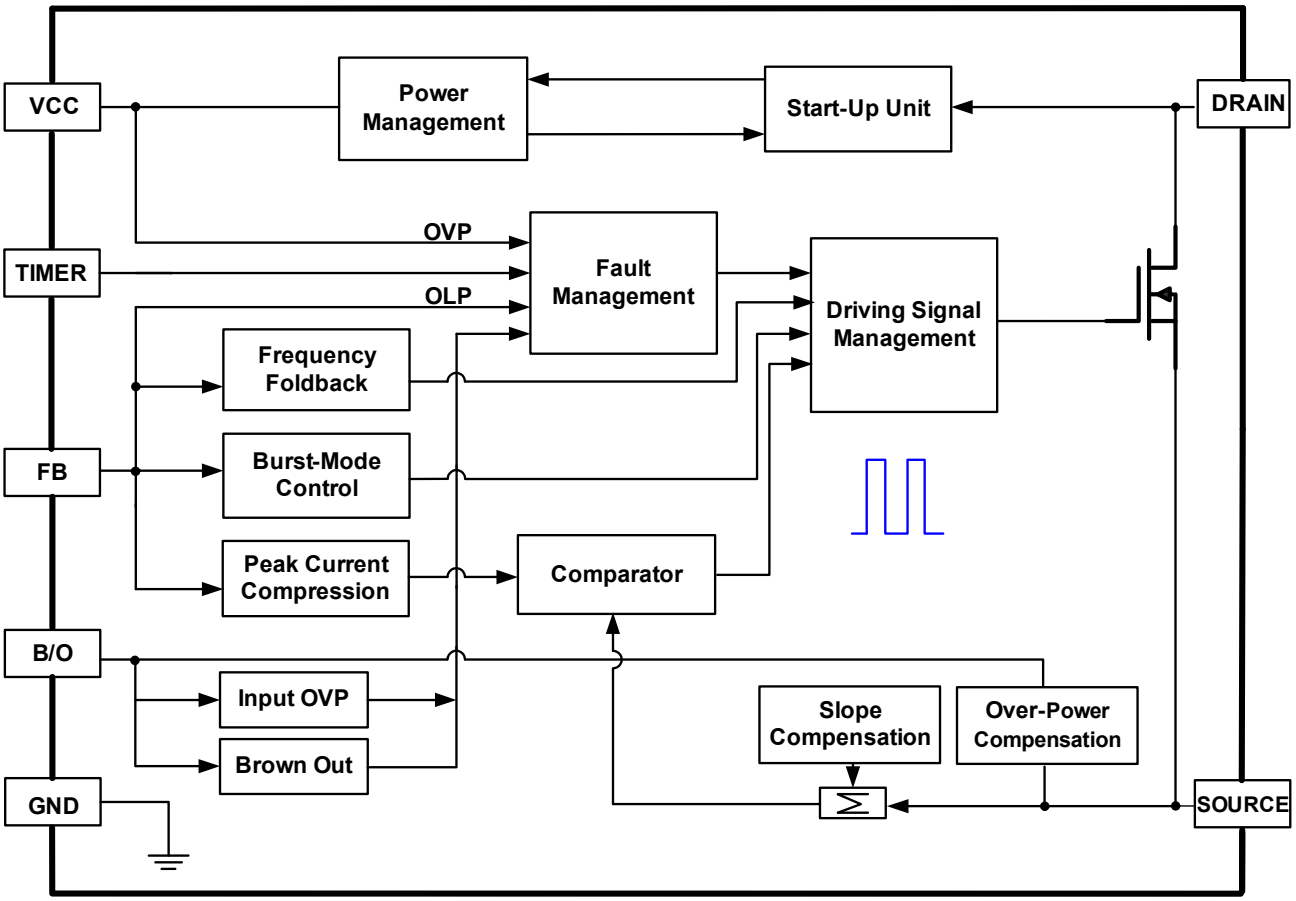

Figure 1: Functional Block Diagram

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OPERATION

The HF500-40 is a fixed-frequency, current-mode regulator with built-in slope compensation that incorporates all of the necessary features to build a reliable switch-mode power supply. In light-load conditions, the HF500-40 freezes the peak current and reduces its switching frequency to 25kHz to minimize switching loss. When the output power falls below a given level, the regulator enters burst mode. The HF500-40 uses frequency jittering to improve electromagnetic interference (EMI) performance.

Fixed Frequency with Jittering

Frequency jittering reduces EMI by spreading out the energy (see Figure 2).

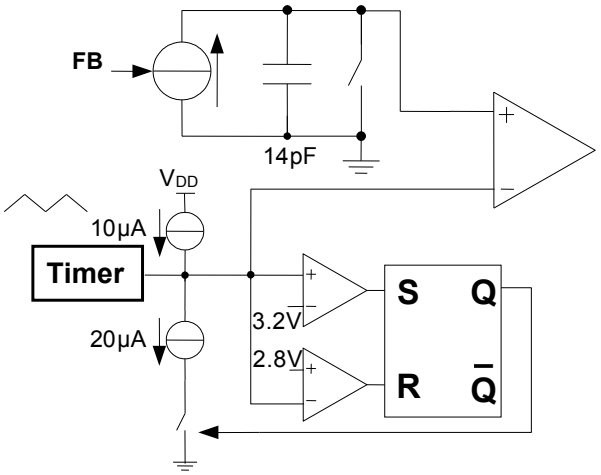

Figure 2: Frequency Jitter Circuit

An internal capacitor is charged with a controlled current source, which is fixed when FB is greater than 2V, and its voltage is compared with the TIMER voltage (V_{TIMER}). V_{TIMER} is a triangular wave between 2.8V and 3.2V with a charging/discharging current (see Figure 3). The switching frequency can be calculated using Equation (1):

$$f_s = \frac{1 \cdot 10^6}{5.28 \cdot V_{TIMER} / V + 0.2} Hz \quad (1)$$

T_{jitter} can be calculated using Equation (2):

$$T_{jitter} = 8 \cdot C_{TIMER} / nF \cdot 10^{-5} s \quad (2)$$

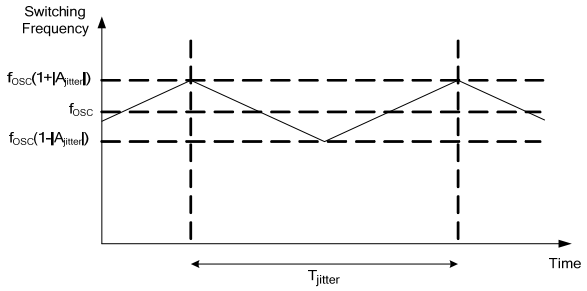

Figure 3: Frequency Jittering

Frequency Foldback

To achieve high efficiency during all load conditions, the HF500-40 implements frequency foldback during light-load conditions.

When the load decreases to a given level, the regulator freezes the V_{FOLD} peak current and reduces the charging current, dropping its switching frequency down to $f_{OSC(min)}$ and reducing switching loss. If the load continues to decrease, the peak current decreases with a fixed frequency to avoid audible noise. Figure 4 shows the frequency and peak current vs. FB.

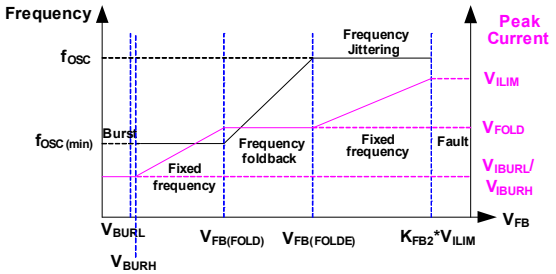

Figure 4: Frequency and Peak Current vs. FB

Current-Mode Operation with Slope Compensation

The primary peak current is controlled by the FB voltage (V_{FB}). When the peak current reaches the level determined by FB, the MOSFET turns off. Its internal synchronous slope compensation (S_{RAMP}) helps prevent sub-harmonic oscillation when the duty cycle is larger than 50% in continuous conduction mode (CCM). This allows the HF500-40 to work with a wide input voltage range.

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High-Voltage Start-Up Current Source

Initially, the IC is self-supplied by the internal high-voltage current source, which is drawn from DRAIN. The IC turns off the current source once the voltage on VCC reaches VCC_{OFF}.

If the voltage on VCC falls below VCC_{UVLO}, the switching pulse stops, and the current source turns on again. The auxiliary winding takes over the power supply for the IC when the output voltage rises normally to the set voltage. The lower threshold of VCC is pulled down from VCC_{UVLO} to VCC_{PRO} when a fault condition occurs, such as overload protection (OLP), short-circuit protection (SCP), brown-out, over-voltage protection (OVP), or over-temperature protection (OTP) (see Figure 5).

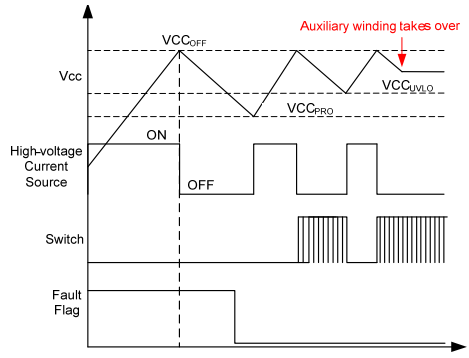

Figure 5: VCC Power Supply Process

Soft Start (SS)

The HF500-40 adopts a soft-start procedure that increases the current limit and switching frequency gradually to reduce stress on the power components.

During soft start, the TIMER capacitor is charged in two steps slowly. The TIMER voltage controls the current limit and switching frequency (see Figure 6).

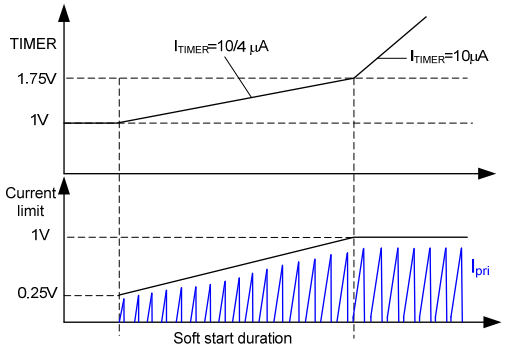

Figure 6: Soft Start

The start-up duration can be adjusted by the capacitor connected to TIMER. The TIMER capacitor determines the start-up duration, shown in Equation (3):

$$T_{Soft-start} = 0.3 \cdot C_{TIMER} / nF \cdot 10^{-3} s \quad (3)$$

Burst Operation

The HF500-40 uses burst-mode operation to minimize power dissipation in no-load or light-load conditions. As the load decreases, V_{FB} decreases. The HF500-40 stops switching when V_{FB} drops below the low threshold (V_{BURL}), which indicates a sufficiently high output voltage. Switching resumes once V_{FB} rises to the high threshold (V_{BURH}), which indicates an insufficient output voltage. This way, the output voltage is regulated. Burst-mode operation enables and disables the switching cycle of the MOSFET alternately, thereby reducing switching loss at no-load or light-load conditions.

Timer-Based Overload Protection (OLP)

If the switching frequency is fixed in a flyback converter, the maximum output power is limited by the peak current. When the load current is larger than the design value, the output voltage drops below the set value due to the max power limit. The current flowing through the primary and secondary optocoupler is reduced, and V_{FB} is pulled high (see Figure 7).

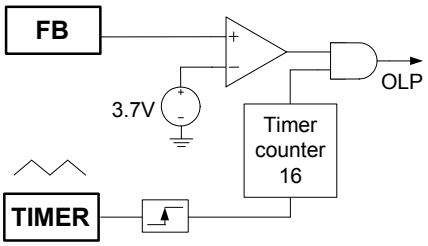

Figure 7: Overload Protection Block

FB rising higher than V_{OLP} is considered to be an error flag and causes the timer to start counting the rising edge of the internal oscillator, which is controlled by TIMER. When the error flag is removed, the timer resets. When the timer has counted to 16, the device enters OLP. This timer-based OLP helps prevent OLP from mistriggering when the power supply is starting up or during a load transition phase (see Figure 8).

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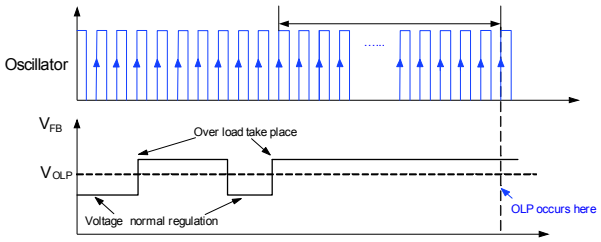

Figure 8: Overload Protection Function

Over-Power Compensation (OPC)

An internal offset proportional to the input voltage is added to the current-sensing voltage. The input voltage (V_{IN}) is sampled by B/O through a resistor divider. This helps equalize the peak current within the entire V_{IN} range by reducing the peak current under a high input voltage. This results in an overall constant OLP point, regardless of V_{IN}. Figure 9 shows the compensation in relation to the voltage on FB and B/O.

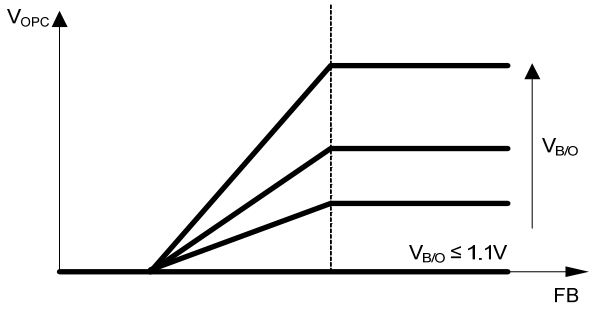

Figure 9: Compensation Voltage vs. FB and B/O

The max OPC voltage (V_{OPC}) can be calculated using Equation (4):

$$V_{OPC} = 0.094 \cdot (V_{B/O} - 1.1V) \quad (4)$$

Input Brown-In/-Out and Input OVP

Input brown-in/out and input OVP are performed through B/O detection.

For the brown-in function, the HF500-40 does not start working until the B/O voltage is higher than V_{B/O_IN}. When the B/O voltage is lower than V_{B/O_OUT}, this is considered to be a brown-out flag. If this condition lasts for $T_{B/O}$, brown-out is triggered, and the HF500-40 stops operation.

OVP is triggered when the B/O voltage is higher than $OVP_{B/O}$ for $T_{OVPB/O}$, and the HF500-40 stops operation.

If the voltage on B/O is higher than V_{DIS}, the input brown-out and input OVP functions are disabled.

If the input brown-in/out, over-power compensation, and input OVP functions are not needed, connect B/O to VCC through a resistor to keep it higher than V_{DIS} under normal operation.

Short-Circuit Protection (SCP)

The HF500-40 features SCP, which senses the SOURCE voltage and stops switching if V_{SOURCE} reaches V_{SCP} after a short leading-edge blanking time for SCP (T_{LEB2}). Once the fault disappears, the power supply resumes operation.

Over-Temperature Protection (OTP)

When the inner temperature of the HF500-40 exceeds T_{OTP}, OTP is triggered. Its switching cycle is kept off by the over-temperature protection logic, and the VCC lower threshold is pulled down from VCC_{UVLO} to VCC_{PRO}. The HF500-40 resumes operation once the temperature drop exceeds $T_{OTP(HYS)}$.

VCC Over-Voltage Protection (OVP)

The HF500-40 enters an auto-restart fault condition if the VCC voltage rises above V_{OVP} for T_{OVP}. Typically, VCC OVP is used for indirect output OVP. This occurs when the optocoupler fails, resulting in the loss of the output voltage regulation.

TIMER Protection

The HF500-40 is latched off by pulling TIMER below $V_{TIMER(LATCH)}$ for T_{LATCH}. This allows external OVP, OTP, or other functions to be used on TIMER to set extra protections.

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Leading-Edge Blanking (LEB)

An internal leading-edge blanking (LEB) unit containing two LEB times is used to prevent a premature switching pulse termination due to MOSFET turn-on current spikes, which are caused by parasitic capacitance. During the blanking time, the current comparator is disabled and cannot turn off the MOSFET (see Figure 10).

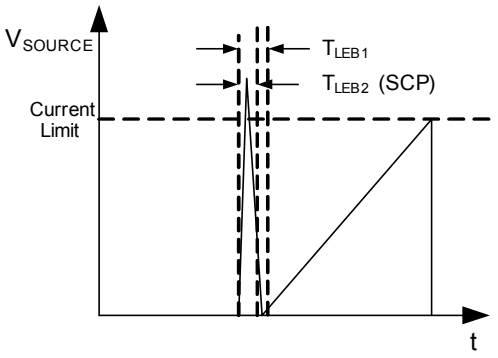

Figure 10: Leading-Edge Blanking

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APPLICATION INFORMATION

VCC Capacitor Selection

When input voltage is applied, the VCC capacitor is charged up by the IC internal high-voltage current source. VCC should be held above VCC_{UVLO} until the output voltage builds up so that VCC is supplied by the auxiliary winding. Otherwise, VCC_{UVLO} terminates the switching, and the output voltage cannot be set normally. For most applications, choose a VCC capacitor value between 10μF and 47μF. The value for the VCC capacitor can be estimated with Equation (5):

$$C_{VCC} > \frac{I_{CC} * T_{rise}}{VCC_{OFF} - VCC_{UVLO}} \quad (5)$$

Where I_{CC} is the internal IC consumption, and T_{rise} is the output voltage rise period.

Primary-Side Inductor Design (Lm)

The HF500-40 uses internal slope compensation to support CCM and duty cycle exceeding 50% working condition. Indicate the CCM depth with K_P, which is the ratio between the primary inductor's ripple current and peak current ($0 < K_P \leq 1$, and $K_P = 1$ stands for discontinuous conduction mode (DCM)) (see Figure 11). An optimal K_P value is between 0.6 and 0.8 for the universal input range, and CrCM or DCM for the 230V_{AC} input range. A large inductance leads to a smaller K_P, which reduces the RMS current but increases the transformer size.

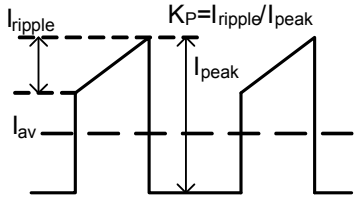

Figure 11: Typical Primary Current Waveform

The input power (P_{in}) at the minimum input can be estimated with Equation (6):

$$P_{in} = \frac{V_O \cdot I_O}{\eta} \quad (6)$$

Where V_O is the output voltage, I_O is the rated output current, and η is the estimated efficiency. η is between 0.75 and 0.85 typically, depending on the input range and output voltage.

For CCM at minimum input voltage, calculate the converter duty cycle with Equation (7):

$$D = \frac{(V_O + V_F) \cdot N}{(V_O + V_F) \cdot N + V_{in(min)}} \quad (7)$$

Where V_F is the secondary diode's forward voltage, N is the transformer turns ratio, and $V_{in(min)}$ is the minimum voltage on the bulk capacitor.

The MOSFET on time is calculated with Equation (8):

$$T_{on} = D \cdot T_s \quad (8)$$

Where T_s is the switching cycle period, and T_S is $1/f_{OSC}$.

The average value of the primary current can be calculated with Equation (9):

$$I_{av} = \frac{P_{in}}{V_{in(min)}} \quad (9)$$

The peak value of the primary current can be calculated with Equation (10):

$$I_{peak} = \frac{I_{av}}{(1 - \frac{K_P}{2}) \cdot D} \quad (10)$$

The ripple value of the primary current can be calculated with Equation (11):

$$I_{ripple} = K_P \cdot I_{peak} \quad (11)$$

The valley value of the primary current can be calculated with Equation (12):

$$I_{valley} = (1 - K_P) \cdot I_{peak} \quad (12)$$

L_m can be calculated with Equation (13):

$$L_m = \frac{V_{in(min)} \cdot T_{on}}{I_{ripple}} \quad (13)$$

Current-Sense Resistor

Figure 12 shows the peak current comparator logic and the subsequent waveform. When the sum of the sensing resistor voltage and the slope compensator reaches V_{limit}, the comparator goes high to reset the RS flip-flop, and the MOSFET turns off.

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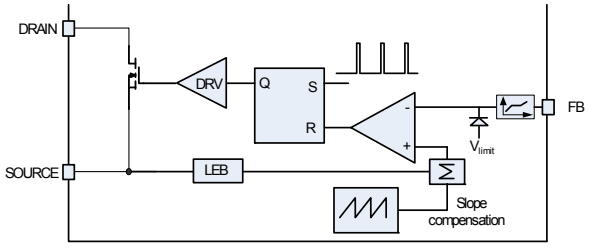
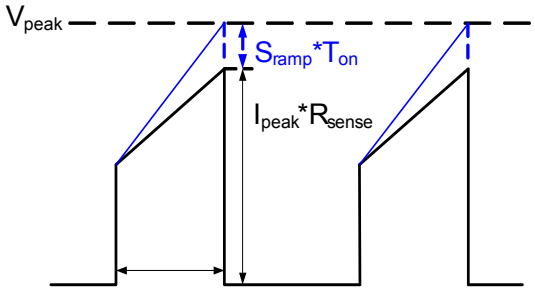


a) Peak Current Comparator Circuit



b) Typical Waveform

Figure 12: Peak Current Comparator

The maximum current limit is V_{ILIM}. The ramp of the slope compensator is S_{RAMP}. Given a certain margin, use 0.95 x V_{ILIM} as V_{peak} at full load. Calculate the voltage on the sensing resistor with Equation (14):

$$V_{sense} = 95\% \cdot V_{ILIM} - S_{RAMP} \cdot T_{on} \quad (14)$$

The value of the sense resistor is then calculated with Equation (15):

$$R_{sense} = \frac{V_{sense}}{I_{peak}} \quad (15)$$

Select a current-sense resistor with an appropriate power rating. Estimate the sense resistor power loss with Equation (16):

$$P = \left[\left(\frac{I_{peak} + I_{valley}}{2} \right)^2 + \frac{1}{12} \left(I_{peak} - I_{valley} \right)^2 \right] \cdot D \cdot R_{sense} \quad (16)$$

Jitter Period

Frequency jitter is used as an effective method for reducing EMI by dissipating energy. The n_{th} order harmonic noise bandwidth is $B_{Tn} = n \cdot (2 \cdot \Delta f + f_{jitter})$, where Δf is the frequency jitter amplitude. If B_{Tn} exceeds the resolution bandwidth (R_{BW}) of the spectrum analyzer (200Hz for noise frequency less than 150kHz, 9kHz for noise frequency between 150kHz and 30MHz), the spectrum analyzer receives less noise energy.

Equation (2) describes the jitter period in theory. A smaller f_{jitter} is more effective for EMI reduction. However, the measurement bandwidth requires f_{jitter} to be large compared to the spectrum analyzer R_{BW} for effective EMI reduction. f_{jitter} should also be less than the control loop gain crossover frequency to avoid disturbing the output voltage regulation.

The TIMER capacitor must be selected carefully. A capacitor that is too large may cause the start-up to fail at full load because of the long, soft start-up duration, shown in Equation (3). However, a TIMER capacitor that is too small causes the timer period to decrease, which overloads the timer count capability and may cause logic problems. For most applications, a f_{jitter} between 200Hz and 400Hz is recommended.

Ramp Compensation

In peak current control, sub-harmonic oscillation occurs when D is greater than 0.5 in CCM. The HF500-40 solves this problem with internal ramp compensation. Calculate α with Equation (17):

$$\alpha = \frac{\frac{D_{max} \cdot V_{in(min)}}{(1-D_{max}) \cdot L_m} \cdot R_{sense} - m_a}{\frac{V_{in(min)}}{L_m} \cdot R_{sense} + m_a} \quad (17)$$

Where m_a = 18mV/μs is the minimum internal slope value of the compensation ramp. $\frac{V_{in(min)}}{L_m}$ and $\frac{D_{max} \cdot V_{in(min)}}{(1-D_{max}) \cdot L_m}$ are the current slew rates of primary side and secondary side converted to the primary side, respectively. For stable operation, α must be less than 1.

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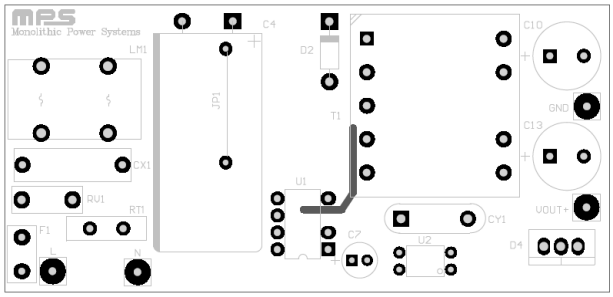
PCB Layout Guidelines

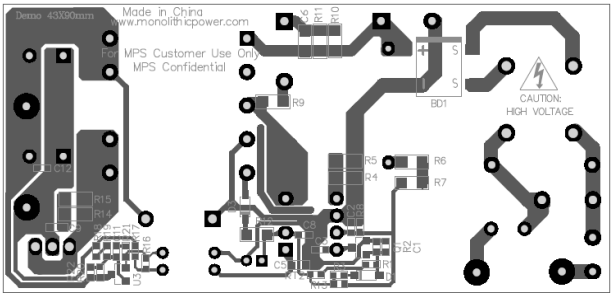
Efficient PCB layout is critical for stable operation, good EMI performance, and good thermal performance. For best results refer to Figure 13 and follow the guidelines below.

1. Minimize the loop area formed by the input capacitor, the transformer's primary winding, the MOSFET DRAIN and SOURCE of the HF500-40, and the sensing resistor to reduce EMI noise.
2. Minimize the voltage jumping area, such as the MOSFET drain, the anode of the secondary diode, etc. for better EMI.

   DRAIN of the HF500-40 is a fused lead pin, which helps with thermal radiation when copper is connected to it. Make a trade-off between EMI and thermal performance if necessary.
3. Minimize the snubber circuit loop to reduce EMI.
4. Minimize the secondary loop area of the output diode and output filter to reduce EMI noise.
5. Provide sufficient copper areas at the cathode terminal of the output diode to act as a heat sink.
6. Place the AC input far away from the switching nodes to minimize any noise coupling that may bypass the input filter.
7. Place the bypass capacitor as close to the IC as possible.
8. Use a single-point connection at the negative terminal of the input filter capacitor for the IC GND and bias winding return.



Top



Bottom

Figure 13: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

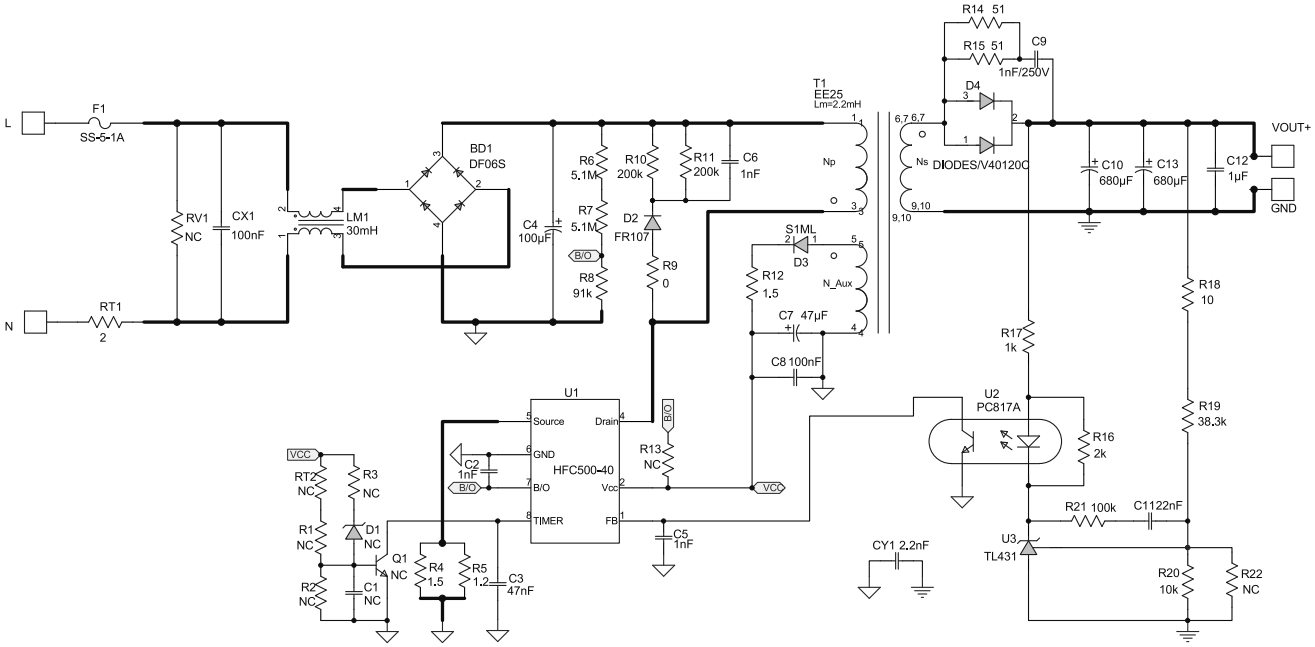

Figure 14: Example of a Typical Application

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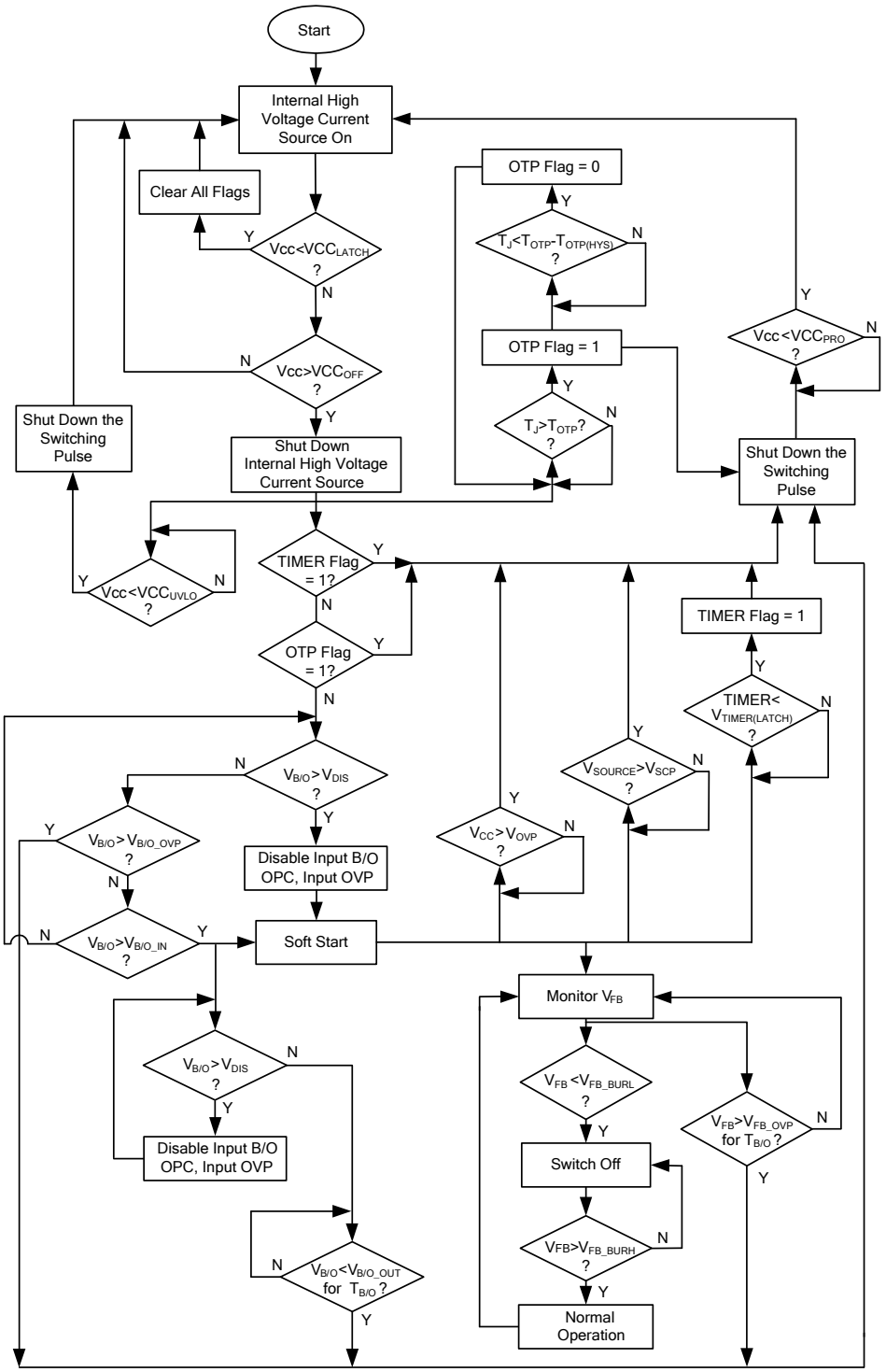
FLOW CHART



VCC UVLO, brown-out, VCC OVP, OLP and OTP are auto restart, only TIMER is latch off mode.
VCC should drop to VCC_{LATCH} to release from the latch condition, usually by disconnecting the input.

Figure 15: Flow Chart

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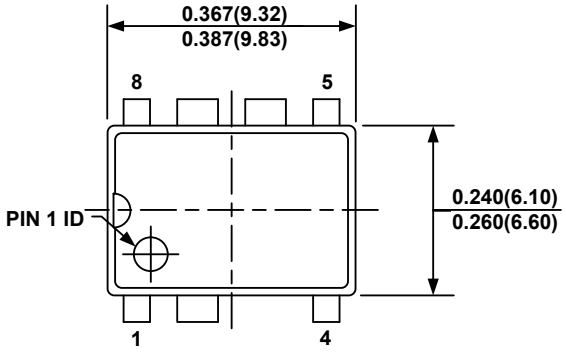
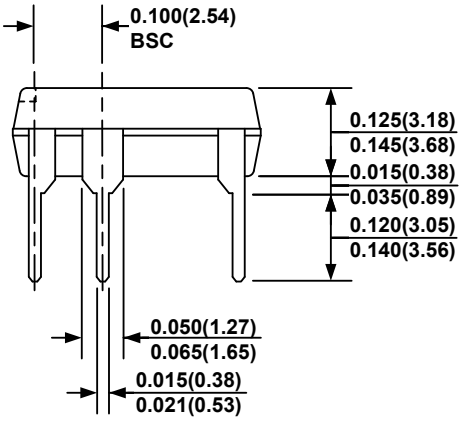
PACKAGE INFORMATION

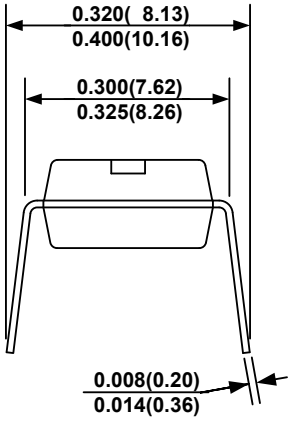
PDIP8-7B



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH, OR PROTRUSIONS.
3) JEDEC REFERENCE IS MS-001.
4) DRAWING IS NOT TO SCALE.

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