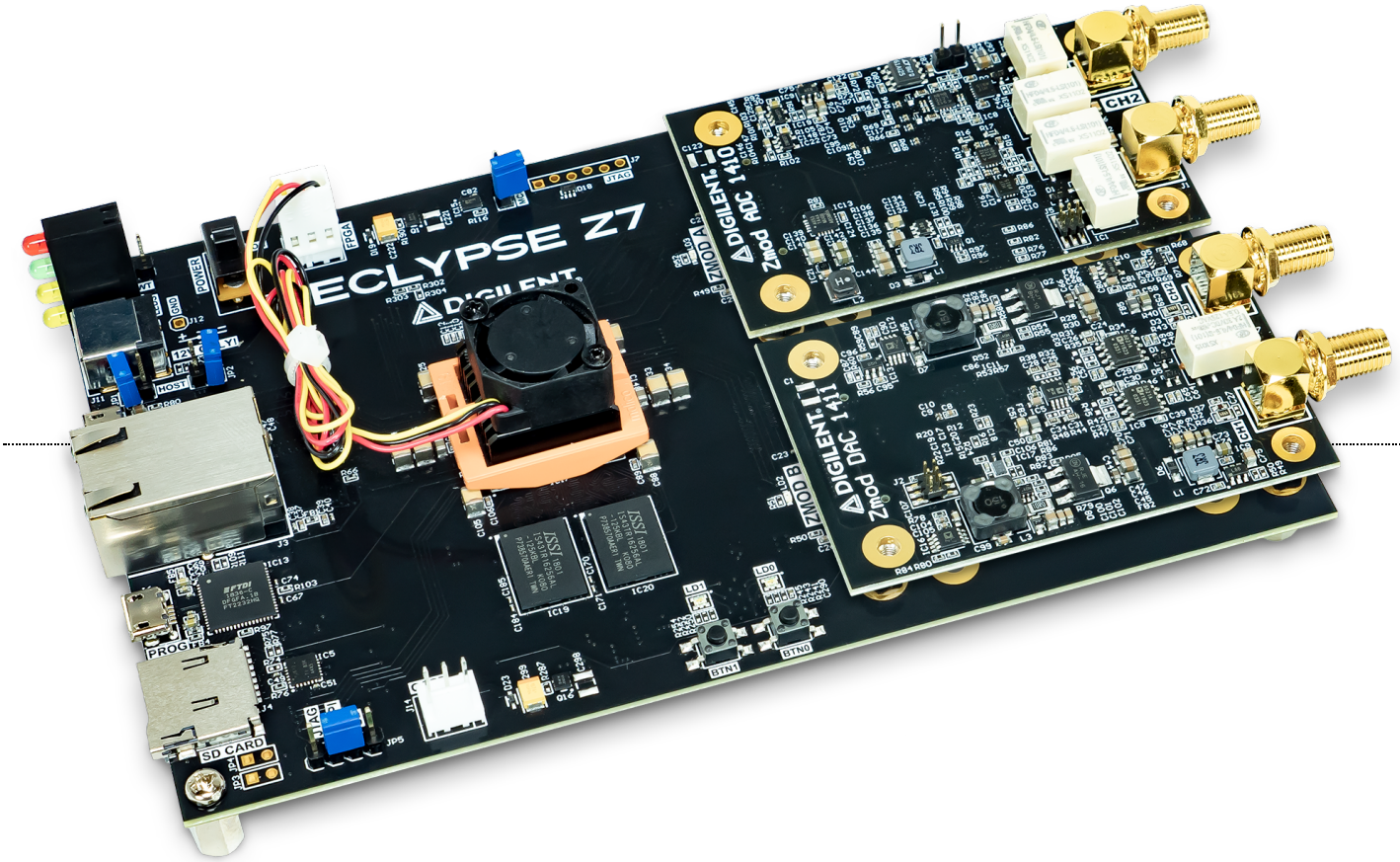
Eclypse Z7 Hardware Reference Manual

The Eclypse Z7 is a powerful prototyping platform, featuring Xilinx's Zynq-7000 APSoC. Two SYZYGY interface connectors are featured, enabling high speed modular systems.

Eclypse is designed to enable high speed analog data capture and analysis right out of the box. It is a platform for research and rapid prototyping of test and measurement applications, potentially including software defined radio, ultrasound, other medical devices, and much more. As a host board for Zmods (https://reference.digilentinc.com/reference/zmod/start), applications for the Eclypse can vary significantly between system configurations.

Petalinux is supported out of the box. Pre-built Linux images are accompanied by a software API for bulk data transfer. This system allows new users to get started without touching hardware until desired. The software supports a variety of common programming languages, including Python, C/C++, and more. Digilent offers fully open and customizable hardware designs, Linux images, and Linux software applications.



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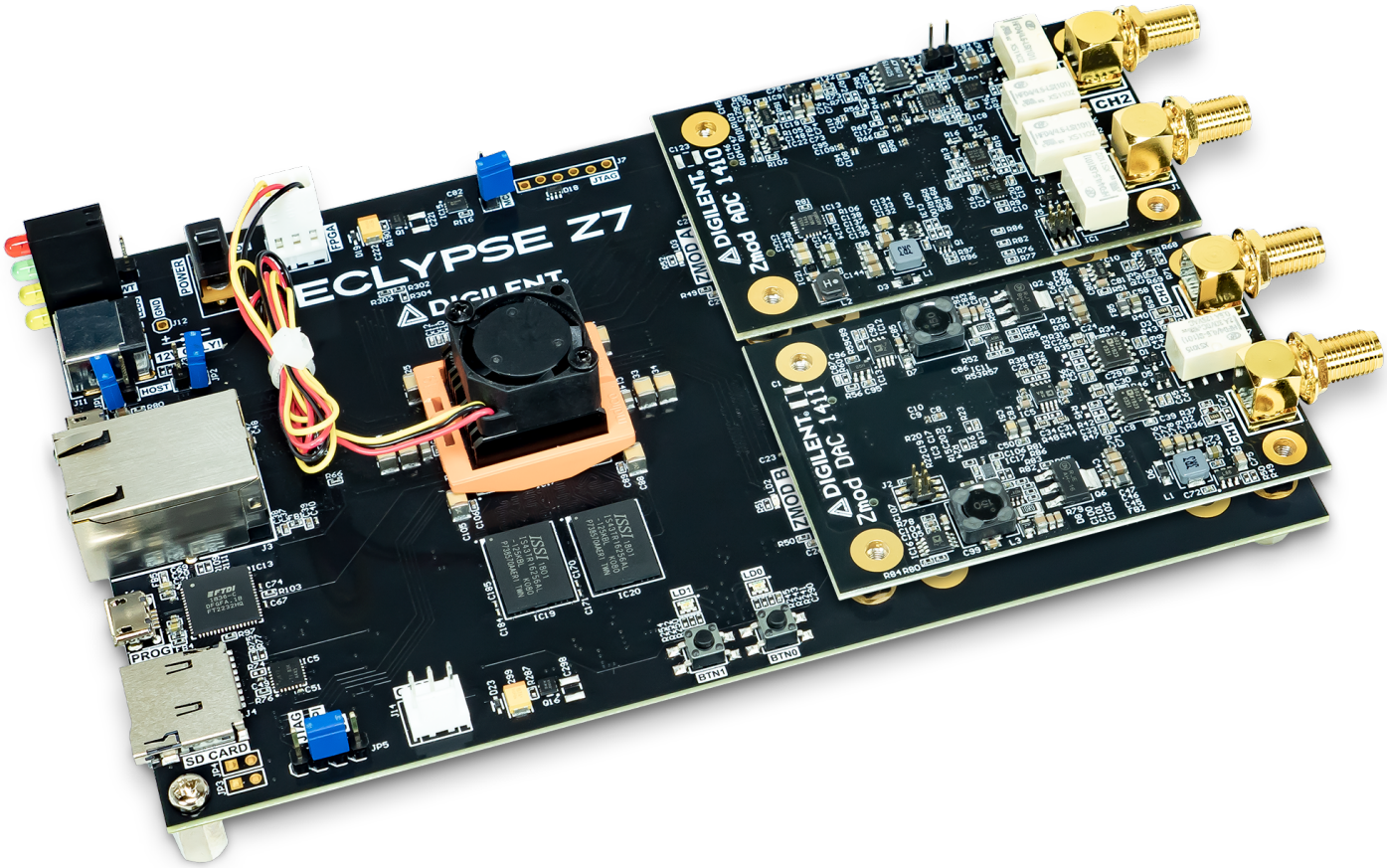
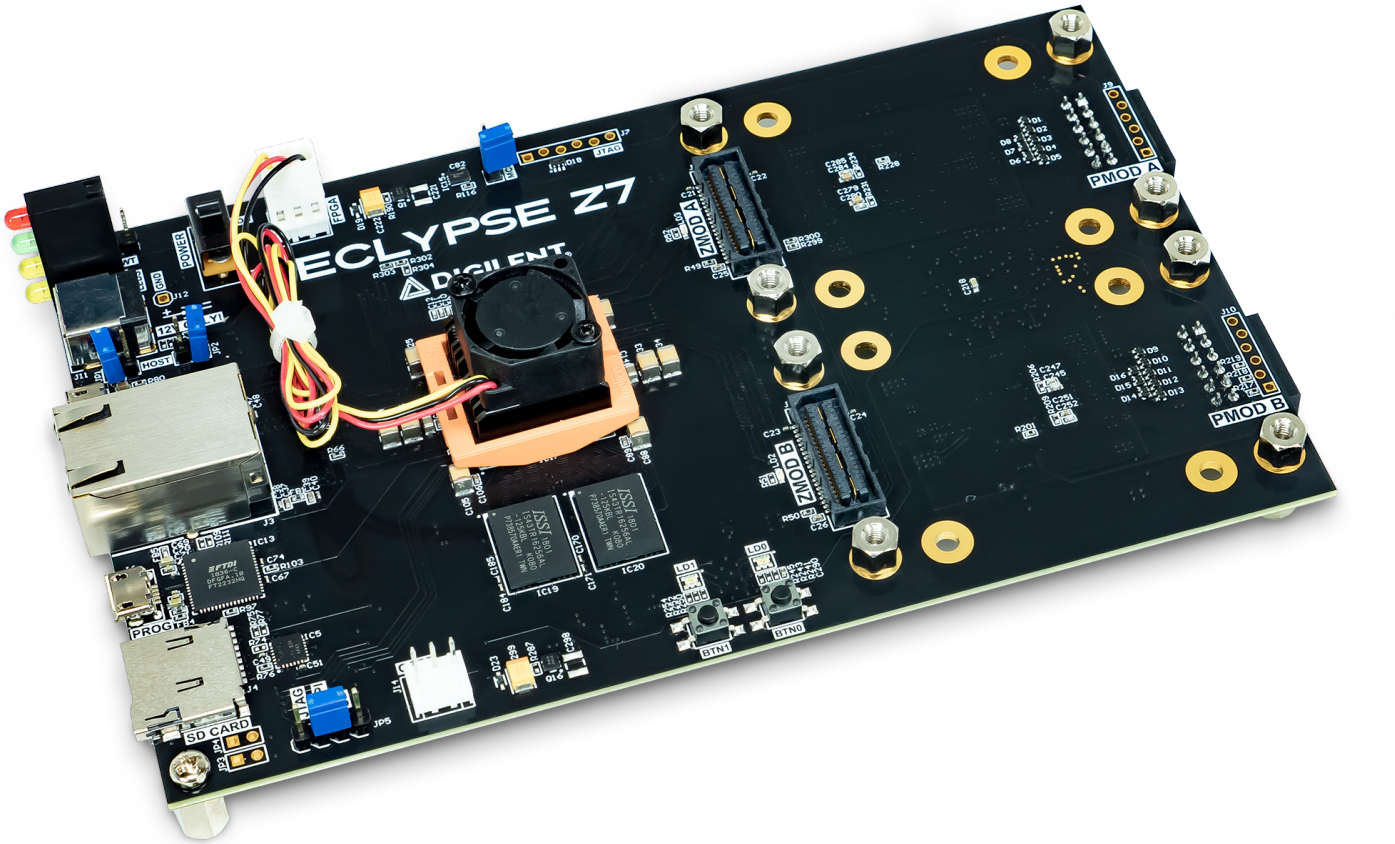

ECLYPSE Z7
DIGILENT
Zmod ADC 1410
Zmod DAC 1411
CH1
CH2
ZMOD A
ZMOD B
JTAG
POWER
PROG
SD CARD
BTN0
BTN1


ECLYPSE Z7
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PMOD A
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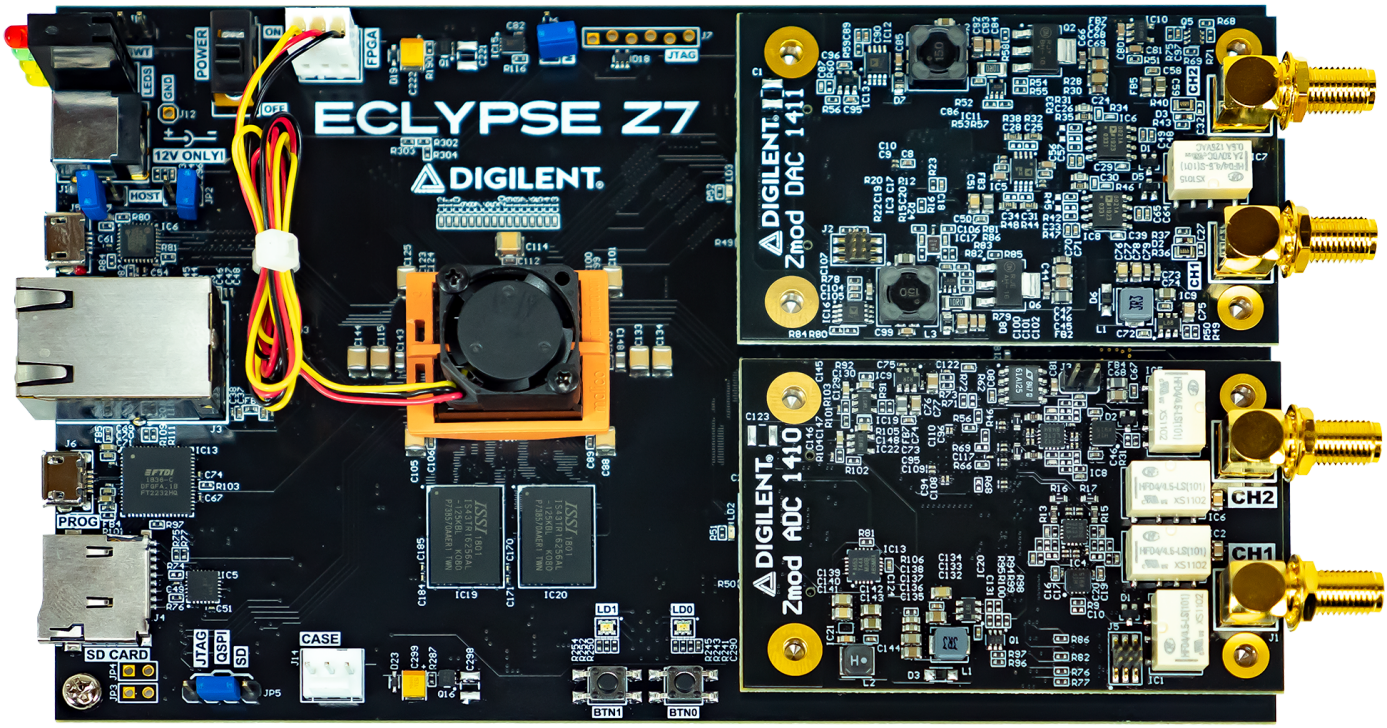
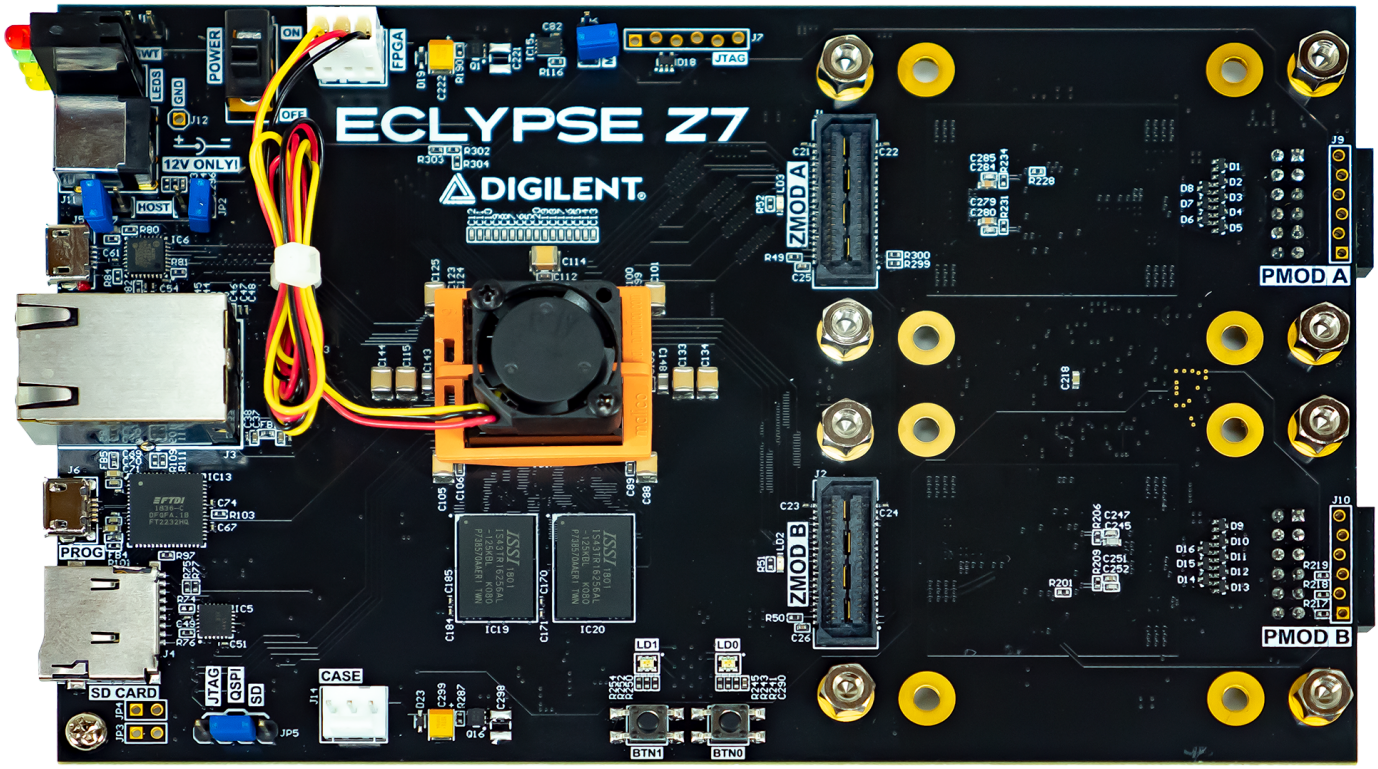
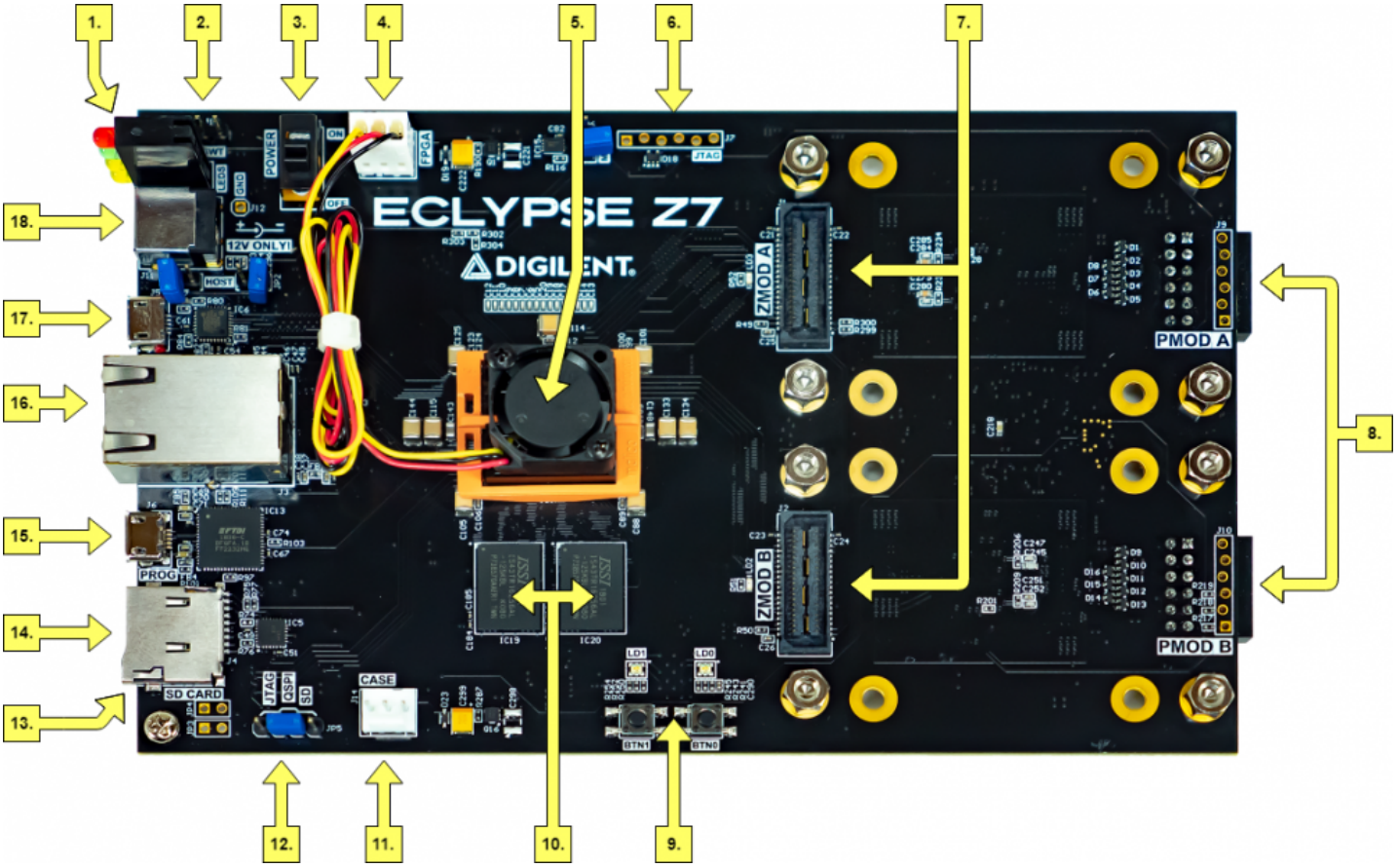




Features

- **Zynq-7000 APSoC (XC7Z020-1CLG484C)**
  - 667 MHz dual-core Cortex-A9 processor
  - DDR3L memory controller with 8 DMA channels and 4 High Performance AXI3 Slave ports
  - High-bandwidth peripheral controllers: 1G Ethernet, USB 2.0, SDIO
  - Low-bandwidth peripheral controllers: SPI, UART, CAN, I2C
  - Programmable from JTAG, Quad-SPI flash, and microSD card
  - Programmable logic equivalent to Artix-7 FPGA
- **Memory**

    - 1 GiB DDR3L with 32-bit bus @ 1066 MT/s
    - 16 MB () Quad-SPI Flash with factory programmed 128-bit random number and 48-bit globally unique EUI-48/64™ compatible identifier
    - microSD card slot
- **Power**
    - Powered from external 12V 5A supply
    - Platform MCU for configuration of adjustable power supplies and temperature management
- **USB and Ethernet**
    - Gigabit Ethernet PHY
    - USB-JTAG programming circuitry
    - USB-UART bridge
    - USB micro AB port with USB 2.0 PHY with Host/Device/OTG capabilities
- **Zmod Ports**
    - 2 ports following the SYZYGY Standard interface specification
    - Compatible with a variety of SYZYGY pods, allowing for a wide variety of applications
    - Dedicated differential clocks for input and output
    - 8 differential I/Os per port
    - 16 single-ended I/Os per port
    - DNA interfaces connected to Platform MCU allowing for various auto-negotiated power supply configurations
- **Pmod Ports**
    - 2 twelve-pin ports for a total of 16 FPGA-connected I/Os
    - High speed voltage translation and protection circuitry
- **User GPIO ()**
    - 2 push-buttons
    - 2 RGB LEDs



(https://reference.digilentinc.com/_detail/reference/programmable-logic/eclypse-z7/reference-manual/eclypse-callout.png?id=reference%3Aprogrammable-logic%3Aeclypse-z7%3Areference-manual) *Eclypse Z7 Callout Diagram*

Callout #	Description	Callout #	Description	Callout #	Description

Callout #	Description	Callout #	Description	Callout #	Description
1	Board Indicator LEDs (LD4)	7	SYZYGY Ports	13	Reset Buttons (underside of board)
2	Header for Case Power Switch	8	Pmod Ports	14	microSD Card Slot
3	Power Switch	9	User Buttons and LEDs	15	USB JTAG/UART Port
4	FPGA Fan Header	10	DDR3L Memory	16	Ethernet Port
5	Zynq-7000 SoC and FPGA Fan	11	Case Fan Header	17	USB AB Host/Device/OTG Port
6	External JTAG Port	12	Programming Mode Select Jumper	18	Power Supply Connector

Purchasing Options

The Eclypse Z7 includes an FPGA fan to dissipate extra heat generated from running complex fast-switching designs. A USB A to Micro B programming cable, a USB A to Micro A cable, and a 12V 5A power supply, are included with the Eclypse Z7.

An Eclypse Z7 Enclosure Kit may optionally be added on, which provides a sturdy case for the Eclypse platform. The Enclosure Kit includes a case fan for additional cooling, and exposes the connectors of loaded Zmod ADCs and DACs, as well as the Eclypse Z7's Pmod expansion connectors, power switch, status LEDs, and more.

For more information on purchasing an Eclypse Z7, see the Eclypse Z7 Product Page (https://store.digilentinc.com/eclypse-z7-zynq-7000-soc-development-board-with-syzygy-compatible-expansion/).

Digilent Zmods (https://reference.digilentinc.com/reference/zmod/start) may also be purchased individually or bundled with the Eclypse Z7. Expansion connectors such as these, or other SYZYGY modules, are required to fully leverage the high-speed I/O capabilities of the Eclypse platform.

Software Support

Zynq platforms are well-suited to be embedded Linux targets, and the Eclypse Z7 is no exception. Digilent provides software examples targeting custom Petalinux projects, including support for each Digilent Zmod for high-speed I/O capabilities.

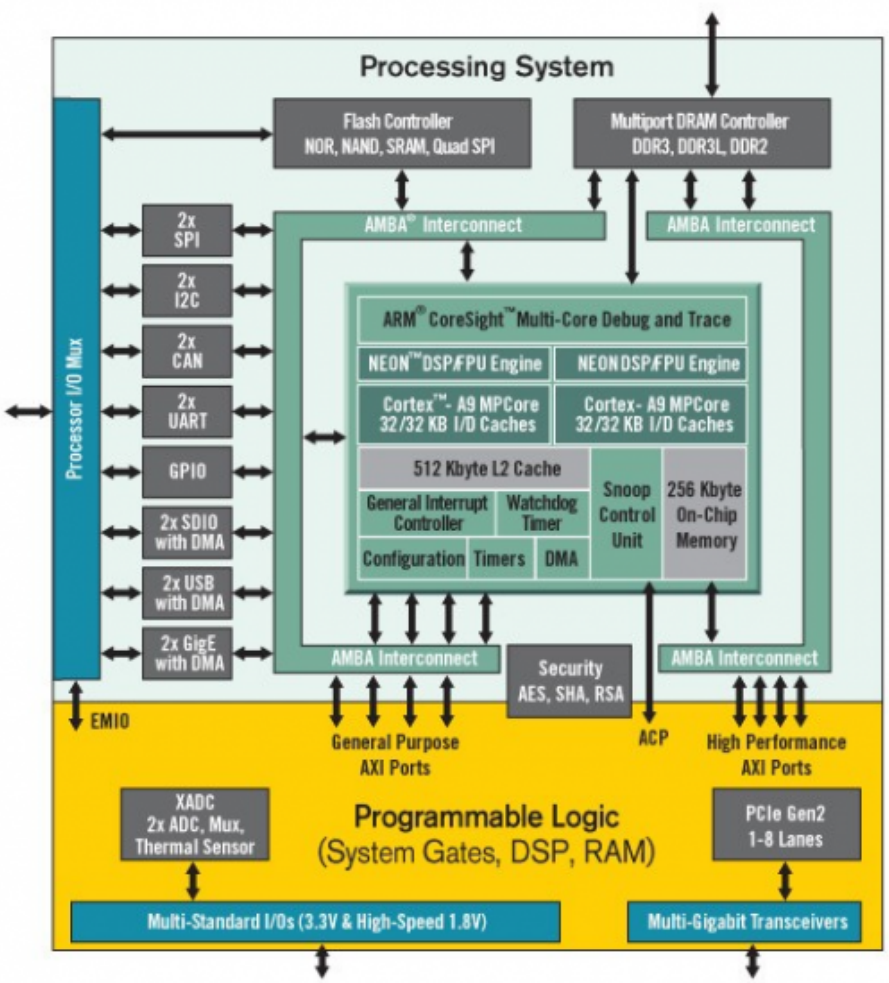
The Eclypse Z7 is fully compatible with Xilinx's high-performance Vivado ® Design Suite. This tool set melds FPGA logic design and embedded ARM software development into an easy to use, intuitive design flow. It can be used for designing systems of any complexity, from a complete operating system running multiple server applications, down to a simple bare-metal program that controls some LEDs. It is also possible to treat the Zynq AP SoC as a standalone FPGA for those not interested in using the processor in their design. The Eclypse Z7 is supported under Vivado's free WebPACK™ license, which means the software is completely free to use, including the Logic Analyzer and High-level Synthesis (HLS) features. The Logic Analyzer assists with debugging logic that is running in hardware, and the HLS tool allows C code to be directly compiled into HDL.

Digilent currently does not provide hardware platforms or examples for Xilinx's Vitis Unified Software Platform, however Vitis support is planned for the near future.

Design resources, example projects, and tutorials are available for download at the Eclypse Z7 Resource Center (https://reference.digilentinc.com/reference/programmable-logic/eclypse-z7/start).

Zynq APSoC Architecture

The Zynq APSoC is divided into two distinct subsystems: The Processing System (PS) and the Programmable Logic (PL). The figure below shows an overview of the Zynq APSoC architecture, with the PS colored light green and the PL in yellow. Note that the PCIe Gen2 controller and Multi-gigabit transceivers are not available on the Zynq-7020 device.



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The PL is nearly identical to a Xilinx 7-series Artix FPGA, except that it contains several dedicated ports and buses that tightly couple it to the PS. The PL also does not contain the same configuration hardware as a typical 7-series FPGA, and it must be configured either directly by the processor or via the JTAG port.

The PS consists of many components, including the Application Processing Unit (APU, which includes 2 Cortex-A9 processors), Advanced Microcontroller Bus Architecture (AMBA) Interconnect, DDR3 Memory controller, and various peripheral controllers with their inputs and outputs multiplexed to 54 dedicated pins (called Multiplexed I/O, or MIO pins). Peripheral controllers that do not have their inputs and outputs connected to MIO pins can instead route their I/O through the PL, via the Extended-MIO (EMIO) interface. The peripheral controllers are connected to the processors as slaves via the AMBA interconnect, and contain readable/writable control registers that are addressable in the processors' memory space. The programmable logic is also connected to the interconnect as a slave, and designs can implement multiple cores in the FPGA fabric that each also contain addressable control registers. Furthermore, cores implemented in the PL can trigger interrupts to the processors and perform DMA accesses to DDR3 memory.

There are many aspects of the Zynq APSoC architecture that are beyond the scope of this document. For a complete and thorough description, refer to the Zynq Technical Reference manual (http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf).

The tables in the dropdowns below depict the external components connected to the MIO pins of the Eclypse Z7. The Vivado board files found on the Eclypse Z7 Resource Center (https://reference.digilentinc.com/reference/programmable-logic/eclypse-z7/start) can be used to properly configure the PS to work with these peripherals. It is also possible to use the example projects found on the resource center as a starting point for custom designs.

MIO 0-15 : Bank 500

MIO 500 3.3 V	**Peripherals**				
Pin	GPIO ()	SPI Flash	ENET 0	SYZYGY	UART 0

0 (N/C)					
1		CS ()			
2		DQ0			
3		DQ1			
4		DQ2			
5		DQ3			
6		SCLK ()			
7 (N/A)					
8		SCLK () FB			
9			Ethernet Reset		
10 (N/A)					
11 (N/A)					
12				DNA SCL (I2C 0)	
13				DNA SDA (I2C 0)	
14					UART Input
15					UART Output

MIO 16-53 : Bank 501

MIO 501 1.8V	**Peripherals**		
Pin	ENET 0	USB 0	SD 0
16	TXCK		
17	TXD0		
18	TXD1		
19	TXD2		
20	TXD3		
21	TXCTL		
22	RXCK		
23	RXD0		
24	RXD1		

25	RXD2		
26	RXD3		
27	RXCTL		
28		DATA4	
29		DIR	
30		STP	
31		NXT	
32		DATA0	
33		DATA1	
34		DATA2	
35		DATA3	
36		CLK	
37		DATA5	
38		DATA6	
39		DATA7	
40			CCLK
41			CMD
42			D0
43			D1
44			D2
45			D3
46		USB Reset	
47			CD
48	Ethernet Interrupt (GPIO ())		
49		USB Overcurrent (GPIO ())	
50 (N/C)			
51 (N/C)			
52	MDC		
53	MDIO		

Functional Description

1. Power Supplies

The Eclypse Z7 power circuitry was carefully designed to meet the requirements of the Zynq-7000 and all peripherals while providing the flexibility needed to power a variety of different configurations of Zmod/SYZYGY modules.

An overview of the power circuit is shown in Figure 1.1.

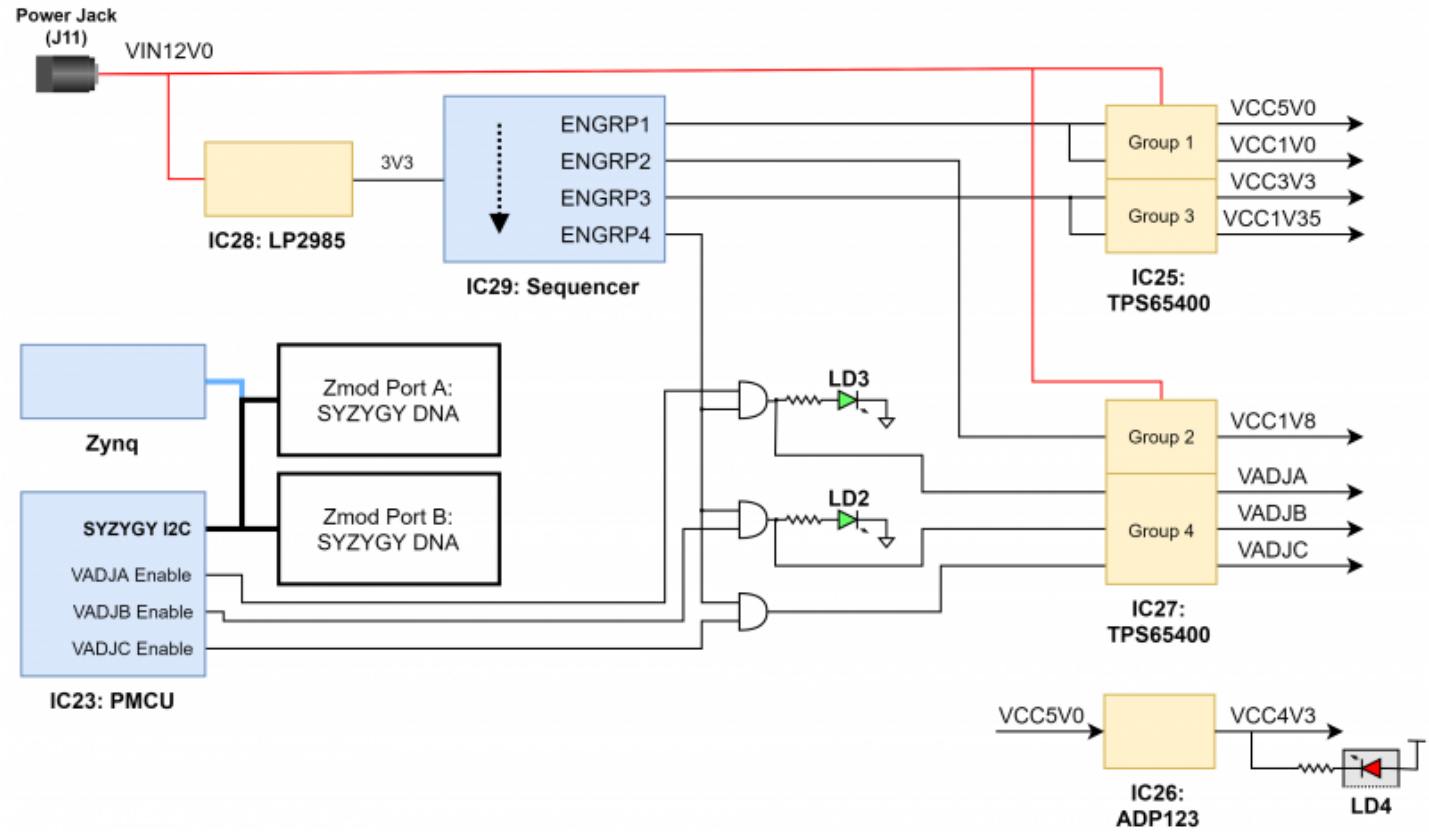

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Figure 1.1: Power circuit overview

All on-board power supplies are enabled or disabled by the power switch (SW1) or by an external SPST switch connected to the SWT header (J13).

Note: *If an external switch is used, SW1 should be placed in the "OFF" position, as the two will be placed in parallel.*

The power indicator LED, the topmost LED of the circuit board indicator (LD4), is illuminated red when all supply rails reach their nominal voltage.

Two additional indicator LEDs are illuminated when the VIO supplies associated with the two Zmod Ports are powered. LD2 is associated with Zmod Port A and the VADJA rail. LD3 is associated with Zmod Port B and the VADJB rail.

1.1. Power Input Source

The Eclypse Z7 should be powered via a wall wart supply with barrel jack, via the barrel connector (J11). The supply must use a center-positive 2.1 mm internal-diameter plug and deliver between 11.5V and 12.5V DC. It should also be able to provide at least 5 A (60 Watts) in order to support power hungry Zynq projects and external peripherals. A compatible power supply ships with the Eclypse Z7.

Table 1.1.1: Eclypse Z7 Power Input Specifications

Connector Type	Connector Label	Schematic Net Name	Min/Rec/Max Voltage (V)	Max Current Consumption
Barrel jack	J11	VIN12V0	11.5/12/12.5	5 A / 60 W

1.2. Power Specifications

Table 1.2.1 describes the characteristics of the Eclypse Z7's on-board power rails. It can be used to estimate power consumption for a project, or determine how much current attached peripherals can draw before being limited.

Table 1.2.1: Eclypse Z7 Power Rail Specifications

Net Name	Upstream Net Name	Power IC Type	Power IC Label	Min/Typ/Max Voltage	Max. Current	Major Devices and Connectors
VCC5V0	VIN12V0	Buck	IC27	5.0V +-5%	3A	Zmods, USB OTG VBUS, RGB LEDs, Case Fan
VCC1V0	VIN12V0	Buck	IC27	1.0V +-5%	1A	Zynq, Ethernet, USB OTG, USB JTAG/UART, microSD
DDR1V35	VIN12V0	Buck	IC25	1.35V +-5%	2A	Zynq, DDR3L
DDRVTT	VIN12V0	LDO	IC21	0.675V +-5%	0.45A	DDR3L
VCC3V3	VIN12V0	Buck	IC25	3.3V +-5%	3.3A	Zynq, Zmods, Pmods, USB OTG, USB JTAG/UART, microSD
VCC4V3	VCC5V0	LDO	IC26	4.3V +-5%	0.3A	Pmods
VADJA	VIN12V0	Buck	IC27	1.2V to 3.3V; +-5%	1.8A	FPGA, Zmod Port A
VADJB	VIN12V0	Buck	IC27	1.2V to 3.3V; +-5%	1.8A	FPGA, Zmod Port B
VADJC	VIN12V0	Buck	IC25	2.5 to 5.5V; +-5%	0.3A	FPGA Fan

The power budget of VCC5V0 is shared by the SYZYGY ports, USB OTG VBUS, RGB LEDs, and Case Fan. As such, the actual maximum current achievable by each peripheral varies with the Eclypse Z7's system configuration. Under worst-case conditions, VCC5V0 is capable of outputting a minimum of 3A of continuous current. In this scenario, 1A is budgeted for each Zmod

The Platform MCU (PMCU) enumerates the SYZYGY ports and determines the power needs of each Zmod installed in the system. The 5V power budget of the Eclypse is then determined based on the needs of each Zmod, as well as the USB OTG VBUS, RGB LEDs, and Fan. Table 1.2.2 describes the 5V power budget of the Eclypse Z7 in more detail.

Table 1.2.2: Eclypse 5V Power Budget

Device or Connector	Max Current (mA)
RGB LEDs	124.8
USB OTG VBUS	500
Zmod Port A	1000
Zmod Port B	1000
Case Fan	250

The two SYZYGY ports share a budget of 2A from the 3.3V supply. The two Pmod ports share a budget of 0.5A, which is allocated to the SYZYGY ports if no Pmods are installed.

Due to the requirements of the custom power sequencer (IC29), Digilent recommends that peripheral modules (Pmods and Zmods) attached to and powered by the Eclypse meet the specifications described in Table 1.2.3.

Table 1.2.3: Recommended Maximum Additional Capacitance for Add-on Modules

Port	Rail	Max Capacitance (µF)
Zmod Port A	VCC5V0	500
Zmod Port A	VCC3V3	500
Zmod Port A	VIO	1000
Zmod Port B	VCC5V0	500
Zmod Port B	VCC3V3	500
Zmod Port B	VIO	1000
Pmod Port A	VCC3V3	500
Pmod Port B	VCC3V3	500

1.3. Power Sequencing

A custom power sequencer (IC29) is used to sequence the power supplies on in the correct order when the power switch is placed in the "ON" position. The power supplies shut down in the opposite order when the power switch is moved to the "OFF" position. The startup sequence is as follows:

1. VCC5V0, FAN5V0
2. VCC1V0
3. VCC1V8
4. DDR1V35, DDRVTT
5. VCC3V3
6. VCC4V3
7. VADJA, VADJB, VADJC

The sequencer is provided 3.3V power by a dedicated regulator, a Texas Instruments LP2985 (IC28).

The sequencer ensures that the supply rails follow the Xilinx-recommended start-up and shut-down sequences.

Note: *VADJA, VADJB, and VADJC are controlled by the Platform MCU (PMCU) and may or may not be enabled, depending on the PMCU configuration and presence (or lack thereof) of any pods connected to Zmod A or Zmod B. If the sum of the currents required by each Zmod is in excess of the 3A budget for VCC5V0, VADJA and VADJB are not turned on.*

1.4. FPGA Fan

The FPGA fan is to be connected to the Eclypse Z7 via fan header J8 (labeled "FPGA") and is powered by VADJC, an adjustable rail controlled by the Platform MCU. The FPGA fan's speed can be configured to Automatic (the default factory setting), High, Medium, Low, or Off, by communicating with the PMCU through its I2C interface. This configuration is preserved by the PMCU in an EEPROM () when the Eclypse's power is cycled. Additional information and configuration settings, including RPM and speed controls, can be accessed through the PMCU's I2C interface.

1.5. Case Fan

In addition to the FPGA fan, the Eclypse Z7 can power a Case Fan, connected to the board via fan header J14 (labeled "CASE"). This fan is powered by the 5V rail, and is limited to 250 mA. A compatible fan is included in the Eclypse Z7 Enclosure Kit (https://store.digilentinc.com/eclypse-z7-enclosure-kit/).

1.6. Platform MCU

As noted in previous sections, the Eclypse Z7 uses an Atmega328PB microcontroller (IC10), referred to as the Platform MCU (PMCU), to implement the SmartVIO requirements of the SYZYGY standard, as well as to monitor the Zynq die temperature, and to control the Eclypse's fan.

When the Eclypse is turned on, the PMCU enumerates the pods attached to the Eclypse's SYZYGY ports and retrieves their DNA, in order to correctly configure the variable supplies.

After SYZYGY enumeration is complete, the PMCU configures itself as an I2C slave device with a chip address of 0x60. Control of the I2C bus is then handed over to the Zynq's I2C 1 peripheral (MIO[12:13]). The Digilent Eclypse Utility (decutil) is included in Petalinux images for the Eclypse Z7 and can be used to get status information from and change some settings of the PMCU. For more information on the PMCU's register space and communication protocol, see the PMCU specification (PDF Download (https://digilent.s3-us-west-2.amazonaws.com/resources/programmable-logic/eclypse/Eclypse-PMCU-Specification-Public.pdf)). For more information on decutil, see the Digilent Eclypse Utility Documentation (https://reference.digilentinc.com/_media/reference/programmable-logic/eclypse-z7/decutil.1.pdf).

The following tables describe the features of the Platform MCU supported by the Eclypse Z7:

Table 1.6.1: Platform MCU Connectivity Map

PMCU Interface	**Connection**
TEMPERATURE A	Zynq Die Temperature
PORT_A, VADJ_A	Zmod A
PORT_B, VADJ_B	Zmod B
FAN_1	FPGA Fan
FAN_2	Case Fan

Table 1.6.2: Supported Platform MCU Optional Features

Optional Features	**Supported**
DDRVCCSEL Control	No
INIT_B Control	No
USB Hub Support	No

Table 1.6.3: Supported Platform MCU Fan COntrol Features

Feature	**FAN_1 (FPGA Fan)**	**FAN_2 (Case Fan)**
Enable / Disable	Yes	No
Fixed Speed Control	Yes	No
Automatic Speed Control	Yes	No
RPM Measurement	Yes (if supported by installed fan)[1)]	Yes (if supported by installed fan)[2)]

1) The optional FPGA fan included with the Eclypse Z7 supports RPM measurement
2) The case fan included in the Eclypse Z7 Enclosure Kit does not support RPM measurement

2. Zynq Configuration

Unlike Xilinx FPGA devices, AP SoC devices such as the Zynq-7020 are designed around the processor, which acts as a master to the programmable logic fabric and all other on-chip peripherals in the processing system. This causes the Zynq boot process to be more similar to that of a microcontroller than an FPGA. This process involves the processor loading and executing a Zynq Boot Image, which includes a

First Stage Bootloader (FSBL), a bitstream for configuring the programmable logic (optional), and a user application.

The boot process is broken into three stages:

Stage 0

After the Eclypse Z7 is powered on or the Zynq is reset (in software or by pressing the PS-SRST button, BTNR), one of the processors (CPU0) begins executing an internal piece of read-only code called the BootROM. If and only if the Zynq was just powered on, the BootROM will first latch the state of the mode pins into the mode register (the mode pins are attached to JP5 on the Eclypse Z7). If the BootROM is being executed due to a reset event, then the mode pins are not latched, and the previous state of the mode register is used. This means that the Eclypse Z7 needs a power cycle to register any change in the programming mode jumper (JP5). Next, the BootROM copies an FSBL from the form of non-volatile memory specified by the mode register to the 256 KB of internal RAM () within the APU (called On-Chip Memory, or OCM). The FSBL must be wrapped up in a Zynq Boot Image in order for the BootROM to properly copy it. The last thing the BootROM does is hand off execution to the FSBL in OCM.

Stage 1

During this stage, the FSBL first finishes configuring the PS components, such as the DDR memory controller. Then, if a bitstream is present in the Zynq Boot Image, it is read and used to configure the PL. Finally, the user application is loaded into memory from the Zynq Boot Image, and execution is handed off to it.

Stage 2

The last stage is the execution of the user application that was loaded by the FSBL. This can be any sort of program, from a simple bare-metal "Hello World" application, to a Second Stage Boot loader used to boot an operating system like Linux. For a more thorough explanation of the boot process, refer to Chapter 6 of the Zynq Technical Reference Manual (http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf).

The Zynq Boot Image is created using Vivado and Xilinx Software Development Kit (Xilinx SDK). For information on creating this image please refer to the available Xilinx documentation for these tools.

The Eclypse Z7 supports three different boot modes: microSD, Quad SPI Flash, and JTAG. The boot mode is selected using the Mode jumper (JP5), which affects the state of the Zynq configuration pins after power-on. Figure 2.1 depicts how the Zynq configuration pins are connected on the Eclypse Z7.

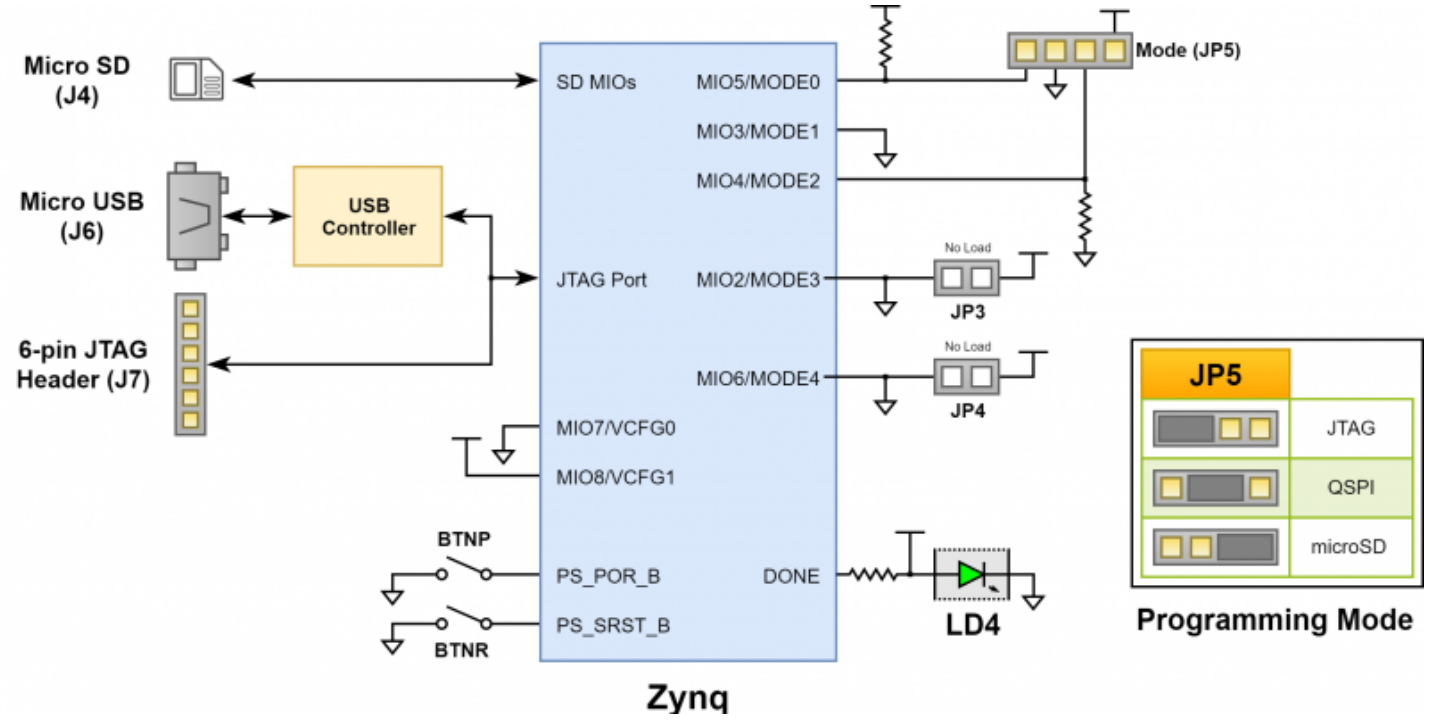

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Figure 2.1: Eclypse Z7 configuration pins.

The three boot modes are described in the following sections.

2.1. microSD Boot Mode

The Eclypse Z7 supports booting from a microSD card inserted into connector J4 (labeled "SD CARD"). The following procedure will allow you to boot the Zynq from microSD with a standard Zynq Boot Image created with the Xilinx tools:

1. Format the microSD card with a FAT32 file system.
2. Copy the Zynq Boot Image created with Xilinx SDK to the microSD card.
3. Rename the Zynq Boot Image on the microSD card to BOOT.bin.
4. Eject the microSD card from your computer and insert it into J4 on the Eclypse Z7.
5. Attach a power supply to the Eclypse Z7 via the barrel jack (J11).
6. Place a single jumper on JP5, shorting the two rightmost pins (labeled "SD").
7. Turn the board on by flipping the power switch to the ON position. The board will now boot the image on the microSD card.

2.2. Quad SPI Boot Mode

The Eclypse Z7 has an onboard 16 MB () Quad-SPI Flash that the Zynq can boot from. Documentation available from Xilinx describes how to use Xilinx SDK to program a Zynq Boot Image into a Flash device attached to the Zynq. Once the Quad SPI Flash has been loaded with a Zynq Boot Image, the following steps can be followed to boot from it:

1. Attach a power supply to the Eclypse Z7 via the barrel jack (J11).
2. Place a single jumper on JP5, shorting the two center pins (labeled "QSPI").
3. Turn the board on by flipping the power switch to the ON position. The board will now boot the image stored in the Quad SPI flash.

2.3. JTAG Boot Mode

When placed in JTAG boot mode, with the two leftmost pins of JP5 shorted (labeled "JTAG"), the processor will wait until software is loaded by a host computer using the Xilinx tools. After software has been loaded, it is possible to either let the software begin executing, or step through it line by line using Xilinx SDK.

It is also possible to directly configure the PL over JTAG, independent of the processor. This can be done using the Vivado Hardware Server.

The Eclypse Z7 is configured to boot in Cascaded JTAG mode, which allows the PS to be accessed via the same JTAG port as the PL. It is also possible to boot the Eclypse Z7 in Independent JTAG mode by shorting unloaded jumper JP3. This will cause the PS to not be accessible from the onboard JTAG circuitry, and only the PL will be visible in the scan chain. To access the PS over JTAG while in independent JTAG mode, users will have to route the signals for the PJTAG peripheral over EMIO, and use an external device to communicate with it.

---

3. DDR3L Memory

The Eclypse Z7 includes two Micron MT41K256M16TW-107 DDR3L memory components creating a single rank, 32-bit wide interface and a total of 1 GiB (Gibi-byte, or 1,073,741,824 bytes) of capacity. The DDR3L is connected to the hard memory controller in the Processor Subsystem (PS), as outlined in the Zynq documentation.

Note: *The Eclypse Z7 may alternatively use an ISSI IS43TR16256A(L)-125KBL DDR3L memory. This part is compatible with the same timings as the Micron part.*

The PS incorporates an AXI memory port interface, a DDR controller, the associated PHY, and a dedicated I/O bank. DDR3L memory interface speeds up to 533 MHz/1066 MT/s are supported.

The Eclypse Z7 was routed with 40 ohm (+/-10%) trace impedance for single-ended signals, and differential clock and strobes set to 80 ohms (+/-10%). A feature called DCI (Digitally Controlled Impedance) is used to match the drive strength and termination impedance of the PS pins to the trace impedance. On the memory side, each chip calibrates its on-die termination and drive strength using a 240 ohm resistor on the ZQ pin.

Both the memory chips and the PS DDR bank are powered from the 1.35V supply. The mid-point reference of 0.675V is created with a simple resistor divider and is available to the Zynq as external reference.

For proper operation it is essential that the PS memory controller is configured properly. Settings range from the actual memory flavor to the board trace delays. For your convenience, the Eclypse Z7 Vivado board files are available on the Eclypse Z7 Resource Center (https://reference.digilentinc.com/reference/programmable-logic/eclypse-z7/start) and automatically configure the Zynq Processing System IP core with the correct parameters.

For best DDR3L performance, DRAM training is enabled for write leveling, read gate, and read data eye options in the PS Configuration Tool in Xilinx tools. Training is done dynamically by the controller to account for board delays, process variations and thermal drift. Optimum starting values for the training process are the board delays (propagation delays) for certain memory signals.

Board delays are specified for each of the byte groups. These parameters are board-specific and were calculated from the PCB trace length reports. The DQS to CLK Delay and Board Delay values are calculated specific to the Eclypse Z7 memory interface PCB design.

For more details on memory controller operation, refer to the Xilinx Zynq Technical Reference manual (http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf).

4. Quad-SPI Flash

The Eclypse Z7 features a Spansion S25FL128S 4-bit Quad-SPI serial NOR flash. The key device attributes are:

- Part number S25FL128S
- 16 MB () of memory
- 1-bit, 2-bit, and 4-bit bus widths supported
- General use clock speeds up to 100 MHz, translating to 400 Mbps in Quad-SPI mode
- Zynq configuration clock speeds up to 94 MHz
- Powered from 3.3V

The Flash memory is used to provide non-volatile code and data storage. It can be used to initialize the PS and PL of the Zynq device with a Zynq Boot Image (also known as BOOT.BIN) generated using Xilinx tools such as Petalinux or Xilinx SDK. For information on booting the Eclypse Z7 with a Zynq Boot image, see section "2.2 Quad SPI Boot Mode".

The Flash is also commonly used to store non-configuration data needed by the application. If doing this from a bare-metal application, The flash memory can be freely accessed using standalone libraries included with a Xilinx SDK BSP project. If doing this from a Petalinux generated embedded Linux system, the Flash can be partitioned as desired and mounted/accessed like a standard MTD block device. See the Petalinux and Xilinx SDK documentation for more information.

The Flash connects to the Quad-SPI Flash controller of the Zynq-7000 PS via pins in MIO Bank 0/500 (specifically MIO[1:6,8]), as outlined in the Zynq Technical Reference Manual. Quad-SPI feedback mode is used, thus qspi_sclk_fb_out/MIO[8] is left to freely toggle and is connected only to a 20K pull-up resistor to 3.3V. This allows a Quad-SPI clock frequency greater than FQSPICLK2. The details of these connections do not need to be known when using the Eclypse Z7 Vivado Board files, as they will automatically configure your project to work correctly with the on-board Flash.

A globally unique MAC address is programmed into the One-Time-Programmable (OTP) region of the Flash on each Eclypse Z7 at the factory. For more information on this, see section 11. Ethernet. The MAC address can also be found on a sticker attached to the board.

The OTP region also includes a factory-programmed read-only 128-bit random number. The very lowest address range [0x00;0x0F] can be read to access the random number. See the Spansion S25FL128S datasheet for information on this random number and accessing the OTP region.

5. Oscillators/Clocks

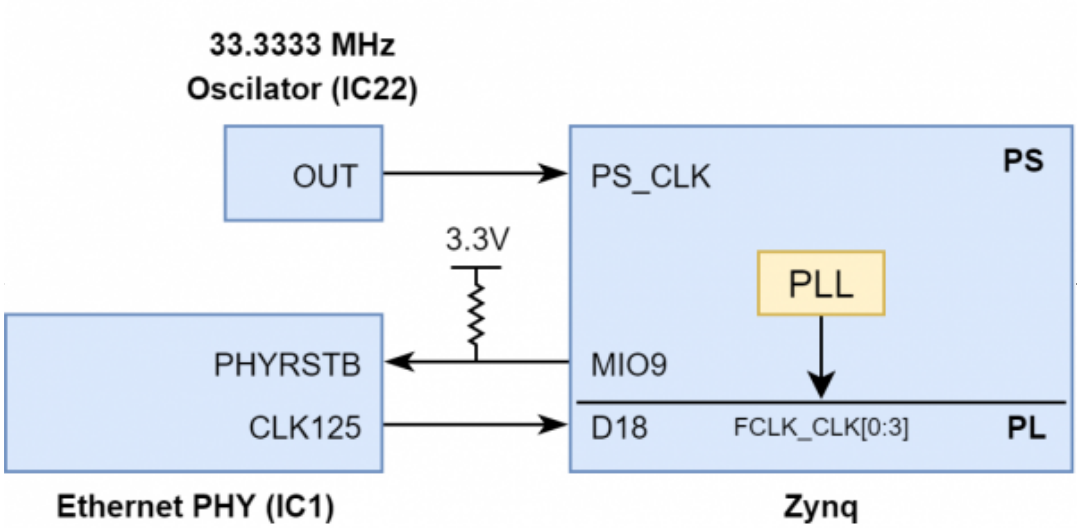
The Eclypse Z7 provides a 33.3333 MHz clock to the Zynq PS_CLK input, which is used to generate the clocks for each of the PS subsystems. The 33.3333 MHz () input allows the processor to operate at a maximum frequency of 667 MHz and the DDR3 memory controller to operate at a maximum clock rate of 533 MHz () (1066 MT/s). The Eclypse Z7 board files, available on the Eclypse Z7 Resource Center (https://reference.digilentinc.com/reference/programmable-logic/eclypse-z7/start), will automatically configure the Zynq processing system IP core in Vivado to work with all PS attached devices, including the 33.3333 MHz () input oscillator.

The PS has a dedicated PLL capable of generating up to four reference clocks, each with settable frequencies, that can be used to clock custom logic implemented in the PL. Additionally, The Eclypse Z7 provides an external 125 MHz () reference clock directly to pin D18 of the PL. The external reference clock allows the PL to be used completely independently of the PS, which can be useful for simple applications that do not require the processor.

The PL of the Zynq-Z7020 also includes four MMCM's and four PLL's that can be used to generate clocks with precise frequencies and phase relationships. Any of the four PS reference clocks or the 125 MHz () external reference clock can be used as an input to the MMCMs and PLLs. For a full description of the capabilities of the Zynq PL clocking resources, refer to the 7 Series FPGAs Clocking Resources User Guide (https://www.xilinx.com/support/documentation/user_guides/ug472_7Series_Clocking.pdf) available from Xilinx.

Xilinx offers the Clocking Wizard IP core to assist in integrating the MMCM's and PLL's into a design. This wizard will properly instantiate the needed MMCMs and PLLs based on the desired frequencies and phase relationships specified by the user. The wizard will then output an easy-to-use wrapper component around these clocking resources that can be inserted into the user's design. The clocking wizard can be accessed from within the Vivado and IP Integrator tools.

Figure 5.1 outlines the clocking scheme used on the Eclypse Z7. Note that the reference clock output from the Ethernet PHY is used as the 125 MHz () reference clock to the PL, in order to cut the cost of including a dedicated oscillator for this purpose. Keep in mind that CLK125 will be disabled when the Ethernet PHY is held in hardware reset by driving the PHYRSTB signal low.



(https://reference.digilentinc.com/_detail/reference/programmable-logic/eclypse-z7/reference-manual/eclypse-clocks.png?id=reference%3Aprogrammable-logic%3Aeclypse-z7%3Areference-manual)

Figure 5.1: Eclypse Z7 clocking.

6. Reset Sources

The Eclypse Z7 provides several different methods of resetting the Zynq-7000 device, as described in the following sections:

6.1. Power-on Reset

The Zynq PS supports external power-on reset signals. The power-on reset is the master reset of the entire chip. This signal resets every register in the device capable of being reset. The Eclypse Z7 drives this signal from the VCC4V3 supply, the final non-adjustable supply to be brought up in the power-on sequence, in order to hold the system in reset until all power supplies are valid. A push-button, labeled BTNP, can be used to toggle the power-on reset signal. BTNP is located on the underside of the Eclypse Z7, below the SD card slot.

6.2. Processor Subsystem Reset

The external system reset button, labeled BTNR, resets the Zynq device without disturbing the debug environment. For example, the previous break points set by the user remain valid after system reset. Due to security concerns, system reset erases all memory content within the PS, including the On-Chip-Memory (OCM). The PL is also cleared during a system reset. System reset does not cause the boot mode strapping pins to be re-sampled. After changing the boot mode jumper a power cycle is needed to act on the new setting. BTNR is located on the underside of the Eclypse Z7, below the SD card slot.

7. USB-UART Bridge (Serial Port)

The Eclypse Z7 includes an FTDI FT2232HQ USB-UART bridge (attached to connector J6) that lets PC applications communicate with the board using standard COM port commands (or the tty interface in Linux). Drivers are automatically installed in Windows and newer versions of Linux when the Eclypse Z7 is attached. Serial port data is exchanged with the Zynq using a two-wire serial port (TXD/RXD). After the drivers are installed, I/O commands can be used from the PC directed to the COM port to produce serial data traffic on the Zynq pins. The port is tied to PS (MIO) pins and can be used in combination with the UART 0 controller.

The Zynq presets file (available in the Eclypse Z7 Resource Center (https://reference.digilentinc.com/reference/programmable-logic/eclypse-z7/start)) takes care of mapping the correct MIO pins to the UART 0 controller and uses the following default protocol parameters: 115200 baud rate, 1 stop bit, no parity, 8-bit character length.

Two status LEDs provide visual feedback on traffic flowing through the port: the transmit LED () (the lower of the two yellow LEDs in the circuit board indicator, LD4) and the receive LED () (the upper of the two yellow LEDs in the circuit board indicator, LD4). Signal names that imply direction are from the point-of-view of the DTE (Data Terminal Equipment), in this case the PC.

The FT2232HQ is also used as the controller for the Digilent USB-JTAG circuitry, but the USB-UART and USB-JTAG functions behave entirely independent of one another. Programmers interested in using the UART functionality of the FT2232 within their design do not need to worry about the JTAG circuitry interfering with the UART data transfers, and vice-versa. The combination of these two features into a single device allows the Zybo Z7 to be programmed and communicated with via UART from a computer attached with a single Micro USB cable.

The connections between the FT2232HQ and the Zynq-7000 are shown in Figure 7.1.

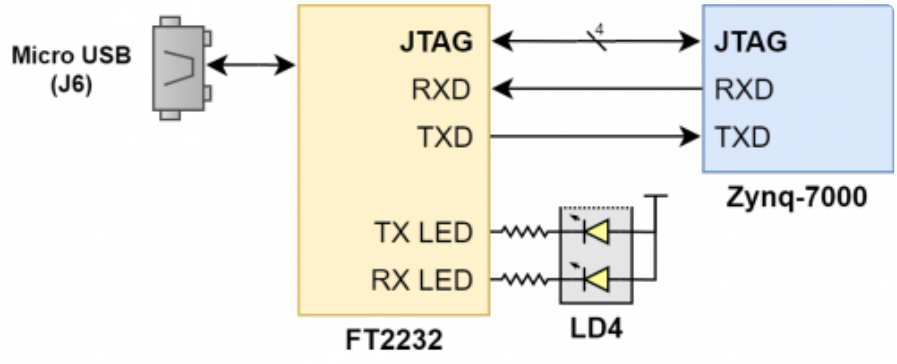


Figure 7.1: UART Connections

8. Zmod Ports

The Eclypse Z7 features two Zmod ports, which use SYZYGY Standard interfaces to communicate with installed SYZYGY pods. Both ports are compatible with version 1.1 of the SYZYGY specification from Opal Kelly.

SYZYGY SmartVIO functionality is implemented by the Eclypse's Platform MCU, as discussed in the 1 Power Supplies section of this document. Each port's SYZYGY DNA is connected to both the Platform MCU and the Zynq's I2C 0 peripheral (MIO12:13) through a single I2C bus. Once the board is fully powered on, and the PMCU has configured itself in I2C slave mode, SYZYGY DNA data can be read directly from the pods, and the negotiated voltages and currents can be read from the PMCU over this bus.

Warning: *SYZYGY pods are NOT hot-swappable. Connecting or disconnecting a pod from the Eclypse while the board is powered on may cause damage to the pod and/or the board, and is to be avoided.*

Each SYZYGY Standard interface contains 16 single-ended I/O pins, 8 differential I/O pairs (which can alternatively be used as 16 additional single-ended I/O pins), and two dedicated differential clocks - one for input and one for output. Each Zmod port has a I/O bank of the Zynq dedicated to it, which is powered by a dedicated adjustable rail, configured by the Platform MCU as the Eclypse is powered on. Template constraints for each Zmod port can be found in the Eclypse Z7's Master XDC file, available through Digilent's digilent-xdc (https://github.com/Digilent/digilent-xdc) repository on Github.

Digilent provides Eclypse-compatible low-level IPs, scripted Vivado flows, and software libraries to support each Digilent Zmod (https://reference.digilentinc.com/reference/zmod/start).

For more information on the SYZYGY standard, see syzygyfpga.io (https://syzygyfpga.io/).

8.1. SYZYGY Pod Compatibility

The Eclypse's Zmod ports are compatible with a variety of different SYZYGY pods. Information required to determine if the Eclypse is compatible with a certain pod is summarized in Table 8.1.1.

Table 8.1.1: SYZYGY Compatibility Table

Parameter	Port A (STD)	Port B (STD)
Port Type	Standard	Standard
	Double-Width Capable	
Total 5V Supply Current	3.0 A (shared with USB VBUS output, Case Fan, and RGB LEDs)	
Total 3.3V Supply Current	2.0 A Shared	
VIO Supply Voltage Range	1.2V to 3.3V	1.2V to 3.3V
Total VIO Supply Current	1.8A (VIO Group 1)	1.8A (VIO Group 2)
Port Groups	Group 1: A	Group 2: B
I/O Count	28 total (8 DP)	28 total (8 DP)

Parameter	Port A (STD)	Port B (STD)
Length Matching	73.7 mm +- 0.2 mm (including Zynq package delay)	

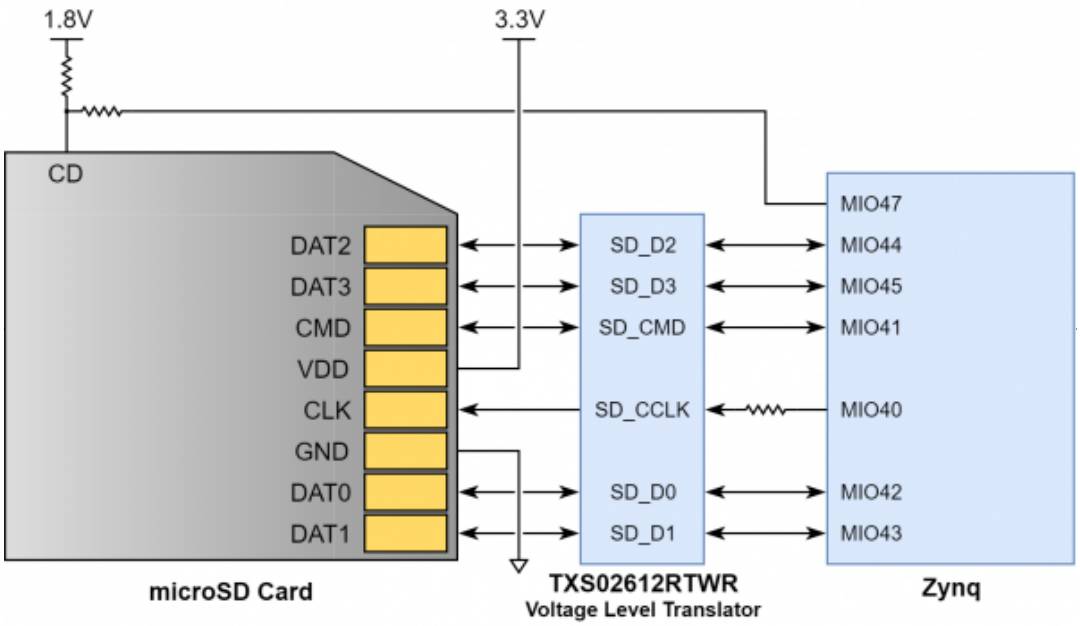
9. microSD Slot

The Eclypse Z7 provides a microSD slot (J4) for non-volatile external memory storage as well as booting the Zynq. The slot is wired to Bank 1/501 MIO[40-45], and also includes a card detect signal attached to MIO 47. On the PS side, peripheral SDIO 0 is mapped out to these pins and controls communication with the SD card. The pinout can be seen in Table 9.1. The peripheral controller supports 1-bit and 4-bit SD transfer modes, but does not support SPI mode. Based on the Zynq Technical Reference Manual (http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf), SDIO host mode is the only mode supported.

Table 9.1: microSD pinout

Signal Name	Description	Zynq Pin	SD Slot Pin
SD_D0	Data[0]	MIO42	7
SD_D1	Data[1]	MIO43	8
SD_D2	Data[2]	MIO44	1
SD_D3	Data[3]	MIO45	2
SD_CCLK	Clock	MIO40	5
SD_CMD	Command	MIO41	3
SD_CD	Card Detect	MIO47	9

The SD slot is powered from 3.3V, but is connected through MIO Bank 1/501 (1.8V). Therefore, a TI TXS02612 level shifter performs this translation. The TXS02612 is actually a 2-port SDIO port expander, but only its level shifter function is used. The connection diagram can be seen on Figure 9.1. Mapping out the correct pins and configuring the interface is handled by the Eclypse Z7 board files, available on the Eclypse Z7 Resource Center (https://reference.digilentinc.com/reference/programmable-logic/eclypse-z7/start).



(https://reference.digilentinc.com/_detail/reference/programmable-logic/eclypse-z7/reference-manual/eclypse-micro-sd.png?id=reference%3Aprogrammable-logic%3Aeclypse-z7%3Areference-manual)

Figure 9.1: microSD slot signals

Both low speed and high speed cards are supported, the maximum clock frequency being 50 MHz (). A Class 4 card or better is recommended.

Refer to section 2.1 microSD Boot Mode for information on how to boot from a microSD card that contains a Zynq Boot Image.

The microSD is also commonly used to store non-configuration data needed by the application. If doing this from a bare-metal application, the microSD card can be freely accessed using standalone libraries included with a Xilinx SDK BSP project. If doing this from a Petalinux generated embedded Linux system, the microSD can be mounted/accessed like a standard block device, typically with a device node named /dev/mmcblk0. See the Petalinux and Xilinx SDK documentation for more information.

10. USB Micro-AB Device/Host/OTG Port

The Eclypse Z7 implements one of the two available PS USB OTG interfaces on the Zynq device. A Microchip USB3320 USB 2.0 Transceiver Chip with an 8-bit ULPI interface is used as the PHY. The PHY features a complete HS-USB Physical Front-End supporting speeds of up to 480Mbs. The PHY is connected to MIO Bank 1/501, which is powered at 1.8V. The usb0 peripheral is used on the PS, connected through MIO[28-39]. The USB OTG interface can act as an host, embedded host, or a peripheral device, through the USB Micro AB connector(J5). The USB mode is controlled from software by manipulating the USB0 peripheral controller in the Zynq PS.

By default, VBUS capacitance is 4.7 µF. Jumper JP1 may be shorted while in host mode in order to increase VBUS capacitance by 150 µF. Jumper JP2 must be installed for the Eclypse to power VBUS for host or embedded host applications. These requirements give three possible configurations for the two jumpers, as presented in Table 10.1.

Whether the Eclypse Z7 is configured as an embedded host or a general purpose host, it can provide at least 500 mA on the 5V VBUS line. More than 500 mA of current can potentially be provided depending on the system configuration and how much power is drawn by installed Zmods. See the 1 Power Supplies section for more information.

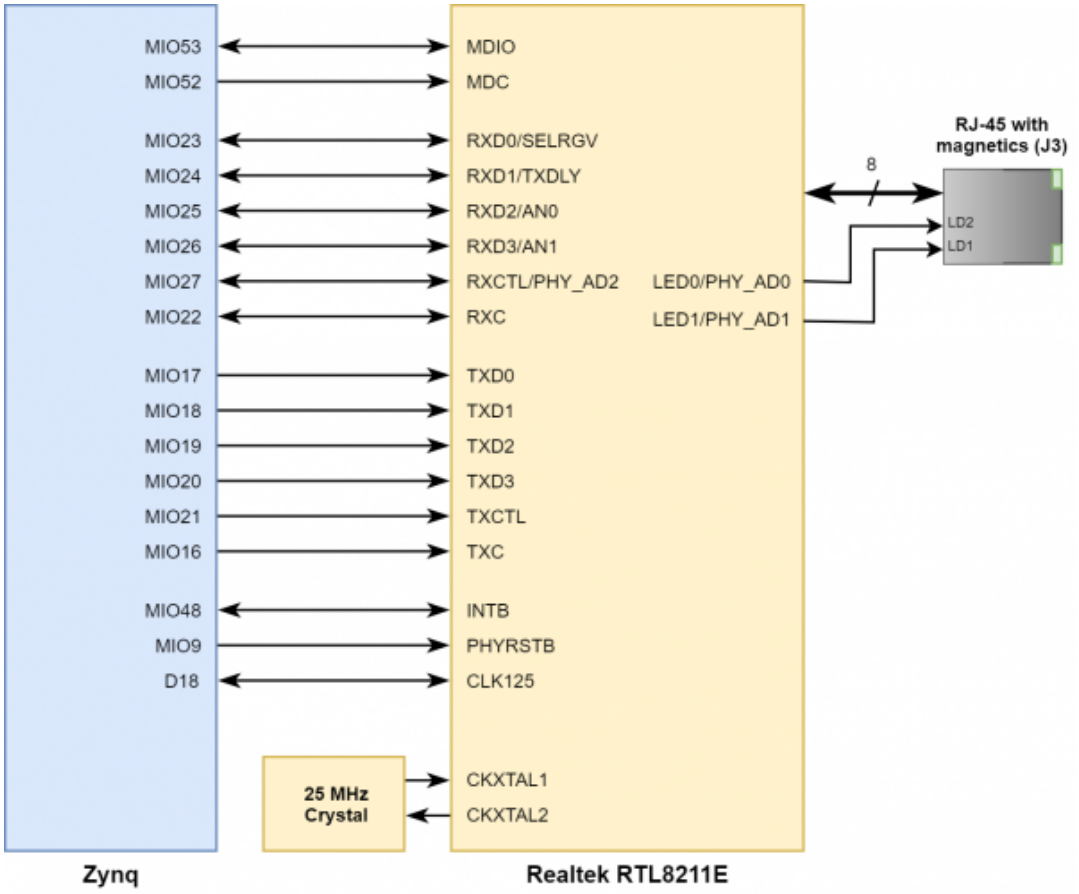
Table 10.1: USB Mode Jumper Positions

Mode	**JP1 Shorted**	**JP2 Shorted**
Embedded Host	No	Yes
General Purpose Host	Yes	Yes
Peripheral Device	No	No

11. Ethernet

The Eclypse Z7 uses a Realtek RTL8211E-VL PHY to implement a 10/100/1000 Ethernet port for network connection. The PHY connects to MIO Bank 501 (1.8V) and interfaces to the Zynq-7000 AP SoC via RGMII for data and MDIO for management. The auxiliary interrupt (INTB) and reset (PHYRSTB) signals connect to PS pins to be accessed through the MIO GPIO () peripheral via MIO48 and MIO9 respectively. The connection diagram can be seen on Figure 11.1.

After power-up the PHY starts with Auto Negotiation enabled, advertising 10/100/1000 link speeds and full duplex. If there is an Ethernet-capable partner connected, the PHY automatically establishes a link with it, even with the Zynq not configured.



(https://reference.digilentinc.com/_detail/reference/programmable-logic/eclypse-z7/reference-manual/eclypse-ethernet.png?id=reference%3Aprogrammable-logic%3Aeclypse-z7%3Areference-manual)

Figure 11.1: Ethernet PHY signals

Two status indicator LEDs are located on the RJ-45 connector (J3) that indicate traffic (J3/LD2, right side of connector) and valid link state (J3/LD1, left side of connector). Table 11.1 shows the default behavior.

Table 11.1: Ethernet status LEDs

Function	Designator	State	Description
LINK	J3/LD1	Steady on	Link 10/100/1000
		Blinking 0.4s ON, 2s OFF	Link, Energy Efficient Ethernet (EEE) mode
ACT	J3/LD2	Blinking	Transmitting or Receiving

The Zynq incorporates two independent Gigabit Ethernet Controllers. They implement a 10/100/1000 half/full duplex Ethernet MAC. Of these two, GEM 0 can be mapped to the MIO pins where the PHY interfaces. Since the MIO bank is powered from 1.8V, the RGMII interface uses 1.8V HSTL Class 1 drivers. For this I/O standard an external reference of 0.9V is provided in bank 501 (PS_MIO_VREF). Mapping out the correct pins and configuring the interface is handled by the Eclypse Z7 Vivado board files.

Although the default power-up configuration of the PHY might be enough in most applications, the MDIO bus is available for management. The RTL8211E-VL is assigned the 5-bit address 00001 on the MDIO bus. With simple register read and write commands, status information can be read out or configuration changed. The Realtek PHY follows industry-standard register map for basic configuration.

The RGMII specification calls for the receive (RXC) and transmit clock (TXC) to be delayed relative to the data signals (RXD[0:3], RXCTL and TXD[0:3], TXCTL). Xilinx PCB guidelines also require this delay to be added. The RTL8211E-VL is capable of inserting a 2ns delay on both the TXC and RXC so that board traces do not need to be made longer.

On an Ethernet network each node needs a unique MAC address. To this end, the one-time-programmable (OTP) region of the Quad-SPI flash has been programmed at the factory with a 48-bit globally unique EUI-48/64™ compatible identifier. The OTP address range [0x20;0x25] contains the identifier with the first byte in transmission byte order being at the lowest address. Refer to the Flash memory

datasheet (https://www.cypress.com/file/448601/download) for information on how to access the OTP regions. When using Petalinux, this is automatically handled in the U-boot boot-loader, and the Linux system is automatically configured to use this unique MAC address. The identifier is also printed on a sticker found on the top-side of the Eclypse Z7 right next to the mode jumper (JP5) and above the headphone output jack.

For getting started using the ethernet port in a bare-metal application, Xilinx provides a lwip TCP/IP stack that can be automatically generated in Xilinx SDK along with an echo server example. When using the Eclypse Z7 with a Petalinux generated embedded Linux system, the ethernet port will automatically appear as a network device typically named eth0. See the Petalinux and Xilinx SDK documentation for more information.

For more low-level information on using the Zynq-7000 Gigabit Ethernet MAC, refer to the Xilinx Zynq Technical Reference Manual.

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12. Basic I/O

The Eclypse Z7 includes two push-buttons and two tri-color LEDs connected to the Zynq PL, as shown in Figure 12.1. These I/Os are connected to the Zynq via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if a pin assigned to a push-button was inadvertently defined as an output).

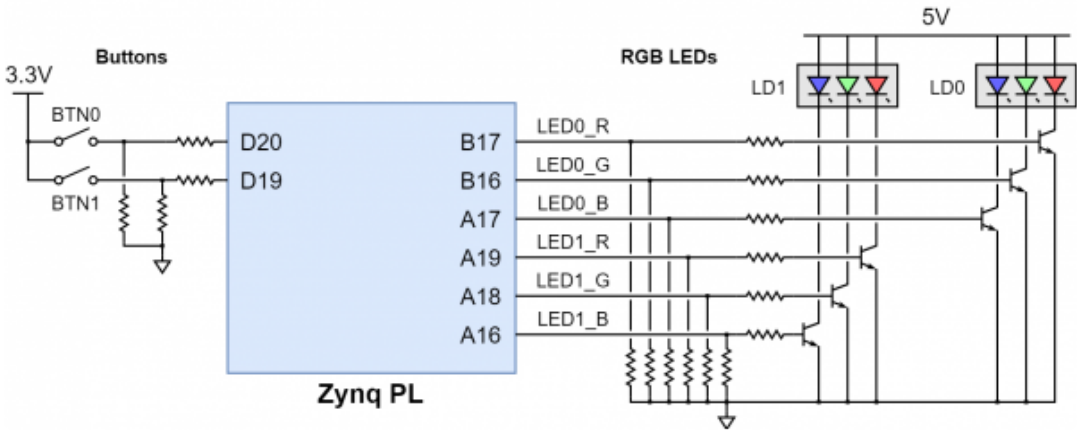

Figure 12.1: Eclypse Z7 Basic I/O

12.1. Push-Buttons

The push-buttons are "momentary" switches that normally generate a low output when they are at rest, and a high output only when they are pressed.

12.2. Tri-Color LEDs

Each tri-color LED () has three input signals that drive the cathodes of three smaller internal LEDs: one red, one blue, and one green. Driving the input signal corresponding to one of these colors low will illuminate the internal LED (). The input signals are driven by the Zynq PL through a transistor, which inverts the signals. Therefore, to light up the tri-color LED (), the corresponding PL pins need to be driven high. The tri-color LED () will emit a color dependent on the combination of internal LEDs that are currently being illuminated. For example, if the red and blue signals are driven high and green is driven low, the tri-color LED () will emit a purple color.

Note: *Digilent strongly recommends the use of pulse-width modulation (PWM) when driving the tri-colo LEDs. Driving any of the signals to a steady logic '1' will result in the LED () being illuminated at an uncomfortably bright level. This can be avoided by ensuring that none of the tri-color signals are driven with more than a 50% duty cycle. Using PWM also greatly expands the potential color palette of the tri-color LED (). Individually adjusting the duty cycle of each color between 0% and 50% causes the different colors to be illuminated at different intensities, allowing virtually any color to be displayed.*

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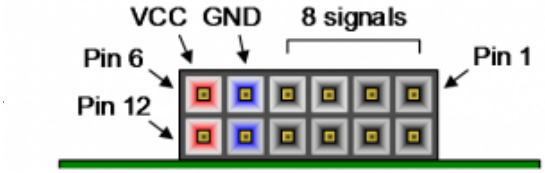
13. Pmod Ports

Pmod ports are 2×6, right-angle, 100-mil spaced female connectors that mate with standard 2×6 pin headers. Each 12-pin Pmod port provides two 3.3V VCC () signals (pins 6 and 12), two Ground signals (pins 5 and 11), and eight logic signals, as shown in Figure 13.1. The VCC () and Ground pins can deliver up to 1A of current, but care must be taken not to exceed any of the power budgets of the on-board regulators or the external power supply (as described in the Power supplies section).



(https://reference.digilentinc.com/_detail/basys3-pmod_connector.png?id=reference%3Aprogrammable-logic%3Aeclypse-z7%3Areference-manual)

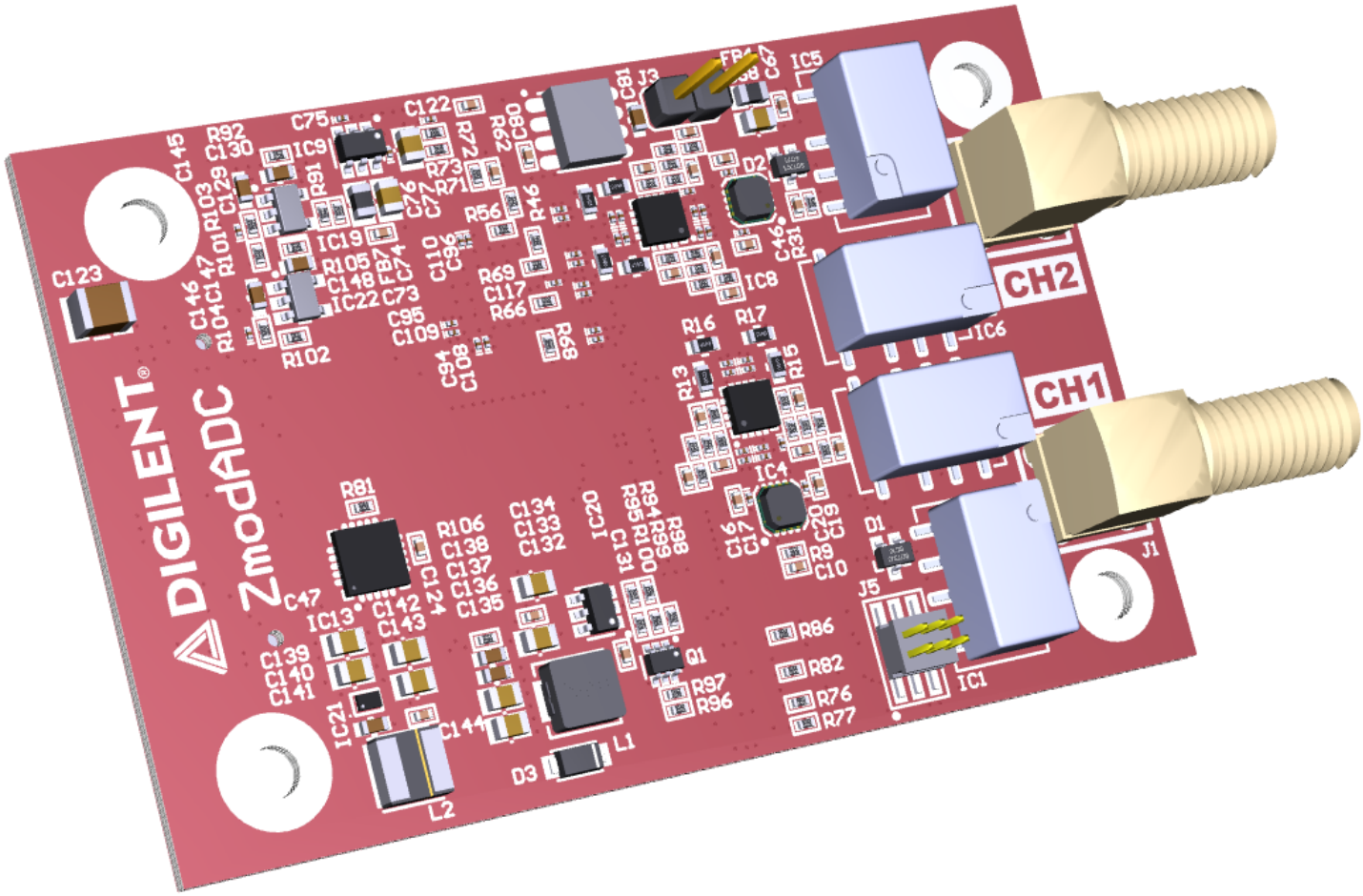
Figure 13.1: Pmod port

Digilent produces a large collection of Pmod accessory boards that can attach to the Pmod ports to add ready-made functions like A/D's, D/A's, motor drivers, sensors, and other functions. See www.digilentinc.com (http://www.digilentinc.com) for more information. The vivado-library repository on the Digilent Github (https://github.com/Digilent/) contains pre-made IP cores for many of these Pmods that greatly reduces the work of integrating them into your project. This repository's `hierarchies` branch contains additional scripts and sources that can be used to speed up the process of integrating these cores. See the Pmod-related tutorials on the Eclypse Z7 Resource Center for help using them.

The Eclypse Z7's two Pmod ports are connected to the Zynq PL via high-speed down translation and protection circuitry. When used as outputs, the Pmod pins are driven at 3.3V. When used as inputs, the Pmod pins are 5V tolerant. The maximum recommended voltage applied to these pins is 5.5V, though the inline resettable fuses will protect the FPGA pins from damage.

Zmod ADC Reference Manual

The Digilent Zmod ADC () is an open-source hardware SYZYGY™ [1]compatible pod containing a dual-channel ADC () and the associated front end. The Zmod ADC () is intended to be used with any SYZYGY™ compatible carrier board having the required capabilities.



(https://reference.digilentinc.com/_media/reference/instrumentation/zmodadc/zmodadc_top_view.png)

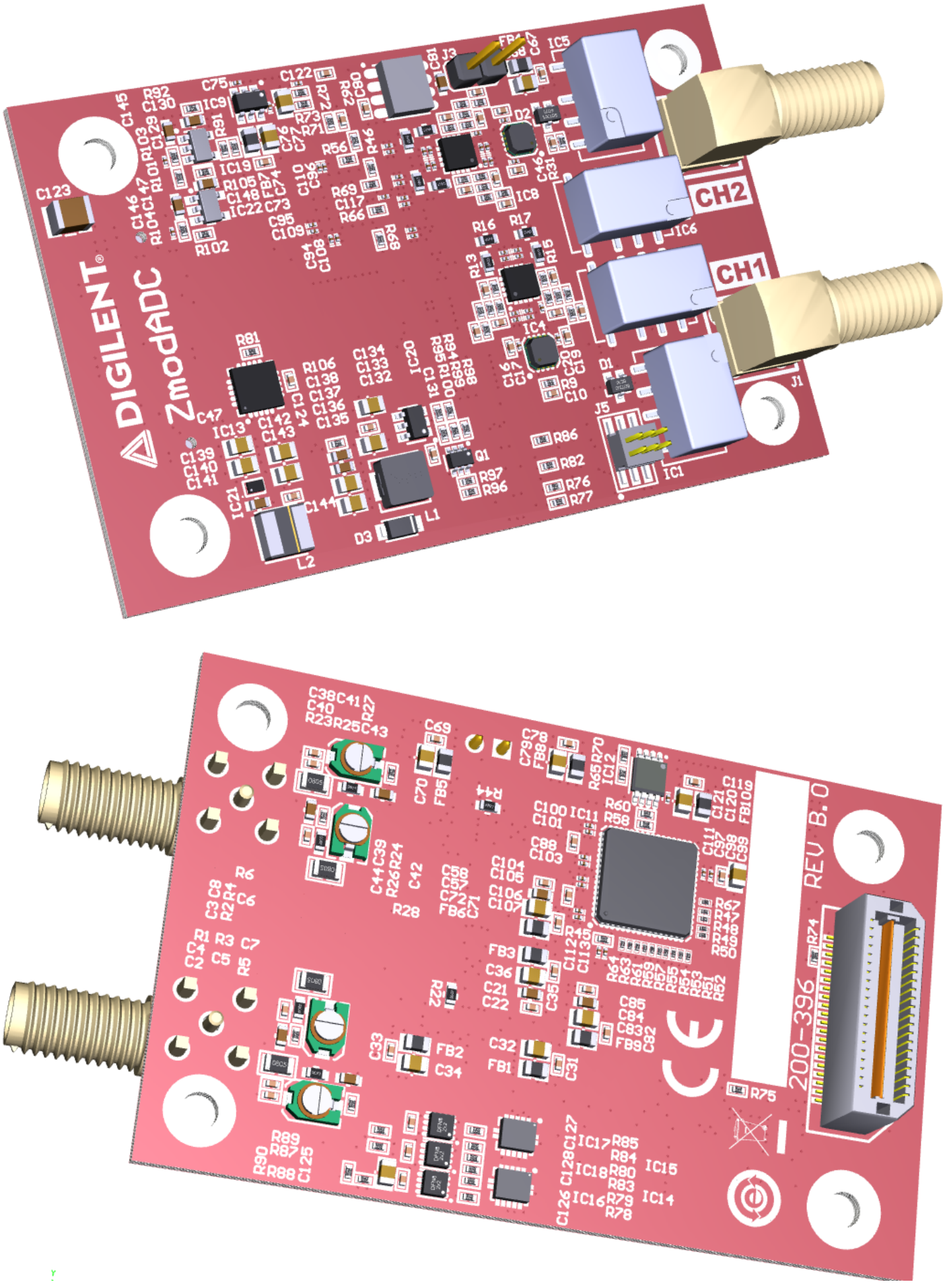

DIGILENT
ZmodADC
CH2
CH1
200-396 REV B.0

Figure 1. Zmod ADC top and bottom views. []

The analog inputs can be connected to a circuit using SMA cables. Driven by the SYZYGY™ carrier, the Zmod ADC () can acquire two simultaneous signals (1MΩ, ±25V, single-ended, 14-bit, 100MS/s, 70MHz+ bandwidth).

The Zmod ADC () was designed to be a piece in a modular, HW and SW open-source ecosystem. Combined with a SYZYGY™ carrier, other SYZYGY™ compatible pods, Zmod ADC () can be used for a variety of applications: data acquisition systems, closed loop controllers, scopes, etc.

Features

- Channels: 2
- Channel type: single ended
- Resolution: 14-bit
- Input range: ±1V (Low Range) or ±25V (High Range)
- Absolute Resolution: 0.13mV (Low Range) or 3.21mV (High Range)
- Accuracy: ±0.2% of Range
- Sample rate (real time): 100MS/s
- Input impedance: 1MΩ||18pF
- Analog bandwidth: 70 MHz ()+ @ 3dB, 30 MHz () @ 0.5dB, 20 MHz () @ 0.1dB
- Input protected to: ±50V

1. Architectural Overview and Block Diagram

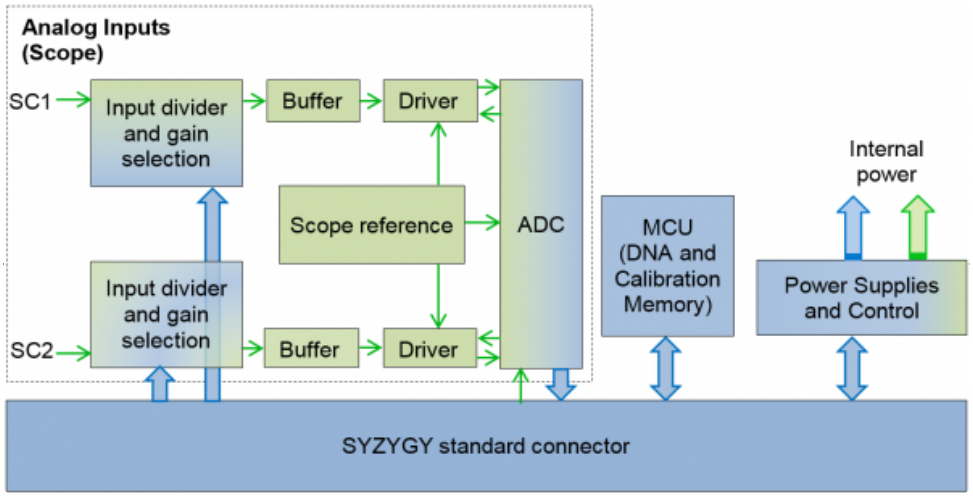
This document describes the Zmod ADC ()'s circuits, with the intent of providing a better understanding of its electrical functions, operations, and a more detailed description of the hardware's features and limitations. It is not intended to provide enough information to enable complete duplication of the Zmod ADC (), but can help users to design custom configurations for programmable parts in the design.

Zmod ADC ()'s block diagram is presented in Fig. 2 below. The core of the Analog Zmod ADC () is the dual channel, high speed, low power, 14-bit, 105MS/s ADC (), AD9648 (https://www.analog.com/en/products/ad9648.html). The carrier board is responsible to configure the internal registers of the ADC () circuit, provide the acquisition clock and receive the data.

The **Analog Input** block is also called the **Scope**, because of similar structure and behavior to such a front end. The signals in this circuitry use a "SC" indexes to indicate they are related to the scope block. Signals and equations also use certain naming conventions. Analog voltages are prefixed with a "V" (for voltage), and suffixes and indexes are used in various ways: to specify the location in the signal path (IN, MUX, BUF, ADC (), etc.); to indicate the related instrument (SC, etc.); to indicate the channel (1 or 2); and to indicate the type of signal (P, N, or diff). Referring to the block diagram in Fig. 2 below:

- The **Analog Inputs/Scope** instrument block includes:
  - **Input Divider and Gain Selection**: high bandwidth input adapter/divider. High or low-gain can be selected by the FPGA
  - **Buffer**: high impedance buffer
  - **Driver**: provides appropriate signal levels and protection to the ADC ().
  - **Scope Reference**: generates and buffers reference voltages for the scope stages
  - **ADC ()**: the analog-to-digital converter for both scope channels.
- The **Power Supplies and Control** block generates all internal supply voltages.
- The **MCU** works as a I2C memory for two different purposes:
  - The **DNA** includes the standard SYZYGY™ (https://syzygyfpga.io) pod identification information.
  - The **Calibration Memory** stores all calibration parameters. Except for the "Probe Calibration" trimmers in the scope Input divider, the Zmod ADC () includes no analog calibration circuitry. Instead, a calibration operation is performed at manufacturing (or by the user), and parameters are stored in memory. The application software uses these parameters to correct the acquired data and the generated signals

In the sections that follow, schematics are not shown separately for identical blocks. For example, the Scope Input Divider and Gain Selection schematic is only shown for channel 1 since the schematic for channel 2 is identical. Indexes are omitted where not relevant. As examples, in equation 1 below, $V_{SCOPE-SMA}$ does not contain the channel index (because the equation applies to both channels 1 and 2).



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/zmodadcblockdiagram.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 2. Zmod ADC Block diagram. []

2. Scope

2.1. Scope Input Divider and Gain Selection

Fig. 3 shows the scope input divider and gain selection stage.

C_5 and C_6 are capacitive trimmers, 3…10pF, -0/+50% tolerance. The worse case range is 4.5…10pF. All other capacitors are 1% tolerance, all the resistors are 0.1%.

The IC1 relay switches between two symmetrical R-C dividers. Each of them provide:

- Scope input impedance = 1MOhm || 18pF
- Two different attenuations for high-gain/low-gain (25:1)
- Controlled capacitance, much higher than the parasitical capacitance of subsequent stages
- Constant attenuation over a large frequency range (trimmer adjusted)

The maximum voltage rating for scope inputs is limited to:

$$-50V < V_{SCOPE-SMA} < 50V \tag{1}$$

The DC low gain is:

$$\frac{V_{SC-LG}}{V_{SCOPE-SMA}} = \frac{R_5}{R_1 + R_3 + R_5} = 0.04 \tag{2}$$

The High Range (at low gain):

$$-25V \leq V_{SCOPE-SMA} \leq 25V \tag{3}$$

The high gain is:

$$\frac{V_{SC-HG}}{V_{SCOPE-SMA}} = \frac{R_4 + R_6}{R_2 + R_4 + R_6} = 0.96 \tag{4}$$

The Low Range (at high gain):

$$-1V \leq V_{SCOPE-SMA} \leq 1V \tag{5}$$

The two dividers are designed to have the same equivalent impedance (both active and reactive):

$$R_{ech} = R_1 + R_3 + R_5 = R_2 + R_4 + R_6 = 1Mohm \tag{6}$$

Experiments shown that there are significant parasitic capacities of the layout and buffer input stage: C_{PH} (high gain divider), parallel to C_6, and C_{PL} (low gain divider), parallel to C_7. The trimmers should compensate for these parasitic capacities and adjust for perfect matching:

$$C_3 * R_2 = (C_{PH} + C_6) * (R_4 + R_6) \tag{7}$$

$$(C_{PH} + C_6) = \frac{C_3 * R_2}{R_4 + R_6} = 18pF \tag{8}$$

$$(C_4 + C_5) * (R_1 + R_3) = (C_{PL} + C_7) * R_5 \tag{9}$$

$$(C_{PL} + C_7) = (C_4 + C_5) * \frac{(R_1 + R_3)}{R_5} \tag{10}$$

With the chosen values, the correct adjustment results in about mid-position of trimmers C_5 and C_6:

$$C_5 = C_6 = 7pF \tag{11}$$

which solves the parasitic capacities as:

$$C_{PH} = 11pF \tag{12}$$

$$C_{PL} = 8.8pF \tag{13}$$

The Low Gain and High Gain dividers have very close equivalent capacitance, within the tolerances and model approximations:

$$C_{HGech} = \frac{C_3 * R_2}{R_2 + R_4 + R_6} = C_{ech} = 17.28pF \tag{14}$$

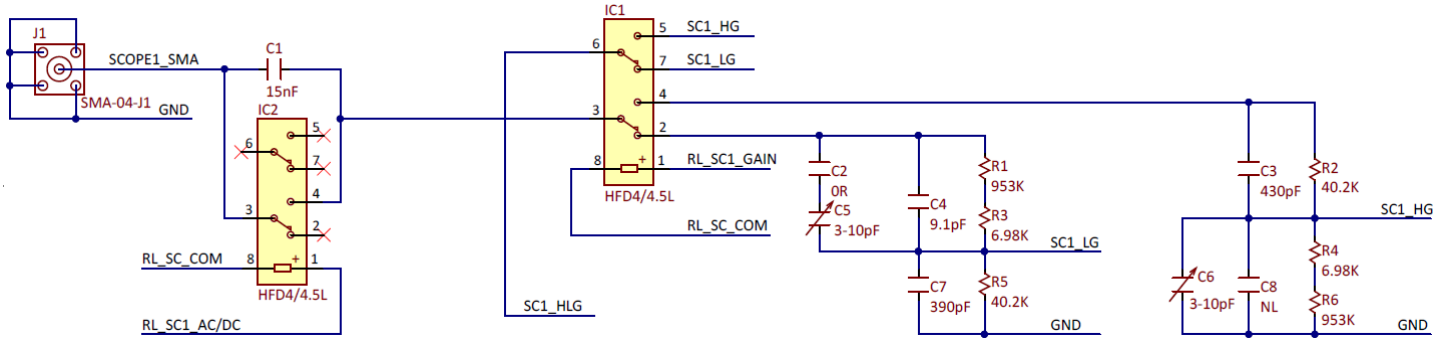
$$C_{LGech} = \frac{(C_7 + C_{PL}) * R_5}{R_1 + R_3 + R_5} = 16.03p \tag{15}$$

Experiments show that the equivalent capacitances are even closer than the values above, about 18pF. The computing error mainly derives from trimmer position approximation.

$$C_{ech} = 18p \tag{16}$$

The IC2 relay shorts the C1 capacitor when DC coupling is desired. Otherwise, C1 forms a High Pass filter with the selected divider, for AC coupling, with the corner frequency:

$$f_c = \frac{1}{2 * \pi * R_{ech} * (C_{ech} + C_1)} \approx \frac{1}{2 * \pi * R_{ech} * C_1} = 10.6Hz \tag{17}$$



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/inputdivider.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

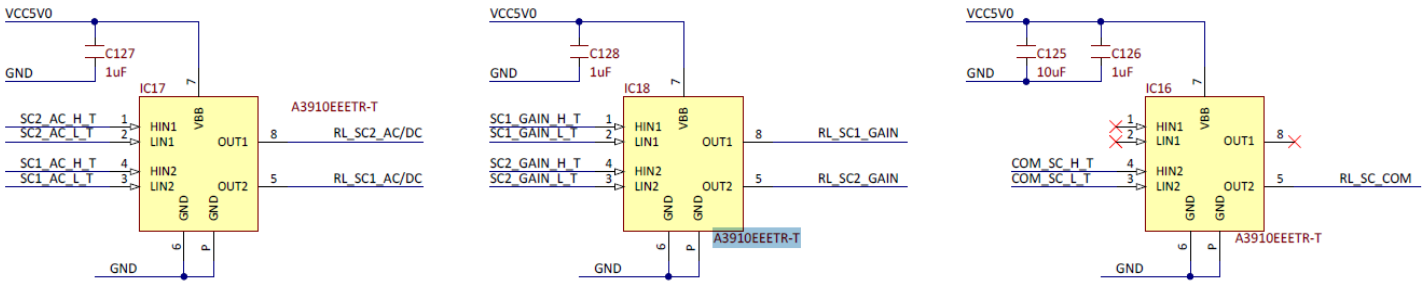
Figure 3. Input divider and gain selection.

IC1 and IC2 in Fig. 3, are HFD4/4.5L (https://hongfa.com/product/detail/70689a00-9d73-4802-b0ac-e36561332f57) latching relays (possible replacement: IM42GR (https://www.te.com/commerce/DocumentDelivery/DDEController?Action=srchrtrv&DocNm=108-98001&DocType=SS&DocLang=EN)). The schematic shows the "reset" position. A relay is "set" when a positive voltage is applied at the coil terminals and it is "reset" when a negative voltage is applied (see the polarity on the schematic symbol). The relay keeps state when no current flows trough the coil (the terminals are driven at the same voltage or at least one of the terminals is "open"). The nominal coil voltage is 4.5V.

The IC16, IC17 and IC18 in Fig. 4 are A3910EEETR-T (https://www.digikey.com/en/datasheets/allegromicrosystemsllc/allegro-microsystems-llca3910datasheetashx) drivers for the relays. They feature:

- Low RDS(on) outputs
- Standby mode with zero current drain
- Small 2 × 2 DFN package
- Crossover Current protection
- Thermal Shutdown protection

Normally, all of them have both HIN and LIN inputs "low" or both "High" driving the "OUT" pins "High Z". To "set" a relay, OUT2 of IC16 is set "Low" (HIN="Low", LIN="High") and the corresponding OUT pin of IC17 or IC18 is set "High" (HIN="High", LIN="Low"). All other OUT pins are set "High Z". To "reset" a relay, OUT2 of IC16 is set "High" (HIN="High", LIN="Low") and the corresponding OUT pin of IC17 or IC18 is set "Low" (HIN="Low", LIN="High"). All other OUT pins are set "High Z".



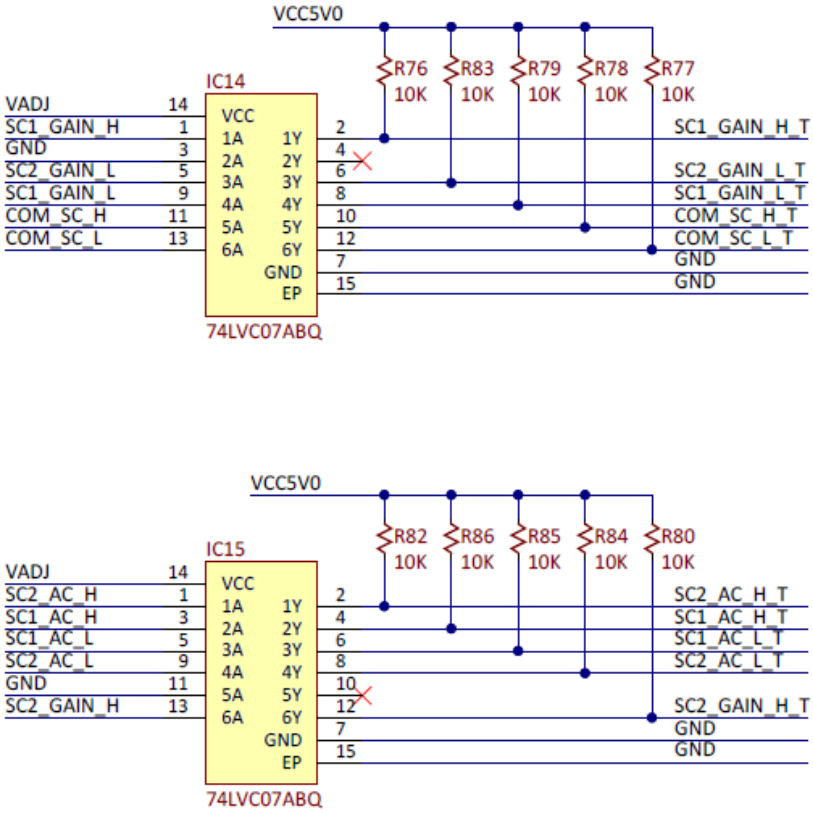
(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/relaydrivers.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 4. Relay Drivers.

IC14 and IC15 in Fig. 5 are 74LVC07ABQ (https://www.nexperia.com/products/analog-logic-ics/asynchronous-interface-logic/buffers-inverters-drivers/74LVC07ABQ.html) open-drain gates used as level translators from VADJ = 1.8V to VCC5V0 = 5V.

- 5 V tolerant inputs and outputs (open-drain) for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Complies with JEDEC standard:

- JESD8-7A (1.65 V to 1.95 V)
- JESD8-5A (2.3 V to 2.7 V)
- JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
- HBM JESD22-A114F exceeds 2000 V
- MM JESD22-A115-B exceeds 200 V
- CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



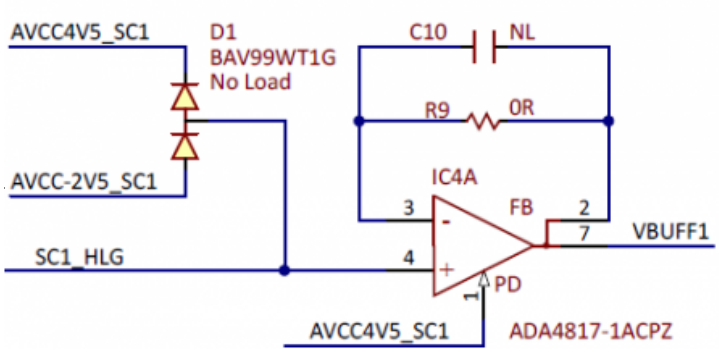
(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/leveltranslators.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 5. Level Translators. []

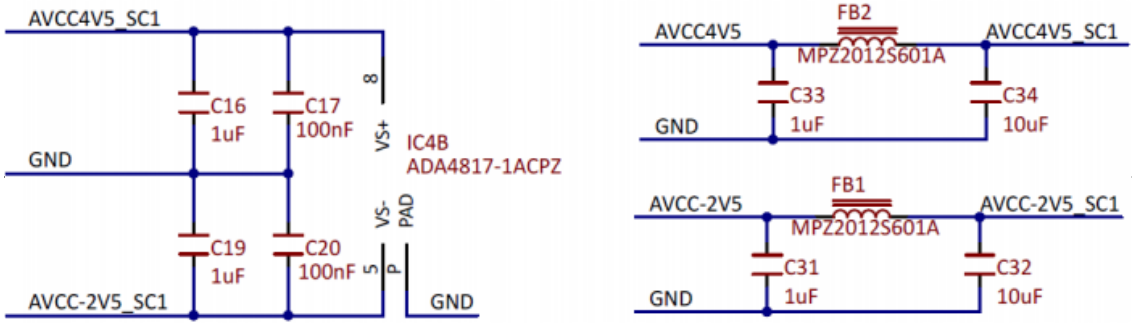
2.2. Scope Buffer

A non-inverting ADA4817 (https://www.analog.com/en/products/ada4817-1.html) stage provides very high impedance as load for the input divider.

- High speed
  - −3 dB bandwidth (G = 1, RL = 100 Ω): 1050 MHz ()
  - Slew rate: 870 V/µs
  - 0.1% settling time: 9 ns
- Input bias current: 2 pAtypical
- Input capacitance
  - Common-mode capacitance: 1.3 pF typical
  - Differential mode capacitance: 0.1 pF typical
- Low input noise
  - Voltage noise: 4 nV/√Hz at 100 kHz ()
  - Current noise: 2.5 fA/√Hz at 100 kHz ()
- Low distortion: −90 dBc at 10 MHz () (G = 1, RL = 1 kΩ)
- Linear output current: 40 mA
- Supply quiescent current per amplifier: 19 mAtypical
- Powered down supply quiescent current per amplifier: 1.5 mAtypical



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/buffer.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/buffersup.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 6. Buffer. []

The ADA4817 (https://www.analog.com/en/products/ada4817-1.html) is supplied +4.5V/-2.5V.

The maximum input voltage swing is:

$$-2.5V < V_{SC-HLG} < 1.7V \tag{18}$$

The maximum output voltage swing is:

$$-1.3V < V_{BUFF} < 3.1V \tag{19}$$

The gain is:

$$\frac{V_{BUFF}}{V_{SC-HLG}} = 1 \tag{20}$$

The actual input and output range (for nominal usage) is:

$$-1V < V_{SC-HLG} = V_{BUFF} < 1V \tag{21}$$

The ADA4817 (https://www.analog.com/en/products/ada4817-1.html) data sheet does not include any explicit or implicit mention of input protection diodes, nor about the maximum current supported by such diodes, so external D1 was added in the schematic for safety. However, the leakage current of D1 adds significant error and experiments proved that the input protection diodes do exist within the ADA4817 (https://www.analog.com/en/products/ada4817-1.html), so D1 is a "No Load".

The Zmod ADC () is specified to resist to accidental input voltages up to +/-50V. In these cases, the buffer input voltage is limited by the protection diodes at 0.6V above the AVCC4V5 or below AVCC-2V5. The protection current is limited by R2 (at High Gain) or R1+R3 (at Low Gain) (see the input divider schematic). The worse case is V_{SCOPE_SMA}=-50V on High Gain scale:

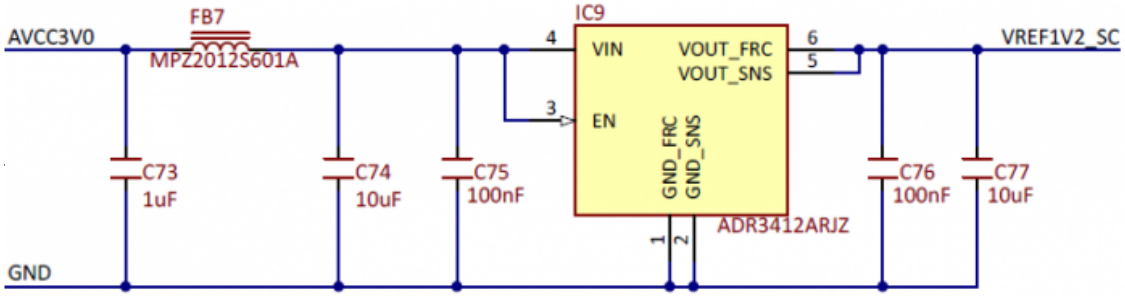
$$I_{+} = \frac{V_{SCOPE-SMA} - V_{AVCC-2V5}}{R_2} = \frac{-50V + 2.5V}{40.2kohm} = -1.18mA \tag{22}$$

2.3. Scope Reference

In Fig. 7, a low noise reference, ADR3412ARJZ (http://www.analog.com/en/special-linear-functions/voltage-references/adr3412/products/product.html), and an ADA4841-2 (https://www.analog.com/en/products/ada4841-2.html) OpAmp are used to generate 1V reference voltage for the ADC ().

ADR3412ARJZ (http://www.analog.com/en/special-linear-functions/voltage-references/adr3412/products/product.html) features:

- Initial accuracy: ±0.1% (maximum)
- Maximum temperature coefficient: 8 ppm/°C
- Operating temperature range: −40°C to +125°C
- Output current: +10 mA source/−3 mA sink
- Low quiescent current: 100 µA (maximum)
- Low dropout voltage: 250 mV at 2 mA
- Output noise (0.1



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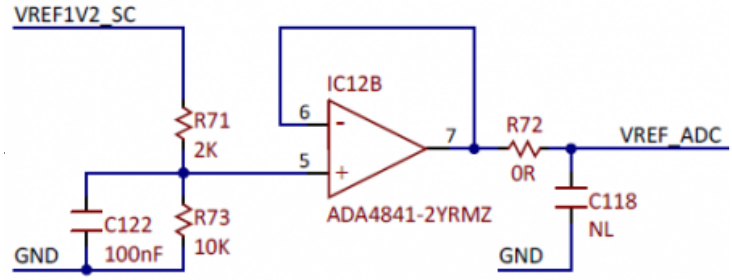


(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/vref1v0.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 7. ADC Reference.

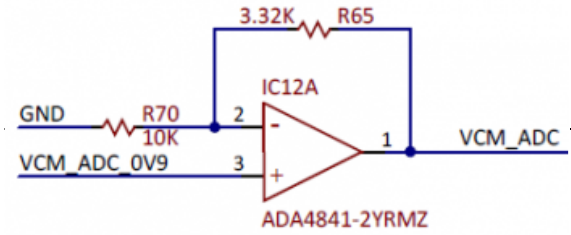
The ADC () reference voltage is:

$$V_{REFADC} = V_{REF1V2SC} * \frac{R_{73}}{R_{71} + R_{73}} = 1V \tag{23}$$

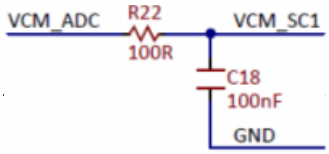
An ADA4841-2 (https://www.analog.com/en/products/ada4841-2.html) OpAmp buffers the VCM voltage generated by the ADC () to feed the ADC () buffer, in Fig. 8.

ADA4841-2 (https://www.analog.com/en/products/ada4841-2.html):

- Low power: 1.1 mA/amp
- Low wideband noise
  - 2.1 nV/√Hz
  - 1.4 pA/√Hz
- Low 1/f noise
  - 7 nV/√Hz @ 10 Hz ()
  - 13 pA/√Hz @ 10 Hz ()
- Low distortion: −105 dBc @ 100 kHz (), VO = 2 V p-p
- High speed
  - 80 MHz (), −3 dB bandwidth (G = +1)
  - 12 V/µs slew rate
  - 175 ns settling time to 0.1%
- Low offset voltage: 0.3 mV maximum
- Rail-to-rail output
- Power down
- Wide supply range: 2.7 V to 12 V



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/vcm.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/vcmfilter.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 8. VCM buffer.

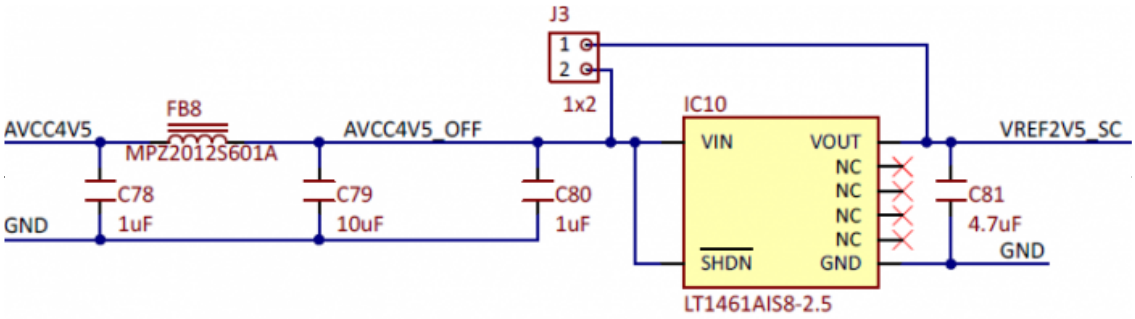
The ADC () VCM voltage is:

$$V_{CMSC} = V_{VCMADC} = V_{VCMADC0V9} * (1 + \frac{R_{65}}{R_{70}}) = 1.2V \quad (24)$$

An LT1461-2.5 (https://www.analog.com/en/products/lt1461.html) reference generates a voltage used for rising the input common mode voltage of the ADC () buffer, in Fig. 10.

LT1461-2.5 (https://www.analog.com/en/products/lt1461.html):

- Trimmed to High Accuracy: 0.04% Max
- Low Drift: 3ppm/°C Max
- Low Supply Current: 50µA Max
- High Output Current: 50mA Min
- Low Dropout Voltage: 300mV Max
- Excellent Thermal Regulation
- Power Shutdown
- Thermal Limiting
- All Parts Guaranteed Functional from –40°C to 125°C
- Voltage Options: 2.5V, 3V, 3.3V, 4.096V and 5V



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/vref2v5.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 9. 2.5V reference. []

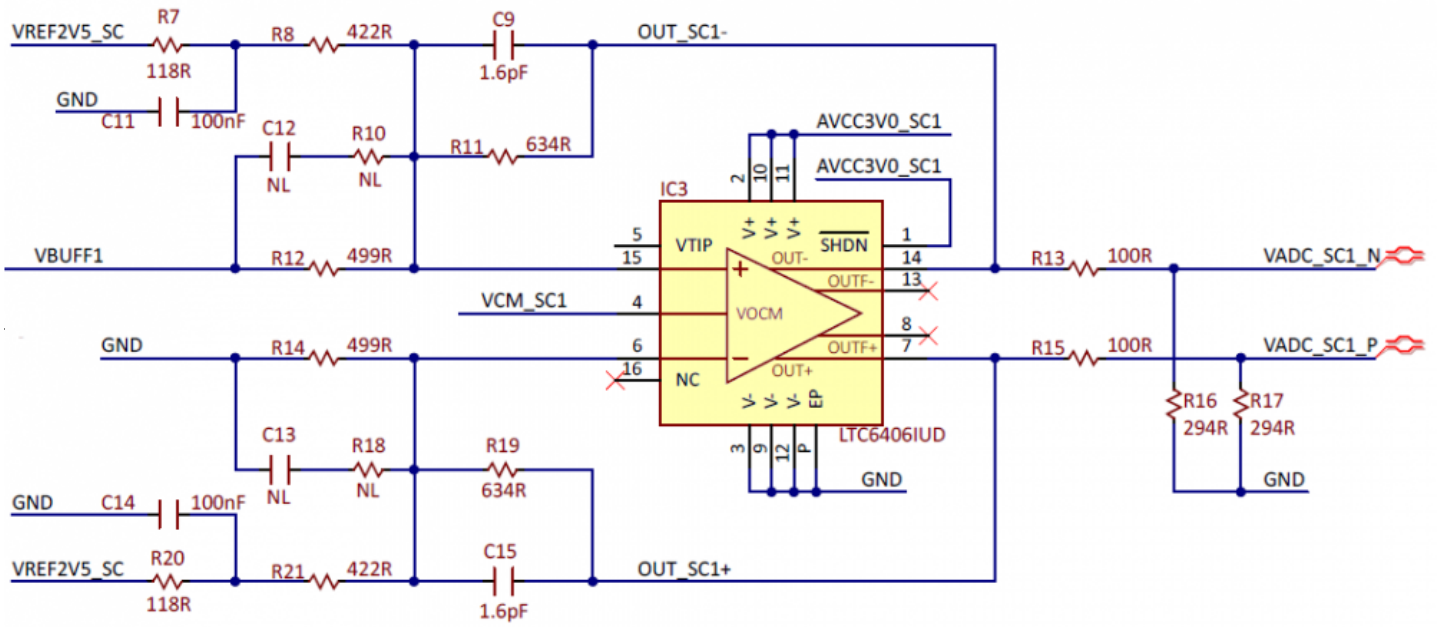
2.4. Scope Driver

IC2, LTC6406 (https://www.analog.com/en/products/ltc6406.html), in Fig. 10 is the ADC () dirver.

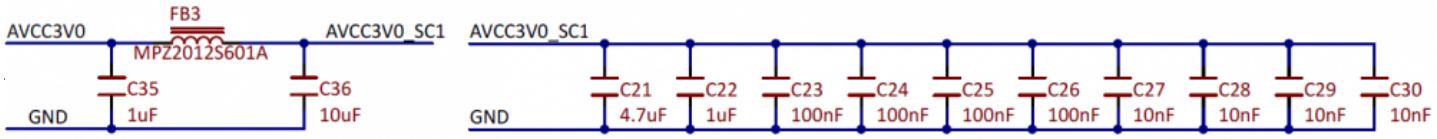
- Low Noise: 1.6nV/√Hz RTI
- Low Power: 18mA at 3V
- Low Distortion (HD2/HD3):
  - –80dBc/–69dBc at 50MHz, 2VP-P
  - –104dBc/–90dBc at 20MHz, 2VP-P
- Rail-to-Rail Differential Input
- 2.7V to 3.5V Supply Voltage Range
- Fully Differential Input and Output
- Adjustable Output Common Mode Voltage
- 800MHz –3dB Bandwidth with AV = 1
- Gain-Bandwidth Product: 3GHz
- Low Power Shutdown
- Available in 8-Lead MSOP and Tiny 16-Lead
- 3mm × 3mm × 0.75mm QFN Packages

It is used for:

- Driving the differential inputs of the ADC () (with low impedance outputs)
- Providing the common mode voltage for the ADC ()
- ADC () protection: IC2 is supplied 3V, while the ADC () inputs only support -0.1…2.1V.



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/driver.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/driversup.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 10. ADC Driver. []

The input common mode voltage range is rail-to-rail:

$$0V \leq V_{+LTC6406} = V_{-LTC6406} \leq 3V \tag{25}$$

The actual input common mode voltage is:

The driver gain is:

$$G_{drv} = \frac{V_{OUTdiff}}{V_{BUFF}} = \frac{R_{11}}{R_{12}} = \frac{R_{19}}{R_{14}} = 1.27 \tag{26}$$

The output divider gain:

$$G_{div} = \frac{V_{ADCdiff}}{V_{OUTdiff}} = \frac{R_{16}}{R_{13} + R_{16}} = \frac{R_{17}}{R_{15} + R_{17}} = 0.746 \tag{27}$$

The nominal Driver input voltage range is:

$$-1V < V_{BUFF} < 1V \tag{28}$$

The nominal Driver output voltage range is:

$$-1.27V < V_{OUT\ diff} < 1.27V \tag{29}$$

With a unity common mode gain, the driver output common mode voltage is:

$$V_{CMOUT} = (V_{OUT+} + V_{OUT-})/2 = V_{CMSC} = 1.2V \tag{30}$$

The nominal Buffer output single ended voltage range is:

$$V_{CMOUT} - V_{OUT\ diff}/2 = 1.2V - 1.27/2 = 0.565V < V_{OUT+}, V_{OUT-} < V_{CMOUT} + V_{OUT\ diff}/2 = 1.2V + 1.27/2 = 1.835V \tag{31}$$

The maximum nominal driver single ended current is:

$$I_{OUT\ max} = \frac{V_{OUT\ max}}{R_{13} + R_{16}} = \frac{1.835V}{394ohm} = 4.65mA \tag{32}$$

which is below the data sheet limit of 5mA, for covering the driver single ended voltage range above.

For passing at the ADC () input, the voltages above are multiplied by the resistive divider gain of G_{div}.

The nominal differential ADC () input voltage range is:

$$-1V < V_{ADC\ diff} < 1V \tag{33}$$

The output divider common mode voltage is close to the recommended 0.9V:

$$V_{CMADC} = (V_{ADCP} + V_{ADCN})/2 = 0.895V \tag{34}$$

The ADC () input single ended voltage range is:

$$0.395V < V_{ADCP}, V_{ADCN} < 1.395V \tag{35}$$

For the ADC () input protection, the maximum driver single ended voltage should be considered. The driver amplifier datasheet only specifies the linear output voltage range. There is no information about the worst case saturated output voltages. Based on the data sheet and measurements, the driver maximum saturated single ended voltage was estimated to:

$$V_{OUT\ max\ sat} < 2.5V \tag{36}$$

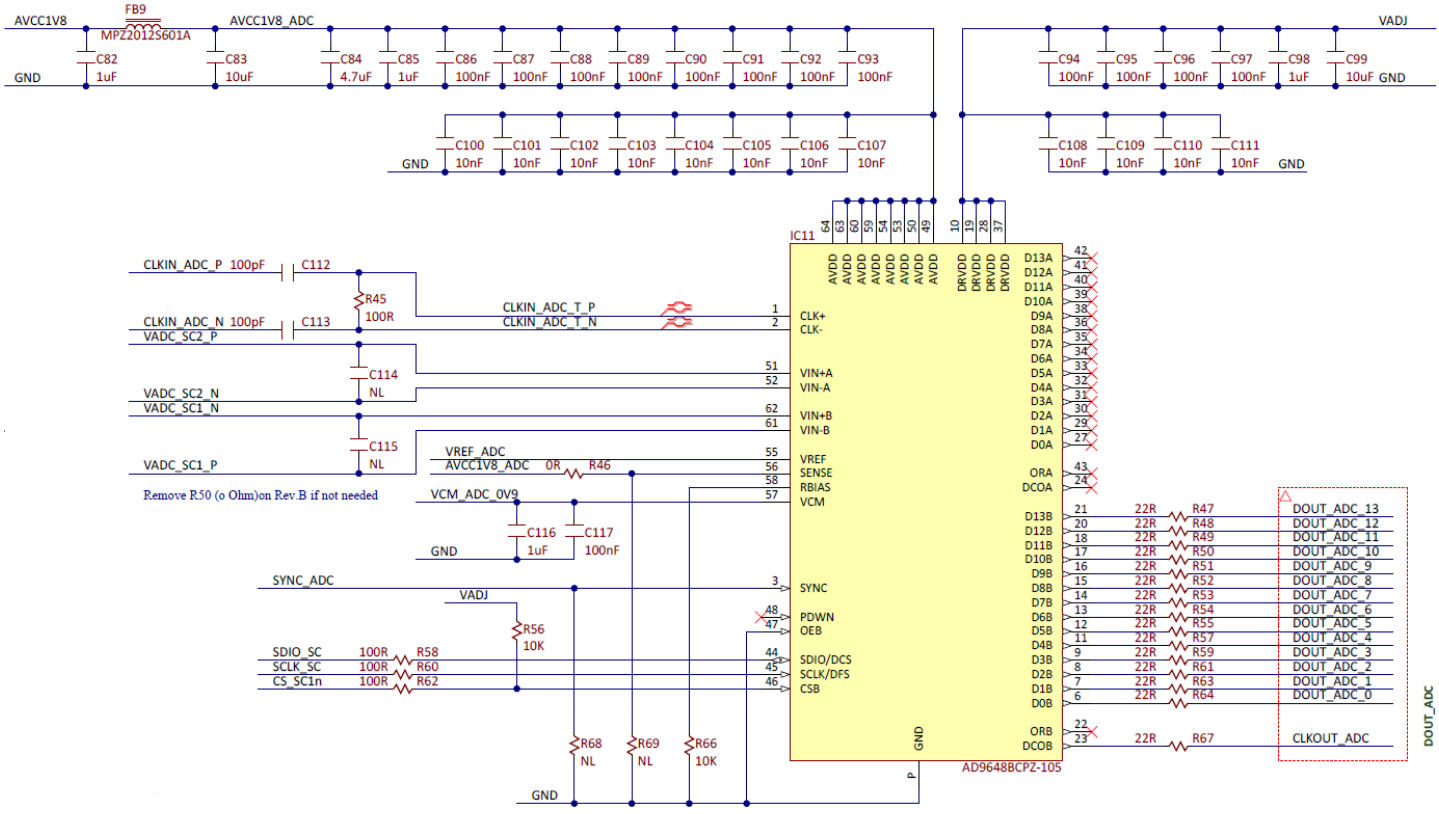
Resulting a stress value at the ADC () input:

$$V_{ADC\ max\ sat} = V_{OUT\ max\ sat} * G_{div} = 1.865V \tag{37}$$

which is less than the allowed voltage at the ADC () input = 2.1V.

2.5. Scope ADC

The Zmod ADC () uses a dual channel, high speed, low power, 14-bit, 105MS/s ADC () (Analog part number AD9648 (http://www.analog.com/en/analog-to-digital-converters/ad-converters/ad9648/products/product.html)), as shown in Fig. 11.



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/adc.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 11. ADC. []

The important features of AD9648:

- SNR = 74.5dBFS @70 MHz ()
- SFDR =91dBc @70 MHz ()
- Low power: 78mW/channel ADC () core@ 125MS/s
- Differential analog input with 650 MHz () bandwidth
- IF sampling frequencies to 200 MHz ()

- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = ±0.35 LSB
- Serial port control options
- Offset binary, gray code, or two's complement data format
- Optional clock duty cycle stabilizer
- Integer 1-to-8 input clock divider
- Data output multiplex option
- Built-in selectable digital test pattern generation
- Energy-saving power-down modes
- Data clock out with programmable clock and data alignment

The differential inputs are driven via a low-pass filter comprised of C114 together with R13, R15, R16, R17 in the buffer stage. The differential clock is AC-coupled and the line is impedance matched. The clock is internally divided by 4 to operate the ADC () at a constant 100 MHz () sampling rate. The ADC () generates the common mode reference voltage (VCM_SC) to be used in the buffer stage.

The digital stage of the ADC () and the corresponding FPGA bank are supplied at 1.8V by the SYZYGY™ voltage V_{adj}.

The multiplexed mode is used, to combine the two channels on a single data bus and minimize the number of used FPGA pins. CLKOUT_SC is provided to the FPGA for synchronizing data.

2.6. Scope Signal Scaling

Combining Gain equations 2, 4, 20, 26, and 27 from previous chapters, the total scope gains are:

$$Low\ gain = \frac{V_{ADC\ diff}}{V_{SCOPE-SMA}} = 0.038 \tag{38}$$

$$High\ gain = \frac{V_{ADC\ diff}}{V_{SCOPE-SMA}} = 0.91 \tag{39}$$

Considering the ADC () input voltage range shown in 33:

$$at\ low\ gain: -26.3V < V_{SCOPE-SMA} < 26.3V$$

$$at\ high\ gain: -1.1V < V_{SCOPE-SMA} < 1.1V \tag{40}$$

To cover component value tolerances and to allow software calibration, only the ranges below are specified.

$$at\ low\ gain: -25V < V_{SCOPE-SMA} < 25V \tag{41}$$

$$at\ high\ gain: -1V < V_{SCOPE-SMA} < 1V \tag{42}$$

With the 14-bit ADC (), the absolute resolution of the scope is:

$$at\ low\ gain: \frac{52.6V}{2^{14}} = 3.21mV \tag{43}$$

$$at\ high\ gain: \frac{2.12V}{2^{14}} = 0.13mV \tag{44}$$

For V_{in} voltage value at the input of the Scope channel, the ZmodADC sends a signed 14 bit integer, N. This value is used to compute V_{in}:

$$V_{in} = \frac{N \cdot Range \cdot (1 + CG)}{2^{13}} + CA \tag{45}$$

were:

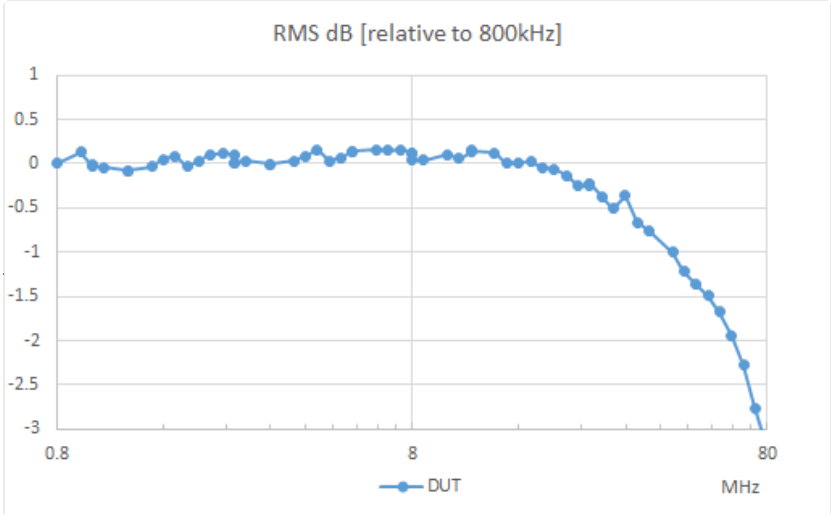
- N = the 14 bit, 2's complement integer number returned by the ADC ()
- V_{in}= the corrected value of the input voltage
- CA = calibration Additive constant (for the appropriate channel and gain; see Table 3)
- CG = calibration Gain constant (for the appropriate channel and gain; see Table 3)
- Range= the ideal Range of the Scope input stage (approximation of the values in equation 40):
  - 1.086 (for low range: ±1V) or
  - 26.25 (for high range: ±25V)

2.7 Scope Spectral Characteristics

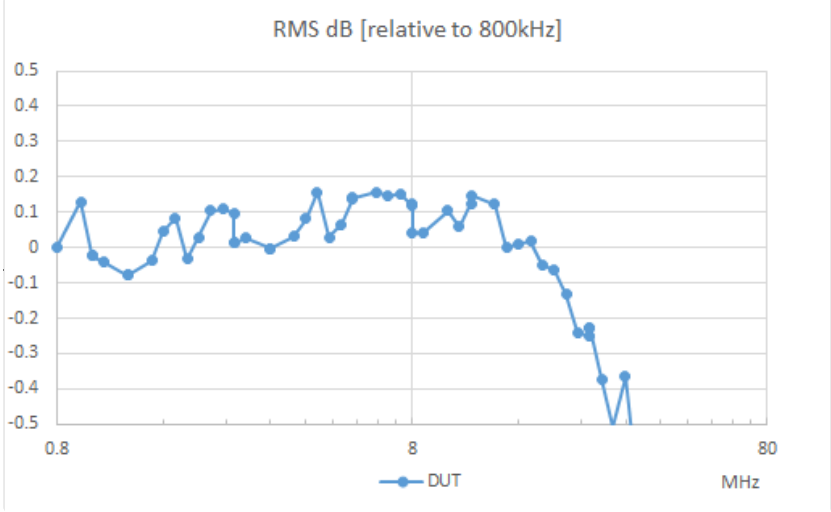
Fig. 12 shows a typical spectral characteristic of the scope input stage. A PXIe-5433 80 MHz () Function/Arbitrary Waveform Generator was used to generate the input signal of 0.9V, for High Gain Scale, respectively 10V for the Low Gain scale. A Tektronix DPO5204B scope was used for measuring the reference signal (at the scope SMA connector) and the output signal (at the input of the ADC ()). A differential probe was used to read the output signal on the pads of the unloaded C115. The signal swept from 800kHz to 80MHz. The effective values of the input and output signals were recorded for each frequency. The measurements were furter processesd to display the input stage frequency characteristics, as shown in Fig. 10.

For both scales, the 3dB bandwidth is 70MHz+. The 0.5dB bandwidth is 30MHz and the 0.1dB bandwidth is 20MHz.

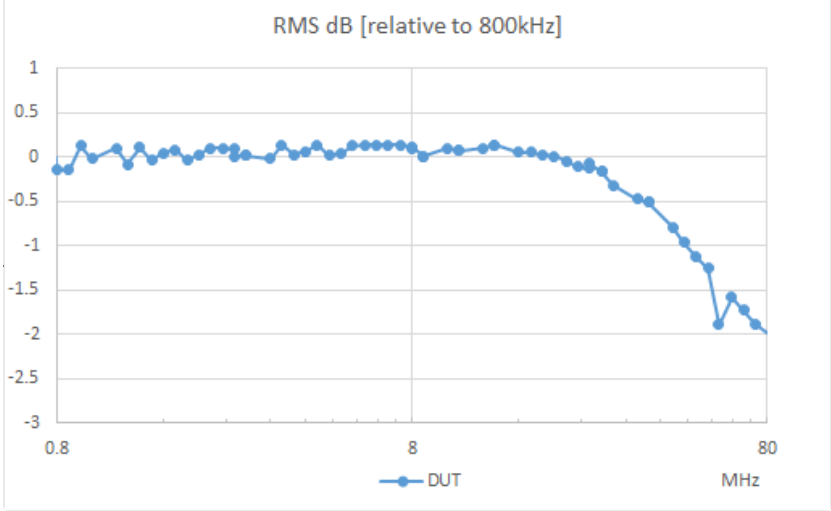
The standard -3dB bandwidth definition is derived from filter theory. At cutout frequency, the scope attenuates the spectral components by 0.707, assuming an error of ~30%, way too high for a measuring instrument. The bandwidth with a specified flatness is useful to better define the scope spectral performances. The Zmod ADC () exhibits 30MHz+ @ 0.5dB, meaning that a 30 MHz () sinusoidal signal is shown with a flatness error of a max 5.6%. 20MHz @ 0.1dB means that a 5 MHz () sinusoidal signal is shown with a flatness error of a max 1.1%.



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/bwdclg3db.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/bwdclg05db.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)



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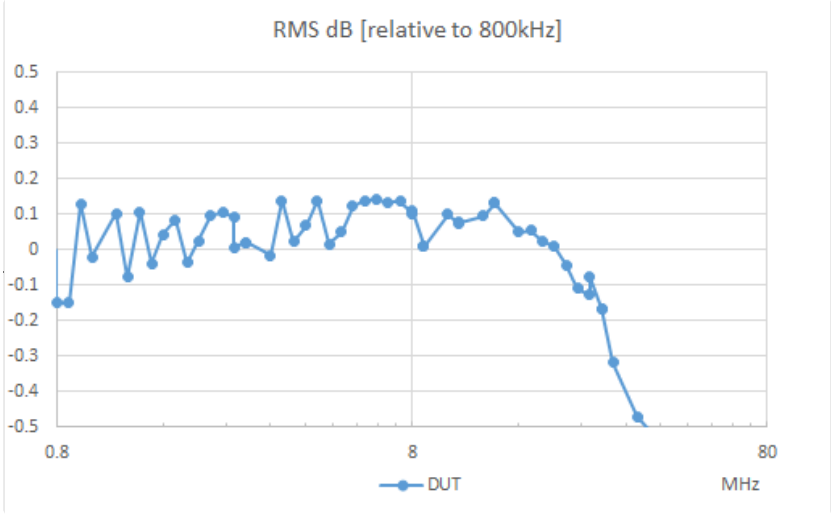


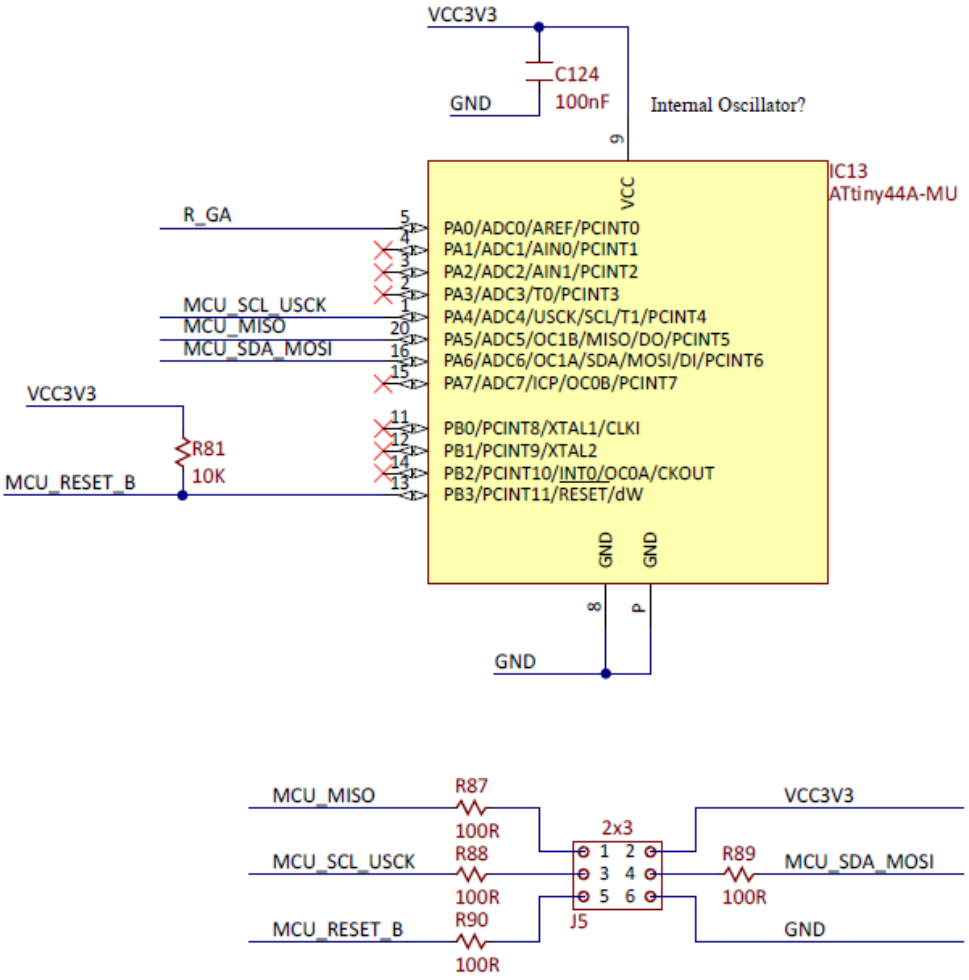
(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/bwdchg05db.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 12. Scope input stage Bandwidth - Low Gain scale (up) and High Gain scale (down). 0.5dB detail (right)

3. MCU

The ATtinny44 (https://www.microchip.com/wwwproducts/en/ATTINY44A) MCU in Fig. 13 works as a I2C memory, storing the SYZYGY™ DNA information and the Calibration Coefficients. The J5 connector is used for programming the MCU and the SYZYGY™ DNA at manufacturing.

The DNA and the Factory Calibration Coefficients are stored in the Flash memory of the MCU, which appears to the I2C interface as "read-only". The User Calibration Coefficients are stored in the EEPROM () memory of the MCU, which is write-protected via a magic number at a magic address. The memory structure can be consulted below.



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/mcu.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 13. The MCU

- Program Memory Type: Flash
- Program Memory Size (KB): 4
- CPU Speed (MIPS/DMIPS): 20
- SRAM Bytes: 256
- Data EEPROM ()/HEF (bytes): 256
- Digital Communication Peripherals: 1-SPI, 1-I2C
- Capture/Compare/PWM Peripherals: 1 Input Capture, 1 CCP, 4PWM
- Timers: 1 x 8-bit, 1 x 16-bit
- Number of Comparators: 1
- Temperature Range (C): -40 to 85
- Operating Voltage Range (V): 1.8 to 5.5
- Pin Count: 14
- Low Power: Yes

Table 1. The Flash memory structure []

Address	Function	Size (Bytes)
0x8000 - 0x80FF	DNA	256
0x8100 - 0x817F	Factory Calibration	128
0x8180 - 0x83FF	Future use	896

3.1. SYZYGY™ DNA

The Zmod ADC () is compliant with SYZYGY™ Specification (https://syzygyfpga.io/specification/). It contains an MCU able to calculate the Geographical Address and provide the DNA information via I2C. The DNA is stored in the MCU FLASH at the address range: 0x8000 - 0x80FF with the following structure:

Table 2. The Zmod ADC DNA structure []

Contents	Type	Size(Bytes)	Value	Address
DNA full data length	uint16	2	91	0x8000
DNA header length	uint16	2	40	0x8002
SYZYGY DNA major version	uint8	1	1	0x8004
SYZYGY DNA minor version	uint8	1	0	0x8005
Required SYZYGY DNA major version	uint8	1	1	0x8006
Required SYZYGY DNA minor version	uint8	1	0	0x8007
Maximum operating 5V load (mA)	uint16	2	400	0x8008
Maximum operating 3.3V load (mA)	uint16	2	100	0x800A
Maximum VIO load (mA)	uint16	2	270	0x800C
Attribute flags	uint16	2	0	0x800E
Minimum operating VIO (10 mV steps)	uint16	2	180	0x8010
Maximum operating VIO (10 mV steps)	uint16	2	180	0x8012
Minimum operating VIO (10 mV steps)	uint16	2	170	0x8014
Maximum operating VIO (10 mV steps)	uint16	2	190	0x8016
Minimum operating VIO (10 mV steps)	uint16	2	0	0x8018
Maximum operating VIO (10 mV steps)	uint16	2	0	0x801A

Contents	Type	Size(Bytes)	Value	Address
Minimum operating VIO (10 mV steps)	uint16	2	0	0x801C
Maximum operating VIO (10 mV steps)	uint16	2	0	0x801E
Manufacturer name length	uint8	1	12	0x8020
Product name length	uint8	1	13	0x8021
Product model / Part number length	uint8	1	13	0x8022
Product version / revision length	uint8	1	1	0x8023
Serial number length	uint8	1	12	0x8024
RESERVED	uint8	1	0	0x8025
CRC-16 (most significant byte)	uint8	1	0x40	0x8026
CRC-16 (least significant byte)	uint8	1	0xF0	0x8027
END DATA HEADER				
Manufacturer name	string	12	Digilent Inc	0x8028
Product name	string	13	Zmod ADC () 1410	0x8034
Product model / Part number	string	13	Zmod ADC () 1410	0x8041
Product version / revision	string	1	B	0x804E
Serial number	string	12	210396000000	0x804F

3.2. Calibration Memory

The analog circuitry described in previous chapters includes passive and active electronic components. The datasheet specs show parameters (resistance, capacitance, offsets, bias currents, etc.) as typical values and tolerances. The equations in previous chapters consider typical values. Component tolerances affect DC and AC performances of the Zmod ADC (). To minimize these effects, the design uses:

- 0.1% resistors and 1% capacitors in all the critical analog signal paths
- Capacitive trimmers for balancing the Scope Input Divider and Gain Selection
- No other mechanical trimmers (as these are big, expensive, unreliable and affected by vibrations, aging, and temperature drifts)
- Software calibration, at manufacturing
- User software calibration, as an option

A software calibration is performed on each device as a part of the manufacturing test. Reference signals are connected to the Scope inputs. A set of measurements is used to identify all the DC errors (Gain, Offset) of each analog stage. Correction (Calibration) parameters are computed and stored in the Calibration Memory, on the Zmod ADC () device, both as Factory Calibration Data and User Calibration Data. The WaveForms software allows the user performing an in-house calibration and overwrite the User Calibration Data. Returning to Factory Calibration is always possible.

The Software reads the calibration parameters from the Zmod ADC () MCU via the I2C bus and uses them to correct the acquired signals. The structure of the calibration data is shown below:

Table 3. The Calibration Data Structure

Heading 1	Name	Size (Bytes)	Type	Flash Address (Factory Calibration)	EEPROM () Address (User Calibration)
Magic ID		1	uchar 0xAD	0x8100	0x7000
Calibration Time		4	unix timestamp	0x8104	0x7004
Channel 1 LG Gain	CG	4	float32	0x8108	0x7008
Channel 1 LG Offset	CA	4	float32	0x810C	0x700C

Heading 1	Name	Size (Bytes)	Type	Flash Address (Factory Calibration)	EEPROM () Address (User Calibration)
Channel 1 HG Gain	CG	4	float32	0x8110	0x7010
Channel 1 HG Offset	CA	4	float32	0x8114	0x7014
Channel 2 LG Gain	CG	4	float32	0x8118	0x7018
Channel 2 LG Offset	CA	4	float32	0x811C	0x701C
Channel 2 HG Gain	CG	4	float32	0x8120	0x7020
Channel 2 HG Offset	CA	4	float32	0x8124	0x7024
Reserved Area		68	-	0x8168	0x7068
Log		22	string	0x817E	0x707E
CRC		1	uchar	0x817F	0x707F

Table 4. The EEPROM Memory Map

Address	Function	Size (Bytes)
0x7000 - 0x707F	User Calibration	128
0x7080 - 0x70FF	Future Use	128

At the power up the EEPROM () memory is protected against write operations. To disable the write protection one has to write a magic number to a magic address over I2C. To re-enable the write protection one has to write a any other number to the magic address.

Table 5. The Write Protection Disable magic number and address

Magic Number	Magic Adress
0xD2	0x6FFF

4. Power Supplies and Control

This block includes the internal power supplies.

The Zmod ADC () gets the digital rails from the carrier board, via the SYZYGY connector:

- VCC5V0 - used for relays and analog supplies
- VCC3V3 - used for the MCU and analog supplies
- Vadj = 1.8V - used for the ADC () digital rail

The internal analog rails sequence is:

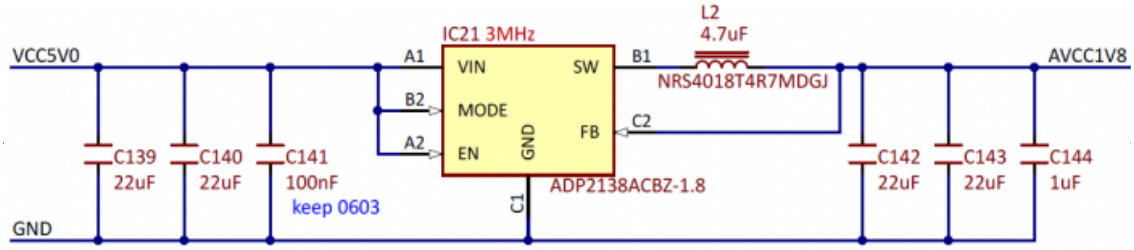
- AVCC1V8 - ADC () analog rail
- AVCC3V0 - ADC () driver
- AVCC-2V5, AVCC4V5 - Scope buffer, reference voltage

4.1. AVCC1V8

The analog supply AVCC1V8 is built from VCC5V0 using IC21, an ADP2138 (http://www.analog.com/en/power-management/switching-regulators-integrated-fet-switches/adp2138/products/product.html) Fixed Output Voltage, 800mA, 3MHz, Step-Down DC-to-DC converter. To insure low output voltage ripple a second LC filter (FB9 in Fig. 9) is added and forced PWM mode is selected.

- Input voltage: 2.3 V to 5.5 V
- Peak efficiency: 95%
- 3 MHz () fixed frequency operation
- Typical quiescent current: 24 µA
- Very small solution size

- 6-lead, 1 mm × 1.5 mm WLCSP package
- Fast load and line transient response
- 100% duty cycle low dropout mode
- Internal synchronous rectifier, compensation, and soft start
- Current overload and thermal shutdown protections
- Ultra-low shutdown current: 0.2 µA (typical)
- Forced PWM and automatic PWM/PSM modes



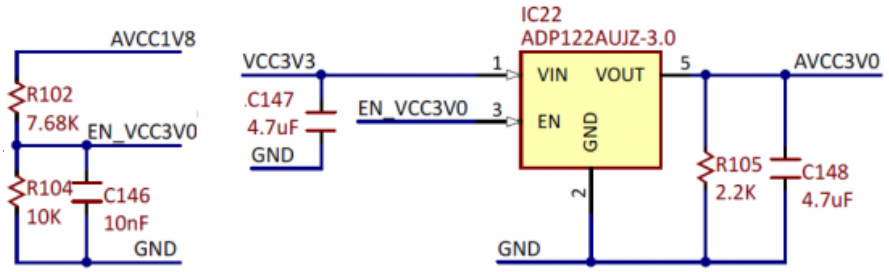
(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/avcc1v8.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 14. AVCC1V8

4.2. AVCC3V0

The analog supply AVCC3V0 is built from VCC3V3 using IC22, an ADP122 (https://www.analog.com/en/products/adp122.html) 5.5 V Input, 300 mA, Low Quiescent Current, CMOS Linear Regulator, Fixed Output Voltage. To reduce noise and reduce the crosstalk between supplied circuits, the rail uses individual LC filters: FB3 in Fig. 10, FB6 (Channel 2 ADC () Driver - not shown), FB7 in Fig. 7.

- Input voltage supply range: 2.3 V to 5.5 V
- 300 mA maximum output current
- Fixed and adjustable output voltage versions
- Very low dropout voltage: 85 mV at 300 mA load
- Low quiescent current: 45 µA at no load
- Low shutdown current: <1 µA
- Initial accuracy: ±1% accuracy
- Up to 31 fixed-output voltage options available from
- 1.75 V to 3.3 V
- Adjustable-output voltage range
- 0.8 V to 5.0 V (ADP123)
- Excellent PSRR performance: 60 dB at 100 kHz ()
- Excellent load/line transient response
- Optimized for small 1.0 µF ceramic capacitors
- Current limit and thermal overload protection
- Logic controlled enable
- Compact packages: 5-lead TSOT and 6-lead 2 mm × 2 mm LFCSP



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/avcc3v0.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

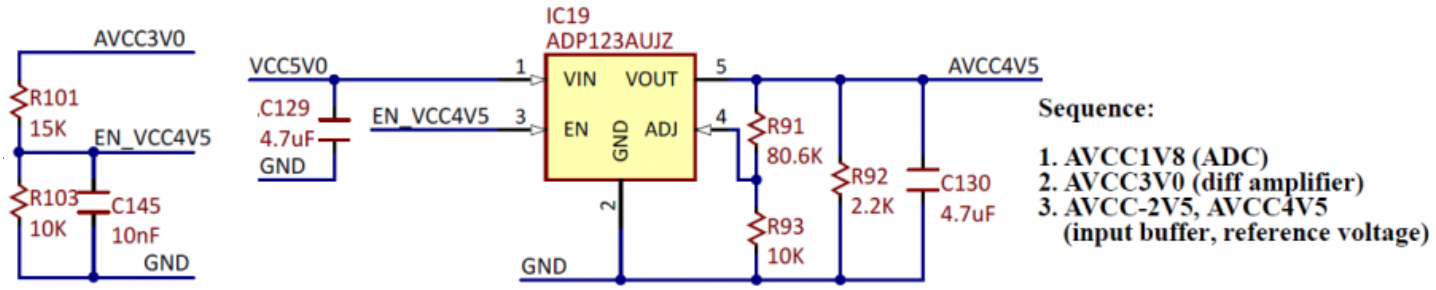
Figure 15. AVCC3V0

4.3. AVCC4V5

The analog supply AVCC4V5 is built from VCC5V0 using IC19, an ADP123 (https://www.analog.com/en/products/adp123.html) 5.5 V Input, 300 mA, Low Quiescent Current, CMOS Linear Regulator, Adjustable Output Voltage. To reduce noise and reduce the crosstalk between supplied circuits, the rail uses individual LC filters: FB2 in Fig. 6, FB5 (Channel 2 ADC () Buffer - not shown), FB8 in Fig. 9.

- Input voltage supply range: 2.3 V to 5.5 V
- 300 mA maximum output current
- Fixed and adjustable output voltage versions
- Very low dropout voltage: 85 mV at 300 mA load
- Low quiescent current: 45 µA at no load
- Low shutdown current: <1 µA
- Initial accuracy: ±1% accuracy
- Up to 31 fixed-output voltage options available from
- 1.75 V to 3.3 V

- Adjustable-output voltage range
- 0.8 V to 5.0 V (ADP123)
- Excellent PSRR performance: 60 dB at 100 kHz ()
- Excellent load/line transient response
- Optimized for small 1.0 µF ceramic capacitors
- Current limit and thermal overload protection
- Logic controlled enable
- Compact packages: 5-lead TSOT and 6-lead 2 mm × 2 mm LFCSP



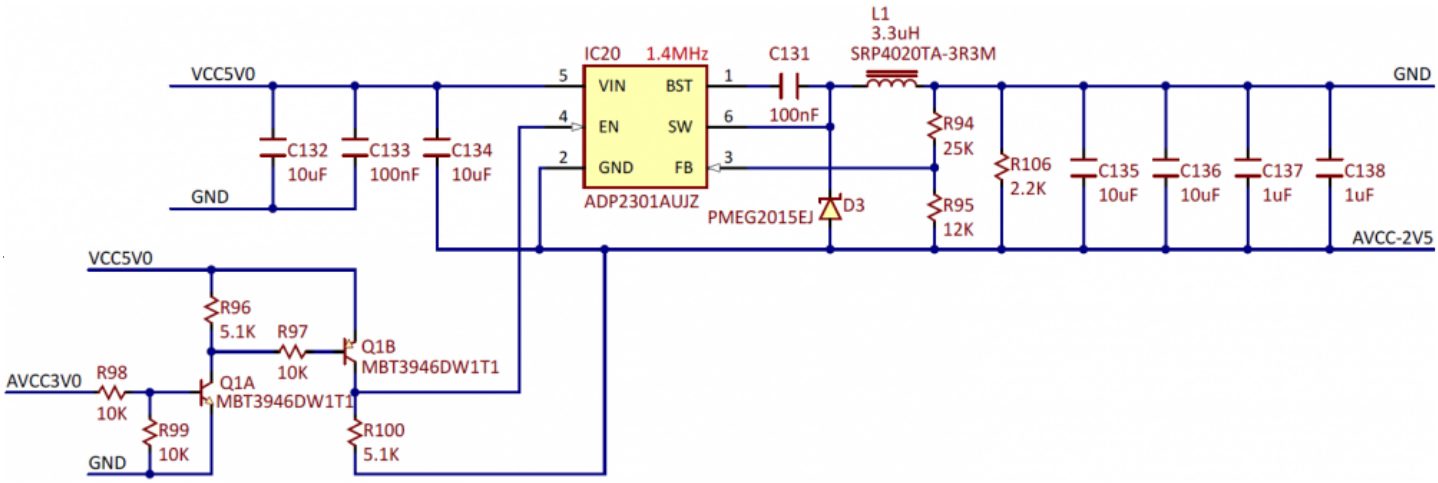
(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/avcc4v5.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 16. AVCC4V5 []

4.4. AVCC-2V5

The AVCC-2V5 analog power supply is implemented with the ADP2301 (http://www.analog.com/en/power-management/switching-regulators-integrated-fet-switches/adp2301/products/product.html) Step-Down regulator in an inverting Buck-Boost configuration. See application Note AN-1083: Designing an Inverting Buck Boost Using the ADP2300 and ADP2301 (http://www.analog.com/static/imported-files/application_notes/AN-1083.pdf). To reduce noise and reduce the crosstalk between supplied circuits, the rail uses individual LC filters: FB1 in Fig. 6, FB4 (Channel 2 ADC ()) Buffer - not shown). The ADP2301 features:

- 1.2 A maximum load current
- ±2% output accuracy over temperature range
- 1.4 MHz () switching frequency
- High efficiency up to 91%
- Current-mode control architecture
- Output voltage from 0.8 V to 0.85 × VIN
- Automatic PFM/PWM mode switching
- Integrated high-side MOSFET and bootstrap diode,
- Internal compensation and soft start
- Undervoltage lockout (UVLO), Overcurrent protection (OCP) and thermal shutdown (TSD)
- Available in ultrasmall, 6-lead TSOT package



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/avccneg2v5.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

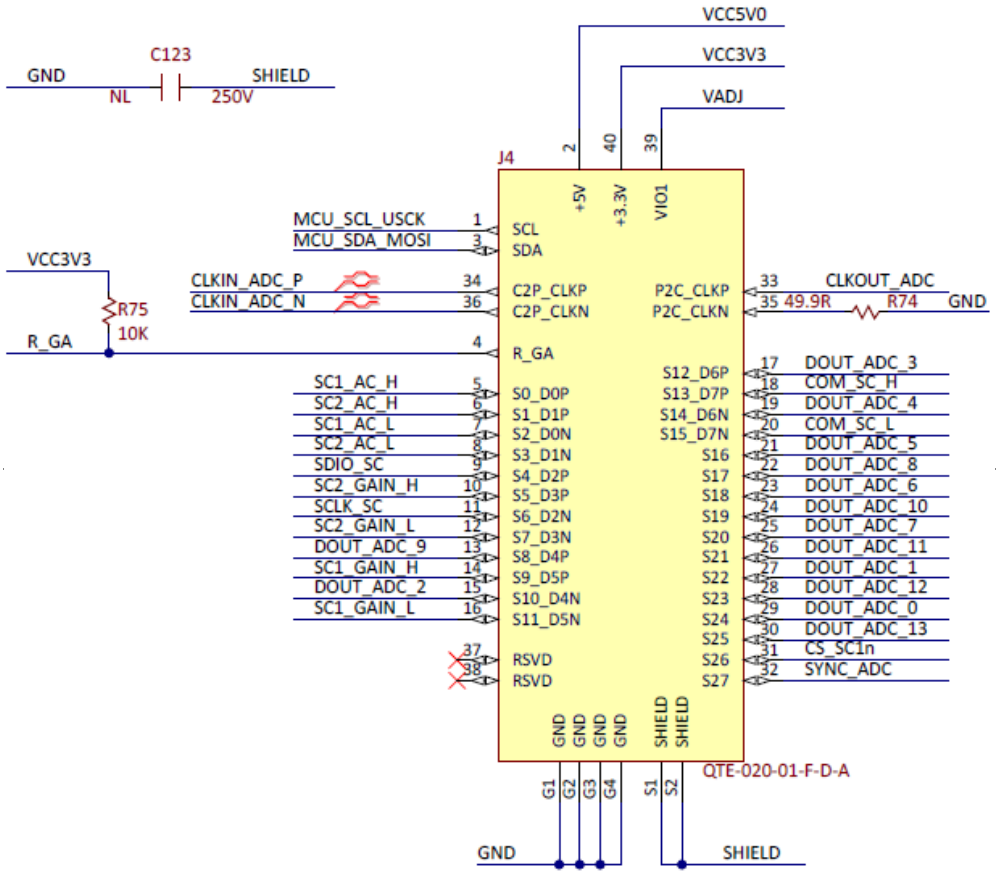
Figure 17. AVCC-2V5 []

5. The SYZYGY™ Connector

The SYZYGY™ connector in provides the interface with the carrier board. The used signals are:

- Power rails
  - VCC5V0
  - VCC3V3
  - VADJ - needs to be set by the carier board to 1.8V

    - GND_()
    - Shield
- SYZYGY™ I2C bus:
    - MCU_SCLUSCK
    - MCU_SDA_MOSI_()
- ADC_() differential input clock
    - CLKIN_ADC_()_P
    - CLKIN_ADC_()_N
- ADC_() single ended output clock:
    - CLKOUT_ADC_() (coupled with GND_() in the differential P2C pair)
- R_GA for geographical address identification
- SYNC_ADC_() for ADC_() internal clock divider synchronization
- ADC_() data bus: DOUT_ADC_()_0…13
- ADC_() SPI bus:
    - CS_()_SC1n
    - SCLK_()_SC
    - SDIO_SC
- relay control
    - SCx_yy_z



(https://reference.digilentinc.com/_detail/reference/instrumentation/zmodadc/syzygyconn.png?id=reference%3Azmod%3Azmodadc%3Areference-manual)

Figure 18. SYZYGY™ connector []

6. The SYZYGY™ compatibility table

Table 6. The SYZYGY™ compatibility table []

Parameter	Value
Maximum 5V supply current	400mA
Maximum 3.3V supply current	100mA
VIO supply voltage	1.8V
Maximum VIO supply current	270mA

Parameter	Value
Total number of I/O	28
Number of differential I/O pairs	0
Width	Single

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