Product Change Notification / SYST-24EVEA235

Date:

28-Sep-2020

Product Category:

Interface- Controller Area Network (CAN)

PCN Type:

Document Change

Notification Subject:

ERRATA - MCP2518FD Silicon Errata and Data Sheet Clarification Document Revision

Affected CPNs:

SYST-24EVEA235_Affected_CPN_09282020.pdf
SYST-24EVEA235_Affected_CPN_09282020.csv

Notification Text:

SYST-24EVEA235

Microchip has released a new Product Documents for the MCP2518FD Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at MCP2518FD Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
This revision includes the following updates to Data Sheet Clarifications:
1) Added ECC Module, SPI Module, SPI/RAM Module and SPI/GPIO Module.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 28 Sep 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

MCP2518FD Silicon Errata and Data Sheet Clarification

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Affected Catalog Part Numbers (CPN)

MCP2518FDT-E/QBB
MCP2518FDT-E/QBBV02
MCP2518FDT-E/QBBVAO
MCP2518FDT-E/SL
MCP2518FDT-E/SLVAO
MCP2518FDT-H/QBB
MCP2518FDT-H/QBBV01
MCP2518FDT-H/QBBVAO
MCP2518FDT-H/SL
MCP2518FDT-H/SLVAO

MCP2518FD
Silicon Errata and Data Sheet Clarification

The functionality of the MCP2518FD devices is described in the Device Data Sheet (DS20006027A), except for the anomalies described below.

1. Module: SPI Module

TX MAB underflow due to long delays between SPI bytes:

The SPI interface blocks the CAN FD Controller module from accessing RAM between the 15th and 18th rising edge of SCK, during an SPI READ instruction, while accessing RAM.

If the CAN FD Controller module is blocked for more than TSPIMAXDLY, a TX MAB underflow can occur.

Fix/Work Around:

Keep the delay between two SPI bytes shorter than TSPIMAXDLY; see Figure 1.

The maximum allowed delay between two bytes depends on which CAN Message Frame is transmitted, and on the selected Nominal Bit Time (NBT) and Data Bit Time (DBT). Table 1 lists TSPIMAXDLY for the worst-case scenarios.

For example, TSPIMAXDLY is 8.5 µs for a CAN FD frame at 500 kbps/2 Mbps. In comparison, an SPI byte takes 0.67 µs at 12 MHz SCK. A delay of ten times the duration of one SPI byte could cause a TX MAB underflow. It is highly unlikely for an MCU application to introduce such a long delay, but this error could occur when running an operation system, such as Linux® on a slower MPU.

In case of a TX MAB underflow, the device will notify the application by setting SERRIF and MODIF, and by transitioning to Restricted Operation or Listen Only mode (depending on CiCON.SERR2LOM). After the application requests Normal mode, the CAN FD Controller module will automatically attempt to retransmit the message that caused the TX MAB underflow. It is not necessary to reset the device.

FIGURE 1: MAXIMUM DELAY BETWEEN SPI BYTES

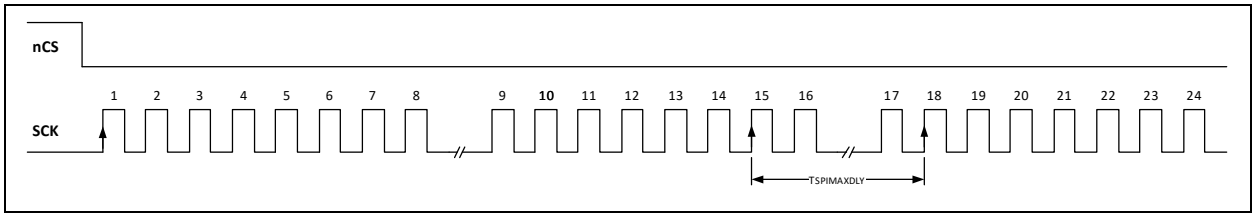

TABLE 1: WORST-CASE SCENARIOS

Scenario	Frame Format	TSPIMAXDLY
1	CAN Base Frame	5 NBT
2	CAN FD Control Field	3 NBT + 5 DBT
3	CAN FD Data Phase	32 DBT

2. Module: ECC Module

ECC single error correction does not work in all cases:

Fix/Work Around:

Enable single error correction and double error detection interrupts by setting SECIE and DEDIE. Handle SECIF as a detection interrupt and do not rely on the error correction. Instead, handle both interrupts as a notification that the RAM word at ERRADDR was corrupted.

3. Module: SPI Module

SFR address rollover does not work:

The SFR address rollover, from 0x3FF to 0x000 and from 0xFFF to 0xE00, does not work. Instead, the address changes from 0x3FF to 0x400 and from 0xFFF to 0x000.

The address rollover for the RAM works as described.

Fix/Work Around:

None.

4. Module: SPI/RAM Module

The SPI can write corrupted data to the RAM at fast SPI speeds:

Simultaneous activity on the CAN bus while writing data to RAM via the SPI interface, with high SCK frequency, can lead to corrupted data being written to RAM.

Fix/Work Around:

Ensure that FSCK is less than or equal to 0.85 * (FSYSCLK/2).

5. Module: SPI/GPIO Module

Writing multiple bytes to the IOCON register using one SPI `WRITE` instruction may overwrite LAT0 and LAT1:

Writing Byte 2 and Byte 3 of the IOCON register using one SPI `WRITE` instruction clears LAT0 and LAT1.

Fix/Work Around:

When setting LAT0 or LAT1, do not use a multi-data byte SPI `WRITE` instruction.

Instead, write the bit fields in the IOCON register using single data byte SFR `WRITE` instructions.

Clarifications/Corrections to the Data Sheet:

In the MCP2518FD Data Sheet (DS20006027A), the following clarifications and corrections should be noted.

None.

APPENDIX A: REVISION HISTORY

Revision B (September 2020)

- Added **ECC Module**, **SPI Module**, **SPI/RAM Module** and **SPI/GPIO Module**.

Revision A (May 2018)

- Initial Release of this Document.

NOTES:

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