LM317 3-Terminal Adjustable Regulator

1 Features

- Output Voltage Range Adjustable From 1.25 V to 37 V
- Output Current Greater Than 1.5 A
- Internal Short-Circuit Current Limiting
- Thermal Overload Protection
- Output Safe-Area Compensation

2 Applications

- ATCA Solutions
- DLP: 3D Biometrics, Hyperspectral Imaging, Optical Networking, and Spectroscopy
- DVR and DVS
- Desktop PC
- Digital Signage and Still Camera
- ECG Electrocardiogram
- EV HEV Charger: Level 1, 2, and 3
- Electronic Shelf Label
- Energy Harvesting
- Ethernet Switch
- Femto Base Station
- Fingerprint and Iris Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- High-Speed Data Acquisition and Generation
- Hydraulic Valve
- IP Phone: Wired and Wireless
- Intelligent Occupancy Sensing
- Motor Control: Brushed DC, Brushless DC, Low-Voltage, Permanent Magnet, and Stepper Motor
- Point-to-Point Microwave Backhaul
- Power Bank Solutions
- Power Line Communication Modem
- Power Over Ethernet (PoE)
- Power Quality Meter
- Power Substation Control
- Private Branch Exchange (PBX)
- Programmable Logic Controller
- RFID Reader
- Refrigerator
- Signal or Waveform Generator
- Software Defined Radio (SDR)
- Washing Machine: High-End and Low-End
- X-ray: Baggage Scanner, Medical, and Dental

3 Description

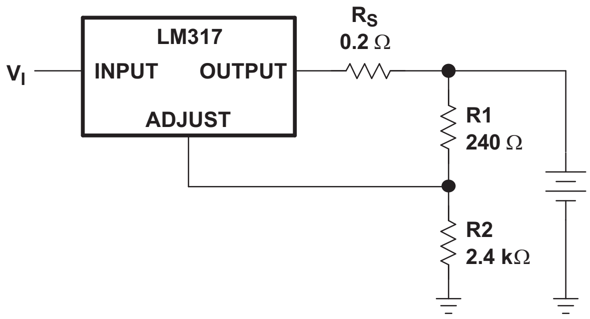
The LM317 device is an adjustable three-terminal positive-voltage regulator capable of supplying more than 1.5 A over an output-voltage range of 1.25 V to 37 V. It requires only two external resistors to set the output voltage. The device features a typical line regulation of 0.01% and typical load regulation of 0.1%. It includes current limiting, thermal overload protection, and safe operating area protection. Overload protection remains functional even if the ADJUST terminal is disconnected.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM317DCY	SOT-223 (4)	6.50 mm × 3.50 mm
LM317KCS	TO-220 (3)	10.16 mm × 9.15 mm
LM317KCT	TO-220 (3)	10.16 mm × 8.59 mm
LM317KTT	TO-263 (3)	10.16 mm × 9.01 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Battery-Charger Circuit



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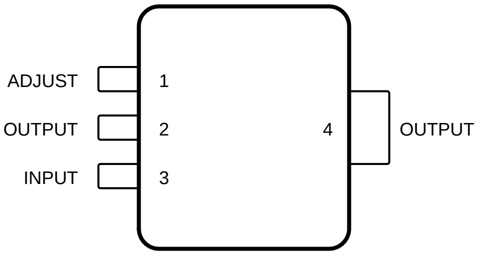
4 Revision History

Changes from Revision W (January 2015) to Revision X	Page
• Changed body size dimensions for KCS TO-220 Package on *Device information* table	1
• Changed body size dimensions for KTT TO-263 Package on *Device information* table	1
• Changed V_O Output Voltage max value from 7 to 37 on *Recommended Operating Conditions* table	4
• Added min value to I_O Output Current in *Recommended Operating Conditions* table	4
• Changed values in the Thermal Information table to align with JEDEC standards	4
• Added KCT package data to *Thermal Information* table	4
• Deleted Section 9.3.6 "Adjusting Multiple On-Card Regulators with a Single Control"	13
• Updated Adjustsable 4-A Regulator Circuit graphic	16
• Added *Receiving Notification of Documentation Updates* section and *Community Resources* section	19

Changes from Revision V (February 2013) to Revision W	Page
• Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Deleted *Ordering Information* table.	1

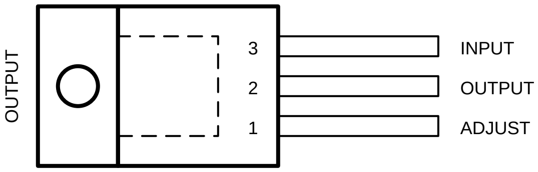
5 Pin Configuration and Functions

DCY Package
3-Pin SOT-223
Top View



Not to scale

KCS or KCT Package
3-Pin TO-220
Top View



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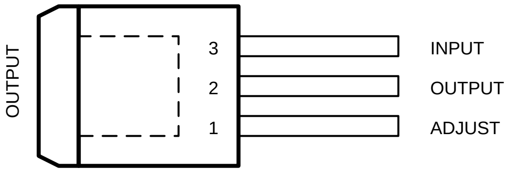
KTT Package
3-Pin TO-263
Top View



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Pin Functions

PIN			I/O	DESCRIPTION
NAME	TO-263, TO-220	SOT-223		
ADJUST	1	1	I	Output voltage adjustment pin. Connect to a resistor divider to set V_O
INPUT	3	3	I	Supply input pin
OUTPUT	2	2, 4	O	Voltage output pin

6 Specifications

6.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_I - V_O$	Input-to-output differential voltage		40	V
T_J	Operating virtual junction temperature		150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_O	Output voltage	1.25	37	V
$V_I - V_O$	Input-to-output differential voltage	3	40	V
I_O	Output current	0.01	1.5	A
T_J	Operating virtual junction temperature	0	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM317				UNIT
		DCY (SOT-223)	KCS (TO-220)	KCT (TO-220)	KTT (TO-263)	
		4 PINS	3 PINS	3 PINS	3 PINS	
$R_{\theta(JA)}$	Junction-to-ambient thermal resistance	66.8	23.5	37.9	38.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.2	15.9	51.1	36.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.9	7.9	23.2	18.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	3.0	13.0	6.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.8	7.8	22.8	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	0.1	4.2	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended ranges of operating virtual junction temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
Line regulation[2]	$V_I - V_O$ = 3 V to 40 V		T_J = 25°C		0.01	0.04	%/V
			T_J = 0°C to 125°C		0.02	0.07	
Load regulation	I_O = 10 mA to 1500 mA	C_{ADJ}[3] = 10 μF, T_J = 25°C	$V_O \le 5$ V			25	mV
			$V_O \ge 5$ V		0.1	0.5	%V_O
		T_J = 0°C to 125°C	$V_O \le 5$ V		20	70	mV
			$V_O \ge 5$ V		0.3	1.5	%V_O
Thermal regulation	20-ms pulse,	T_J = 25°C			0.03	0.07	%V_O/W
ADJUST terminal current					50	100	μA
Change in ADJUST terminal current	$V_I - V_O$ = 2.5 V to 40 V, $P_D \le 20$ W, I_O = 10 mA to 1500 mA				0.2	5	μA
Reference voltage	$V_I - V_O$ = 3 V to 40 V, $P_D \le 20$ W, I_O = 10 mA to 1500 mA			1.2	1.25	1.3	V
Output-voltage temperature stability	T_J = 0°C to 125°C				0.7		%V_O
Minimum load current to maintain regulation	$V_I - V_O$ = 40 V				3.5	10	mA
Maximum output current	$V_I - V_O \le 15$ V,	$P_D < P_{MAX}$[4]		1.5	2.2		A
	$V_I - V_O \le 40$ V,	$P_D < P_{MAX}$[4],	T_J = 25°C	0.15	0.4		
RMS output noise voltage (% of V_O)	f = 10 Hz to 10 kHz,	T_J = 25°C			0.003		%V_O
Ripple rejection	V_O = 10 V,	f = 120 Hz	C_{ADJ} = 0 μF[3]		57		dB
			C_{ADJ} = 10 μF[3]	62	64		
Long-term stability	T_J = 25°C				0.3	1	%/1k hr

(1) Unless otherwise noted, the following test conditions apply: $|V_I - V_O|$ = 5 V and I_{OMAX} = 1.5 A, T_J = 0°C to 125°C. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

(2) Line regulation is expressed here as the percentage change in output voltage per 1-V change at the input.

(3) C_{ADJ} is connected between the ADJUST terminal and GND.

(4) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

6.6 Typical Characteristics

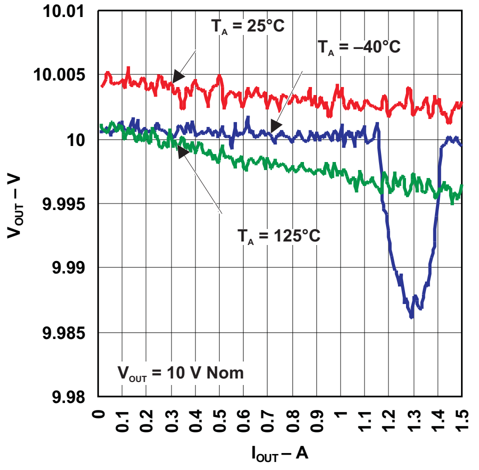


Figure 1. Load Regulation

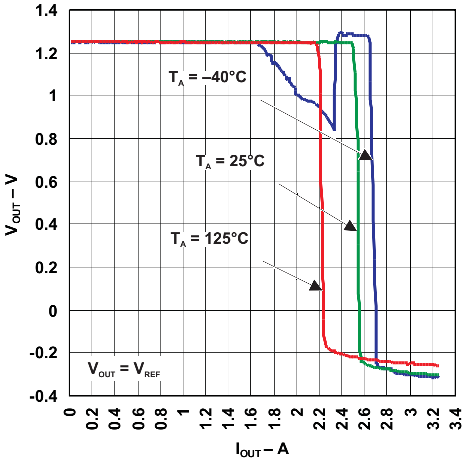


Figure 2. Load Regulation

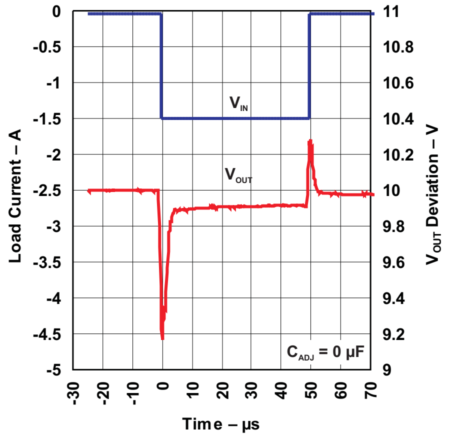


Figure 3. Load Transient Response

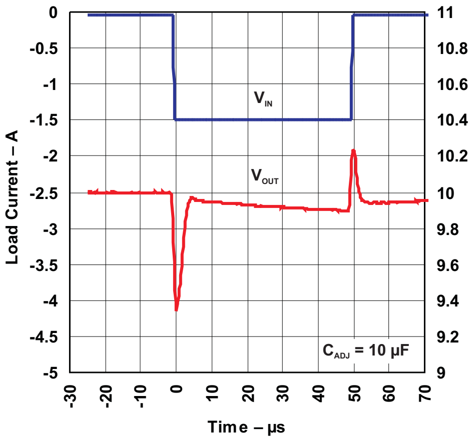


Figure 4. Load Transient Response

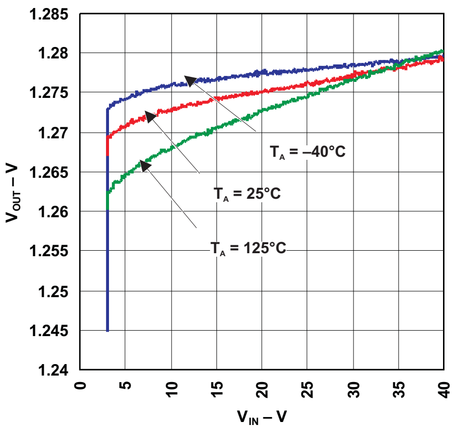


Figure 5. Line Regulation

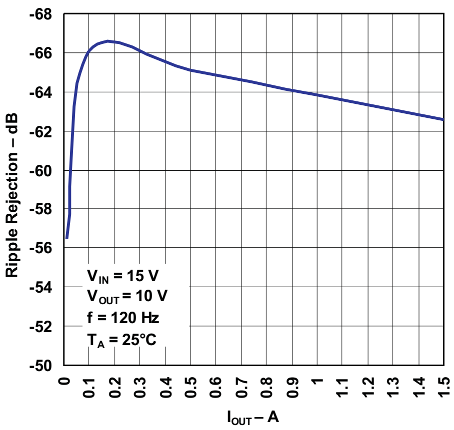


Figure 6. Ripple Rejection vs Output Current

Typical Characteristics (continued)

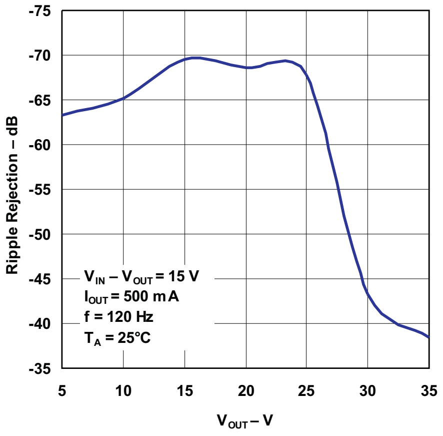


Figure 7. Ripple Rejection vs Output Voltage

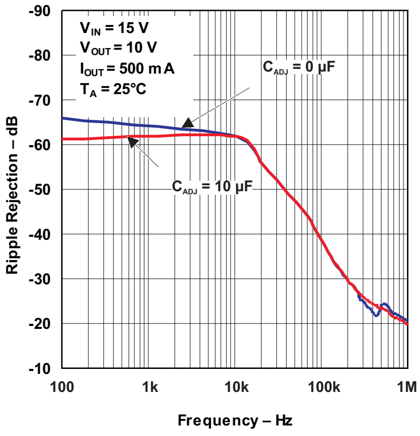


Figure 8. Ripple Rejection vs Frequency

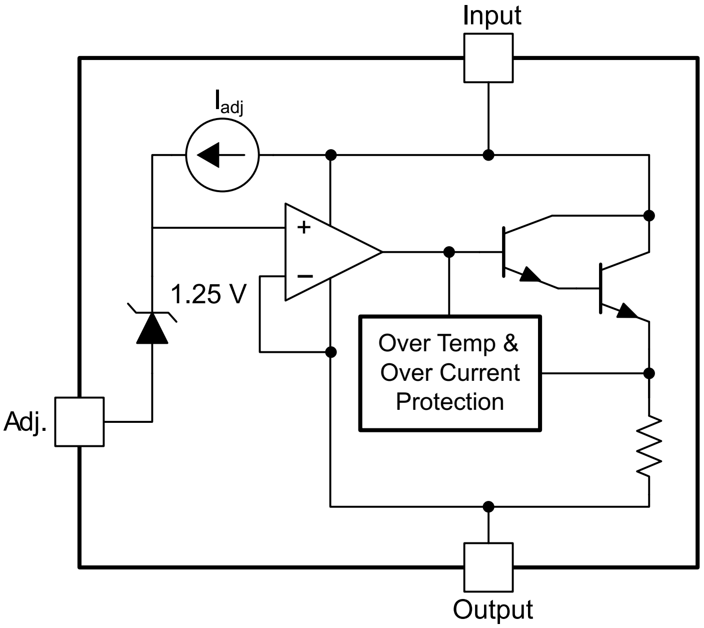
7 Detailed Description

7.1 Overview

The LM317 device is an adjustable three-terminal positive-voltage regulator capable of supplying up to 1.5 A over an output-voltage range of 1.25 V to 37 V. It requires only two external resistors to set the output voltage. The device features a typical line regulation of 0.01% and typical load regulation of 0.1%. It includes current limiting, thermal overload protection, and safe operating area protection. Overload protection remains functional even if the ADJUST terminal is disconnected.

The LM317 device is versatile in its applications, including uses in programmable output regulation and local on-card regulation. Or, by connecting a fixed resistor between the ADJUST and OUTPUT terminals, the LM317 device can function as a precision current regulator. An optional output capacitor can be added to improve transient response. The ADJUST terminal can be bypassed to achieve very high ripple-rejection ratios, which are difficult to achieve with standard three-terminal regulators.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 NPN Darlington Output Drive

NPN Darlington output topology provides naturally low output impedance and an output capacitor is optional. 3-V headroom is recommended (V_I – V_O) to support maximum current and lowest temperature.

7.3.2 Overload Block

Over-current and over-temperature shutdown protects the device against overload or damage from operating in excessive heat.

7.3.3 Programmable Feedback

Op amp with 1.25-V offset input at the ADJUST terminal provides easy output voltage or current (not both) programming. For current regulation applications, a single resistor whose resistance value is 1.25 V/I_O and power rating is greater than $(1.25\ V)^2/R$ should be used. For voltage regulation applications, two resistors set the output voltage.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device OUTPUT pin will source current necessary to make OUTPUT pin 1.25 V greater than ADJUST terminal to provide output regulation.

7.4.2 Operation With Low Input Voltage

The device requires up to 3-V headroom (V_I – V_O) to operate in regulation. The device may drop out and OUTPUT voltage will be INPUT voltage minus drop out voltage with less headroom.

7.4.3 Operation at Light Loads

The device passes its bias current to the OUTPUT pin. The load or feedback must consume this minimum current for regulation or the output may be too high. See the *Electrical Characteristics* table for the minimum load current needed to maintain regulation.

7.4.4 Operation In Self Protection

When an overload occurs the device shuts down Darlington NPN output stage or reduces the output current to prevent device damage. The device will automatically reset from the overload. The output may be reduced or alternate between on and off until the overload is removed.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The flexibility of the LM317 allows it to be configured to take on many different functions in DC power applications.

8.2 Typical Application

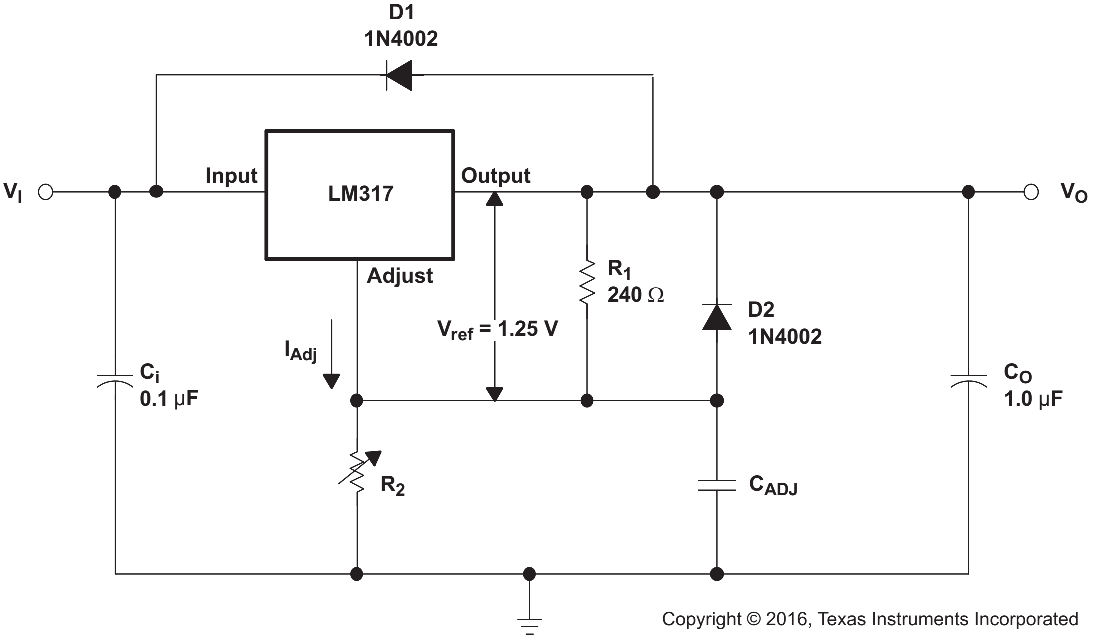


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Figure 9. Adjustable Voltage Regulator

8.2.1 Design Requirements

- R1 and R2 are required to set the output voltage.
- C_{ADJ} is recommended to improve ripple rejection. It prevents amplification of the ripple as the output voltage is adjusted higher.
- C_i is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1-µF or 1-µF ceramic or tantalum capacitor provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used.
- C_O improves transient response, but is not needed for stability.
- Protection diode D2 is recommended if C_{ADJ} is used. The diode provides a low-impedance discharge path to prevent the capacitor from discharging into the output of the regulator.
- Protection diode D1 is recommended if C_O is used. The diode provides a low-impedance discharge path to prevent the capacitor from discharging into the output of the regulator.

8.2.2 Detailed Design Procedure

V_O is calculated as shown in Equation 1. I_{ADJ} is typically 50 µA and negligible in most applications.

$$V_O = V_{REF} (1 + R2 / R1) + (I_{ADJ} \times R2) \quad (1)$$

Typical Application (continued)

8.2.3 Application Curves

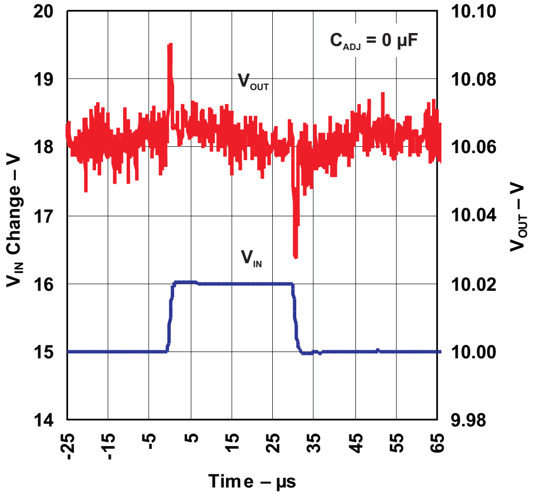

Figure 10. Line-Transient Response

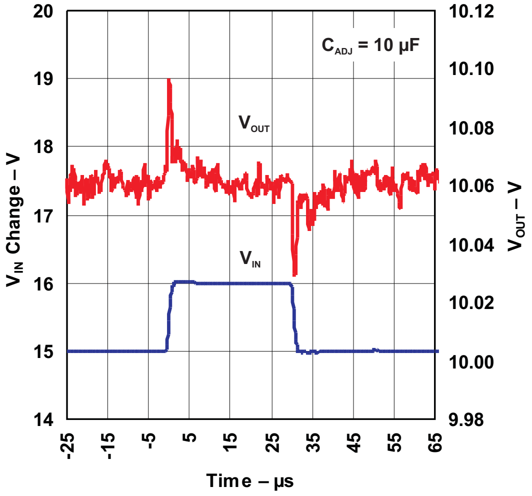

Figure 11. Line-Transient Response

8.3 System Examples

8.3.1 0-V to 30-V Regulator Circuit

Here, the voltage is determined by

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2 + R_3}{R_1}\right) - 10\,V$$

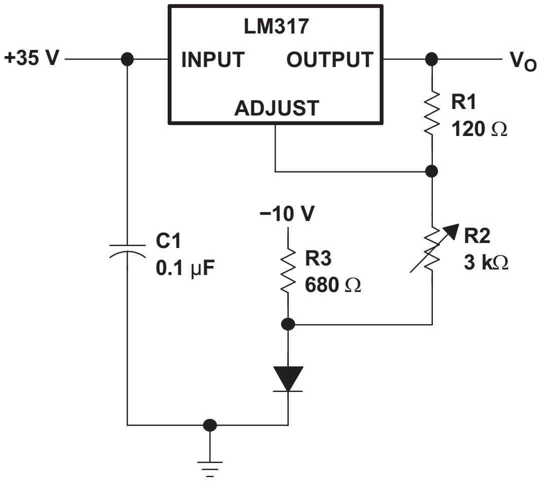

Figure 12. 0-V to 30-V Regulator Circuit

System Examples (continued)

8.3.2 Adjustable Regulator Circuit With Improved Ripple Rejection

C2 helps to stabilize the voltage at the adjustment pin, which helps reject noise. Diode D1 exists to discharge C2 in case the output is shorted to ground.

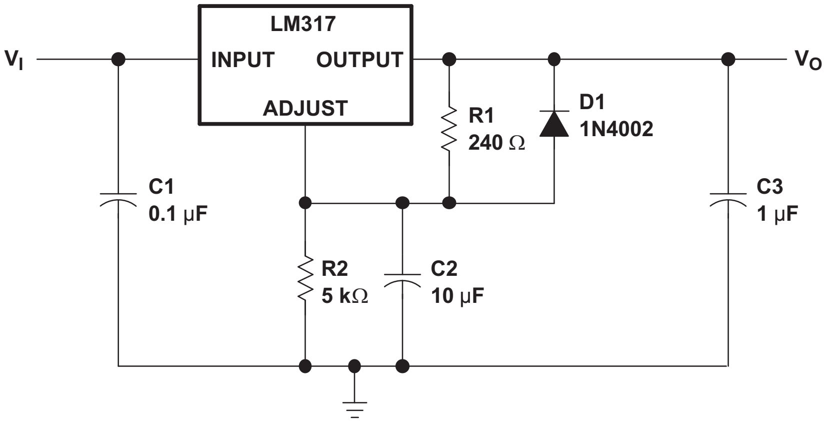

Figure 13. Adjustable Regulator Circuit with Improved Ripple Rejection

8.3.3 Precision Current-Limiter Circuit

This application limits the output current to the I_{LIMIT} in the diagram.

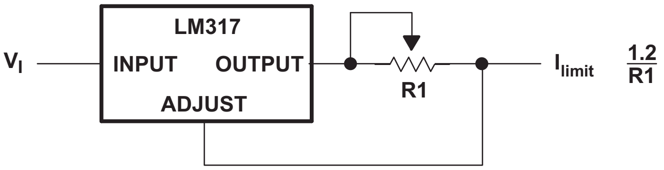

Figure 14. Precision Current-Limiter Circuit

8.3.4 Tracking Preregulator Circuit

This application keeps a constant voltage across the second LM317 in the circuit.

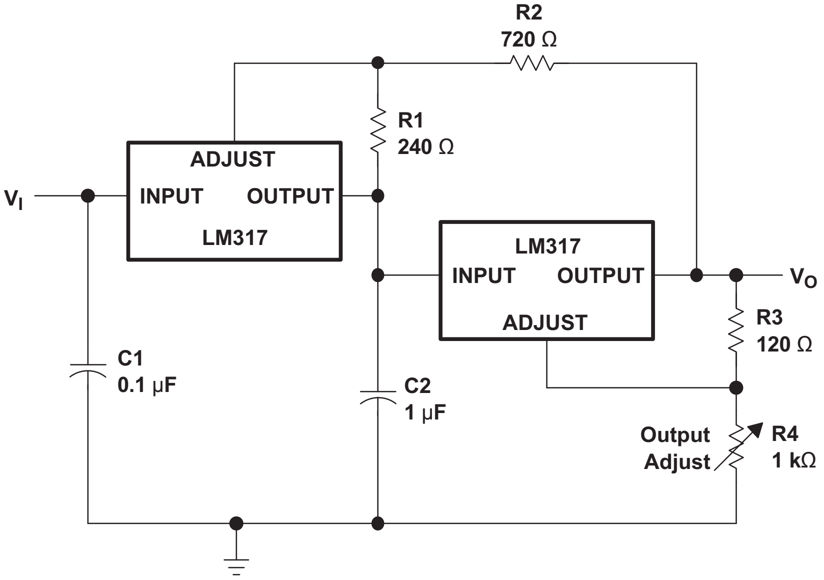

Figure 15. Tracking Preregulator Circuit

System Examples (continued)

8.3.5 1.25-V to 20-V Regulator Circuit With Minimum Program Current

Because the value of V_{REF} is constant, the value of R1 determines the amount of current that flows through R1 and R2. The size of R2 determines the IR drop from ADJUSTMENT to GND. Higher values of R2 translate to higher V_{OUT}.

$$V_{OUT} = V_{REF}\left(1+\frac{R_2+R_3}{R_1}\right) - 10\,V \tag{2}$$

$$\left(R1+R2\right)min = VoIreg(min) \tag{3}$$

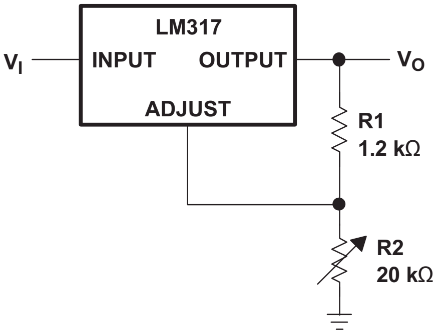

Figure 16. 1.25-V to 20-V Regulator Circuit With Minimum Program Current

8.3.6 Battery-Charger Circuit

The series resistor limits the current output of the LM317, minimizing damage to the battery cell.

$$V_{OUT} = 1.25V \times \left(\frac{R2}{R1+1}\right) \tag{4}$$

$$I_{OUT}(short) = \frac{1.25V}{RS} \tag{5}$$

$$\text{Output impendance} = RS \times \left(\frac{R2}{R1+1}\right) \tag{6}$$

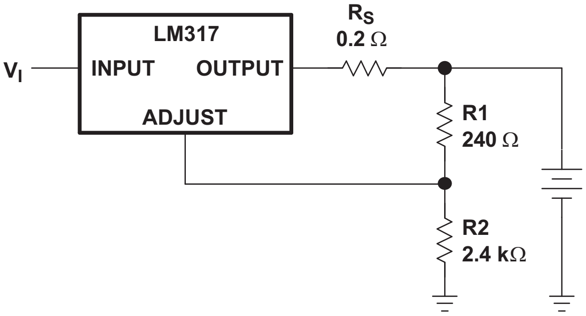

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Figure 17. Battery-Charger Circuit

System Examples (continued)

8.3.7 50-mA Constant-Current Battery-Charger Circuit

The current limit operation mode can be used to trickle charge a battery at a fixed current. I_{CHG} = 1.25 V ÷ 24 Ω. V_I should be greater than V_{BAT} + 4.25 V. (1.25 V [V_{REF}] + 3 V [headroom])

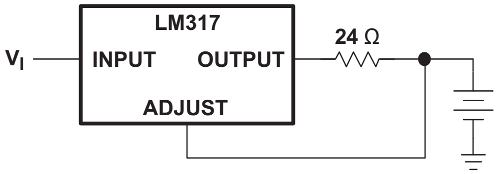


Figure 18. 50-mA Constant-Current Battery-Charger Circuit

8.3.8 Slow Turn-On 15-V Regulator Circuit

The capacitor C1, in combination with the PNP transistor, helps the circuit to slowly start supplying voltage. In the beginning, the capacitor is not charged. Therefore output voltage starts at V_{C1}+ V_{BE} + 1.25 V = 0 V + 0.65 V + 1.25 V = 1.9 V. As the capacitor voltage rises, V_{OUT} rises at the same rate. When the output voltage reaches the value determined by R1 and R2, the PNP will be turned off.

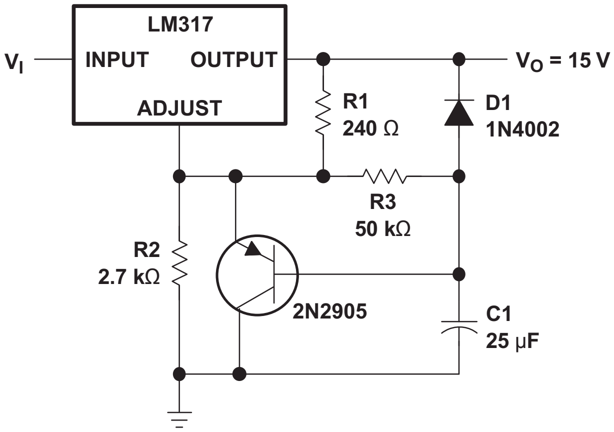


Figure 19. Slow Turn-On 15-V Regulator Circuit

8.3.9 AC Voltage-Regulator Circuit

These two LM317s can regulate both the positive and negative swings of a sinusoidal AC input.

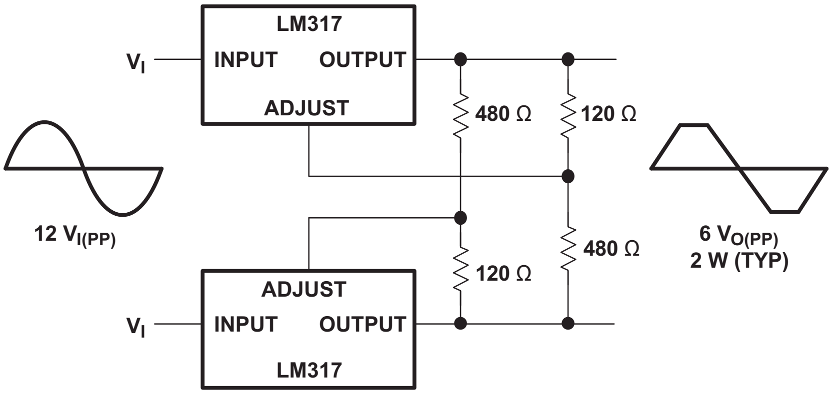


Figure 20. AC Voltage-Regulator Circuit

System Examples (continued)

8.3.10 Current-Limited 6-V Charger Circuit

As the charge current increases, the voltage at the bottom resistor increases until the NPN starts sinking current from the adjustment pin. The voltage at the adjustment pin drops, and consequently the output voltage decreases until the NPN stops conducting.

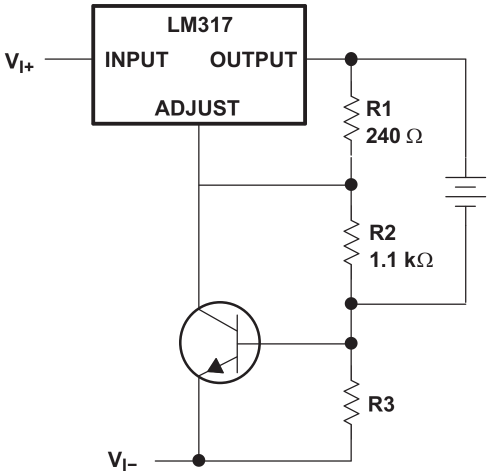


Figure 21. Current-Limited 6-V Charger Circuit

8.3.11 Adjustable 4-A Regulator Circuit

This application keeps the output current at 4 A while having the ability to adjust the output voltage using the adjustable (1.5 kΩ in schematic) resistor.

System Examples (continued)

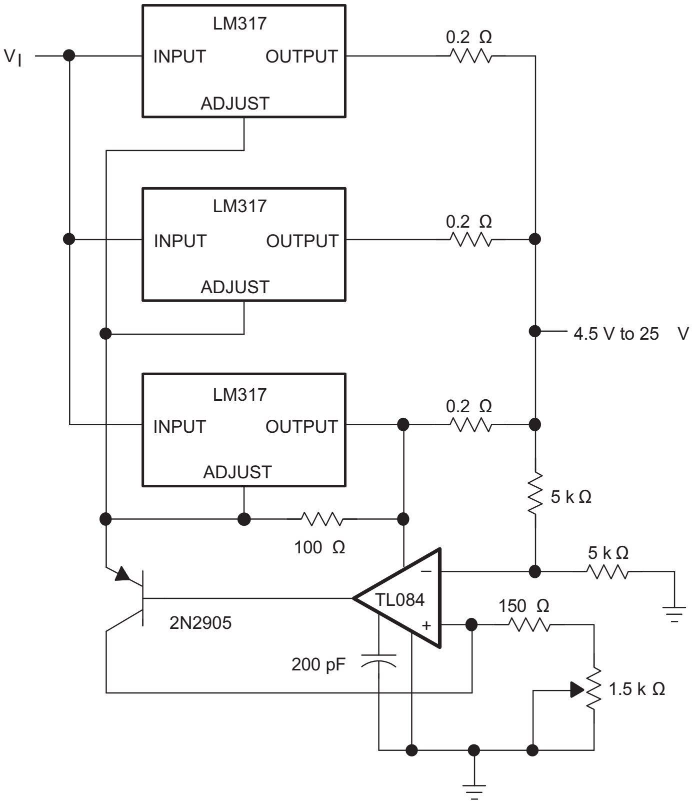


Figure 22. Adjustable 4-A Regulator Circuit

System Examples (continued)

8.3.12 High-Current Adjustable Regulator Circuit

The NPNs at the top of the schematic allow higher currents at V_{OUT} than the LM317 can provide, while still keeping the output voltage at levels determined by the adjustment pin resistor divider of the LM317.

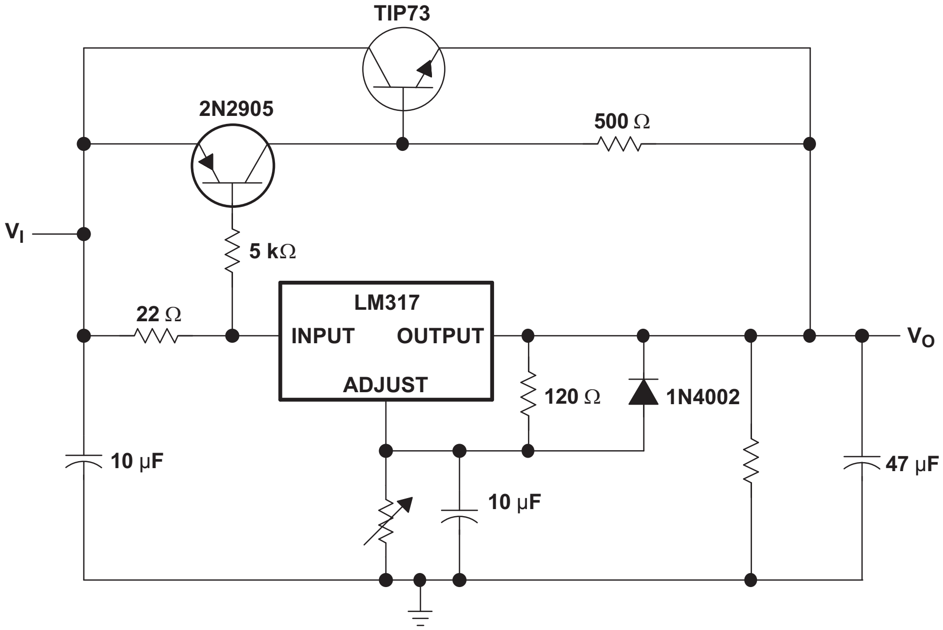


Figure 23. High-Current Adjustable Regulator Circuit

9 Power Supply Recommendations

The LM317 is designed to operate from an input voltage supply range between 1.25 V to 37 V greater than the output voltage. If the device is more than six inches from the input filter capacitors, an input bypass capacitor, 0.1 µF or greater, of any type is needed for stability.

10 Layout

10.1 Layout Guidelines

- TI recommends that the input terminal be bypassed to ground with a bypass capacitor.
- The optimum placement is closest to the input terminal of the device and the system GND. Take care to minimize the loop area formed by the bypass-capacitor connection, the input terminal, and the system GND.
- For operation at full rated load, TI recommends to use wide trace lengths to eliminate I × R drop and heat dissipation.

10.2 Layout Example

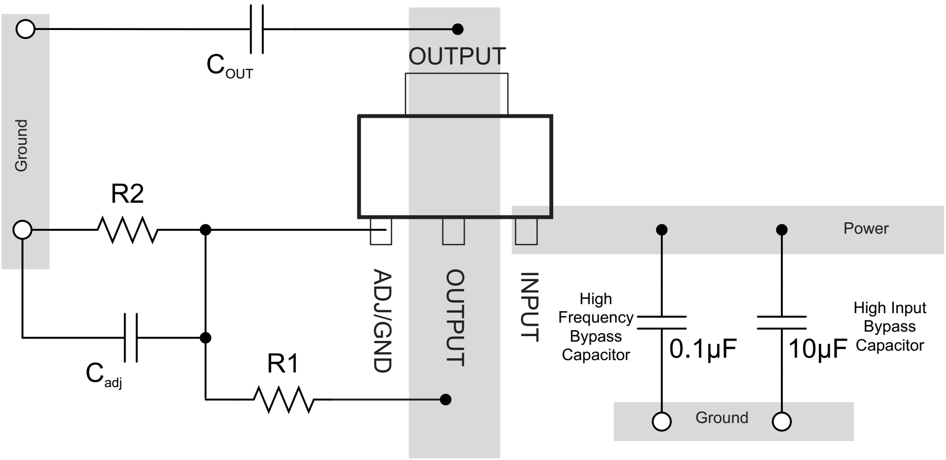


Figure 24. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM317DCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	L3	Samples
LM317DCYG3	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	L3	Samples
LM317DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	L3	Samples
LM317DCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 125	L3	Samples
LM317KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	LM317	Samples
LM317KCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	LM317	Samples
LM317KCT	ACTIVE	TO-220	KCT	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	LM317	Samples
LM317KTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	LM317	Samples
LM317KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	LM317	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

---

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

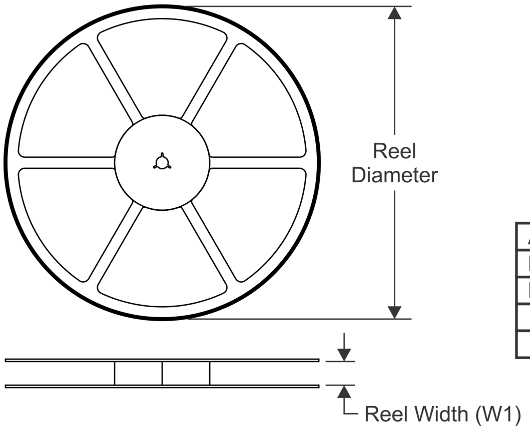
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

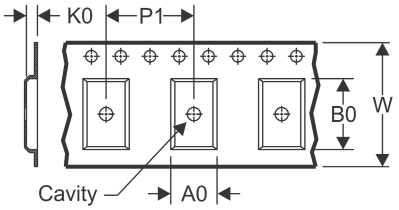
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

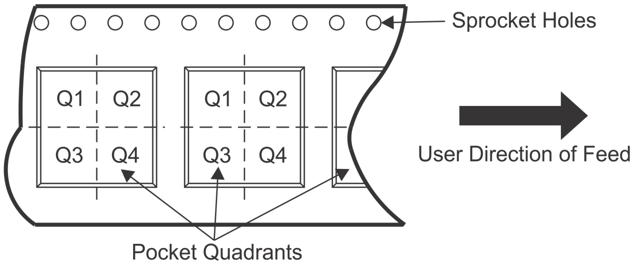


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

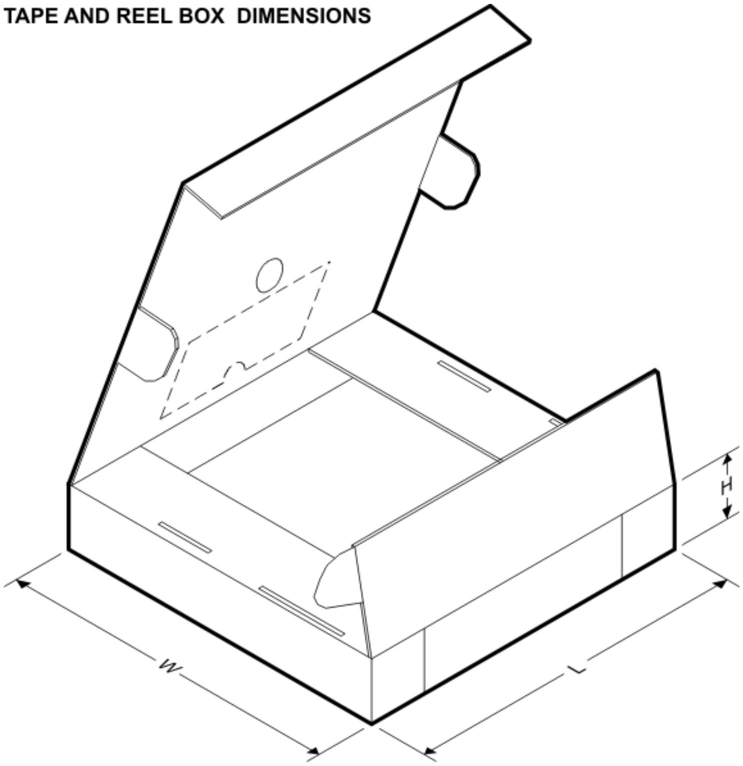
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM317DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.0	7.42	2.0	8.0	12.0	Q3
LM317DCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
LM317DCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
LM317KTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.1	4.9	16.0	24.0	Q2

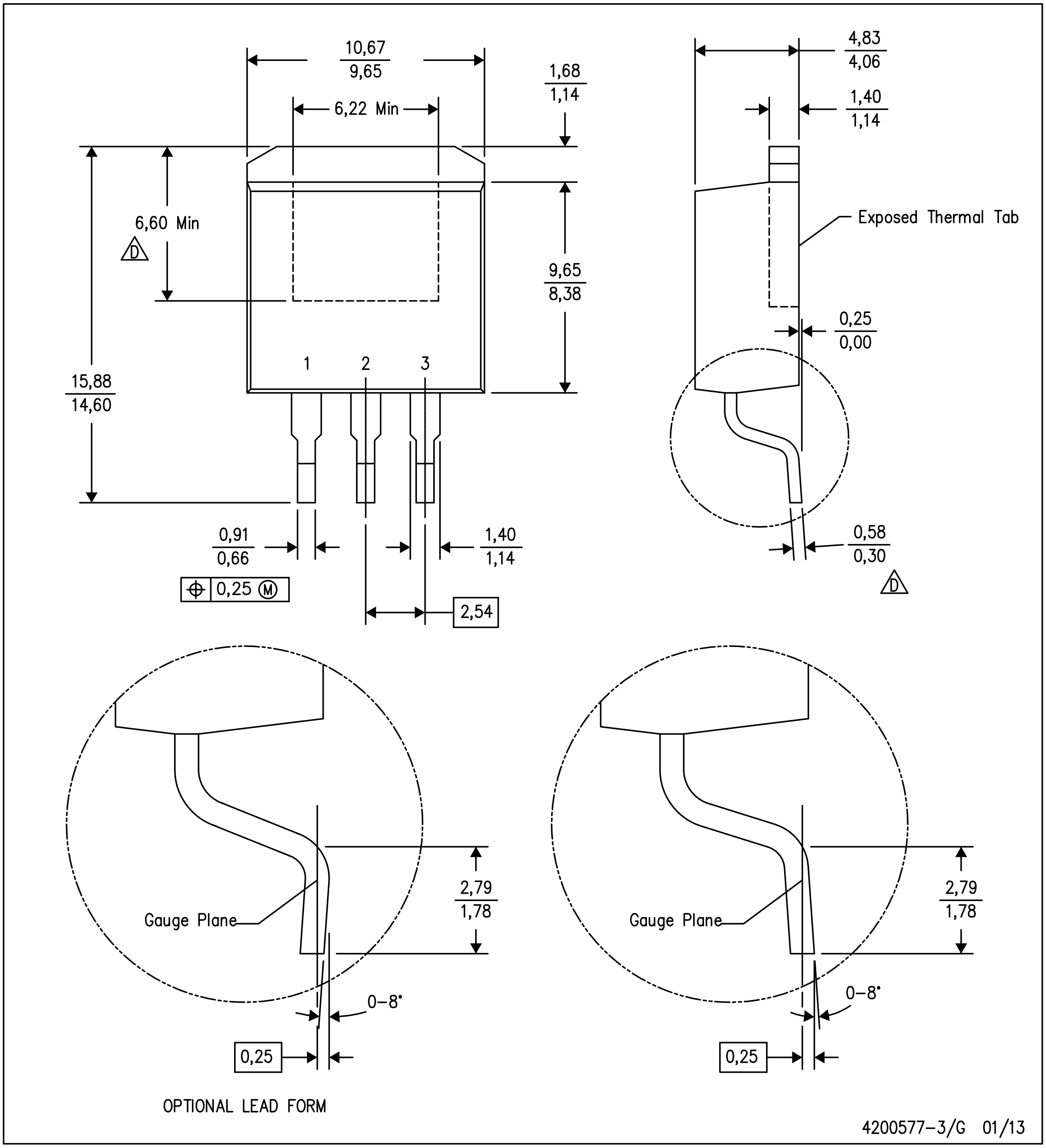
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

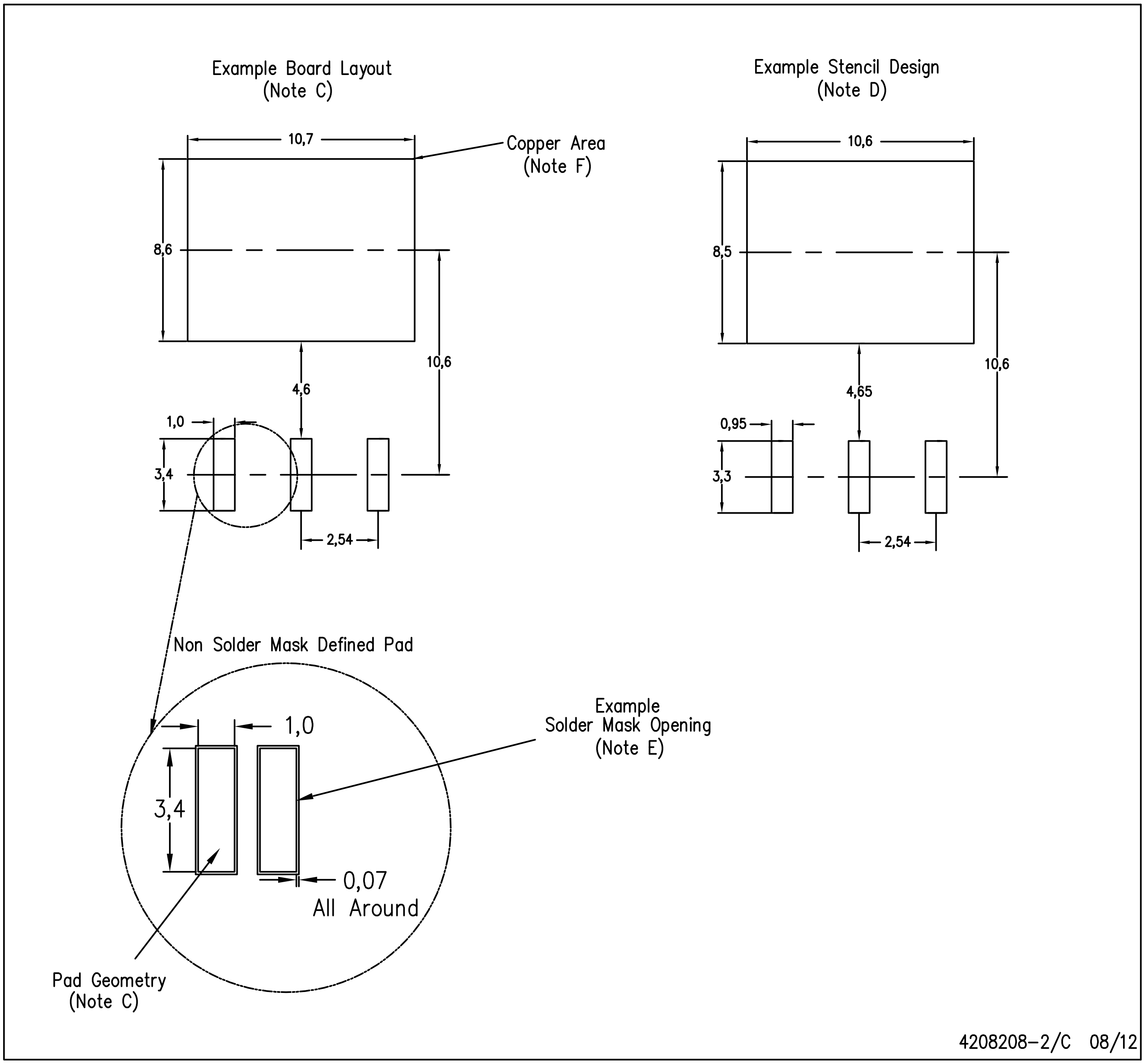
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM317DCYR	SOT-223	DCY	4	2500	350.0	334.0	47.0
LM317DCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
LM317DCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
LM317KTTR	DDPAK/TO-263	KTT	3	500	350.0	334.0	47.0

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- △D Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

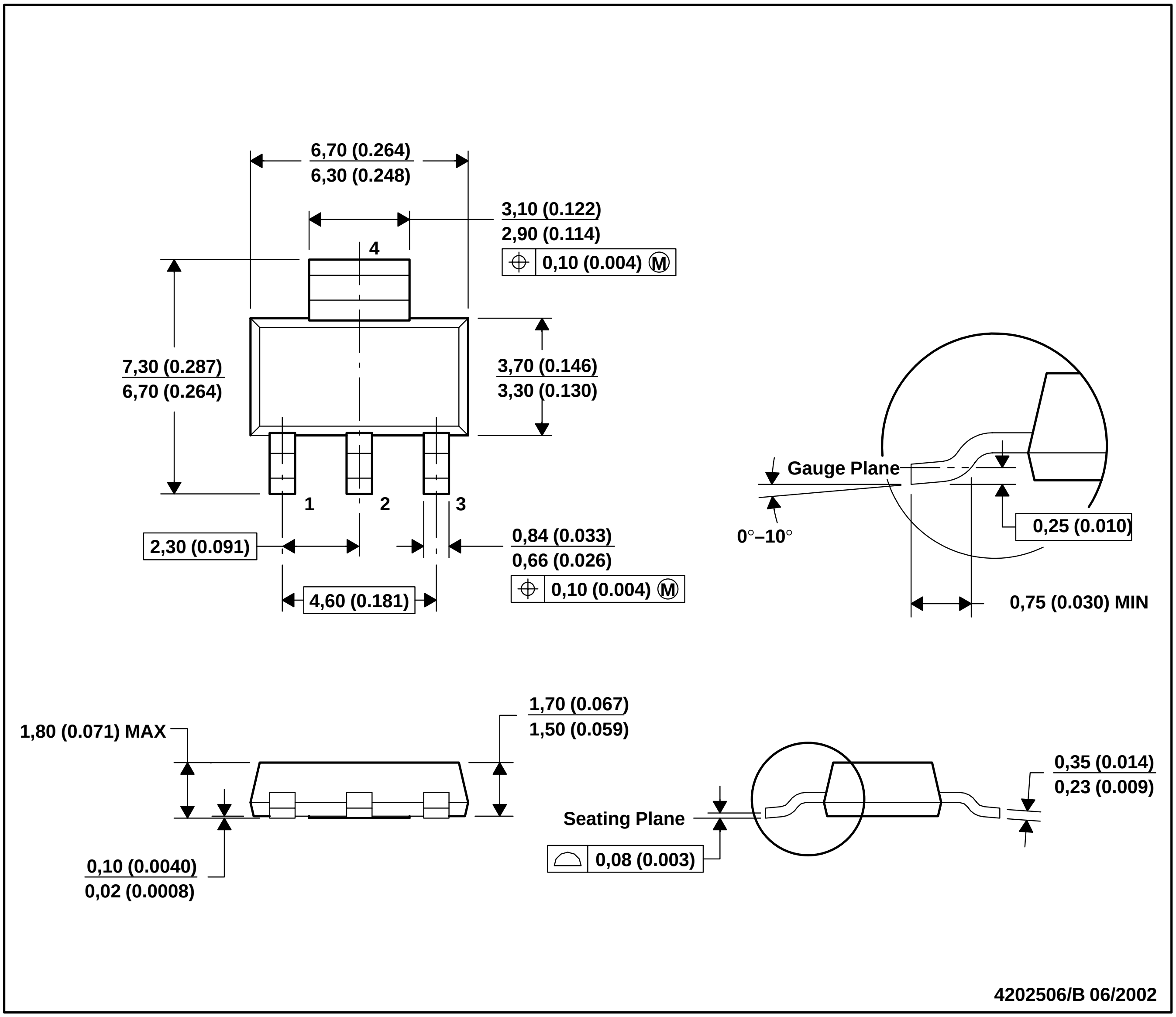
KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



4208208–2/C 08/12

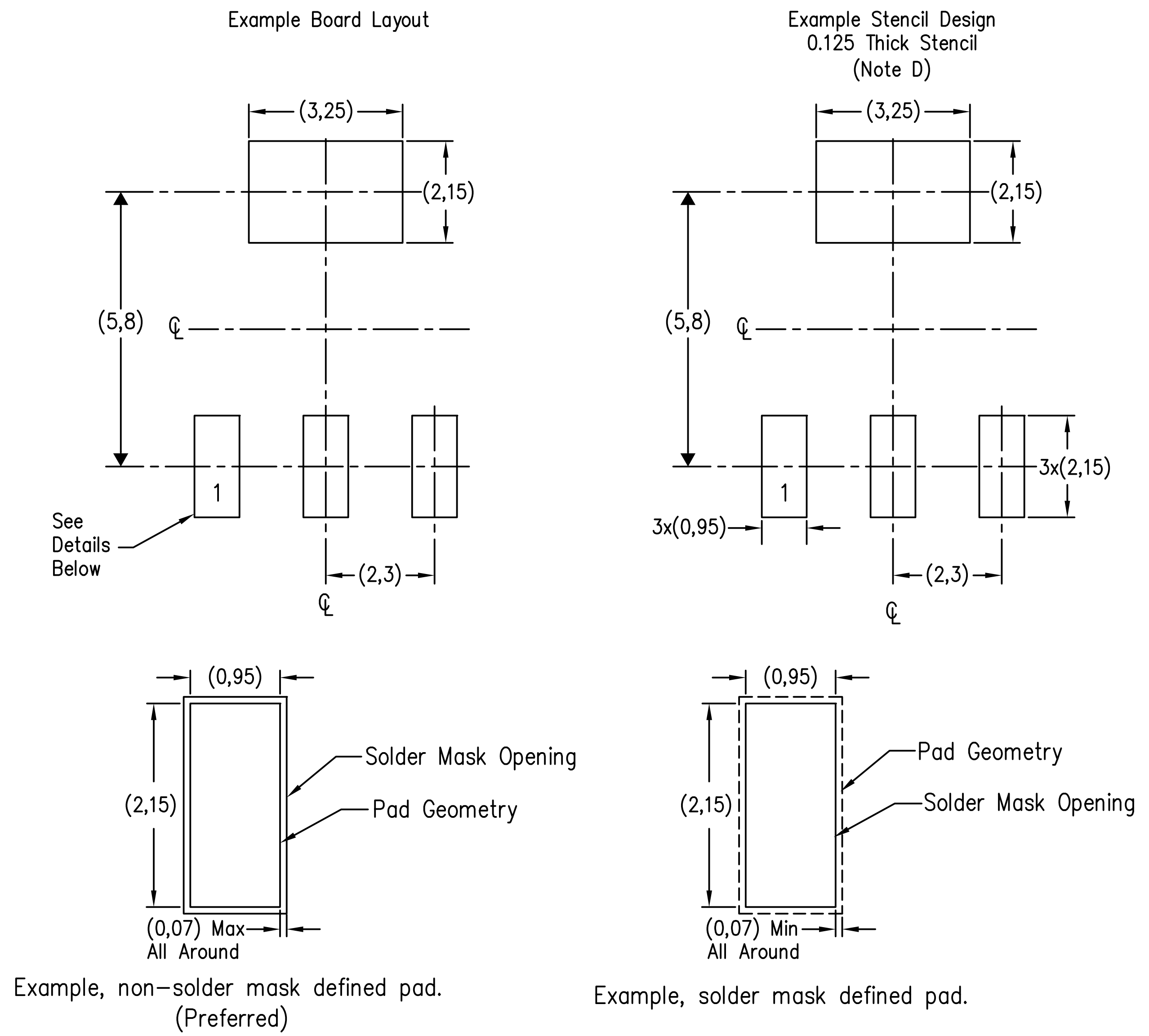
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–SM–782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES:
- A. All linear dimensions are in millimeters (inches).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



Example, non–solder mask defined pad.
(Preferred)

Example, solder mask defined pad.

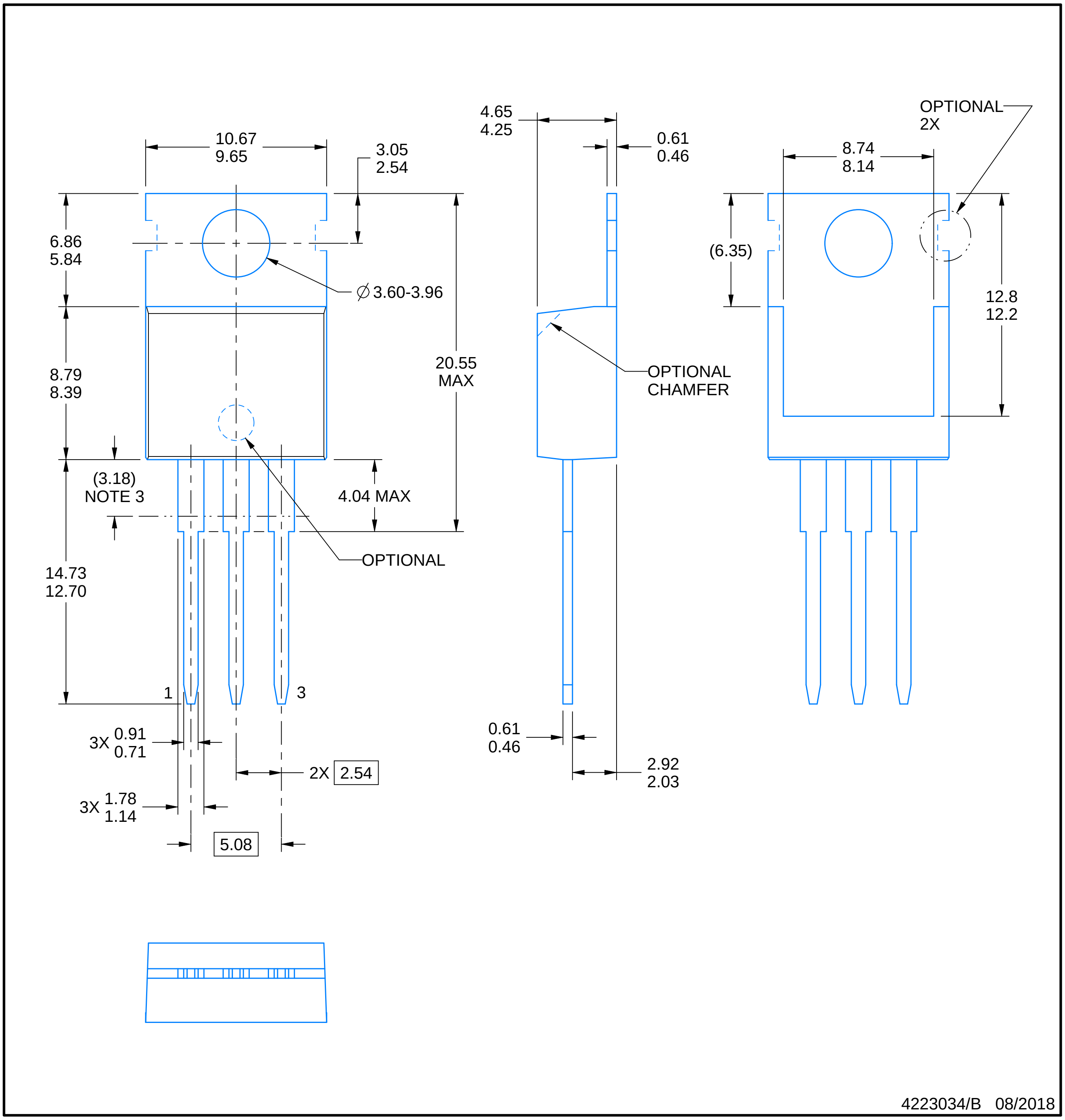
4210278/C 07/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

KCT0003A

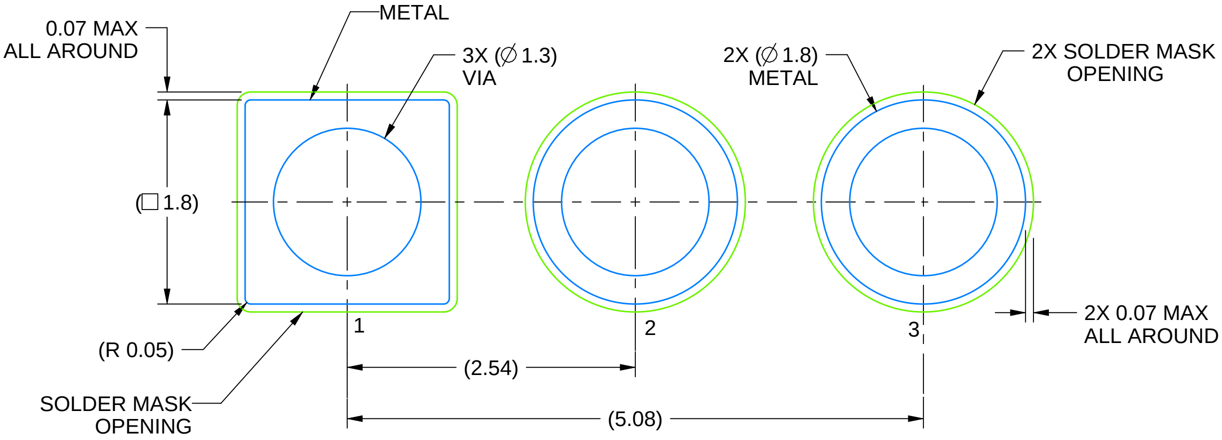
TO-220 - 20.55 mm max height

TO-220

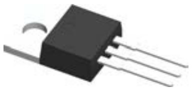


NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

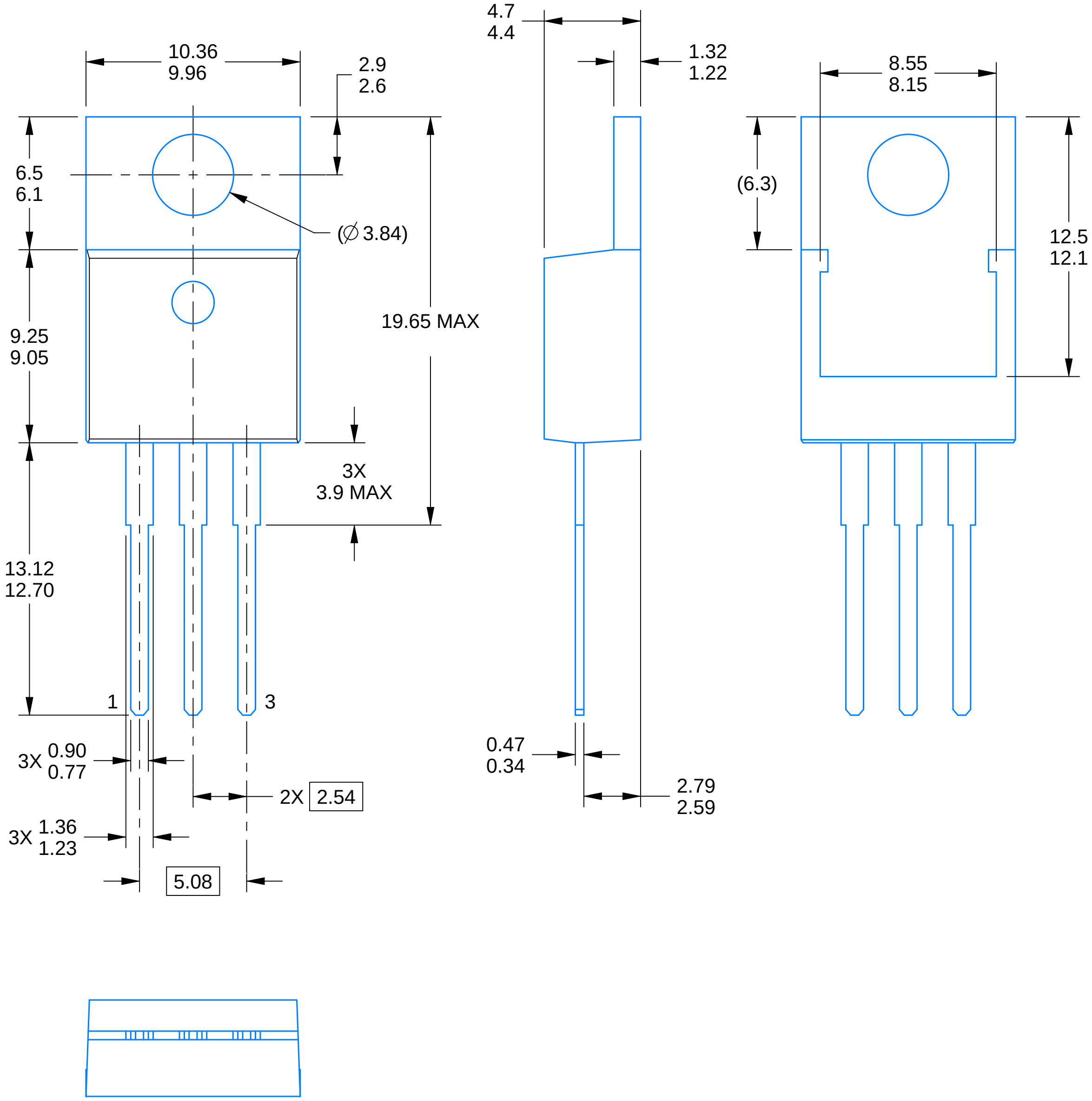


PACKAGE OUTLINE

KCS0003B

TO-220 - 19.65 mm max height

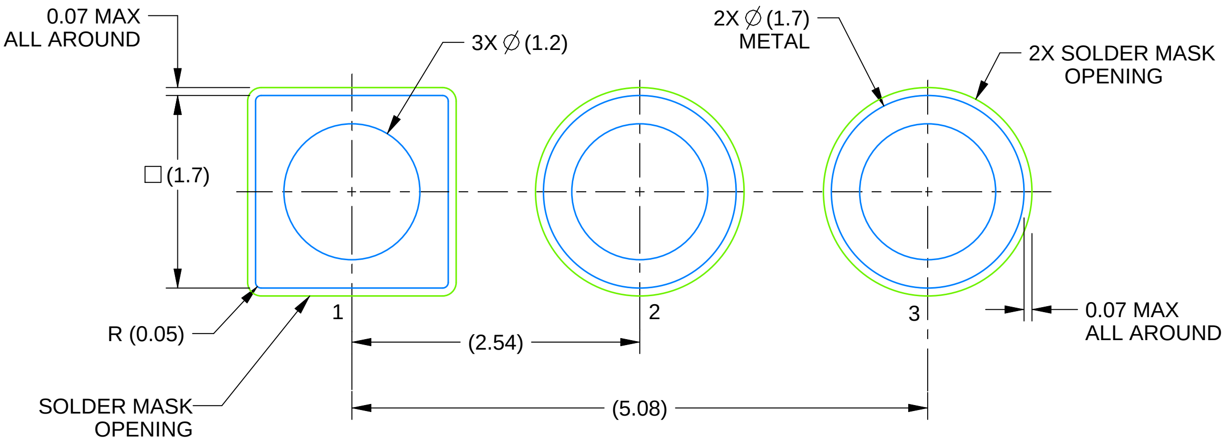
TO-220



4222214/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

IMPORTANT NOTICE AND DISCLAIMER

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

μA78xx Fixed Positive Voltage Regulators

1 Features

- 3-Terminal Regulators
- Available in fixed 5-V/8-V/10-V/12-V/15-V/24-V options
- Output Current up to 1.5 A
- Internal Thermal-Overload Protection
- High Power-Dissipation Capability
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Capacitor Not Needed for Stability

2 Applications

- On-card Regulation
- Portable Devices
- Computing & Servers
- Telecommunications

3 Description

This series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current-limiting and thermal-shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents, and also can be used as the power-pass element in precision regulators.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
μA78xx	TO-220 (3)	10.16 mm x 8.82 mm
	TO-220 (3)	10.16 mm x 8.82 mm
	TO-263 (3)	10.06 mm x 9.02 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

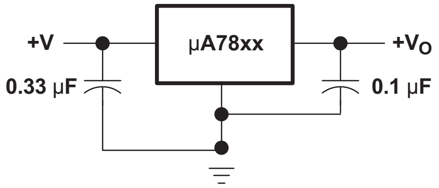


Table of Contents

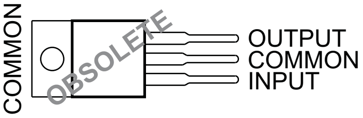
5 Revision History

Changes from Revision O (August 2012) to Revision P **Page**

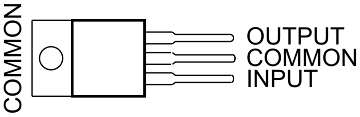
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Deleted *Ordering Information* table. 1

6 Pin Configuration and Functions

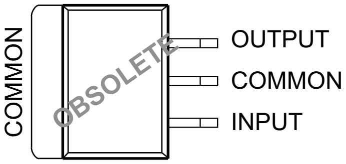
KC (TO-220) PACKAGE
(TOP VIEW)



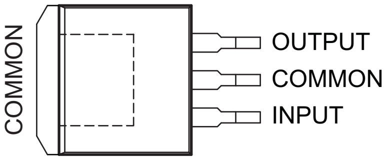
KCS OR KCT (TO-220) PACKAGE
(TOP VIEW)



KTE (PowerFLEX™) PACKAGE
(TOP VIEW)



KTT (TO-263) PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
COMMON	2	—	Ground
INPUT	1	I	Supply Input
OUTPUT	3	O	Voltage Output

7 Specifications

7.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage	μA7824C		40	V
		All others		35	
T_J	Operating virtual junction temperature			150	°C
	Lead temperature	1,6 mm (1/16 in) from case for 10 s		260	°C
T_{stg}	Storage temperature range		–65	150	°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_I	Input voltage	μA7805	7	25	V
		μA7808	10.5	25	
		μA7810	12.5	28	
		μA7812	14.5	30	
		μA7815	17.5	30	
		μA7824	27	38	
I_O	Output current			1.5	A
T_J	Operating virtual junction temperature		0	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		μA78XX			UNIT
		KTE	KCS, KCT, KC	KTT	
		3 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23	19	25.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	3	17	18	
$R_{\theta JP(top)}$	Junction-to-exposed-pad thermal resistance	2.7	3	1.94	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics — uA7805

at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	µA7805C			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, V_I = 7 V to 20 V, $P_D \leq$ 15 W	25°C	4.8	5	5.2	V
		0°C to 125°C	4.75		5.25	
Input voltage regulation	V_I = 7 V to 25 V	25°C		3	100	mV
	V_I = 8 V to 12 V			1	50	
Ripple rejection(2)	V_I = 8 V to 12 V, f = 120 Hz	0°C to 125°C	62	78		dB
	V_I = 8 V to 12 V, f = 120 Hz (KCT)			68		
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Output resistance	f = 1 kHz	0°C to 125°C		0.017		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.2	8	mA
Bias current change	V_I = 7 V to 25 V	0°C to 125°C			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		750		mA
Peak output current		25°C		2.2		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

(2) This parameter is validated by design and verified during product characterization. It is not tested in production.

7.6 Electrical Characteristics — uA7808

at specified virtual junction temperature, V_I = 14 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	µA7808C			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, V_I = 10.5 V to 23 V, P_D ≤ 15 W	25°C	7.7	8	8.3	V
		0°C to 125°C	7.6		8.4	
Input voltage regulation	V_I = 10.5 V to 25 V	25°C		6	160	mV
	V_I = 11 V to 17 V			2	80	
Ripple rejection(2)	V_I = 11.5 V to 21.5 V, f = 120 Hz	0°C to 125°C	55	72		dB
	V_I = 11.5 V to 21.5 V, f = 120 Hz (KCT)			62		
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	160	mV
	I_O = 250 mA to 750 mA			4	80	
Output resistance	f = 1 kHz	0°C to 125°C		0.016		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		52		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 10.5 V to 25 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		450		mA
Peak output current		25°C		2.2		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.
(2) This parameter is validated by design and verified during product characterization. It is not tested in production.

7.7 Electrical Characteristics — uA7810

at specified virtual junction temperature, V_I = 17 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	µA7810C			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, V_I = 12.5 V to 25 V, P_D ≤ 15 W	25°C	9.6	10	10.4	V
		0°C to 125°C	9.5		10.5	
Input voltage regulation	V_I = 12.5 V to 28 V	25°C		7	200	mV
	V_I = 14 V to 20 V			2	100	
Ripple rejection(2)	V_I = 13 V to 23 V, f = 120 Hz	0°C to 125°C	55	71		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	200	mV
	I_O = 250 mA to 750 mA			4	100	
Output resistance	f = 1 kHz	0°C to 125°C		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		70		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 12.5 V to 28 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		400		mA
Peak output current		25°C		2.2		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

(2) This parameter is validated by design and verified during product characterization. It is not tested in production.

7.8 Electrical Characteristics — uA7812

at specified virtual junction temperature, V_I = 19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	µA7812C			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, V_I = 14.5 V to 27 V, P_D ≤ 15 W	25°C	11.5	12	12.5	V
		0°C to 125°C	11.4		12.6	
Input voltage regulation	V_I = 14.5 V to 30 V	25°C		10	240	mV
	V_I = 16 V to 22 V			3	120	
Ripple rejection[2]	V_I = 15 V to 25 V, f = 120 Hz	0°C to 125°C	55	71		dB
	V_I = 15 V to 25 V, f = 120 Hz (KCT)			61		
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	240	mV
	I_O = 250 mA to 750 mA			4	120	
Output resistance	f = 1 kHz	0°C to 125°C		0.018		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		75		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.3	8	mA
Bias current change	V_I = 14.5 V to 30 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		350		mA
Peak output current		25°C		2.2		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.
(2) This parameter is validated by design and verified during product characterization. It is not tested in production.

7.9 Electrical Characteristics — uA7815

at specified virtual junction temperature, V_I = 23 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	µA7815C			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, V_I = 17.5 V to 30 V, P_D ≤ 15 W	25°C	14.4	15	15.6	V
		0°C to 125°C	14.25		15.75	
Input voltage regulation	V_I = 17.5 V to 30 V	25°C		11	300	mV
	V_I = 20 V to 26 V			3	150	
Ripple rejection(2)	V_I = 18.5 V to 28.5 V, f = 120 Hz	0°C to 125°C	54	70		dB
	V_I = 18.5 V to 28.5 V, f = 120 Hz (KCT)			60		
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	300	mV
	I_O = 250 mA to 750 mA			4	150	
Output resistance	f = 1 kHz	0°C to 125°C		0.019		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		90		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.4	8	mA
Bias current change	V_I = 17.5 V to 30 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		230		mA
Peak output current		25°C		2.1		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

(2) This parameter is validated by design and verified during product characterization. It is not tested in production.

7.10 Electrical Characteristics — uA7824

at specified virtual junction temperature, V_I = 33 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	µA7824C			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, V_I = 27 V to 38 V, P_D ≤ 15 W	25°C	23	24	25	V
		0°C to 125°C	22.8		25.2	
Input voltage regulation	V_I = 27 V to 38 V	25°C		18	480	mV
	V_I = 30 V to 36 V			6	240	
Ripple rejection (2)	V_I = 28 V to 38 V, f = 120 Hz	0°C to 125°C	50	66		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		12	480	mV
	I_O = 250 mA to 750 mA			4	240	
Output resistance	f = 1 kHz	0°C to 125°C		0.028		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–1.5		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		170		µV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.6	8	mA
Bias current change	V_I = 27 V to 38 V	0°C to 125°C			1	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		150		mA
Peak output current		25°C		2.1		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-µF capacitor across the input and a 0.1-µF capacitor across the output.

(2) This parameter is validated by design and verified during product characterization. It is not tested in production.

7.11 Typical Characteristics

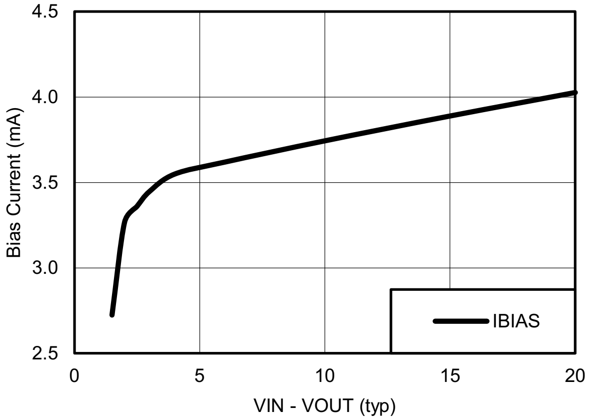


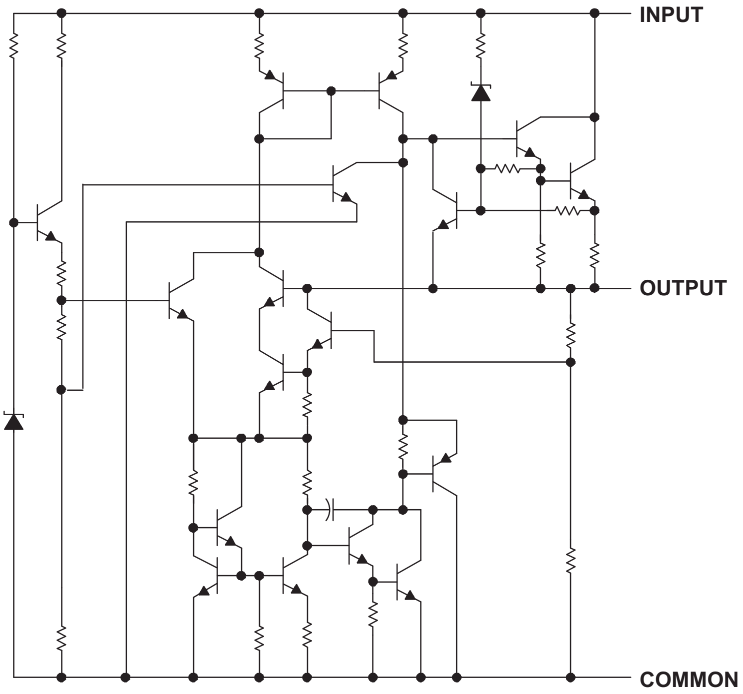
Figure 1. µA7805 Bias Current vs Voltage Differential at 25°C

8 Detailed Description

8.1 Overview

This series of fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current-limiting and thermal-shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents, and also can be used as the power-pass element in precision regulators.

8.2 Functional Schematic



8.3 Feature Description

8.3.1 Thermal Overload

When the die temperature increases to unwanted levels, the device will reduce the output current to lower its temperature. Under heavy loads, the device may alternate between on and off output states to regulate temperature.

8.3.2 Short-Circuit Current Limiting

In the event of a short circuit, the device will limit its own current to safe levels by lowering the bias voltage of internal pass transistors. If the device becomes overheated, the thermal overload protection will take over.

8.4 Device Functional Modes

8.4.1 Fixed-Output Mode

These devices are available in fixed-output voltages. See the orderable part list for the desired output.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following section shows application details of the µA78xx as a linear regulator.

9.2 Typical Application

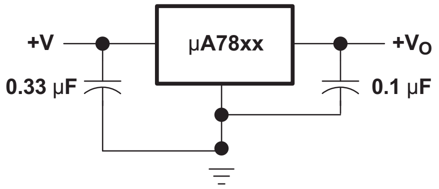


Figure 2. Fixed-Output Regulator

9.2.1 Design Requirements

- Input supply capacitor recommended for filtering noise on the input
- Output supply decoupling capacitor for stabilizing the output

9.2.2 Detailed Design Procedure

9.2.2.1 Operation With a Load Common to a Voltage of Opposite Polarity

In many cases, a regulator powers a load that is not connected to ground but, instead, is connected to a voltage source of opposite polarity (e.g., operational amplifiers, level-shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 3. This protects the regulator from output polarity reversals during startup and short-circuit operation.

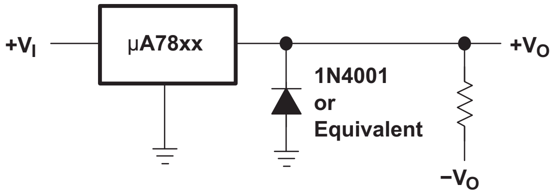


Figure 3. Output Polarity-Reversal-Protection Circuit

9.2.2.2 Reverse-Bias Protection

Occasionally, the input voltage to the regulator can collapse faster than the output voltage. This can occur, for example, when the input supply is crowbarred during an output overvoltage condition. If the output voltage is greater than approximately 7 V, the emitter-base junction of the series-pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be used as shown in Figure 4.

Typical Application (continued)

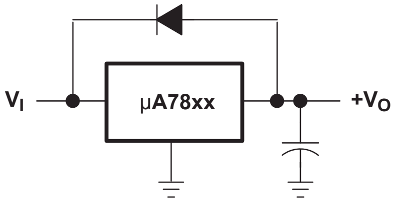


Figure 4. Reverse-Bias-Protection Circuit

9.2.3 Application Curves

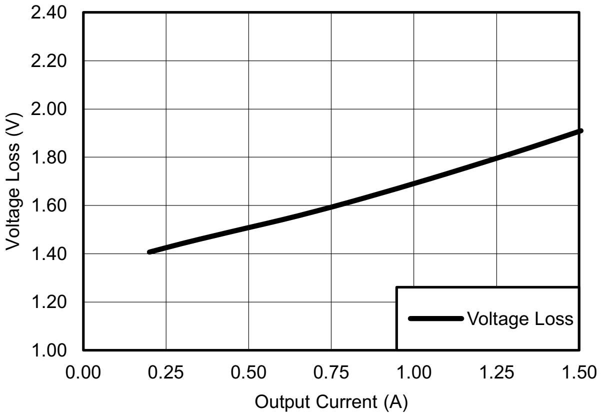


Figure 5. µA7805 Voltage Loss vs Output Current at 25°C

9.2.4 General Configurations

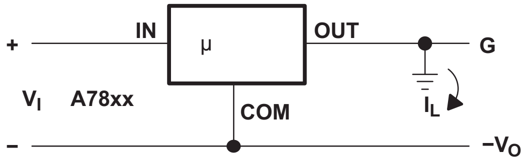
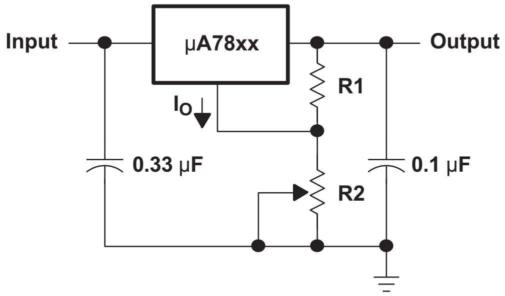


Figure 6. Positive Regulator in Negative Configuration (V_I Must Float)

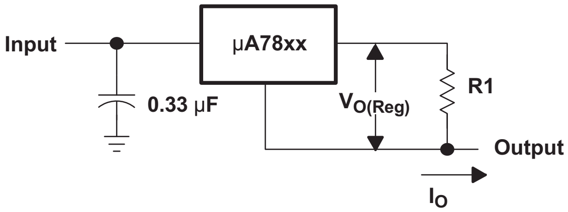


A: The following formula is used when V_{xx} is the nominal output voltage (output to common) of the fixed regulators

$$V_O = V_{xx} + \left(\frac{V_{xx}}{R1} + I_Q\right)R2$$

Figure 7. Adjustable-Output Regulator

Typical Application (continued)



$I_O = (V_O/R1) + I_O$ Bias Current

Figure 8. Current Regulator

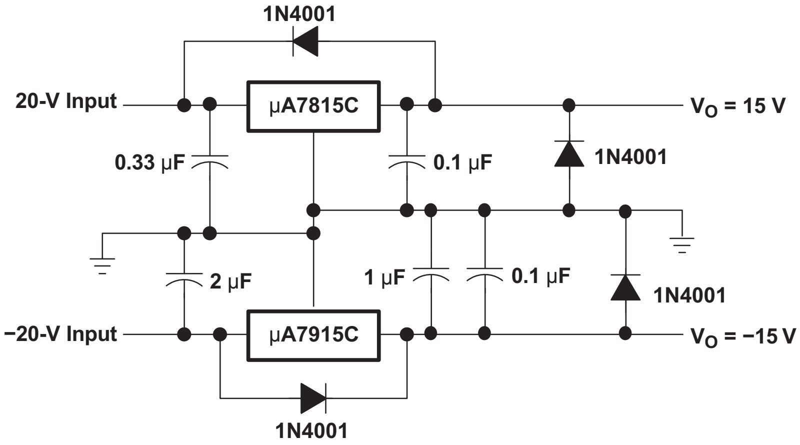


Figure 9. Regulated Dual Supply

10 Power Supply Recommendations

See *Recommended Operating Conditions* for the recommended power supply voltages for each variation of the µA78xx device. Different orderable part numbers will be able to tolerate different levels of voltage. It is also recommended to have a decoupling capacitor on the output of the µA78xx device's power supply to limit noise on the device input.

11 Layout

11.1 Layout Guidelines

Keep trace widths large enough to eliminate problematic I×R voltage drops at the input and output terminals. Input decoupling capacitors should be placed as close to the µA78XX as possible.

11.2 Layout Example

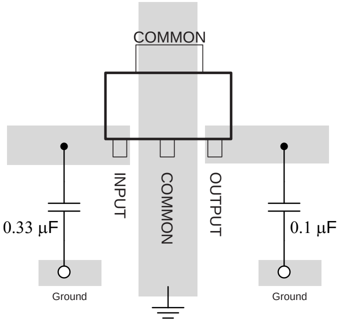


Figure 10. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
µA7805	Click here	Click here	Click here	Click here	Click here
uA7808	Click here	Click here	Click here	Click here	Click here
uA7810	Click here	Click here	Click here	Click here	Click here
uA7812	Click here	Click here	Click here	Click here	Click here
uA7815	Click here	Click here	Click here	Click here	Click here
uA7924	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA7805CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7805C	Samples
UA7805CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7805C	Samples
UA7805CKCT	ACTIVE	TO-220	KCT	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7805C	Samples
UA7805CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7805C	Samples
UA7805CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7805C	Samples
UA7808CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7808C	Samples
UA7808CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7808C	Samples
UA7808CKCT	ACTIVE	TO-220	KCT	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7808C	Samples
UA7808CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7808C	Samples
UA7810CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7810C	Samples
UA7810CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7810C	Samples
UA7810CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7810C	Samples
UA7810CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7810C	Samples
UA7812CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7812C	Samples
UA7812CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7812C	Samples
UA7812CKCT	ACTIVE	TO-220	KCT	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7812C	Samples
UA7812CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7812C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA7812CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7812C	Samples
UA7815CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7815C	Samples
UA7815CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7815C	Samples
UA7815CKCT	ACTIVE	TO-220	KCT	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7815C	Samples
UA7815CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7815C	Samples
UA7824CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7824C	Samples
UA7824CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7824C	Samples
UA7824CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7824C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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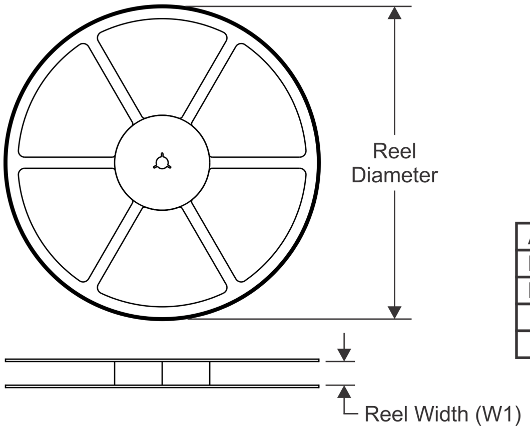
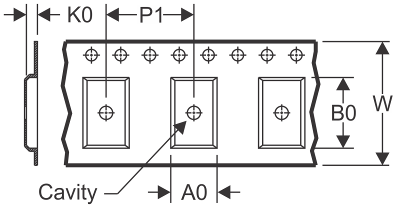
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

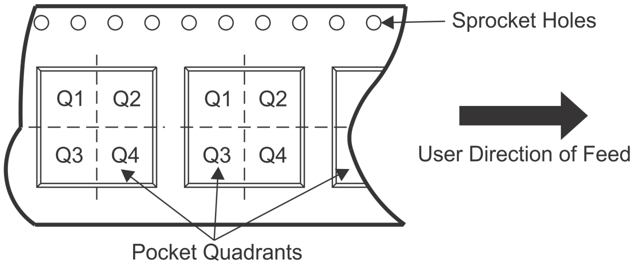


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

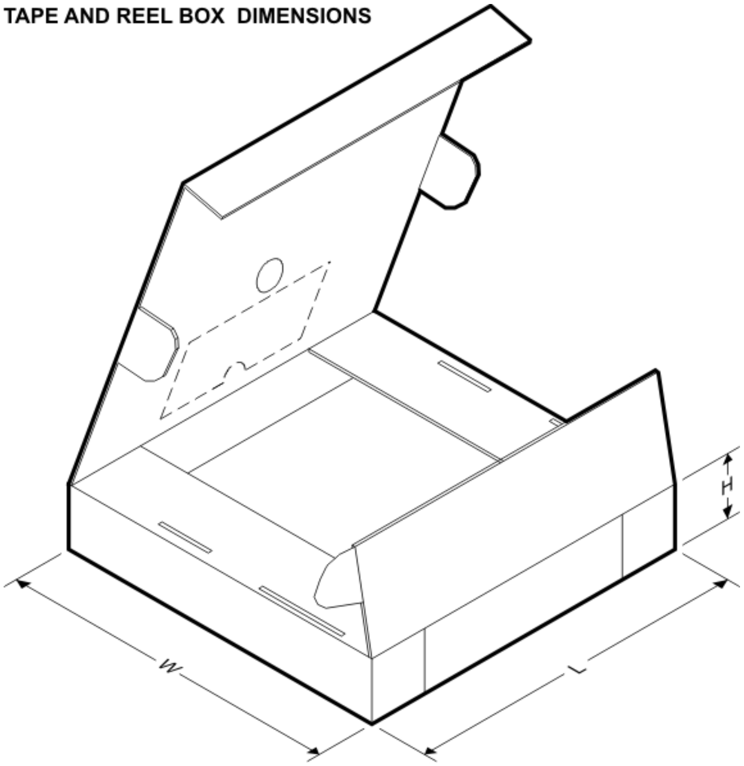
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA7805CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
UA7805CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.1	4.9	16.0	24.0	Q2
UA7808CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
UA7810CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
UA7812CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
UA7812CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.1	4.9	16.0	24.0	Q2
UA7815CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
UA7824CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

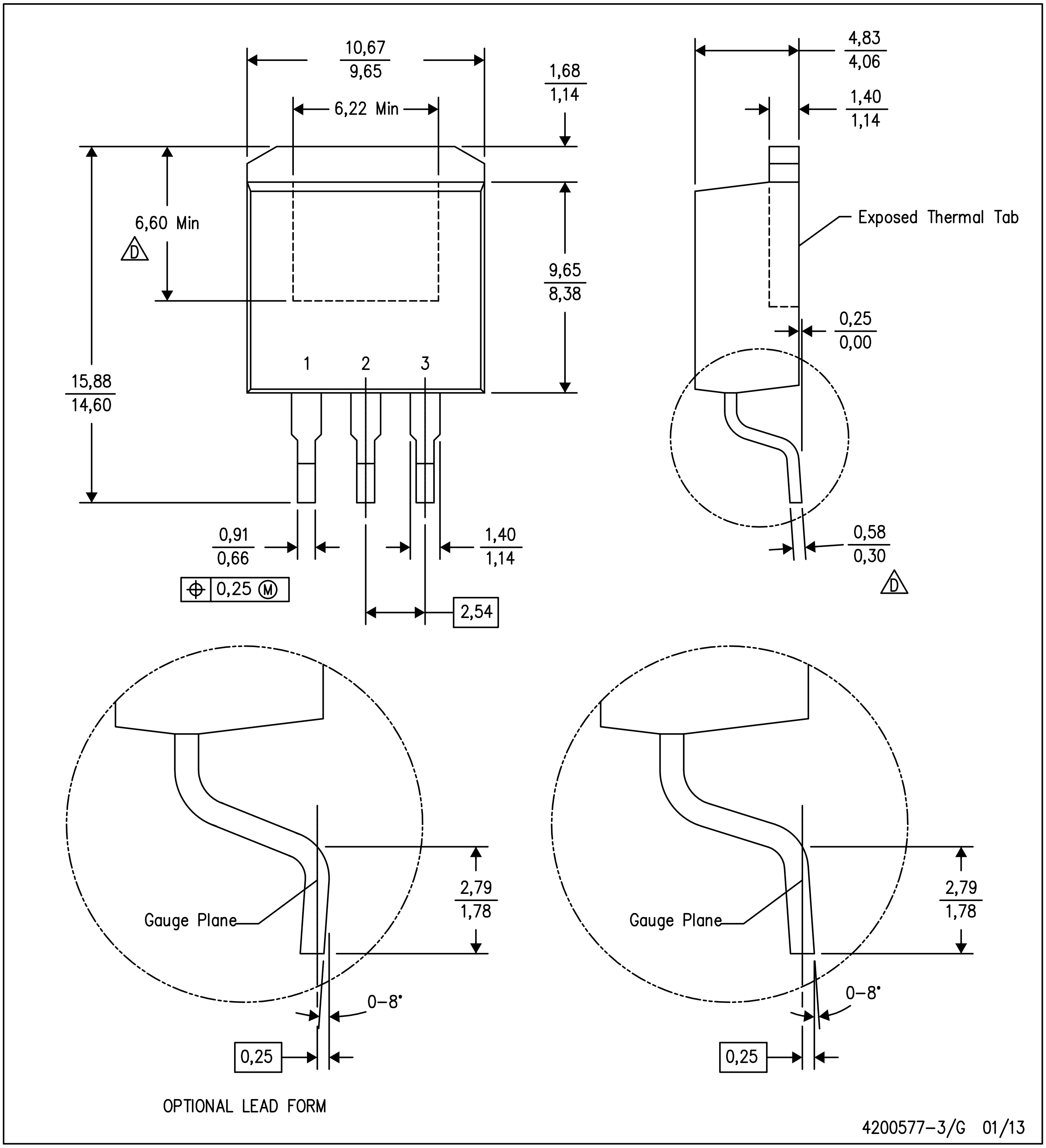
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

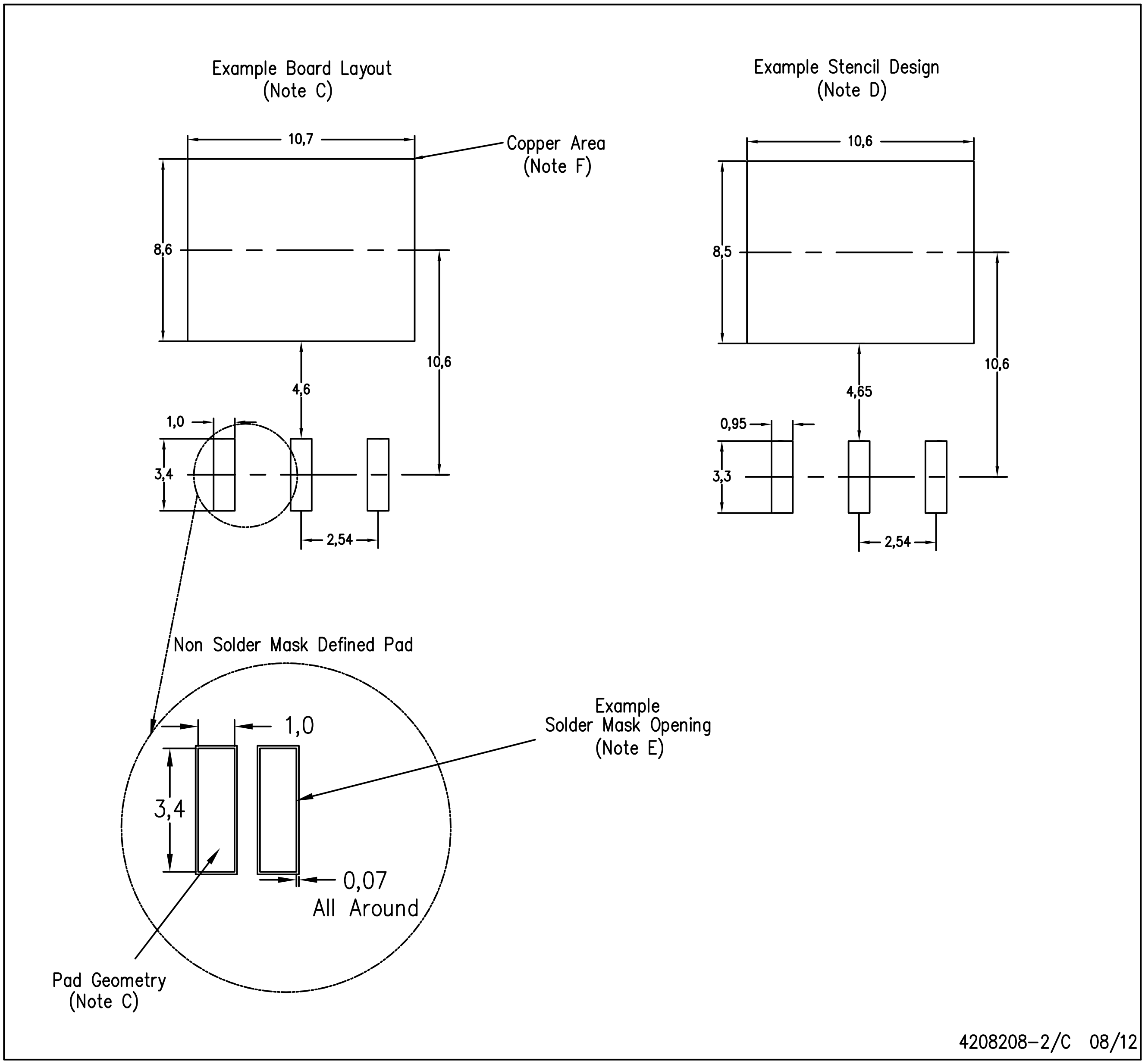
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA7805CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
UA7805CKTTR	DDPAK/TO-263	KTT	3	500	350.0	334.0	47.0
UA7808CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
UA7810CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
UA7812CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
UA7812CKTTR	DDPAK/TO-263	KTT	3	500	350.0	334.0	47.0
UA7815CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
UA7824CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- D Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



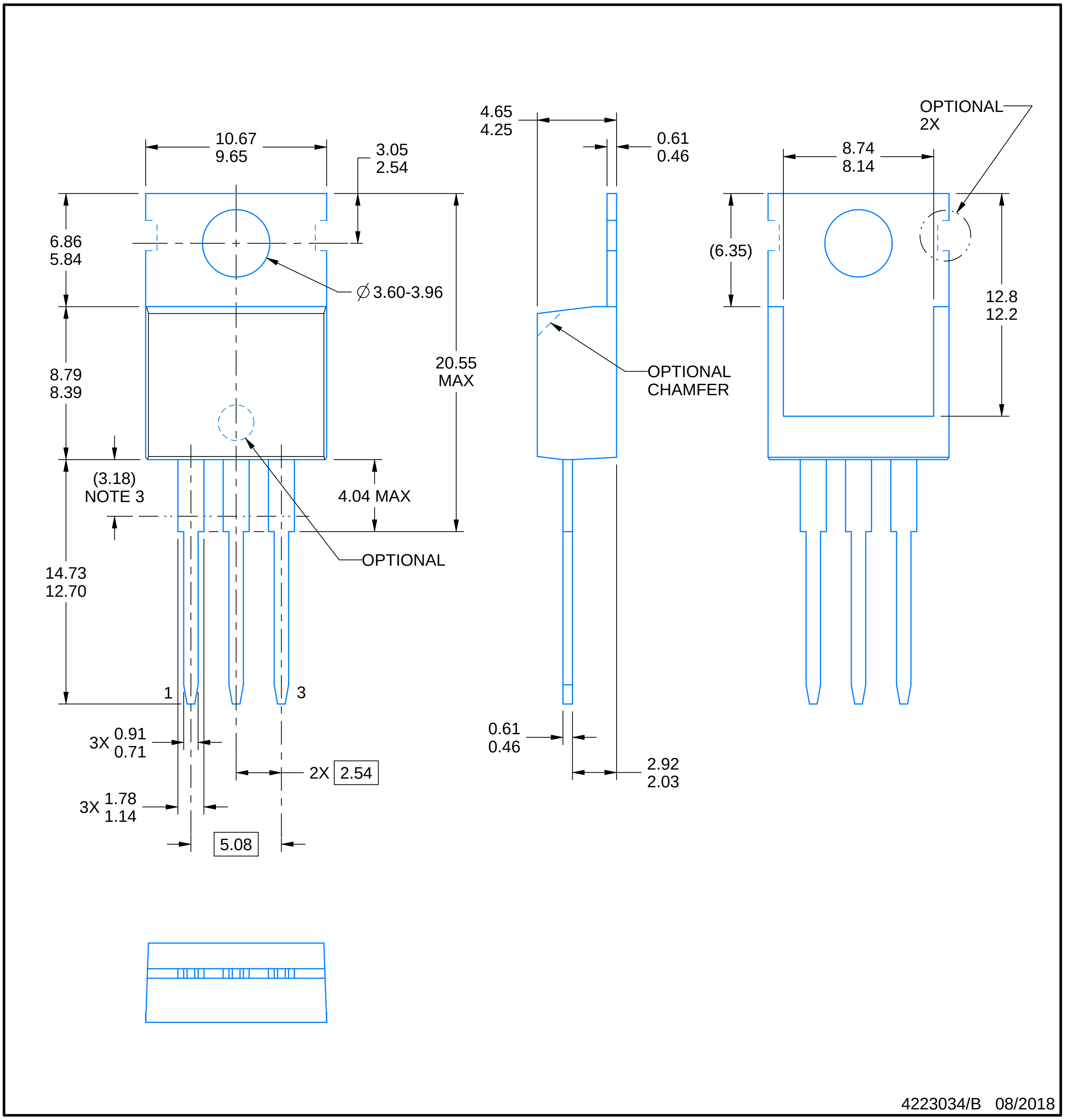
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–SM–782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

PACKAGE OUTLINE

KCT0003A

TO-220 - 20.55 mm max height

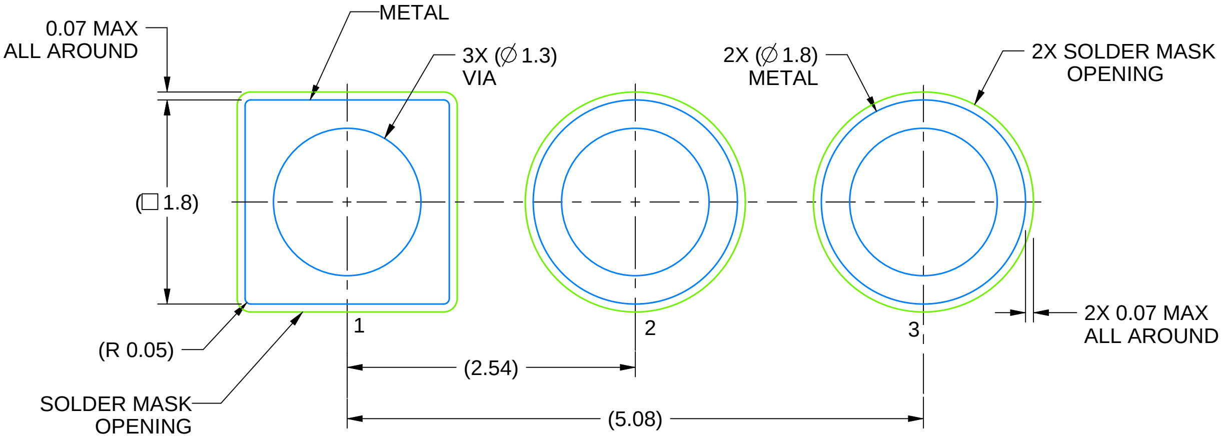
TO-220



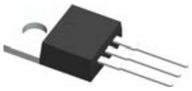
4223034/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

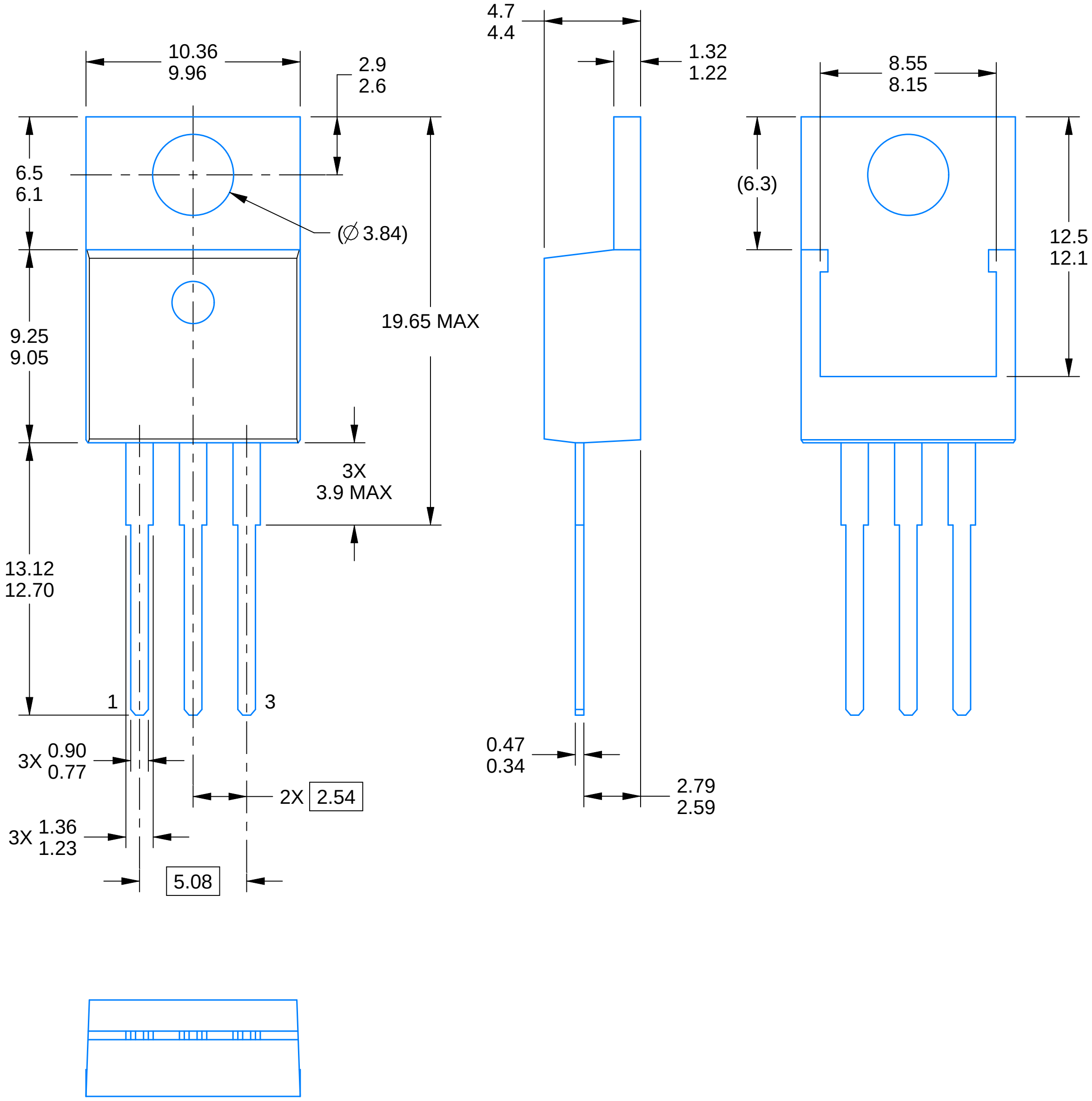


PACKAGE OUTLINE

KCS0003B

TO-220 - 19.65 mm max height

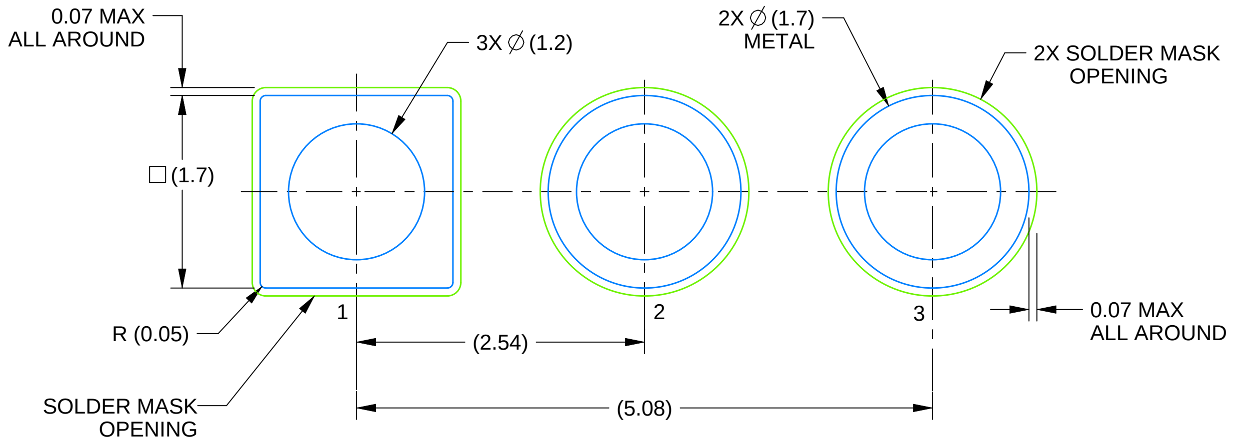
TO-220



4222214/B 08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

IMPORTANT NOTICE AND DISCLAIMER

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

LP295x Adjustable Micropower Voltage Regulators with Shutdown

1 Features

- Wide Input Range: Up to 30 V
- Rated Output Current of 100 mA
- Low Dropout: 380 mV (Typ) at 100 mA
- Low Quiescent Current: 75 µA (Typ)
- Tight Line Regulation: 0.03% (Typ)
- Tight Load Regulation: 0.04% (Typ)
- High V_O Accuracy
  - 1.4% at 25°C
  - 2% Over Temperature
- Can Be Used as a Regulator or Reference
- Stable With Low ESR (>12 mΩ) Capacitors
- Current- and Thermal-Limiting Features
- LP2950 Only (3-Pin Package)
  - Fixed-Output Voltages of 5 V, 3.3 V, and 3 V
- LP2951 Only (8-Pin Package)
  - Fixed- or Adjustable-Output Voltages: 5 V/ADJ, 3.3 V/ADJ, and 3 V/ADJ
  - Low-Voltage Error Signal on Falling Output
  - Shutdown Capability
  - Remote Sense Capability for Optimal Output Regulation and Accuracy

2 Applications

- Applications with High-Voltage Input
- Power Supplies

3 Description

The LP2950 and LP2951 devices are bipolar, low-dropout voltage regulators that can accommodate a wide input supply-voltage range of up to 30 V. The easy-to-use, 3-pin LP2950 is available in fixed-output voltages of 5 V, 3.3 V, and 3 V. However, the 8-pin LP2951 is able to output either a fixed or adjustable output from the same device. By tying the OUTPUT and SENSE pins together, and the FEEDBACK and V_{TAP} pins together, the LP2951 outputs a fixed 5 V, 3.3 V, or 3 V (depending on the version). Alternatively, by leaving the SENSE and V_{TAP} pins open and connecting FEEDBACK to an external resistor divider, the output can be set to any value between 1.235 V to 30 V.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP2950	TO-92 (3)	4.83 mm x 4.83 mm
LP2951	SOIC (8)	4.90 mm x 3.90 mm
	SON (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Dropout Voltage vs Temperature

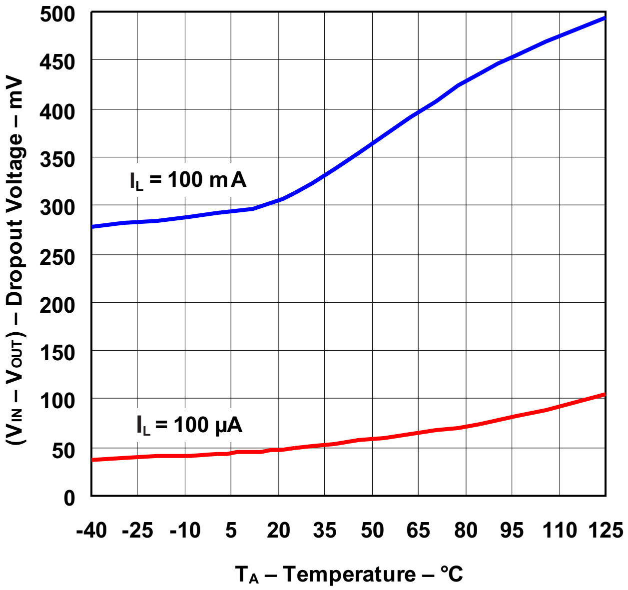


Table of Contents

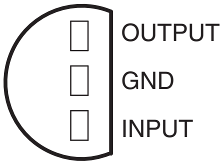
4 Revision History

Changes from Revision H (March 2012) to Revision I **Page**

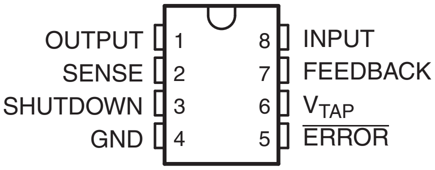
- Added *Applications*, *Device Information* table, *Handling Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Removed *Ordering Information* table. 1

5 Pin Configuration and Functions

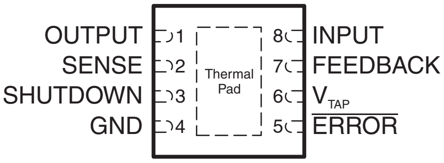
LP2950
LP PACKAGE
(BOTTOM VIEW)



LP2951
D OR P PACKAGE
(TOP VIEW)



LP2951
DRG PACKAGE
(TOP VIEW)



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	LP2950	LP2951		
$\overline{\text{ERROR}}$	—	5	O	Active-low open-collector error output. Goes low when V_{OUT} drops by 6% of its nominal value.
FEEDBACK	—	7	I	Determines the output voltage. Connect to V_{TAP} (with OUTPUT tied to SENSE) to output the fixed voltage corresponding to the part version, or connect to a resistor divider to adjust the output voltage.
GND	2	4	—	Ground
INPUT	3	8	I	Supply input
OUTPUT	1	1	O	Voltage output.
SENSE	—	2	I	Senses the output voltage. Connect to OUTPUT (with FEEDBACK tied to V_{TAP}) to output the voltage corresponding to the part version.
SHUTDOWN	—	3	I	Active-high input. Shuts down the device.
V_{TAP}	—	6	O	Tie to FEEDBACK to output the fixed voltage corresponding to the part version.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage range	–0.3	30	V
V_{SHDN}	SHUTDOWN input voltage range	–1.5	30	V
$V_{\overline{ERROR}}$	$\overline{\text{ERROR}}$ comparator output voltage range (2)	–1.5	30	V
V_{FDBK}	FEEDBACK input voltage range (2) (3)	–1.5	30	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) May exceed input supply voltage
(3) If load is returned to a negative power supply, the output must be diode clamped to GND.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	0	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	See (1)	30	V
T_J	Operating virtual junction temperature	–40	125	°C

(1) Minimum V_{IN} is the greater of:
(a) 2 V (25°C), 2.3 V (over temperature), or
(b) $V_{OUT(MAX)}$ + Dropout (Max) at rated I_L

6.4 Thermal Information

THERMAL METRIC (1)		LP2950	LP2951			UNIT
		LP	D	P	DRG	
		3 PINS	8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140	97	84.6	52.44	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

V_{IN} = V_{OUT} (nominal) + 1 V, I_L = 100 µA, C_L = 1 µF (5-V versions) or C_L = 2.2 µF (3-V and 3.3-V versions), 8-pin version: FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE, $V_{SHUTDOWN}$ ≤ 0.7 V

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
3-V VERSION (LP295x-30)							
V_{OUT}	Output voltage	I_L = 100 µA	25°C	2.970	3	3.030	V
			–40°C to 125°C	2.940	3	3.060	
3.3-V VERSION (LP295x-33)							
V_{OUT}	Output voltage	I_L = 100 µA	25°C	3.267	3.3	3.333	V
			–40°C to 125°C	3.234	3.3	3.366	
5-V VERSION (LP295x-50)							
V_{OUT}	Output voltage	I_L = 100 µA	25°C	4.950	5	5.050	V
			–40°C to 125°C	4.900	5	5.100	
ALL VOLTAGE OPTIONS							
	Output voltage temperature coefficient(1)	I_L = 100 µA	–40°C to 125°C		20	100	ppm/°C
	Line regulation(2)	V_{IN} = [$V_{OUT(NOM)}$ + 1 V] to 30 V	25°C		0.03	0.2	%/V
			–40°C to 125°C			0.4	
	Load regulation(2)	I_L = 100 µA to 100 mA	25°C		0.04%	0.2%	—
			–40°C to 125°C			0.3%	
V_{IN} – V_{OUT}	Dropout voltage(3)	I_L = 100 µA	25°C		50	80	mV
			–40°C to 125°C			150	
		I_L = 100 mA	25°C		380	450	
			–40°C to 125°C			600	
I_{GND}	GND current	I_L = 100 µA	25°C		75	120	µA
			–40°C to 125°C			140	
		I_L = 100 mA	25°C		8	12	mA
			–40°C to 125°C			14	
	Dropout ground current	V_{IN} = $V_{OUT(NOM)}$ – 0.5 V, I_L = 100 µA	25°C		110	170	µA
			–40°C to 125°C			200	
	Current limit	V_{OUT} = 0 V	25°C		160	200	mA
			–40°C to 125°C			220	
	Thermal regulation(4)	I_L = 100 µA	25°C		0.05	0.2	%/W
	Output noise (RMS), 10 Hz to 100 kHz	C_L = 1 µF (5 V only)	25°C		430		µV
		C_L = 200 µF			160		
		LP2951-50: C_L = 3.3 µF, C_{Bypass} = 0.01 µF between pins 1 and 7			100		

(1) Output or reference voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.
(2) Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.
(3) Dropout voltage is defined as the input-to-output differential at which the output voltage drops 100 mV, below the value measured at 1-V differential. The minimum input supply voltage of 2 V (2.3 V over temperature) must be observed.
(4) Thermal regulation is defined as the change in output voltage at a time (T) after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50-mA load pulse at V_{IN} = 30 V, V_{OUT} = 5 V (1.25-W pulse) for t = 10 ms.

Electrical Characteristics (continued)

V_{IN} = V_{OUT} (nominal) + 1 V, I_L = 100 µA, C_L = 1 µF (5-V versions) or C_L = 2.2 µF (3-V and 3.3-V versions),
8-pin version: FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE, $V_{SHUTDOWN}$ ≤ 0.7 V

PARAMETER	TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
(LP2951-xx) 8-PIN VERSION ONLY ADJ						
Reference voltage		25°C	1.218	1.235	1.252	V
		–40°C to 125°C	1.212		1.257	
	V_{OUT} = V_{REF} to (V_{IN} – 1 V), V_{IN} = 2.3 V to 30 V, I_L = 100 µA to 100 mA	–40°C to 125°C	1.200		1.272	
Reference voltage temperature coefficient[1]		25°C		20		ppm/°C
FEEDBACK bias current		25°C		20	40	nA
		–40°C to 125°C			60	
FEEDBACK bias current temperature coefficient		25°C		0.1		nA/°C
$\overline{\text{ERROR}}$ COMPARATOR						
Output leakage current	V_{OUT} = 30 V	25°C		0.01	1	µA
		–40°C to 125°C			2	
Output low voltage	V_{IN} = $V_{OUT(NOM)}$ – 0.5 V, I_{OL} = 400 µA	25°C		150	250	mV
		–40°C to 125°C			400	
Upper threshold voltage ($\overline{\text{ERROR}}$ output high)[5]		25°C	40	60		mV
		–40°C to 125°C	25			
Lower threshold voltage ($\overline{\text{ERROR}}$ output low)[5]		25°C		75	95	mV
		–40°C to 125°C			140	
Hysteresis[5]		25°C		15		mV
SHUTDOWN INPUT						
Input logic voltage	Low (regulator ON)	–40°C to 125°C			0.7	V
	High (regulator OFF)		2			
SHUTDOWN input current	SHUTDOWN = 2.4 V	25°C		30	50	µA
		–40°C to 125°C			100	
	SHUTDOWN = 30 V	25°C		450	600	
		–40°C to 125°C			750	
Regulator output current in shutdown	$V_{SHUTDOWN}$ ≥ 2 V, V_{IN} ≤ 30 V, V_{OUT} = 0, FEEDBACK tied to V_{TAP}	25°C		3	10	µA
		–40°C to 125°C			20	

(5) Comparator thresholds are expressed in terms of a voltage differential equal to the nominal reference voltage (measured at V_{IN} – V_{OUT} = 1 V) minus FEEDBACK terminal voltage. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT}/V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5 V, the $\overline{\text{ERROR}}$ output is specified to go low when the output drops by 95 mV × 5 V/1.235 V = 384 mV. Thresholds remain constant as a percentage of V_{OUT} (as V_{OUT} is varied), with the low-output warning occurring at 6% below nominal (typ) and 7.7% (max).

6.6 Typical Characteristics

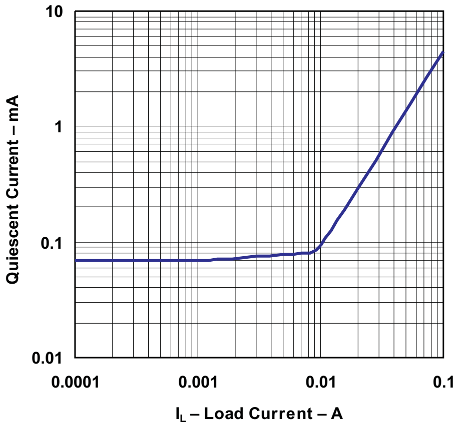


Figure 1. Quiescent Current vs Load Current

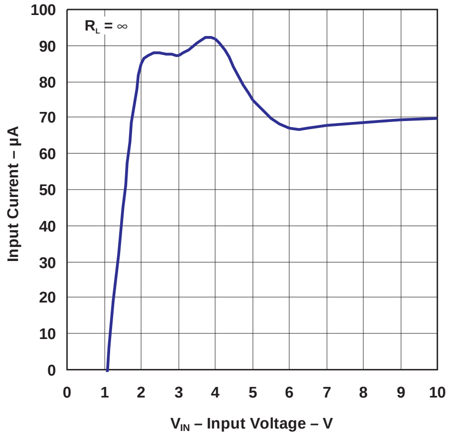


Figure 2. Input Current vs Input Voltage (R_L = OPEN)

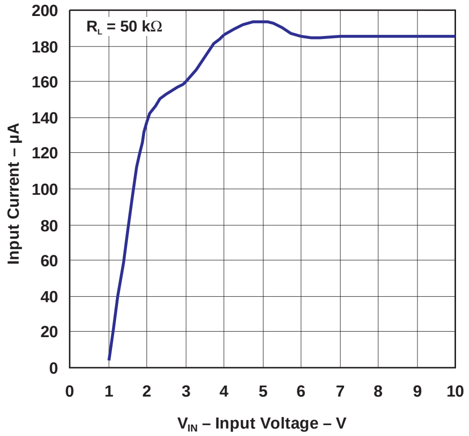


Figure 3. Input Current vs Input Voltage (R_L = 50 kΩ)

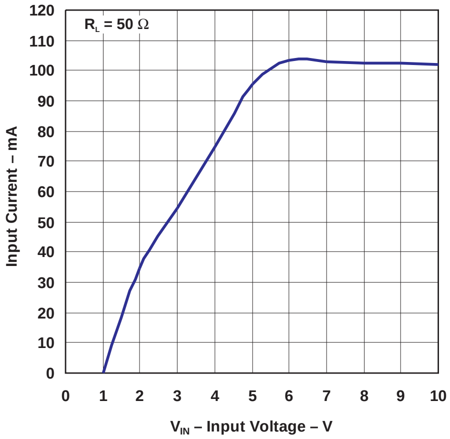


Figure 4. Input Current vs Input Voltage (R_L = 50 Ω)

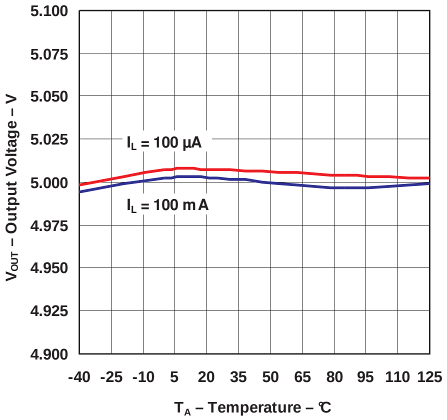


Figure 5. Output Voltage vs Temperature

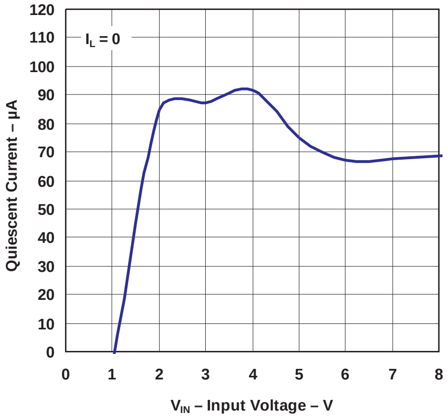


Figure 6. Quiescent Current vs Input Voltage (I_L = 0)

Typical Characteristics (continued)

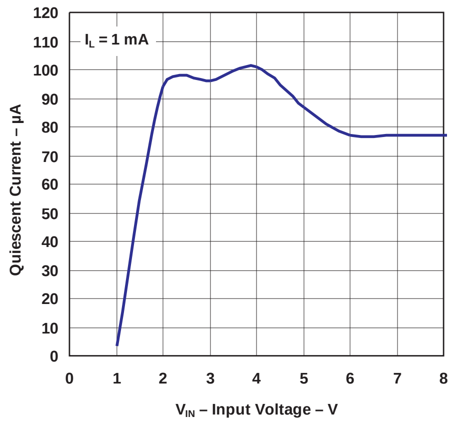


Figure 7. Quiescent Current vs Input Voltage (I_L = 1 mA)

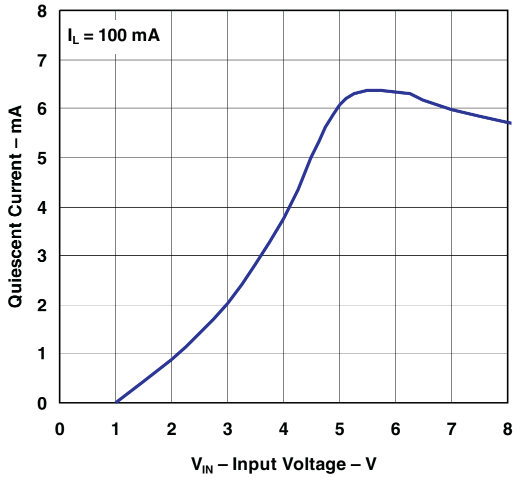


Figure 8. Quiescent Current vs Input Voltage (I_L = 100 mA)

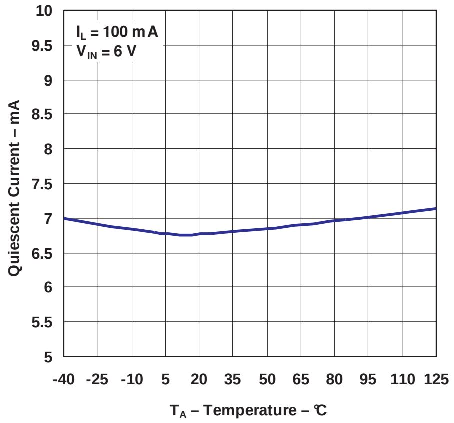


Figure 9. Quiescent Current vs Temperature (I_L = 100 mA)

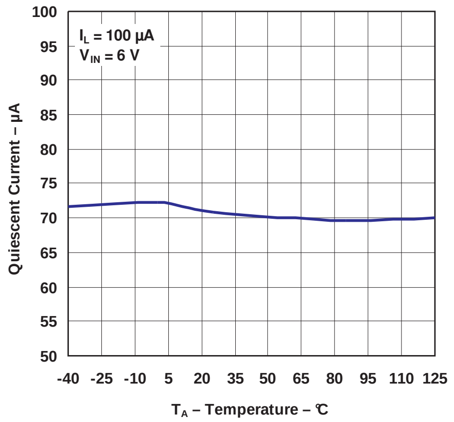


Figure 10. Quiescent Current vs Temperature (I_L = 100 µA)

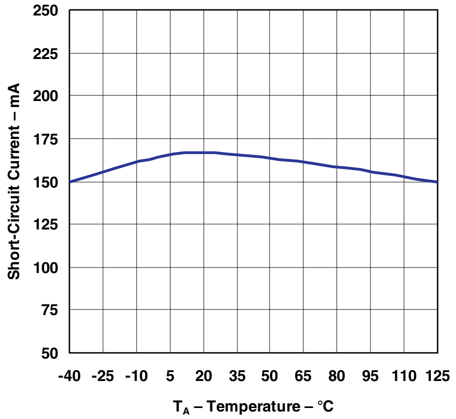


Figure 11. Short-circuit Current vs Temperature

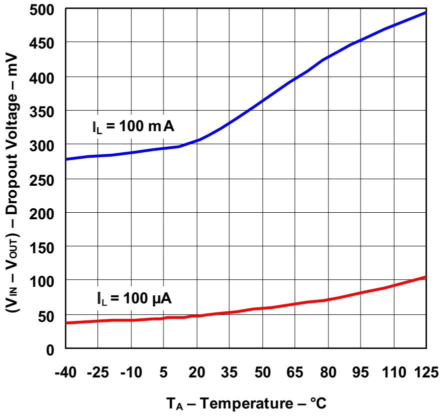


Figure 12. Dropout Voltage vs Temperature

Typical Characteristics (continued)

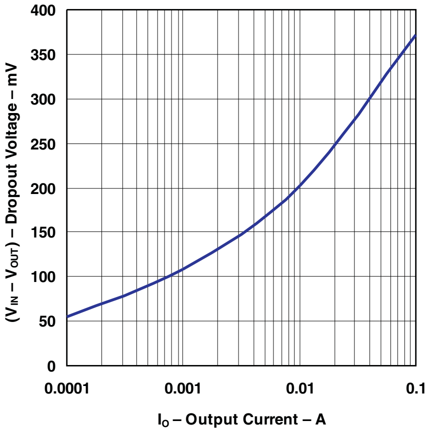


Figure 13. Dropout Voltage vs Dropout Current

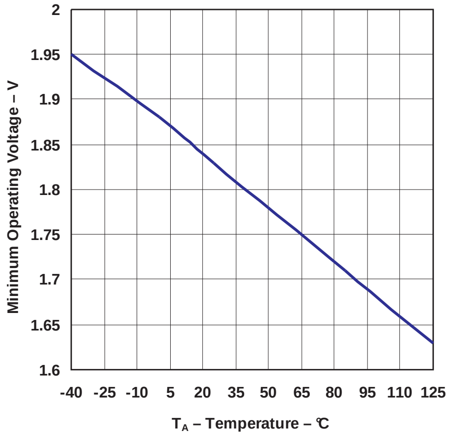


Figure 14. LP2951 Minimum Operating Voltage vs Temperature

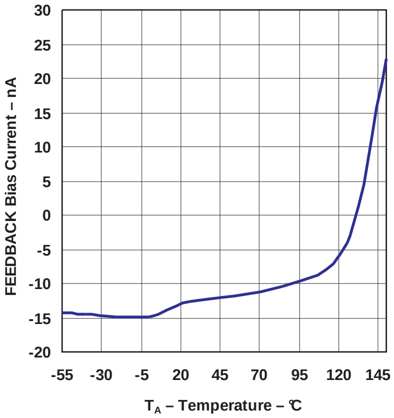


Figure 15. LP2951 FEEDBACK Bias Current vs Temperature

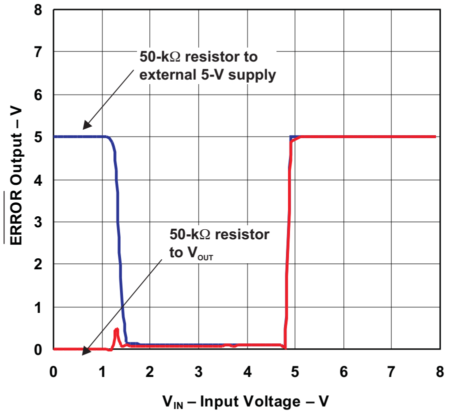


Figure 16. LP2951 $\overline{\text{ERROR}}$ Comparator Output vs Input Voltage

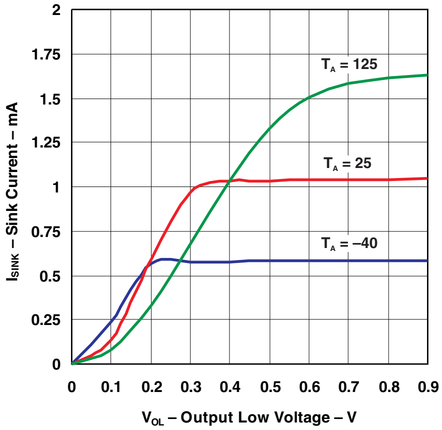


Figure 17. LP2951 $\overline{\text{ERROR}}$ Comparator Sink Current vs Output Low Voltage

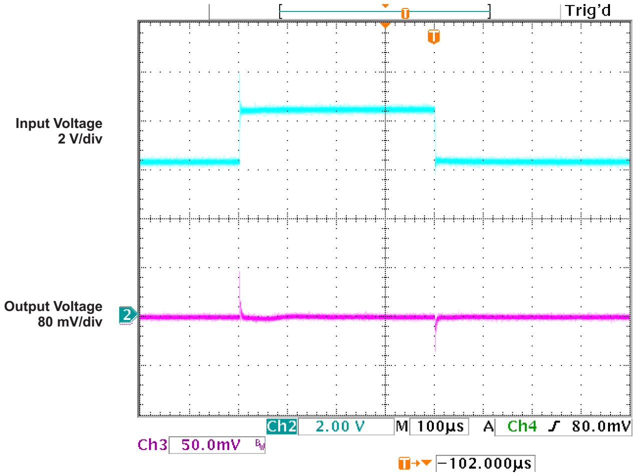


Figure 18. Line Transient Response vs Time

Typical Characteristics (continued)

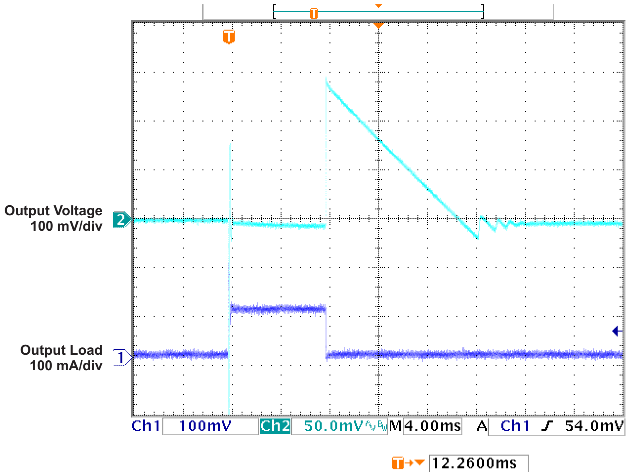


Figure 19. Load Transient Response vs Time (V_{OUT} = 5 V, C_L = 10 µF)

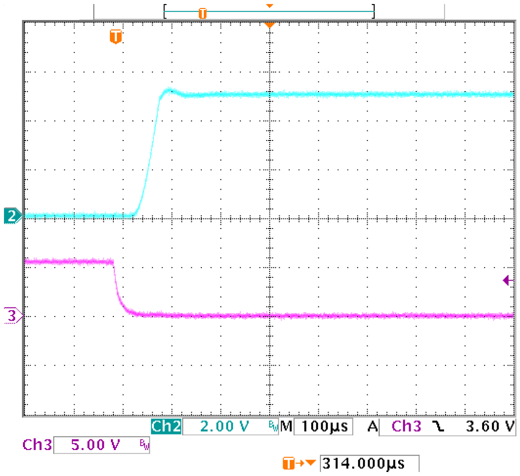


Figure 20. Enable Transient Response vs Time (I_L = 1 mA, C_L = 1 µF)

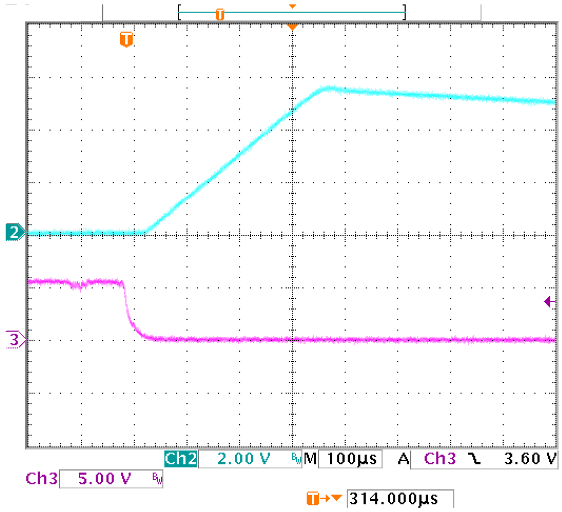


Figure 21. Enable Transient Response vs Time (I_L = 1 mA, C_L = 10 µF)

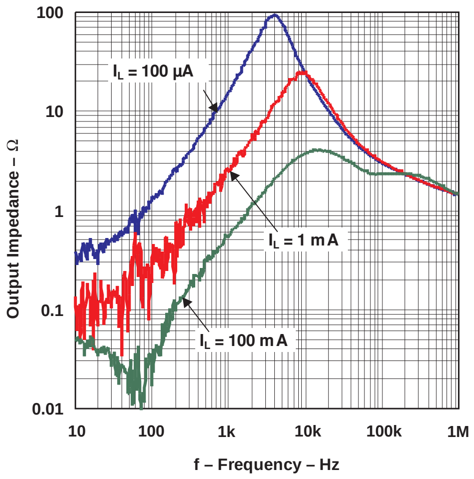


Figure 22. Output Impedance vs Frequency

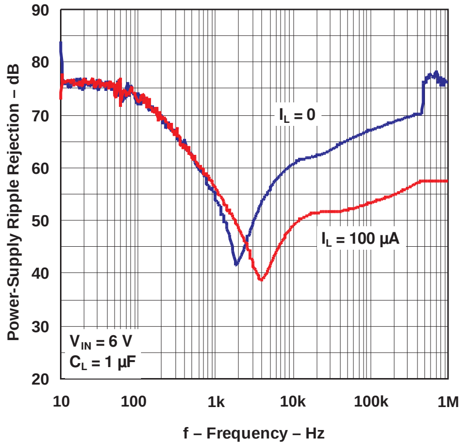


Figure 23. Ripple Rejection vs Frequency

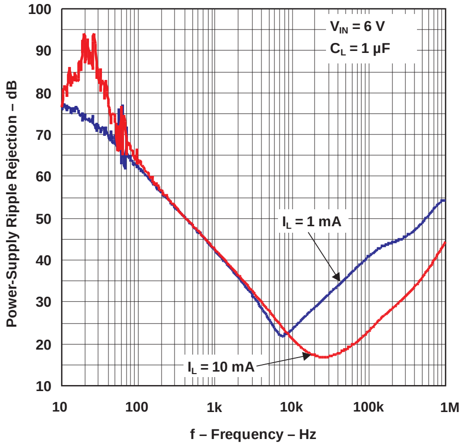


Figure 24. Output Impedance vs Frequency

Typical Characteristics (continued)

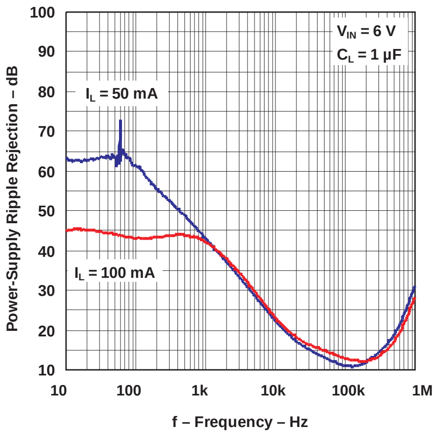


Figure 25. Output Impedance vs Frequency

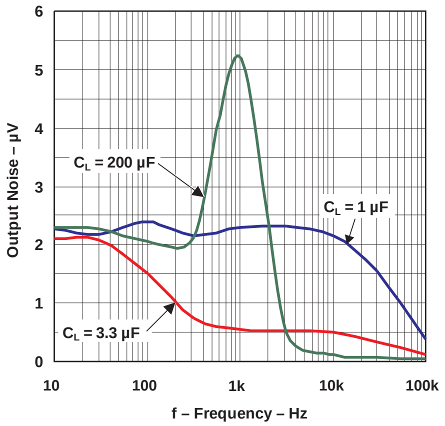


Figure 26. LP2951 Output Noise vs Frequency

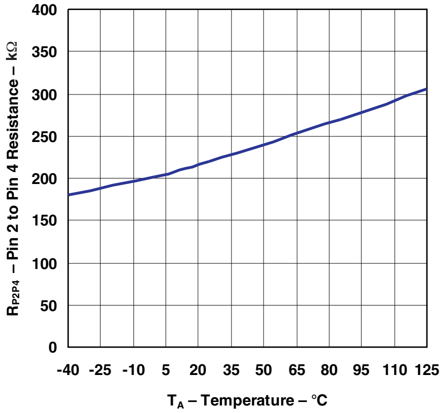


Figure 27. LP2951 Divider Resistance vs Temperature

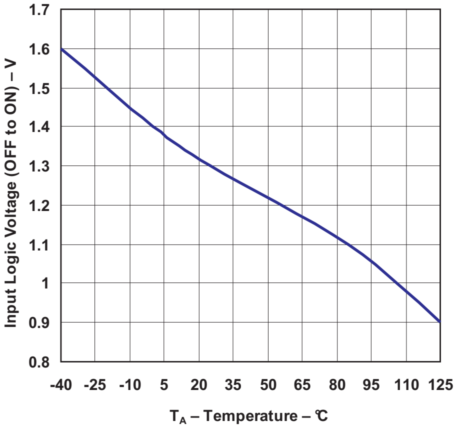


Figure 28. Shutdown Threshold Voltage (Off to On) vs Temperature

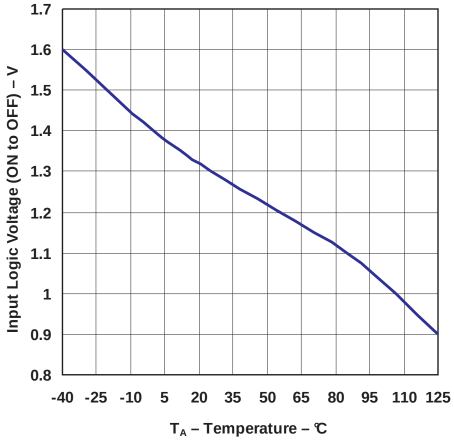


Figure 29. Shutdown Threshold Voltage (On to Off) vs Temperature

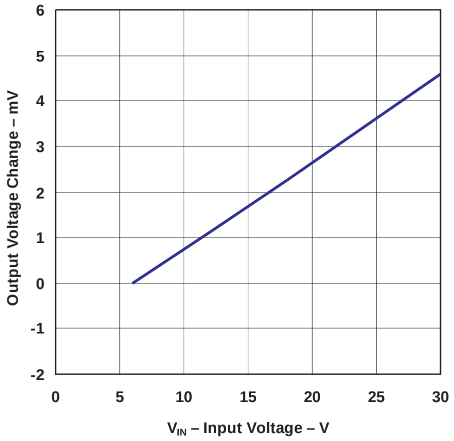


Figure 30. Line Regulation vs Input Voltage

7 Detailed Description

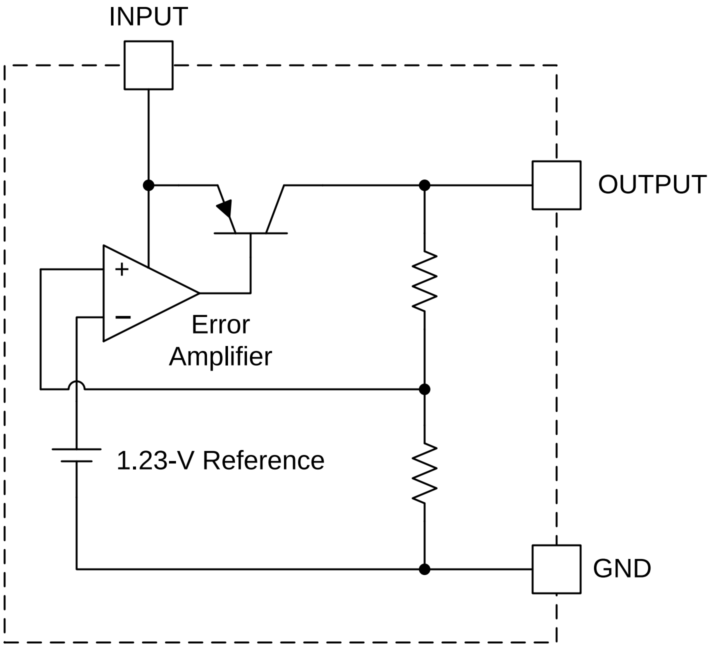
7.1 Overview

The LP2950 and LP2951 devices are bipolar, low-dropout voltage regulators that can accommodate a wide input supply-voltage range of up to 30 V. The easy-to-use, 3-pin LP2950 is available in fixed-output voltages of 5 V, 3.3 V, and 3 V. However, the 8-pin LP2951 device is able to output either a fixed or adjustable output from the same device. By tying the OUTPUT and SENSE pins together, and the FEEDBACK and V_{TAP} pins together, the LP2951 device outputs a fixed 5 V, 3.3 V, or 3 V (depending on the version). Alternatively, by leaving the SENSE and V_{TAP} pins open and connecting FEEDBACK to an external resistor divider, the output can be set to any value between 1.235 V to 30 V.

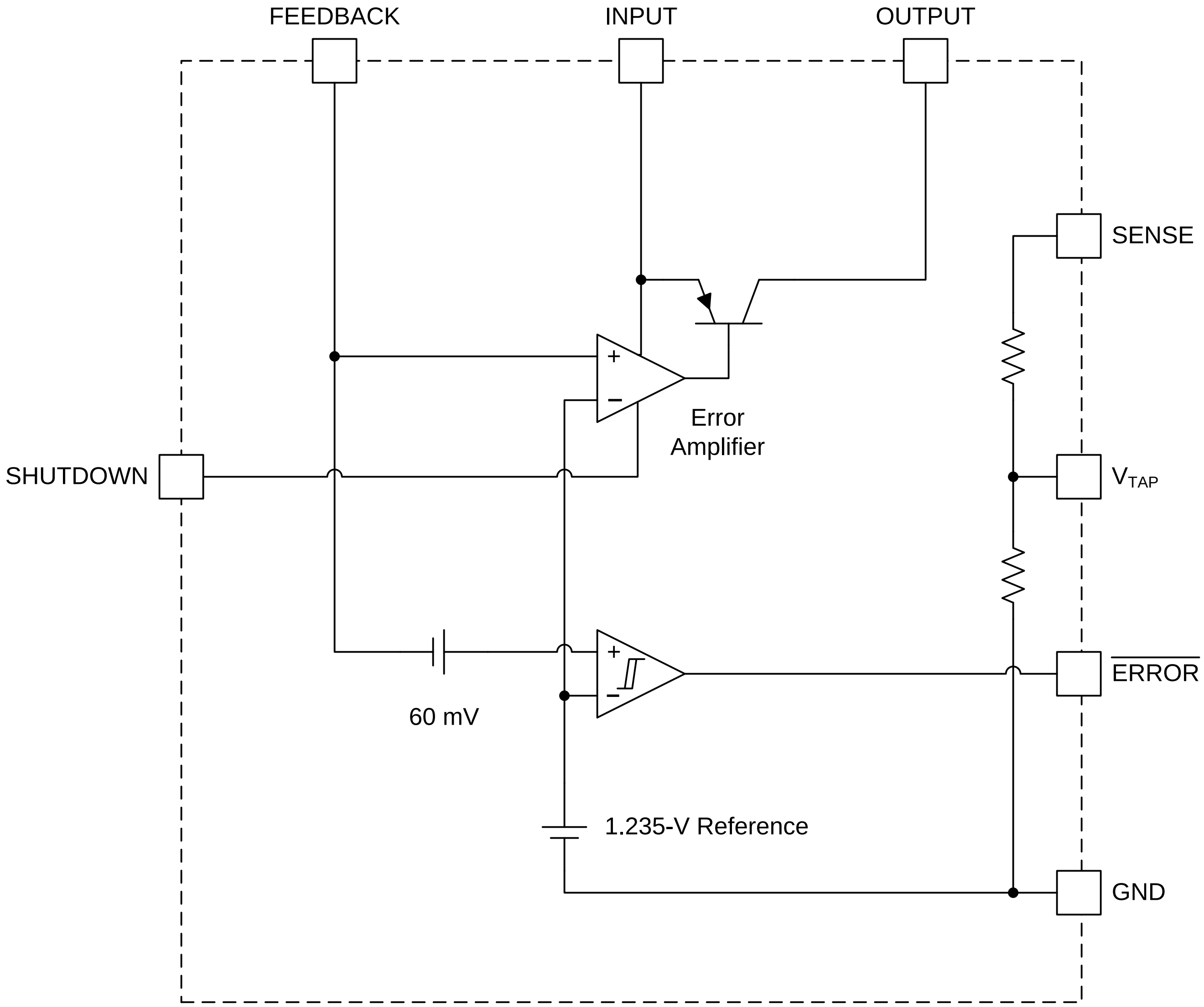
The 8-pin LP2951 device also offers additional functionality that makes it particularly suitable for battery-powered applications. For example, a logic-compatible shutdown feature allows the regulator to be put in standby mode for power savings. In addition, there is a built-in supervisor reset function in which the $\overline{\text{ERROR}}$ output goes low when V_{OUT} drops by 6% of its nominal value for whatever reasons – due to a drop in V_{IN}, current limiting, or thermal shutdown.

The LP2950 and LP2951 devices are designed to minimize all error contributions to the output voltage. With a tight output tolerance (0.5% at 25°C), a very low output voltage temperature coefficient (20 ppm typical), extremely good line and load regulation (0.3% and 0.4% typical), and remote sensing capability, the parts can be used as either low-power voltage references or 100-mA regulators.

7.2 LP2950 Functional Block Diagram



7.3 LP2951 Functional Block Diagram



7.4 Feature Description

7.4.1 $\overline{\text{ERROR}}$ Function (LP2951 Only)

The LP2951 device has a low-voltage detection comparator that outputs a logic low when the output voltage drops by ≈6% from its nominal value, and outputs a logic high when V_{OUT} has reached ≈95% of its nominal value. This 95% of nominal figure is obtained by dividing the built-in offset of ≈60 mV by the 1.235-V bandgap reference, and remains independent of the programmed output voltage. For example, the trip-point threshold ($\overline{\text{ERROR}}$ output goes high) typically is 4.75 V for a 5-V output and 11.4 V for a 12-V output. Typically, there is a hysteresis of 15 mV between the thresholds for high and low $\overline{\text{ERROR}}$ output.

A timing diagram is shown in Figure 31 for $\overline{\text{ERROR}}$ vs V_{OUT} (5 V), as V_{IN} is ramped up and down. $\overline{\text{ERROR}}$ becomes valid (low) when V_{IN} ≈ 1.3 V. When V_{IN} ≈ 5 V, V_{OUT} = 4.75 V, causing $\overline{\text{ERROR}}$ to go high. Because the dropout voltage is load dependent, the output trip-point threshold is reached at different values of V_{IN}, depending on the load current. For instance, at higher load current, $\overline{\text{ERROR}}$ goes high at a slightly higher value of V_{IN}, and vice versa for lower load current. The output-voltage trip point remains at ~4.75 V, regardless of the load. Note that when V_{IN} ≤ 1.3 V, the $\overline{\text{ERROR}}$ comparator output is turned off and pulled high to its pullup voltage. If V_{OUT} is used as the pullup voltage, rather than an external 5-V source, $\overline{\text{ERROR}}$ typically is ~1.2 V. In this condition, an equal resistor divider (10 kΩ is suitable) can be tied to $\overline{\text{ERROR}}$ to divide down the voltage to a valid logic low during any fault condition, while still enabling a logic high during normal operation.

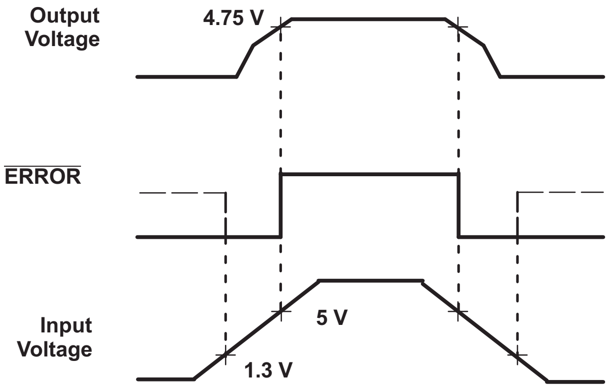


Figure 31. $\overline{\text{ERROR}}$ Output Timing

Because the $\overline{\text{ERROR}}$ comparator has an open-collector output, an external pullup resistor is required to pull the output up to V_{OUT} or another supply voltage (up to 30 V). The output of the comparator is rated to sink up to 400 µA. A suitable range of values for the pullup resistor is from 100 kΩ to 1 MΩ. If $\overline{\text{ERROR}}$ is not used, it can be left open.

Feature Description (continued)

7.4.2 Programming Output Voltage (LP2951 Only)

A unique feature of the LP2951 device is its ability to output either a fixed voltage or an adjustable voltage, depending on the external pin connections. To output the internally programmed fixed voltage, tie the SENSE pin to the OUTPUT pin and the FEEDBACK pin to the V_{TAP} pin. Alternatively, a user-programmable voltage ranging from the internal 1.235-V reference to a 30-V max can be set by using an external resistor divider pair. The resistor divider is tied to V_{OUT}, and the divided-down voltage is tied directly to FEEDBACK for comparison against the internal 1.235-V reference. To satisfy the steady-state condition in which its two inputs are equal, the error amplifier drives the output to equal Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) - I_{FB}R_1 \tag{1}$$

Where:

V_{REF} = 1.235 V applied across R2 (see Figure 32)

I_{FB} = FEEDBACK bias current, typically 20 nA

A minimum regulator output current of 1 μA must be maintained. Thus, in an application where a no-load condition is expected (for example, CMOS circuits in standby), this 1-μA minimum current must be provided by the resistor pair, effectively imposing a maximum value of R2 = 1.2 MΩ (1.235 V/1.2 MΩ ≉ 1 μA).

I_{FB} = 20 nA introduces an error of ≉0.02% in V_{OUT}. This can be offset by trimming R1. Alternatively, increasing the divider current makes I_{FB} less significant, thus, reducing its error contribution. For instance, using R2 = 100 kΩ reduces the error contribution of I_{FB} to 0.17% by increasing the divider current to ≉12 μA. This increase in the divider current still is small compared to the 600-μA typical quiescent current of the LP2951 under no load.

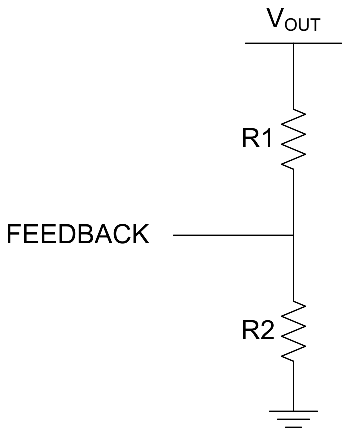


Figure 32. Adjusting the Feedback on the LP2951

7.5 Device Functional Modes

7.5.1 Shutdown Mode

These devices can be placed in shutdown mode with a logic high at the SHUTDOWN pin. Return the logic level low to restore operation or tie SHUTDOWN to ground if the feature is not being used.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP295x devices are used as low-dropout regulators with a wide range of input voltages.

8.2 Typical Application

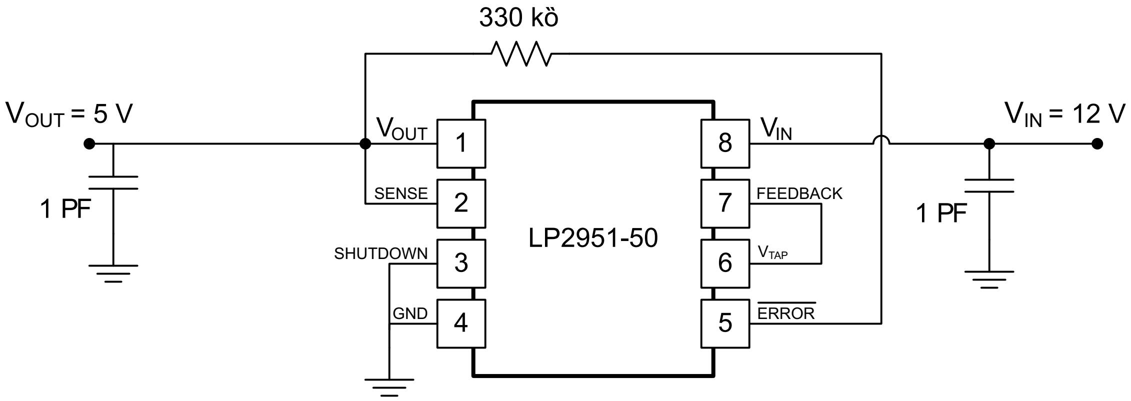


Figure 33. 12-V to 5-V Converter

8.2.1 Design Requirements

8.2.1.1 Input Capacitor (C_{IN})

A 1-µF (tantalum, ceramic, or aluminum) electrolytic capacitor should be placed locally at the input of the LP2950 or LP2951 device if there is, or will be, significant impedance between the ac filter capacitor and the input; for example, if a battery is used as the input or if the ac filter capacitor is located more than 10 in away. There are no ESR requirements for this capacitor, and the capacitance can be increased without limit.

8.2.1.2 Output Capacitor (C_{OUT})

As with most PNP LDOs, stability conditions require the output capacitor to have a minimum capacitance and an ESR that falls within a certain range.

Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Capacitance Value

For $V_{OUT} \geq 5$ V, a minimum of 1 µF is required. For lower V_{OUT}, the regulator's loop gain is running closer to unity gain and, thus, has lower phase margins. Consequently, a larger capacitance is needed for stability. For $V_{OUT} = 3$ V or 3.3 V, a minimum of 2.2 µF is recommended. For worst case, $V_{OUT} = 1.23$ V (using the ADJ version), a minimum of 3.3 µF is recommended. C_{OUT} can be increased without limit and only improves the regulator stability and transient response. Regardless of its value, the output capacitor should have a resonant frequency greater than 500 kHz.

The minimum capacitance values given above are for maximum load current of 100 mA. If the maximum expected load current is less than 100 mA, then lower values of C_{OUT} can be used. For instance, if $I_{OUT} < 10$ mA, then only 0.33 µF is required for C_{OUT}. For $I_{OUT} < 1$ mA, 0.1 µF is sufficient for stability requirements. Thus, for a worst-case condition of 100-mA load and $V_{OUT} = V_{REF} = 1.235$ V (representing the highest load current and lowest loop gain), a minimum C_{OUT} of 3.3 µF is recommended.

For the LP2950/51, no load stability is inherent in the design — a desirable feature in CMOS circuits that are put in standby (such as RAM keep-alive applications). If the LP2951 is used with external resistors to set the output voltage, a minimum load current of 1 µA is recommended through the resistor divider.

8.2.2.2 Capacitor Types

Most tantalum or aluminum electrolytics are suitable for use at the input. Film-type capacitors also work but at higher cost. When operating at low temperature, care should be taken with aluminum electrolytics, as their electrolytes often freeze at –30°C. For this reason, solid tantalum capacitors should be used at temperatures below –25°C.

Ceramic capacitors can be used, but due to their low ESR (as low as 5 mΩ to 10 mΩ), they may not meet the minimum ESR requirement previously discussed. If a ceramic capacitor is used, a series resistor between 0.1 Ω to 2 Ω must be added to meet the minimum ESR requirement. In addition, ceramic capacitors have one glaring disadvantage that must be taken into account — a poor temperature coefficient, where the capacitance can vary significantly with temperature. For instance, a large-value ceramic capacitor (≥ 2.2 µF) can lose more than half of its capacitance as temperature rises from 25°C to 85°C. Thus, a 2.2-µF capacitor at 25°C drops well below the minimum C_{OUT} required for stability as ambient temperature rises. For this reason, select an output capacitor that maintains the minimum 2.2 µF required for stability for the entire operating temperature range.

8.2.2.3 C_{BYPASS}: Noise and Stability Improvement

In the LP2951 device, an external FEEDBACK pin directly connected to the error amplifier noninverting input can allow stray capacitance to cause instability by shunting the error amplifier feedback to GND, especially at high frequencies. This is worsened if high-value external resistors are used to set the output voltage, because a high resistance allows the stray capacitance to play a more significant role; i.e., a larger RC time delay is introduced between the output of the error amplifier and its FEEDBACK input, leading to more phase shift and lower phase margin. A solution is to add a 100-pF bypass capacitor (C_{BYPASS}) between OUTPUT and FEEDBACK; because C_{BYPASS} is in parallel with R1, it lowers the impedance seen at FEEDBACK at high frequencies, in effect offsetting the effect of the parasitic capacitance by providing more feedback at higher frequencies. More feedback forces the error amplifier to work at a lower loop gain, so C_{OUT} should be increased to a minimum of 3.3 µF to improve the regulator's phase margin.

C_{BYPASS} can be also used to reduce output noise in the LP2951 device. This bypass capacitor reduces the closed loop gain of the error amplifier at the high frequency, so noise no longer scales with the output voltage. This improvement is more noticeable with higher output voltages, where loop gain reduction is greatest. A suitable C_{BYPASS} is calculated as shown in Equation 2:

$$f_{(CBYPASS)} \simeq 200\,\text{Hz} \rightarrow C_{(BYPASS)} = \frac{1}{2\pi \times R1 \times 200\,\text{Hz}} \tag{2}$$

On the 3-pin LP2950 device, noise reduction can be achieved by increasing the output capacitor, which causes the regulator bandwidth to be reduced, thus eliminating high-frequency noise. However, this method is relatively inefficient, as increasing C_{OUT} from 1 µF to 220 µF only reduces the regulator's output noise from 430 µV to 160 µV (over a 100-kHz bandwidth).

Typical Application (continued)

8.2.2.4 ESR Range

The regulator control loop relies on the ESR of the output capacitor to provide a zero to add sufficient phase margin to ensure unconditional regulator stability; this requires the closed-loop gain to intersect the open-loop response in a region where the open-loop gain rolls off at 20 dB/decade. This ensures that the phase is always less than 180° (phase margin greater than 0°) at unity gain. Thus, a minimum-maximum range for the ESR must be observed.

The upper limit of this ESR range is established by the fact that an ESR that is too high could result in the zero occurring too soon, causing the gain to roll off too slowly. This, in turn, allows a third pole to appear before unity gain and introduces enough phase shift to cause instability. This typically limits the maximum ESR to approximately 5 Ω.

Conversely, the lower limit of the ESR range is tied to the fact that an ESR that is too low shifts the zero too far out, past unity gain, which allows the gain to roll off at 40 dB/decade at unity gain, resulting in a phase shift of greater than 180°. Typically, this limits the minimum ESR to approximately 20 mΩ to 30 mΩ.

For specific ESR requirements, see *Typical Characteristics*.

8.2.3 Application Curves

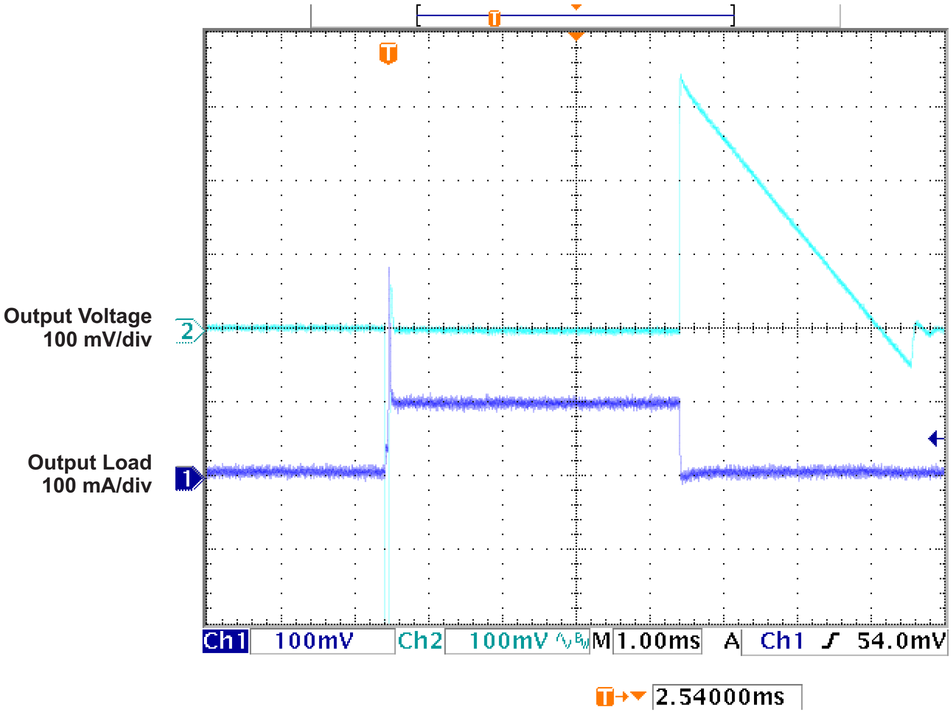


Figure 34. Load Transient Response vs Time (V_{OUT} = 5 V, C_L = 1 μF)

9 Power Supply Recommendations

Maximum input voltage should be limited to 30 V for proper operation. Place input and output capacitors as close to the device as possible to take advantage of their high frequency noise filtering properties.

10 Layout

10.1 Layout Guidelines

- Make sure that traces on the input and outputs of the device are wide enough to handle the desired currents. For this device, the output trace will need to be larger in order to accommodate the larger available current.
- Place input and output capacitors as close to the device as possible to take advantage of their high frequency noise filtering properties.

10.2 Layout Example

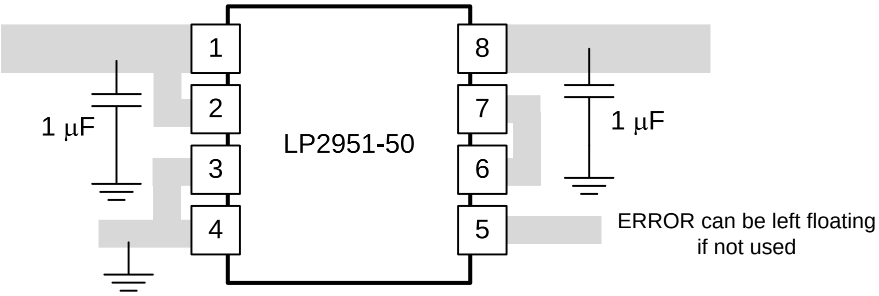


Figure 35. LP2951 Layout Example (D or P Package)

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2950-30LP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	KY5030	Samples
LP2950-30LPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	KY5030	Samples
LP2950-30LPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	KY5030	Samples
LP2950-33LPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	KY5033	Samples
LP2950-33LPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	KY5033	Samples
LP2950-50LPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 125	KY5050	Samples
LP2951-30D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KY5130	Samples
LP2951-30DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KY5130	Samples
LP2951-30DRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZUD	Samples
LP2951-33D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KY5133	Samples
LP2951-33DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KY5133	Samples
LP2951-33DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KY5133	Samples
LP2951-33DRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZUE	Samples
LP2951-50D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KY5150	Samples
LP2951-50DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KY5150	Samples
LP2951-50DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	KY5150	Samples
LP2951-50DRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZUF	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2951D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP2951	Samples
LP2951DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP2951	Samples
LP2951DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP2951	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP2951 :

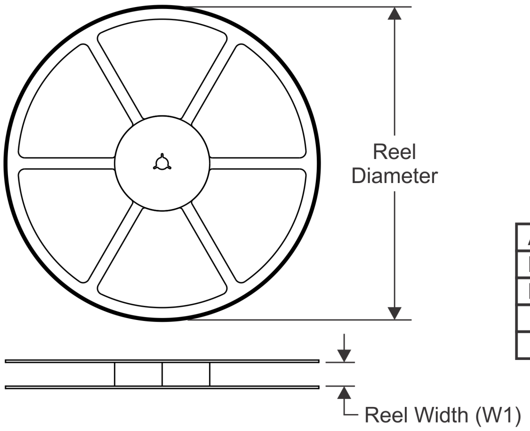
- Automotive: LP2951-Q1

NOTE: Qualified Version Definitions:

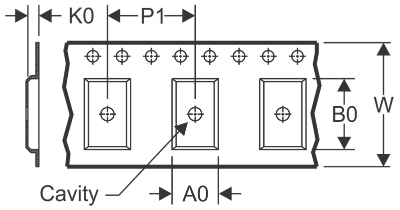
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

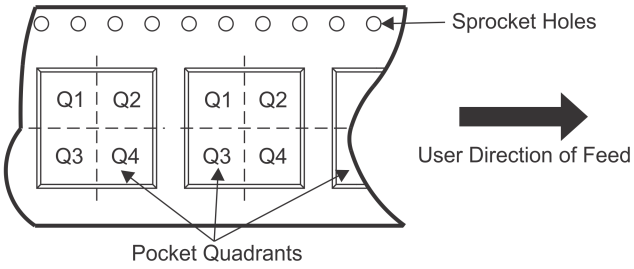


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

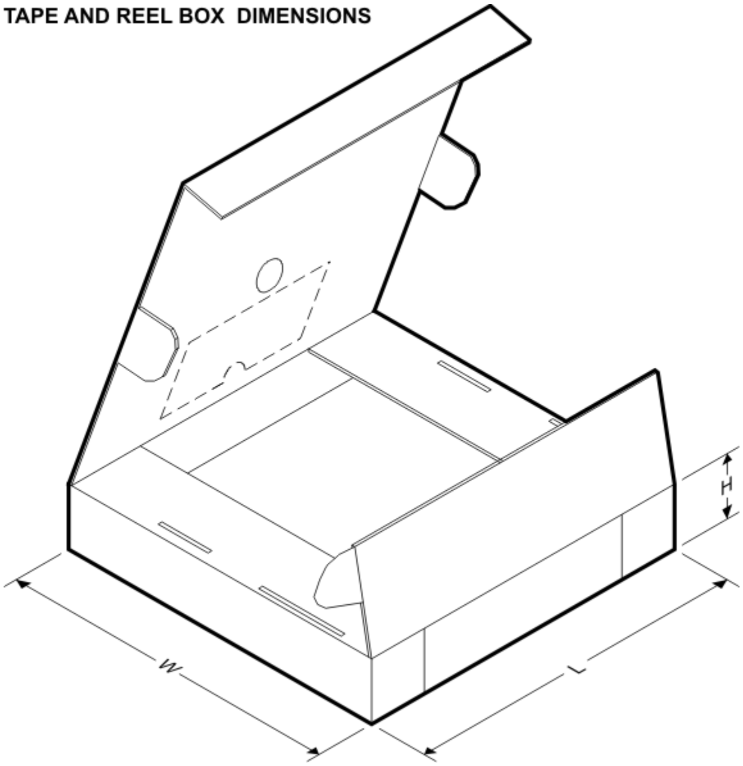
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2951-30DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LP2951-30DRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP2951-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LP2951-33DRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP2951-50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LP2951-50DRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP2951DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



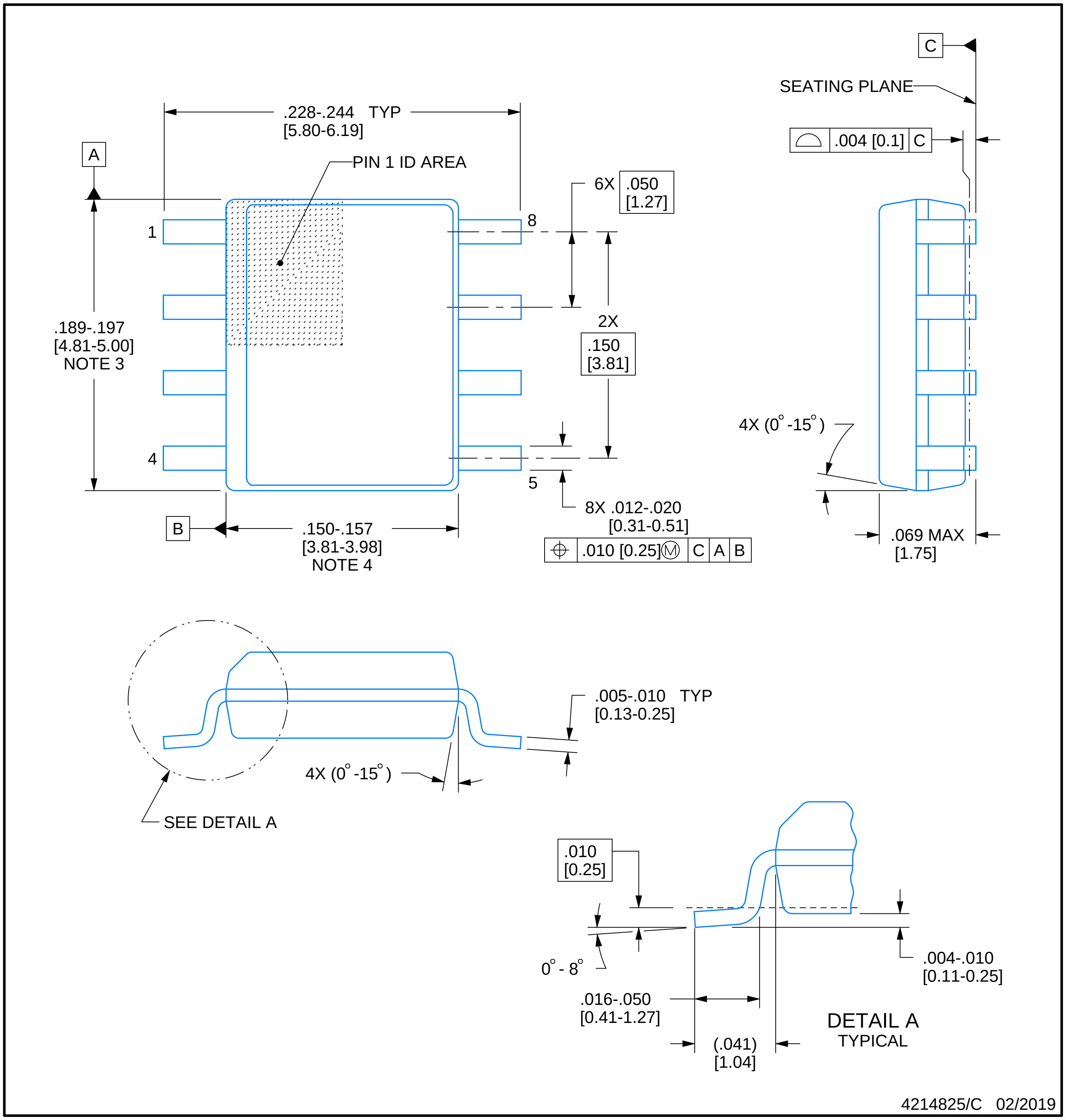
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2951-30DR	SOIC	D	8	2500	340.5	338.1	20.6
LP2951-30DRGR	SON	DRG	8	3000	367.0	367.0	35.0
LP2951-33DR	SOIC	D	8	2500	340.5	338.1	20.6
LP2951-33DRGR	SON	DRG	8	3000	367.0	367.0	35.0
LP2951-50DR	SOIC	D	8	2500	340.5	338.1	20.6
LP2951-50DRGR	SON	DRG	8	3000	367.0	367.0	35.0
LP2951DR	SOIC	D	8	2500	340.5	338.1	20.6

PACKAGE OUTLINE

SOIC - 1.75 mm max height

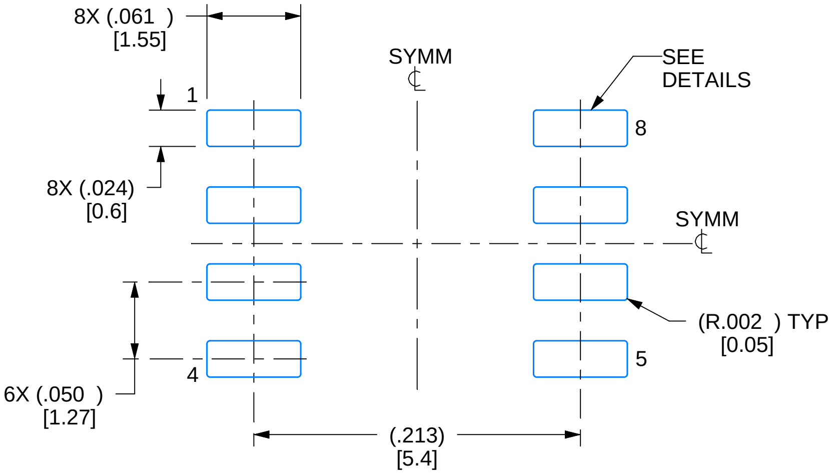
SMALL OUTLINE INTEGRATED CIRCUIT



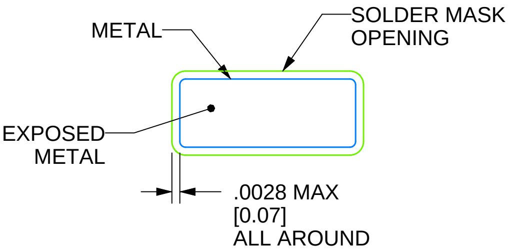
4214825/C 02/2019

NOTES:

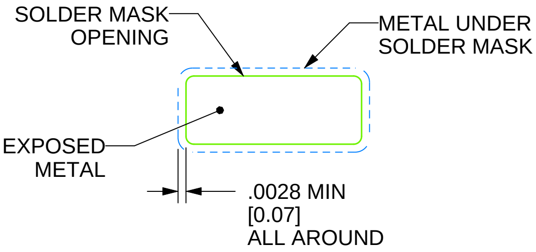
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

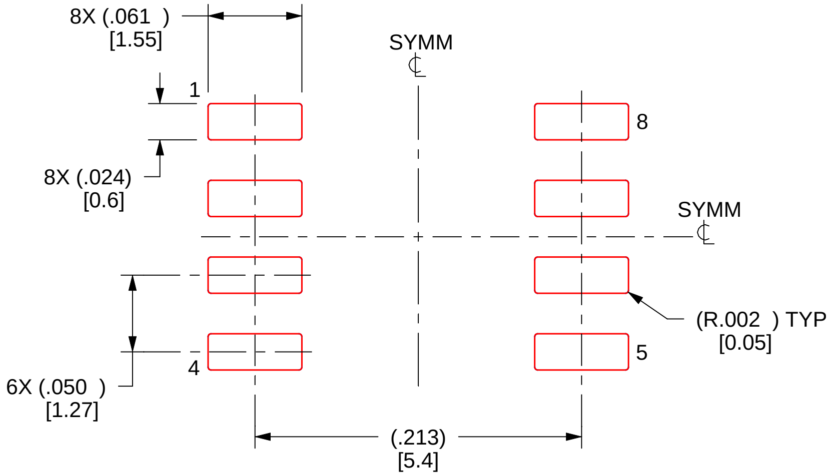


SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



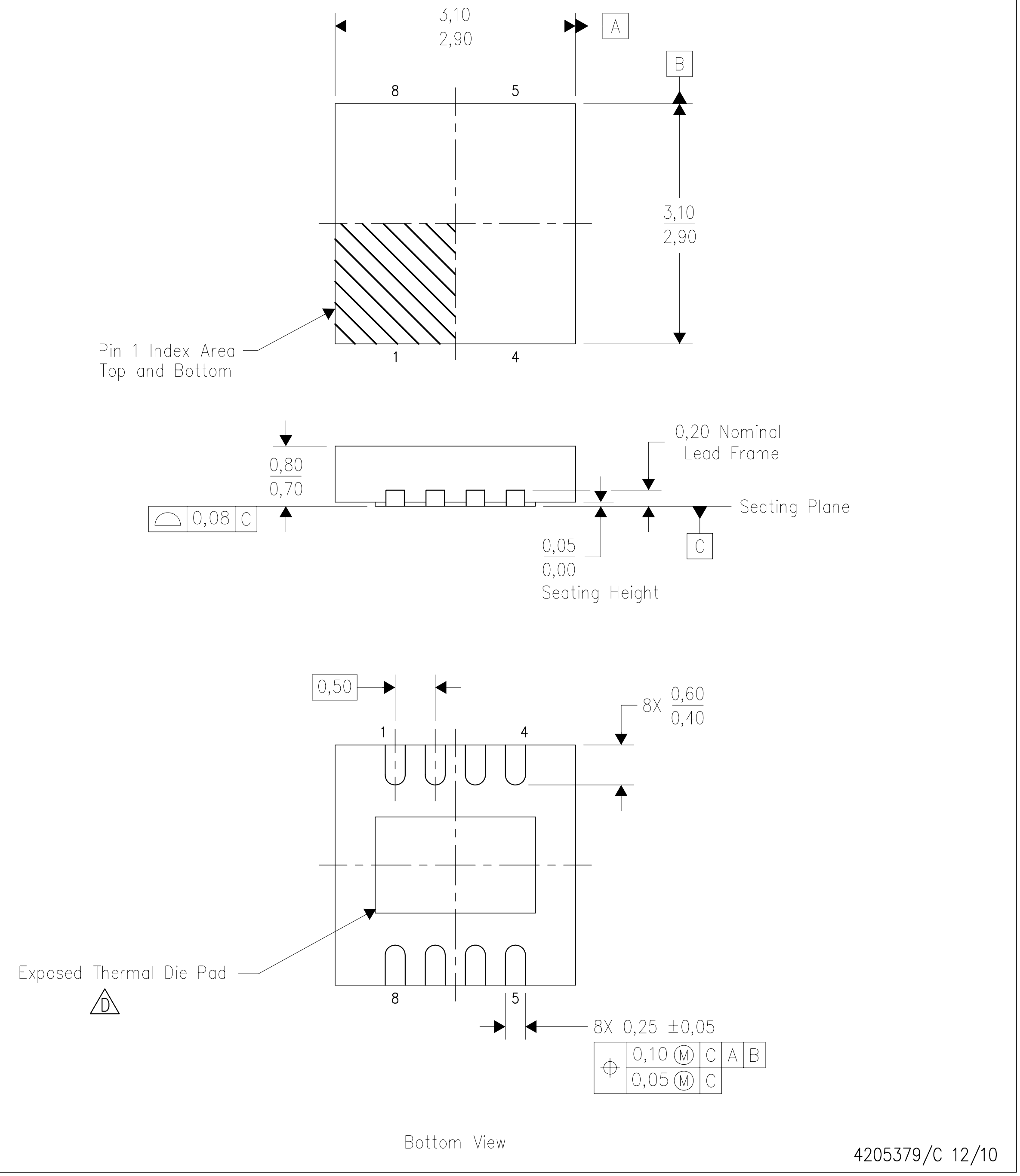
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



4205379/C 12/10

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. JEDEC MO–229 package registration pending.

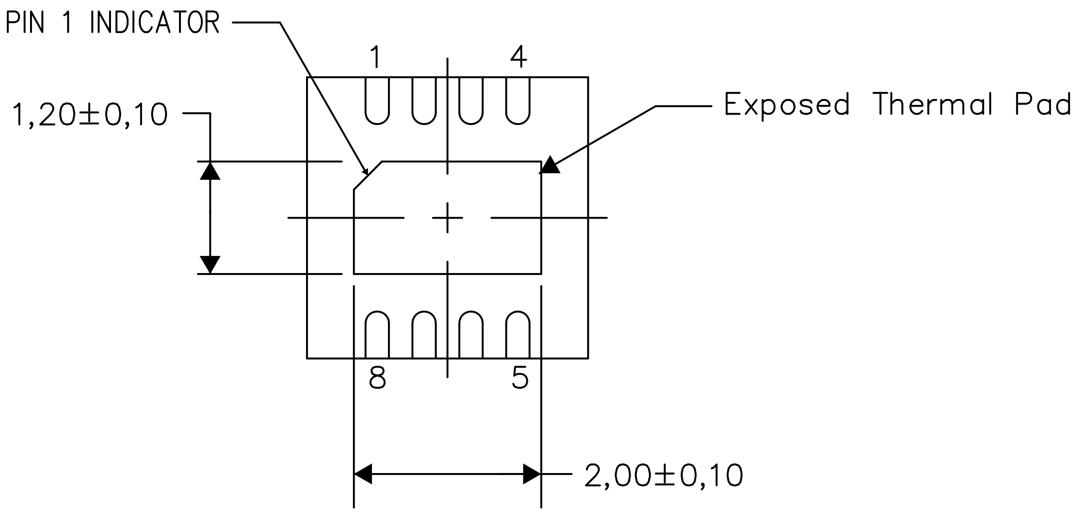
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



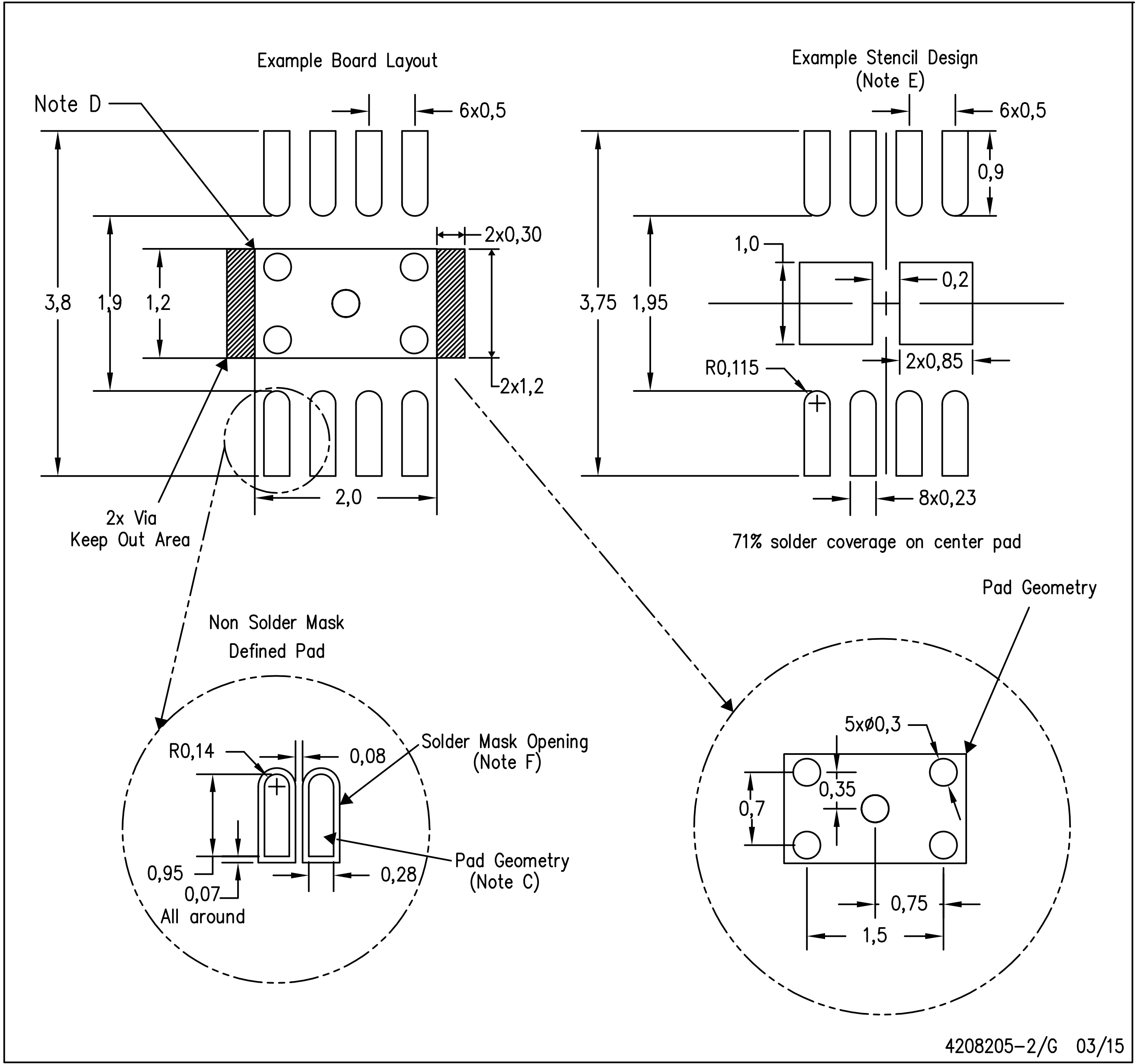
Bottom View

Exposed Thermal Pad Dimensions

4206881–2/I 03/15

NOTE: All linear dimensions are in millimeters

DRG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



4208205-2/G 03/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-SM-782 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

LP 3

TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE

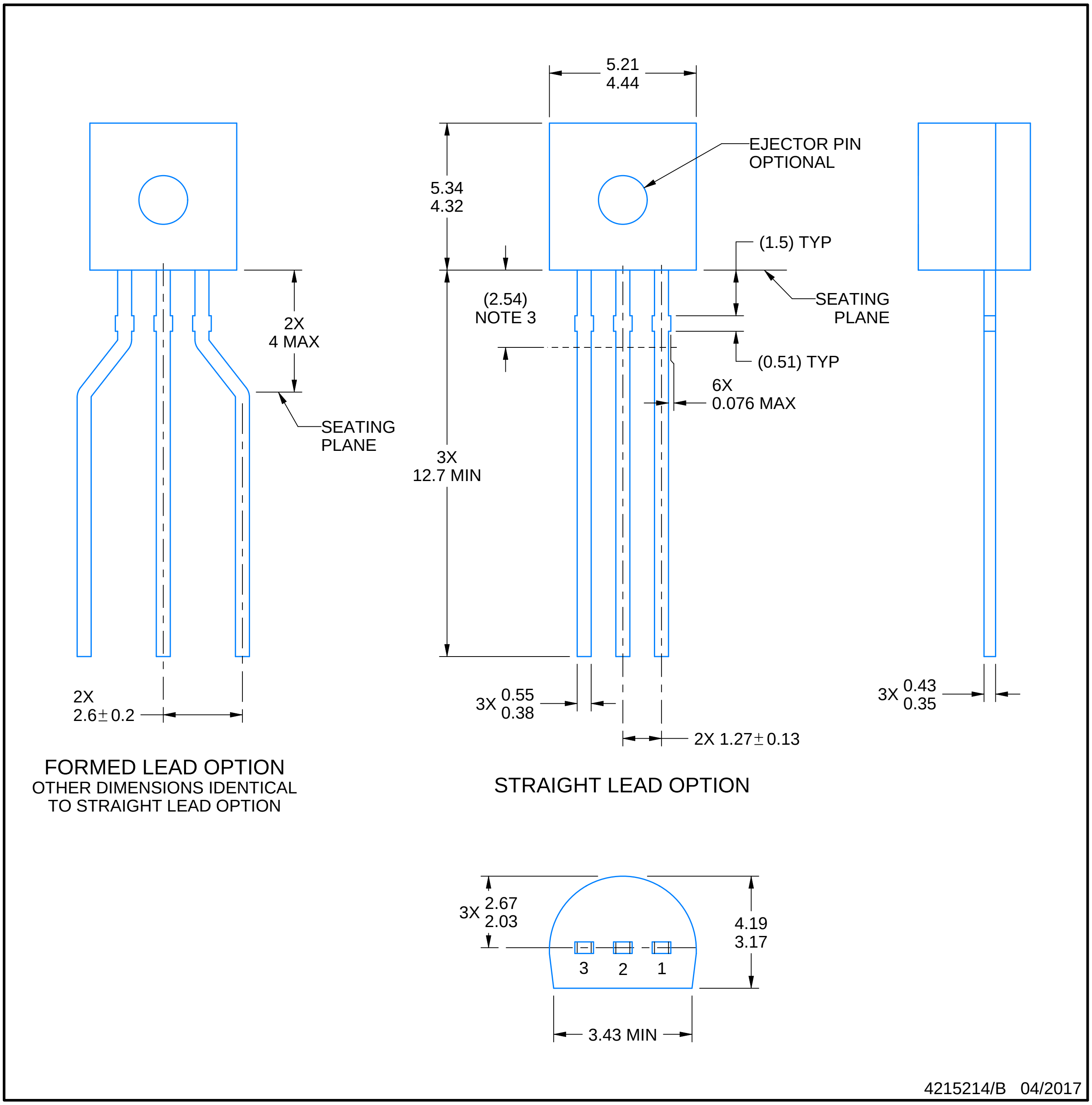
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040001-2/F

PACKAGE OUTLINE

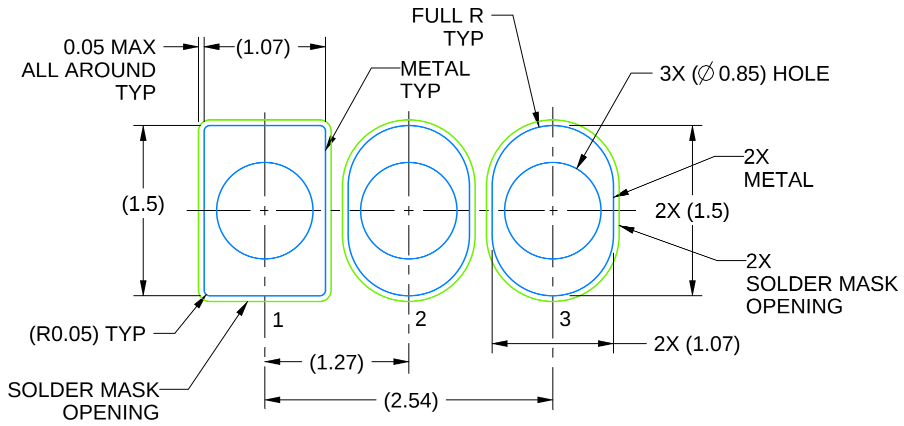
TO-92 - 5.34 mm max height

TO-92

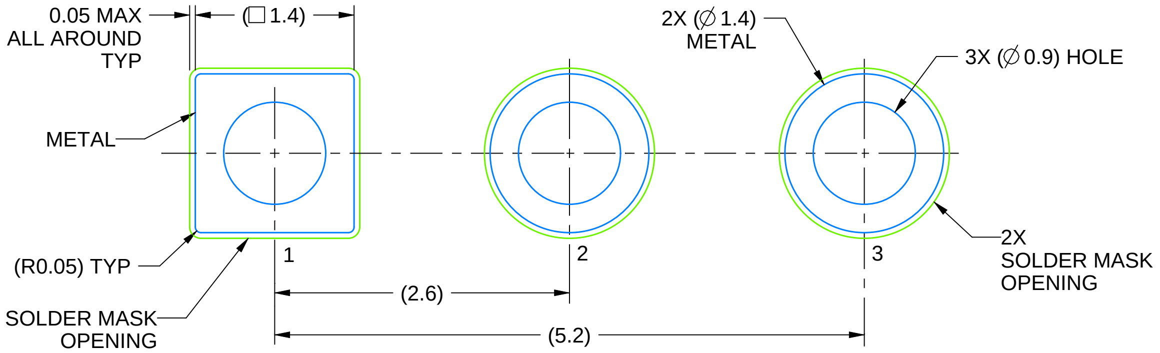


NOTES:

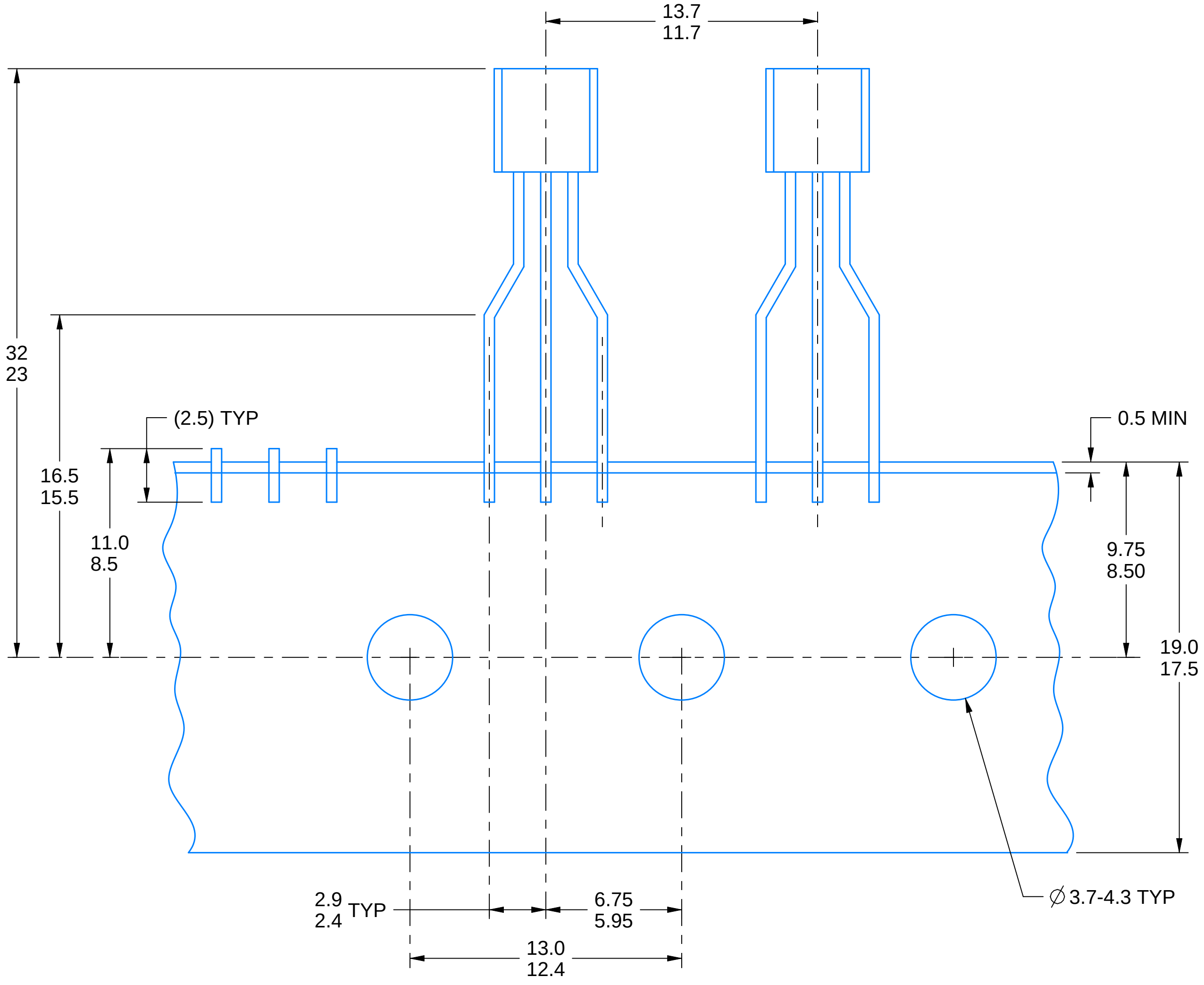
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

IMPORTANT NOTICE AND DISCLAIMER

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

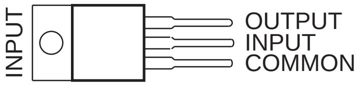
µA7900 SERIES
NEGATIVE-VOLTAGE REGULATORS

SLVS058H – JUNE 1976 – REVISED NOVEMBER 2006

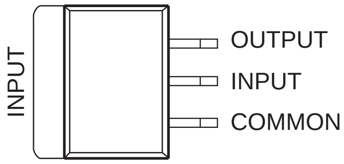
FEATURES

- **3-Terminal Regulators**
- **Output Current up to 1.5 A**
- **No External Components**
- **Internal Thermal-Overload Protection**
- **High Power-Dissipation Capability**
- **Internal Short-Circuit Current Limiting**
- **Output Transistor Safe-Area Compensation**

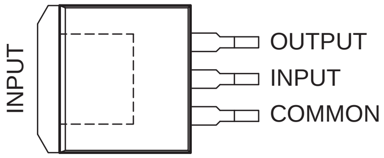
KCS (TO-220) PACKAGE
(TOP VIEW)



KTE (PowerFLEX™) PACKAGE
(TOP VIEW)



KTT (TO-263) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

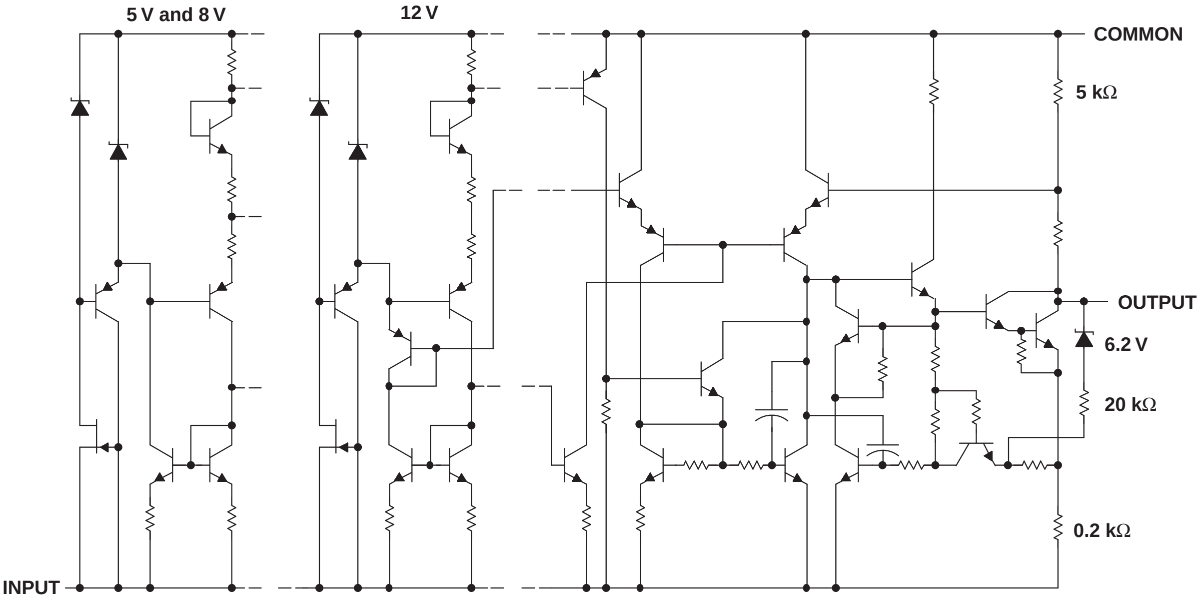
This series of fixed-negative-voltage integrated-circuit voltage regulators is designed to complement Series µA7900 in a wide range of applications. These applications include on-card regulation for elimination of noise and distribution problems associated with single-point regulation. Each of these regulators can deliver up to 1.5 A of output current. The internal current limiting and thermal shutdown features of these regulators essentially make them immune to overload. In addition to use as fixed-voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power-pass element in precision regulators.

ORDERING INFORMATION(1)

T_J	$V_{O(NOM)}$	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	–12 V	TO-220, short shoulder – KCS	Tube of 50	UA7912CKCS	UA7912C
	–8 V	PowerFLEX™ – KTE	Reel of 2000	UA7908CKTER	UA7908C
		TO-220, short shoulder – KCS	Tube of 50	UA7908CKCS	UA7908C
	–5 V	PowerFLEX – KTE	Reel of 2000	UA7905CKTER	UA7905C
		TO-220, short shoulder – KCS	Tube of 50	UA7905CKCS	UA7905C
		TO-263 – KTT	Reel of 500	UA7905CKTTR	UA7905C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

SCHEMATIC



All component values are nominal.

Absolute Maximum Ratings(1)

over virtual junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage		–35	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Package Thermal Data(1)

PACKAGE	BOARD	θ_{JA}	θ_{JC}	θ_{JP}(2)
PowerFLEX (KTE)	High K, JESD 51-5	23°C/W	3°C/W	2.7°C/W
TO-220 (KCS)	High K, JESD 51-5	19°C/W	17°C/W	3°C/W
TO-263 (KTT)	High K, JESD 51-5	25.3°C/W	18°C/W	1.94°C/W

(1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

(2) For packages with exposed thermal pads, such as QFN, PowerPAD™, or PowerFLEX, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_I	Input voltage	μA7905	–7	–25	V
		μA7908	–10.5	–25	
		μA7912	–14.5	–30	
I_O	Output current			1.5	A
T_J	Operating virtual junction temperature		0	125	°C

uA7905 Electrical Characteristics

at specified virtual junction temperature, V_I = –10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	µA7905C			UNIT
			MIN	TYP	MAX	
Output voltage (2)	I_O = 5 mA to 1 A, V_I = –7 V to –20 V, $P_D \le 15$ W	25°C	–4.8	–5	–5.2	V
		0°C to 125°C	–4.75		–5.25	
Input regulation	V_I = –7 V to –25 V			12.5	50	mV
	V_I = –8 V to –12 V			4	15	
Ripple rejection	V_I = –8 V to –12 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A			15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–0.4		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		125		µV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = –7 V to –25 V			0.15	0.5	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output.

(2) This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7908 Electrical Characteristics

at specified virtual junction temperature, V_I = –14 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	µA7908C			UNIT
			MIN	TYP	MAX	
Output voltage (2)	I_O = 5 mA to 1 A, V_I = –10.5 V to –23 V, $P_D \le 15$ W	25°C	–7.7	–8	–8.3	V
		0°C to 125°C	–7.6		–8.4	
Input regulation	V_I = –10.5 V to –25 V			12.5	160	mV
	V_I = –11 V to –17 V			4	80	
Ripple rejection	V_I = –11.5 V to –21.5 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A			15	160	mV
	I_O = 250 mA to 750 mA			5	80	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–0.6		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		200		µV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		1.5	2	mA
Bias current change	V_I = –10.5 V to –25 V			0.15	1	mA
	I_O = 5 mA to 1 A			0.08	0.5	
Peak output current		25°C		2.1		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-µF capacitor across the input and a 1-µF capacitor across the output.

(2) This specification applies only for dc power dissipation permitted by absolute maximum ratings.

uA7912 Electrical Characteristics

at specified virtual junction temperature, V_I = –19 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J (1)	μA7912C			UNIT
			MIN	TYP	MAX	
Output voltage (2)	I_O = 5 mA to 1 A, V_I = –14.5 V to –27 V, $P_D \leq$ 15 W	25°C	–11.5	–12	–12.5	V
		0°C to 125°C	–11.4		–12.6	
Input regulation	V_I = –14.5 V to –25 V			5	80	mV
	V_I = –16 V to –22 V			3	30	
Ripple rejection	V_I = –15 V to –25 V, f = 120 Hz	0°C to 125°C	54	60		dB
Output regulation	I_O = 5 mA to 1.5 A			15	200	mV
	I_O = 250 mA to 750 mA			5	75	
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–0.8		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		300		μV
Dropout voltage	I_O = 1 A	25°C		1.1		V
Bias current		25°C		2	3	mA
Bias current change	V_I = –14.5 V to –25 V			0.04	0.5	mA
	I_O = 5 mA to 1 A			0.06	0.5	
Peak output current		25°C		2.1		A

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 2-μF capacitor across the input and a 1-μF capacitor across the output.

(2) This specification applies only for dc power dissipation permitted by absolute maximum ratings.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA7905CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7905C	Samples
UA7905CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7905C	Samples
UA7905CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	0 to 125	UA7905C	Samples
UA7908CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7908C	Samples
UA7908CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 125	UA7908C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

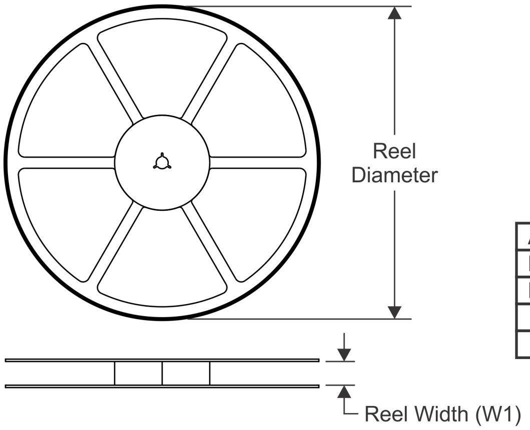
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

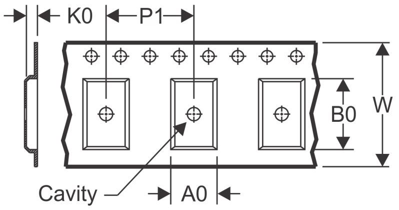
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

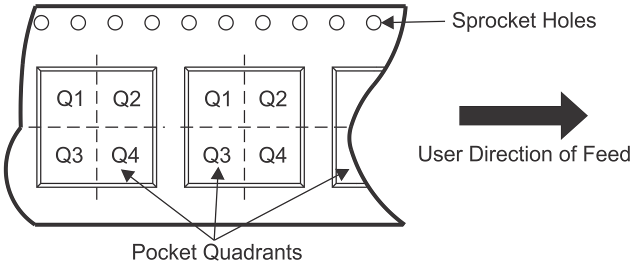


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

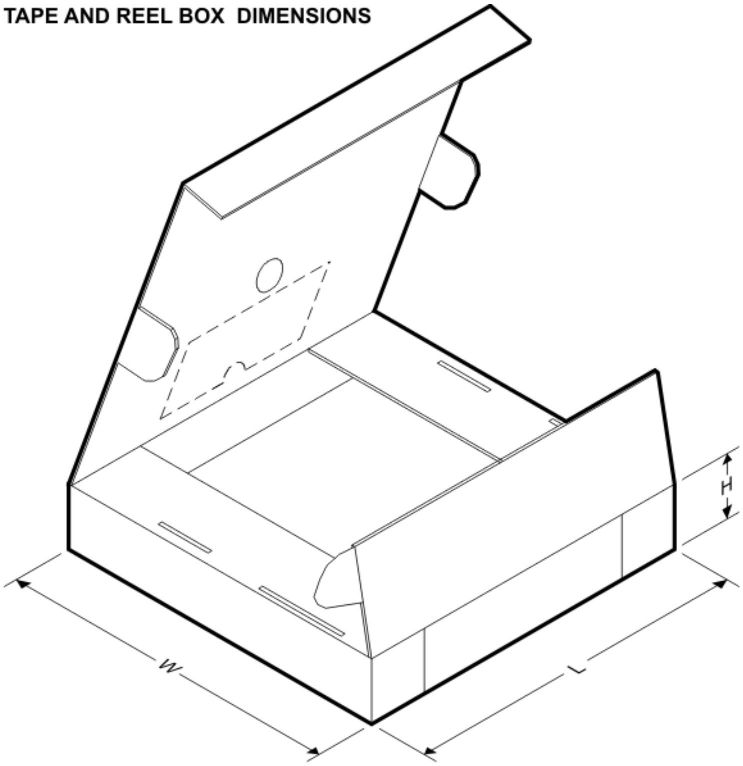
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA7905CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

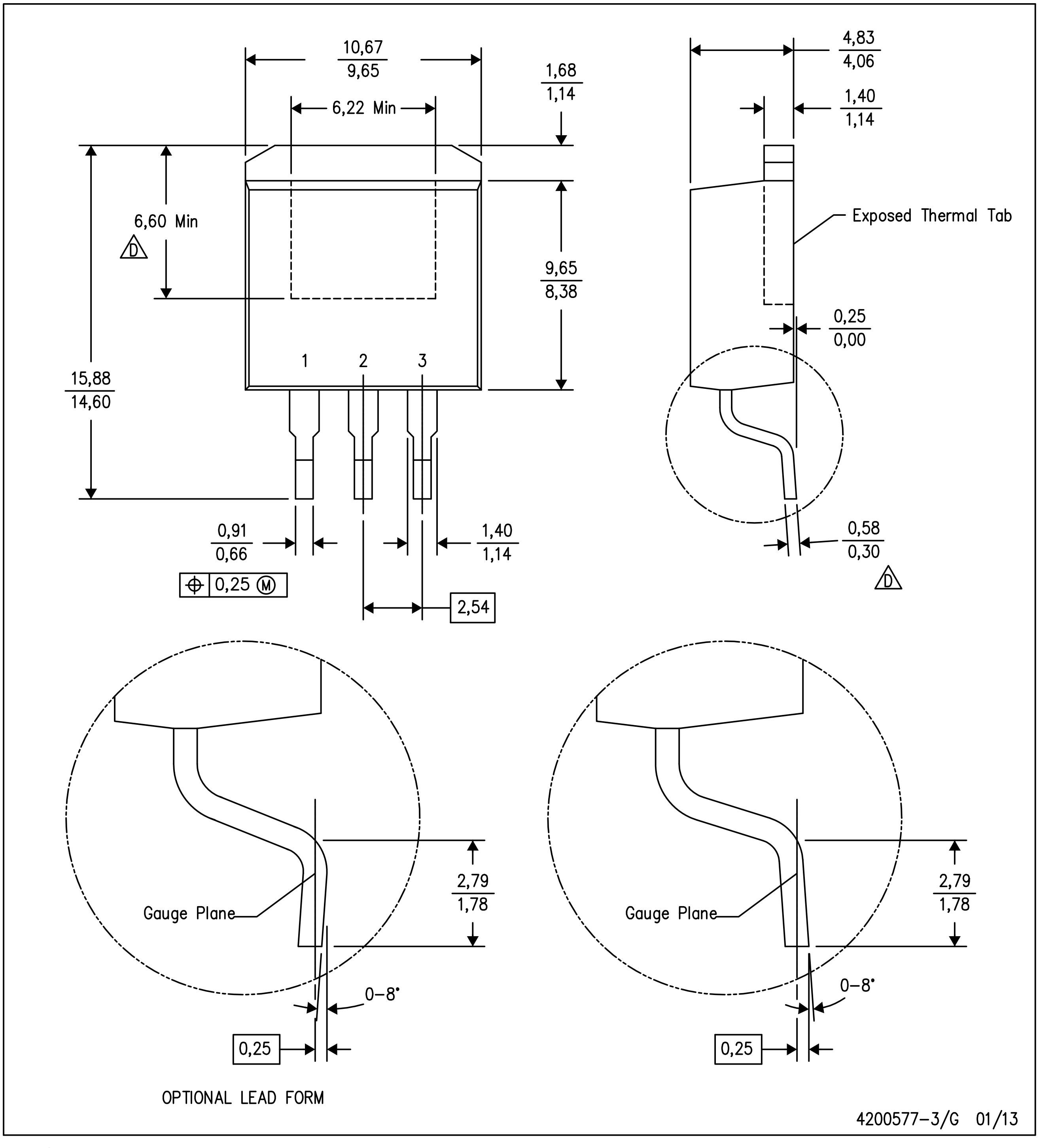
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

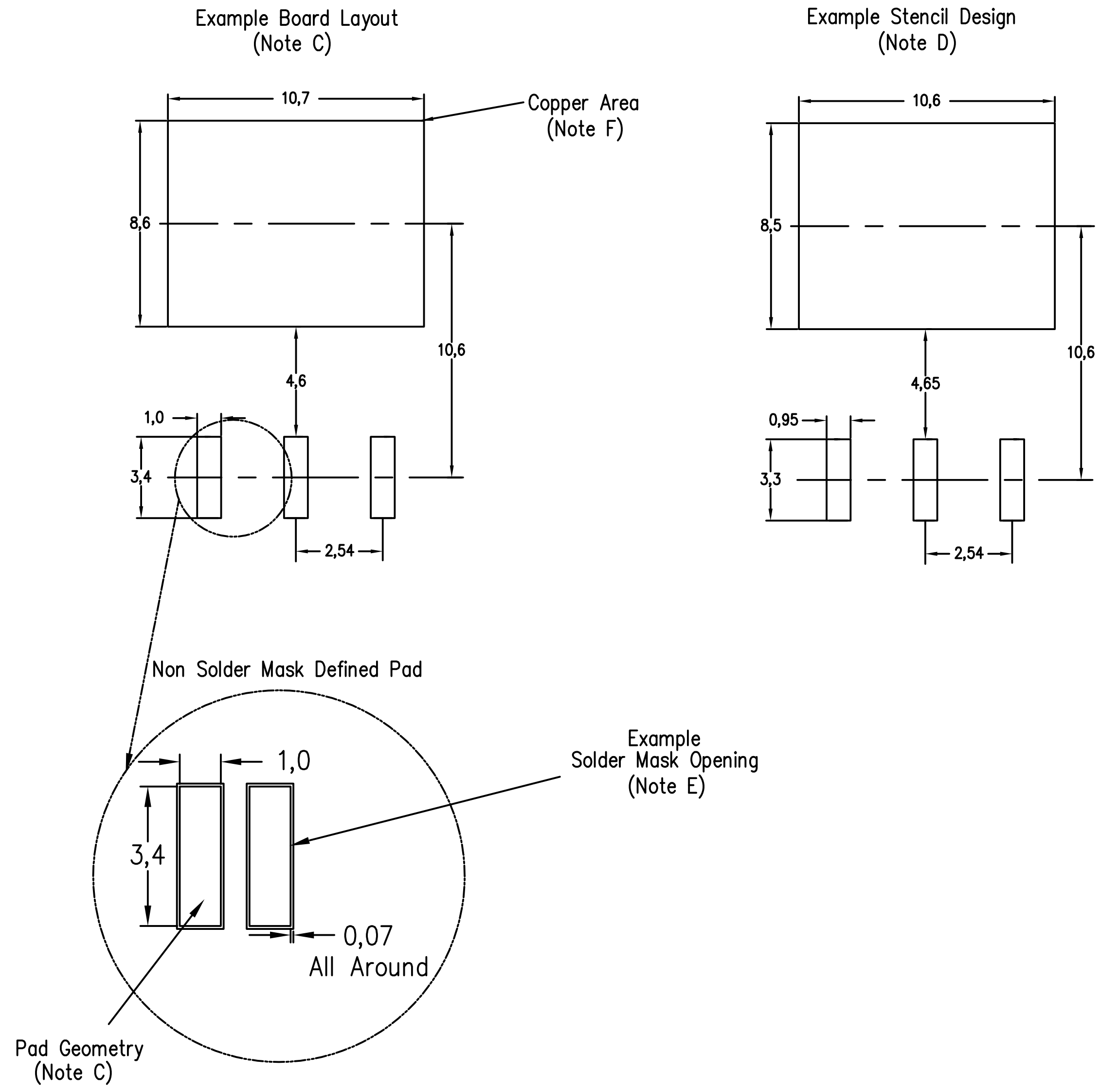
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA7905CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



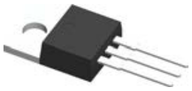
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



4208208–2/C 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–SM–782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

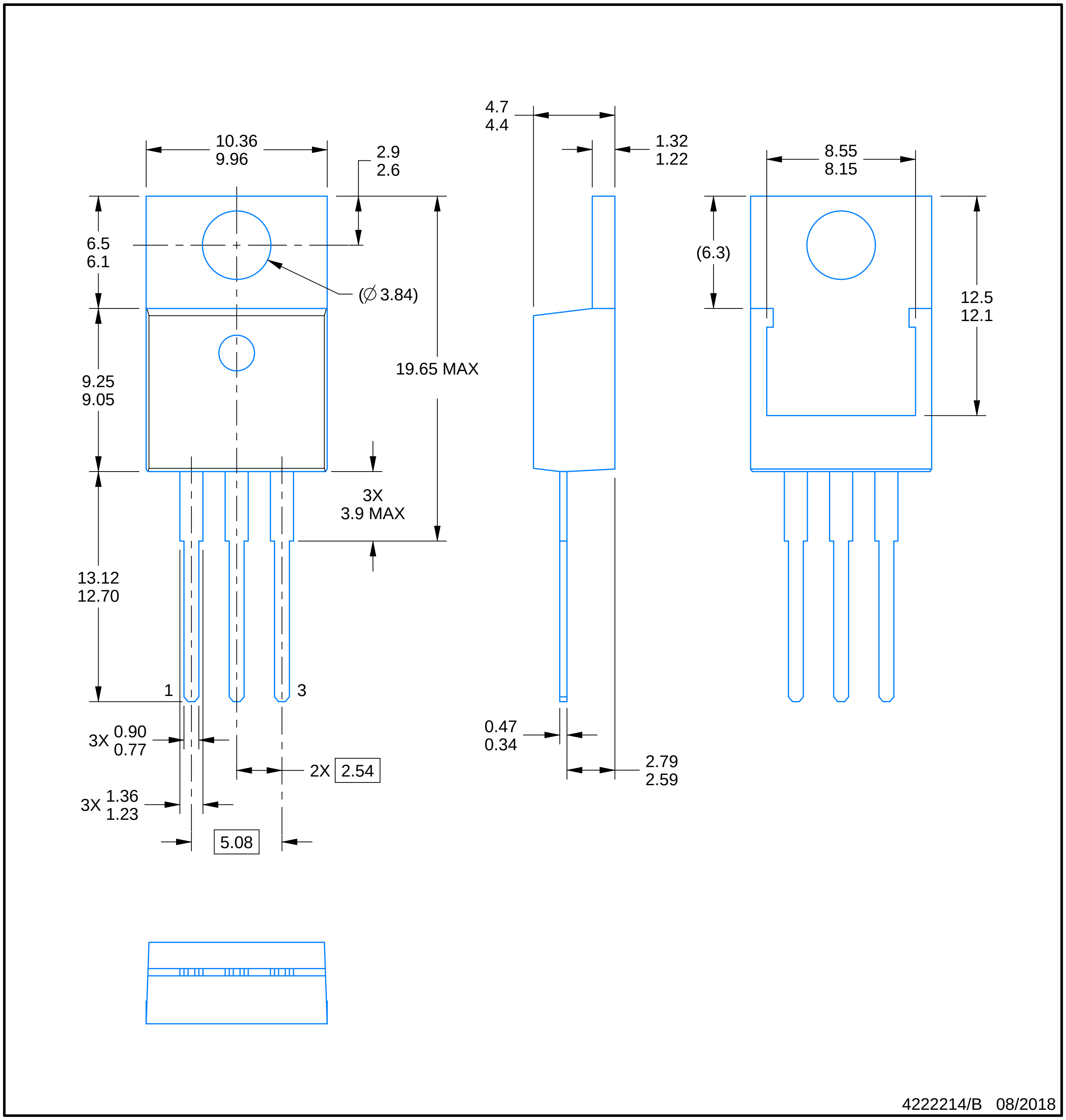


PACKAGE OUTLINE

KCS0003B

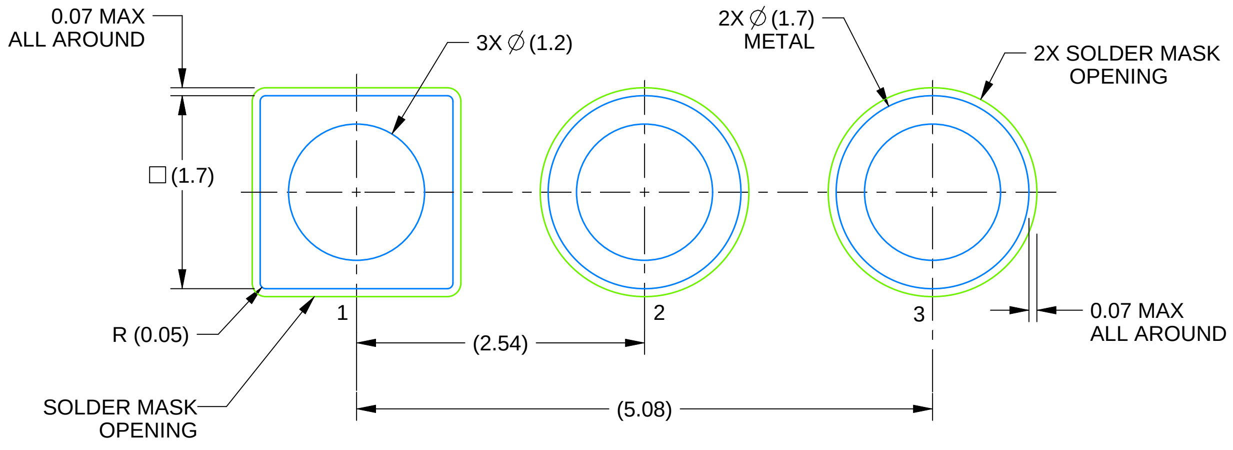
TO-220 - 19.65 mm max height

TO-220



NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

IMPORTANT NOTICE AND DISCLAIMER

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265