NI 5781R User Guide and Specifications

This document contains installation instructions, configuration information, and specifications for the National Instruments 5781R, comprised of an NI FlexRIO FPGA module and an NI 5781 FlexRIO adapter module. This document also contains tutorial sections that demonstrate how to generate and acquire data using a LabVIEW FPGA example VI and how to create and run your own LabVIEW project with the NI 5781R.

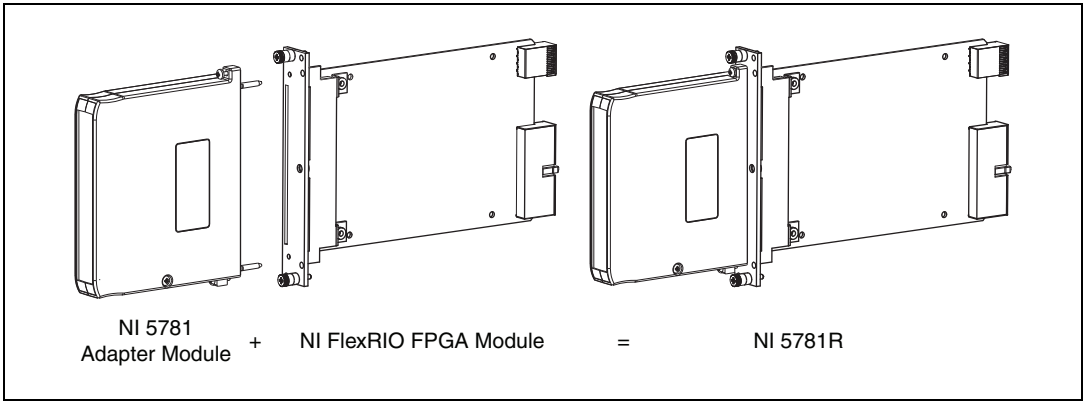

Figure 1. Building the NI 5781R

Caution To avoid permanent damage to the NI 5781, disconnect all signals connected to the NI 5781 before powering down the module, and only connect signals after the module has been powered on by the NI FlexRIO FPGA module.

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NATIONAL INSTRUMENTS

Required Components

The following items are necessary to set up and use the NI 5781R:

- ❑ The following NI FlexRIO hardware:
  - NI FlexRIO FPGA module
  - NI 5781 FlexRIO adapter module
- ❑ The following software packages:
  - LabVIEW
  - LabVIEW FPGA Module
  - NI-RIO device drivers
  - NI FlexRIO Adapter Module Support
  - (Optional) LabVIEW Real-Time Module

  Refer to *Step 1. Install Application Software and Driver* for information about NI FlexRIO software support.
- ❑ PXI/CompactPCI or PXI Express/CompactPCI Express chassis with PXI/CompactPCI or PXI Express/CompactPCI Express embedded controller, or MXI kit and a PC, running Windows 7/Vista/2000 or Windows XP Professional.
- ❑ At least one cable for connecting signals to and from the NI 5781R. For a list of applicable cables and accessories, refer to the *Connectivity Options* section.

Step 1. Install Application Software and Driver

Before installing the NI 5781R, you must install the application software and device driver. Visit `ni.com/info` and enter `rdsoftwareversion` to determine which minimum versions of software you need for your device.

Refer to the *LabVIEW Release Notes* for installation instructions for LabVIEW and system requirements for the LabVIEW software. Refer to the *LabVIEW Upgrade Notes* for additional information about upgrading to the most recent version of LabVIEW for Windows.

Refer to the *LabVIEW FPGA Module Release and Upgrade Notes* for installation instructions and information about getting started with the LabVIEW FPGA Module.

Refer to the *LabVIEW Real-Time Module Release and Upgrade Notes* for system requirements, installation instructions, and additional information about using the LabVIEW Real-Time Module.

Refer to the *NI-RIO Readme* on NI-RIO installation media for system requirements and installation instructions for the NI-RIO driver.

Refer to the *NI FlexRIO Adapter Module Support Readme* on NI FlexRIO Adapter Module Support installation media for system requirements and installation instructions.

The LabVIEW documents are available from `ni.com/manuals`. In LabVIEW, you can also view the LabVIEW Manuals directory that contains these documents by selecting **Start»All Programs» National Instruments»LabVIEW»LabVIEW Manuals**.

Step 2. Install the NI 5781R

This section describes how to unpack and install the NI FlexRIO FPGA module and the NI 5781.

Note You *must* install LabVIEW, the LabVIEW FPGA Module, NI-RIO, and NI FlexRIO Adapter Module Support before installing the NI 5781R.

Unpacking

The NI FlexRIO FPGA module and the NI 5781 are shipped in antistatic packages to prevent electrostatic discharge from damaging device components. To prevent such damage when handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object, such as your computer chassis.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Caution *Never* touch the exposed pins of connectors.

Remove the device from the package and inspect the devices for loose components or any other sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into the chassis.

Store the NI FlexRIO FPGA module and NI 5781 in the antistatic envelopes when not in use.

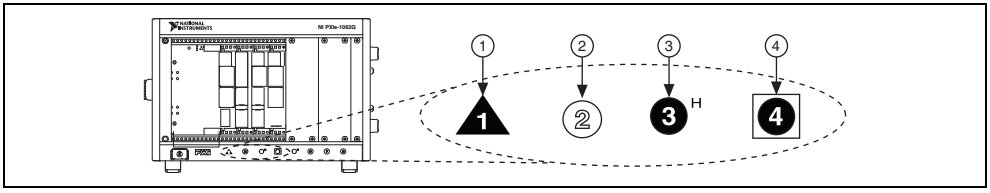
Installing the NI FlexRIO FPGA Module

Complete the following steps to install an NI FlexRIO FPGA module:

Note You must install the software before installing the hardware. For software installation information, refer to *Step 1. Install Application Software and Driver*.

Caution Refer to the *Read Me First: Safety and Electromagnetic Compatibility* document packaged with your PXI chassis or device before removing equipment covers or connecting or disconnecting any signal wires.

1. Power off and unplug the PXI/PXI Express chassis. Refer to your chassis manual to install or configure the chassis.
2. Identify a supported PXI/PXI Express slot in the chassis. Figure 2 shows the symbols that indicate the slot types for a PXI/PXI Express chassis.

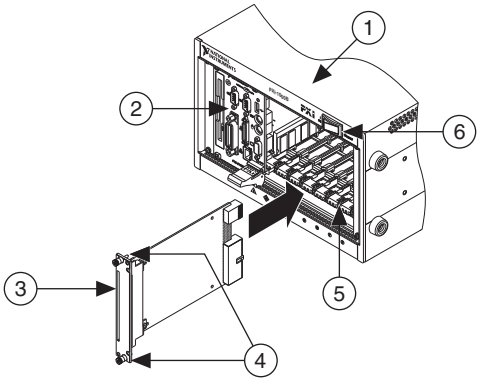


1	PXI Express System Controller Slot	3	PXI Express Hybrid Peripheral Slot
2	PXI Peripheral Slot	4	PXI Express System Timing Slot

Figure 2. Symbols for PXI Express/PXI Express Hybrid/PXI Slots

If you are using a PXI Express chassis, you can place PXI devices in the PXI slots. If a PXI device is hybrid slot compatible, you can use the PXI Express Hybrid slots. PXI Express devices can be placed only in PXI Express slots and PXI Express Hybrid slots. Refer to the chassis documentation for details.

3. Remove the filler panel of an unused PXI/PXI Express slot.
4. Touch any metal part of the chassis to discharge any static electricity.
5. Place the PXI/PXI Express module edges into the module guides at the top and bottom of the chassis, as shown in Figure 3.



1	PXI/PXI Express Chassis	4	Front-Panel Mounting Screws
2	PXI/PXI Express System Controller	5	Module Guides
3	NI FlexRIO FPGA Module	6	Power Switch

Figure 3. Installing an NI FlexRIO FPGA Module in the PXI/PXI Express Chassis

6. Secure the device front panel to the chassis front panel mounting rail using the front-panel mounting screws.
7. Plug in and power on the PXI/PXI Express chassis.

Confirming That the Device Is Recognized

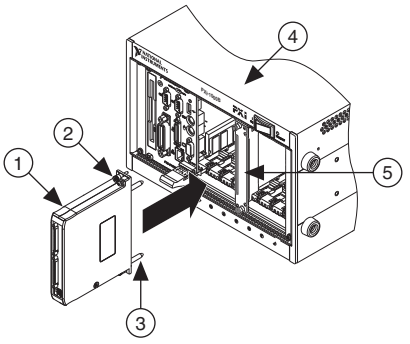
To confirm that your device is recognized, complete the following steps:

1. Select **Start»All Programs»National Instruments»Measurement & Automation** to open Measurement & Automation Explorer (MAX).
2. Expand **Devices and Interfaces**.
3. Verify that the device appears under **Devices and Interfaces»RIO Devices**.

Installing the NI 5781

Complete the following steps to connect the NI 5781 FlexRIO adapter module to the NI FlexRIO FPGA module.

1. Gently insert the guide pins and the high-density card edge of the NI 5781 into the corresponding connectors of the NI FlexRIO FPGA module, as shown in Figure 4. The connection may be tight, but do not force the adapter module into place.



1	NI 5781 FlexRIO Adapter Module	4	PXI/PXI Express Chassis
2	Captive Screw	5	NI FlexRIO FPGA Module
3	Guide Pin		

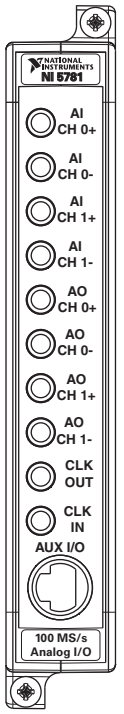
Figure 4. Installing the NI 5781

2. Tighten the captive screws on the NI 5781 to secure it to the NI FlexRIO FPGA module.

Step 3. Connect Signals

Table 1 shows the front panel connector and signal descriptions for the NI 5781 MCX connectors. Refer to the *Specifications* section for additional signal information.

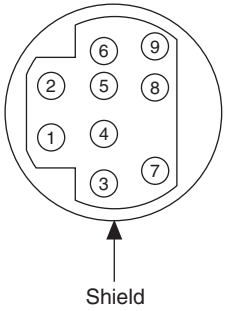
Table 1. NI 5781 Front Panel Connectors

Device Front Panel	Connector	Signal Description
	AI CH 0+	Differential analog input channel 0.
	AI CH 0–	
	AI CH 1+	Differential analog input channel 1.
	AI CH 1–	
	AO CH 0+	Differential analog output channel 0.
	AO CH 0–	
	AO CH 1+	Differential analog output channel 1.
	AO CH 1–	
	CLK OUT	Provides a clock signal for export.
	CLK IN	Provides the device with an external Sample clock.
	AUX I/O	Refer to Table 2 for the signal listing and descriptions.

Note For EMC compliance, you must install two ferrites per cable, on the 9-pin DIN and CLK OUT cables (NI part number 711849-01 for CLK OUT, and NI part number 711627-01 for the 9-pin DIN cable). For best results, snap the ferrites onto the cables as close as possible to the connectors at each end, as shown in the *Attaching Ferrites to Your Cables Note to Users* document included in your kit.

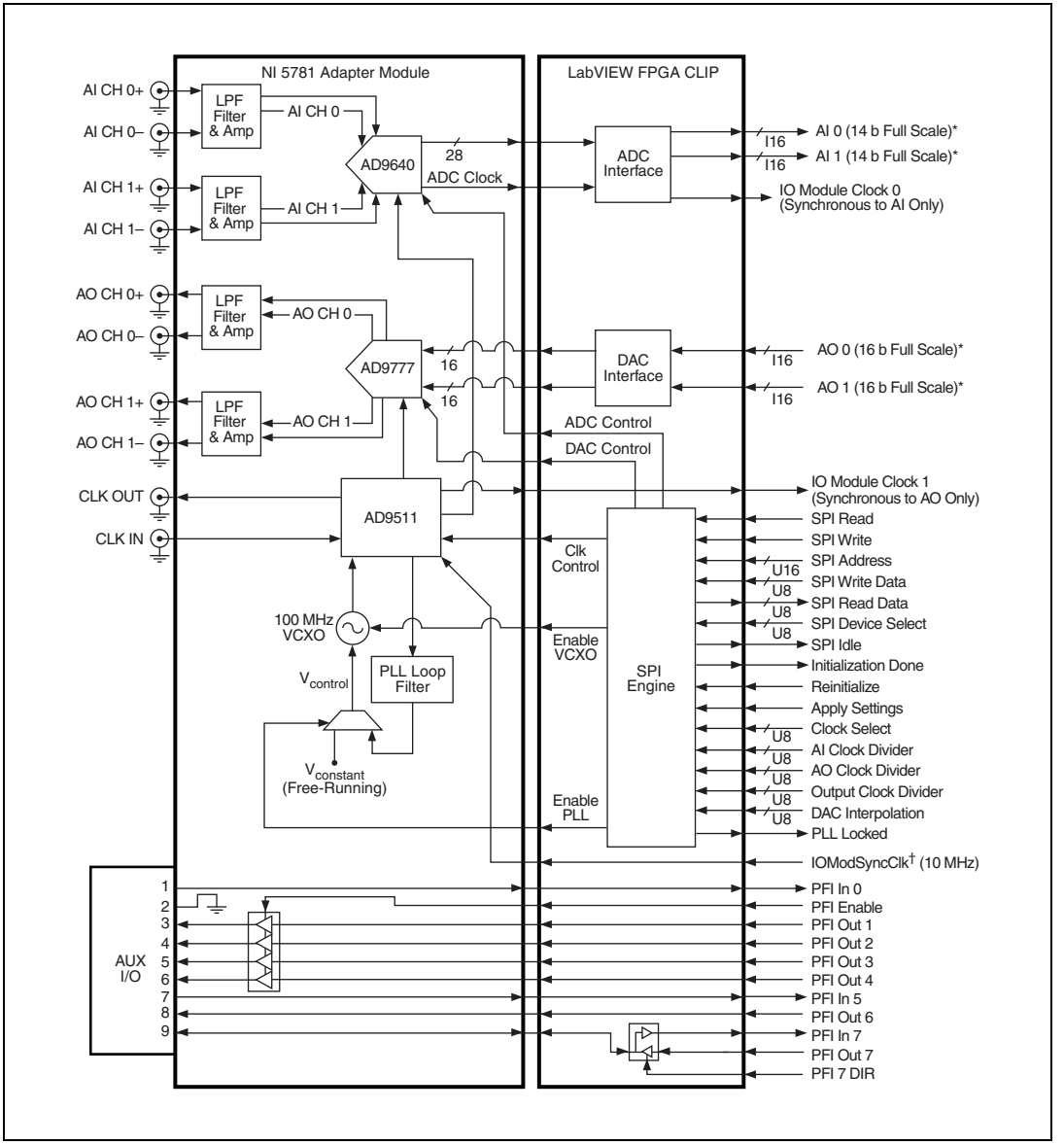
Table 2 shows the pins assignments for the 9-pin DIN connector.

Table 2. NI 5781 AUX I/O Connector Pin Assignments

9-Pin AUX Connector	Pin	Signal	Direction	Signal Description
	1	PFI In 0	Input	General-purpose input
	2	GND	—	Ground potential
	3	PFI Out 1	Output	General-purpose output
	4	PFI Out 2	Output	General-purpose output
	5	PFI Out 3	Output	General-purpose output
	6	PFI Out 4	Output	General-purpose output (I^2C capable, SCL)
	7	PFI In 5	Input	General-purpose input
	8	PFI Out 6	Output	General-purpose output
	9	PFI In 7/ PFI Out 7	Bidirectional	General-purpose input/output (I^2C capable, SDA)
	Shield	GND	—	Ground potential

Caution Connections that exceed any of the maximum ratings of any connector on the NI 5781R can damage the device and the chassis. NI is *not* liable for any damage resulting from such signal connections. For the maximum input and output ratings for each signal, refer to the *Specifications* section.

Figure 5 shows the NI 5781 signal flow to and from the NI 5781 component-level intellectual property (CLIP) by way of the adapter module and the corresponding NI 5781 CLIP in LabVIEW FPGA.



* ADC full scale is ±8,191. DAC full scale is ±32,767.
† IoModSyncClk is only available on the NI PXIe-796*x*R FlexRIO FPGA module, and it is limited to a 10 MHz clock. This clock can be used only as a Reference clock.

Figure 5. NI 5781 Connector Signals and NI 5781 CLIP Signal Block Diagram

Note AI signals and AO signals must be accessed from within their respective clock domains, IO Module Clock 0 (AI) and IO Module Clock 1 (AO).

Connectivity Options

NI recommends that you use the following cables with the NI 5781R:

- MCX-MCX cable (NI part number 188374)—50 Ω MCX-plug-to-MCX-plug coaxial cable
- MCX-BNC cable (NI part number 188375)—50 Ω MCX-plug-to-BNC-plug coaxial cable
- MCX-SMB cable (NI part number 188376)—50 Ω MCX-plug-to-SMB-plug coaxial cable
- MCX-SMA cable (NI part number 188377)—50 Ω MCX-plug-to-SMA-plug coaxial cable
- MCX 50 Ω termination (NI part number 778831)—MCX 50 Ω termination plug to GND
- SH9MD-AUX cable (NI part number 185258)—9-pin DIN to 9-pin DIN shielded cable

For information about connecting I/O signals, refer to the *Specifications* section.

Sample Clock

The NI 5781 Sample clock controls the sample rate and other timing functions on the device. Table 3 contains information about the possible NI 5781 Sample clock sources.

Table 3. NI 5781 Sample Clock Sources

Source	Frequency	Description
Internal VCXO	100 MHz fixed	The internal VCXO can be used as a free-running clock or locked to IoModSyncClk using a 200 Hz PLL bandwidth. IoModSyncClk can be provided only by the NI PXIe-796*x*R devices. Refer to *Internal Sample Clock* in the *Specifications* section for more information.
CLK IN	20 MHz to 100 MHz	An external clock can be provided through the CLK IN front panel connector. This clock can only be used as a Sample clock and cannot be used as a Reference clock. Refer to *CLK IN* in the *Specifications* section for more requirements.

The NI 5781 Sample clock is distributed to three sections of the adapter module for correct operation. These sections are shown in the following table.

Table 4. NI 5781 Sample Clock Distribution

Destination	Frequency (*f = Sample clock/N, where N = 1, 2 × M*)	Description
AI Clock*	*M* = <1..5>	This clock sets the data and Sample clock rates of the analog input (IO Module Clock 0).
AO Clock*	*M* = <1..5>	This clock sets the data rate of the analog output (IO Module Clock 1). The actual AO Sample clock rate is dependent on the interpolation factor.
CLK OUT	*M* = <1..16>	This clock provides a clock signal for export.
* When using CLK IN as the Sample clock, AI clock, and AO clock frequencies must be kept between 20 MHz and 100 MHz. **Note**: *N* is independently selected for each clock destination.		

The AO on the NI 5781 has a selectable interpolation of 1×, 2×, 4×, or 8×. The AO interpolated sample rate must be less than or equal to 400 megasamples/second (MS/s) to satisfy the following equation:

$$AO\ interpolated\ sample\ rate = AO\ data\ rate \times Interpolation\ factor$$

The AO data rate must match the AO clock rate (IO Module Clock 1). By default, the NI 5781 AO runs at 400 MS/s, (which is 100 MHz VCXO × 4× interpolation factor).

Step 4. Use Your NI 5781R with a LabVIEW FPGA Example VI

The NI FlexRIO Adapter Module Support installation includes a variety of example projects to help get you started creating your LabVIEW FPGA program. This section demonstrates how to use an existing LabVIEW FPGA example project to generate and acquire samples with the NI 5781R. This example requires four MCX-MCX cables (NI part number 188374) or equivalent cables to connect the AO lines to the AI lines.

Note Examples available for your device are dependent on the device-specific minimum software requirements. For more information about software requirements for your device, refer to *Step 1. Install Application Software and Driver*.

Each NI 5781R example project includes the following components:

- A LabVIEW FPGA VI that can be compiled and run embedded in FPGA hardware
- A VI that runs in LabVIEW for Windows and interacts with the LabVIEW FPGA VI

Note In NI application software, NI FlexRIO adapter modules are referred to as *IO Modules*.

Complete the following steps to run an example that generates a waveform from AO CH 0 and AO CH 1 and acquires the waveform on AI CH 0 and AI CH 1, respectively.

1. Using the four MCX-MCX cables, make the following connections on the NI 5781R front panel:
   - Connect AO CH0+ to AI CH0+
   - Connect AO CH0– to AI CH0–
   - Connect AO CH1+ to AI CH1+
   - Connect AO CH1– to AI CH1–

2. Launch LabVIEW.
3. In the **Getting Started** window, click **Find Examples** to display the NI Example Finder.
4. In the **NI Example Finder** window, select **Hardware Input and Output»FlexRIO» IO Modules»NI 5781**.
5. Select **NI 5781 Wrapback.lvproj**.
6. In the **Project Explorer** window, open **NI 5781 Wrapback (Host).vi** under **My Computer**. The host VI opens. This VI uses the NI 7952R as the FPGA target by default. If you are using an NI FlexRIO FPGA module other than the NI 7952R, complete the following steps to change to an FPGA VI that supports your target.
   a. Select **Window»Show Block Diagram** to open the VI block diagram.
   b. On the block diagram, right-click the Open FPGA VI Reference (PXI-7952R) function and select **Configure Open FPGA VI Reference**.
   c. In the **Configure Open FPGA VI Reference** dialog box, click the **Browse Project** button in the Open VI section.
   d. In the **Select VI** dialog box that opens, expand the tree view for your device, select the VI under your device and click **OK**.
   e. Click **OK** in the **Configure Open FPGA VI Reference** dialog box.
   f. Save the VI.
7. On the front panel, enter appropriate values in the **Resource**, **Output Frequency**, and **Samples Per Trigger** boxes.
8. In the **Resource** box, select a 5781R resource that corresponds with the target configured in step 6.
9. Click the **Run** button to run the VI.
10. Click the **Acquire** button. The VI acquires the number of samples indicated by the **Samples Per Trigger** control and displays the captured waveform on the **Acquired Data** graph. By default, only the first 64 samples are displayed.
11. Click **STOP** to stop the VI.
12. Close the VI.

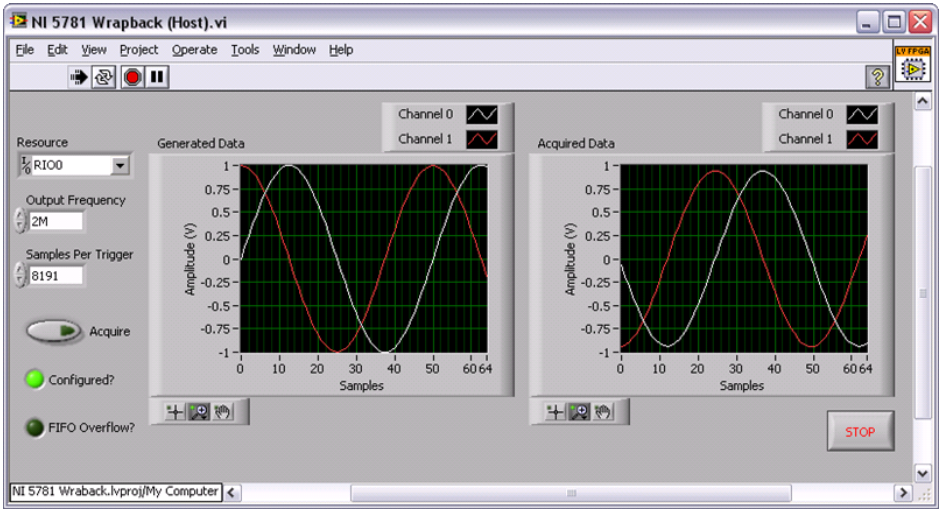


Figure 6. NI 5781 Wrapback (Host) VI Front Panel

Step 5. Create a LabVIEW Project and Run a VI on an FPGA Target

This section demonstrates how to create a LabVIEW project, FPGA VI, and host VI that writes a value to the NI 5781R and reads that value back. This exercise also demonstrates how to compile the FPGA VI onto your target and run a VI on the host machine.

Creating a Project

1. Launch LabVIEW, or if LabVIEW is already running, select **File»New**.
2. In the **New** dialog box, select **Project»Empty Project**. Click **OK**. The new project opens in the **Project Explorer** window.
3. Save the project as `5781SampleGen.lvproj`.

Creating an FPGA Target VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»Targets and Devices**.
2. In the **Add Targets and Devices on My Computer** dialog box, select the **Existing Target or Device** option button and expand the FPGA Target. The target is displayed.
3. Select your device and click **OK**. The target and target properties are loaded into the project tree.
4. In the **Project Explorer** window, expand **FPGA Target (RIO*x*, PXI-79*xx*R)**.
5. Right-click **IO Module** and select **Properties**. In the General category, you can see the available CLIP for the NI 5781 in the Component Level IP pane. If the category information is dimmed, select the **Enable IO Module** checkbox.
6. Select **NI 5781** to use the NI 5781 CLIP reference. Click **OK**.
7. Right-click the FPGA target and select **New»FPGA Base Clock**.
8. In the **Resource** pull-down menu, select **IO Module Clock 0**.
9. Enter `100 MHz` in the **Compile for single frequency** control.
10. Rename the clock and click **OK** to save these settings for this clock. For this example, IO Module Clock 0 is renamed *AI Clock*.
11. Repeat steps 7 through 10 to add IO Module Clock 1. For this example, IO Module Clock 1 is renamed *AO Clock*.

Note The analog input signals (AI 0, AI 1) are synchronous to IO Module Clock 0, and the analog output signals (AO 0, AO 1) are synchronous to IO Module Clock 1. To ensure proper operation, you should only access the AI and AO nodes in their respective clock domains. For more information about CLIP and the signals available for the NI 5781, refer to the *NI 5781 Component-Level Intellectual Property (CLIP)* section. Refer also to the *LabVIEW Help* for more information about using CLIP with the NI 5781.

12. In the **Project Explorer** window, right-click the FPGA target and select **New»VI**. A blank VI opens.
13. Select **Window»Show Block Diagram** to open the VI block diagram.
14. In the **Project Explorer** window, expand the **IO Module (NI 5781 : NI 5781)** tree view.
15. Select **AI 0** and **AO 0** and drag them onto the block diagram.
16. Add a Timed Loop around each of the two nodes.
17. Wire a Control to the input terminal of the **IO Module\AO 0** node.
18. Wire an Indicator from the output terminal of the **IO Module\AI 0** node.
19. Wire an **FPGA Clock Constant** to the input node of each Timed Loop.

20. Click the **FPGA Clock Constant** and select the appropriate clock for each loop from the pull-down menu.

Your block diagram should now resemble the block diagram in Figure 7.

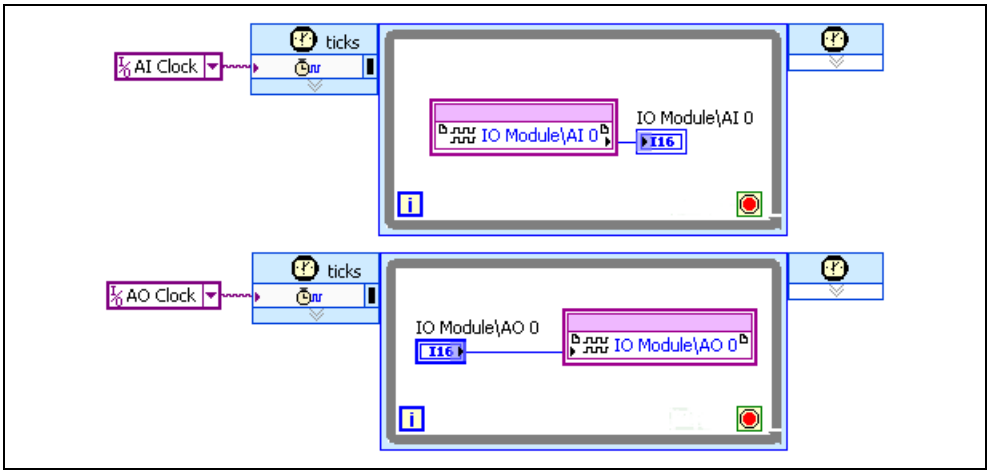


Figure 7. 5781SampleGen (FPGA).vi Block Diagram

Tip Click the **Clean Up Diagram** button on the toolbar to cleanly organize the VI block diagrams.

21. Save the VI as `5781SampleGen(FPGA).vi`.
22. Close the VI.
23. In the Project Explorer window under **My Computer**, expand the tree view for your device, right-click **5781SampleGen (FPGA).vi** and select **Compile** to compile the files for your target.

    The **Generating Intermediate Files** window opens and displays the compilation progress. The **LabVIEW FPGA Compile Server** window opens and runs. The compilation takes several minutes.
24. When the compilation completes, click the **Stop Server** button.
25. Click **Close** in the **Successful Compile Report** window.
26. Save and close the VI.
27. Save the project.

Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»VI**. A blank VI opens. Select **Window»Show Block Diagram** to open the VI block diagram.
2. Add the Open FPGA VI Reference function, located on the **FPGA Interface** palette, to the block diagram.
3. Right-click the Open FPGA VI Reference function, labeled `No Target`, and select **Configure Open FPGA VI Reference**.
4. In the **Configure Open FPGA VI Reference** dialog box, select the **VI** option button.
5. In the **Select VI** window that opens, select **5781SampleGen (FPGA).vi** under your device, and click **OK**.
6. Click **OK** in the **Configure Open FPGA VI Reference** dialog box. The new target name appears under the Open FPGA VI Reference function in the block diagram.

7. Add a While Loop to the block diagram.
8. Right-click the stop condition inside the While Loop and select **Create Control** to create a STOP control on the VI front panel.
9. Add the Read/Write Control function, located on the **FPGA Interface** palette, inside the While Loop.
10. Wire the **FPGA VI Reference Out** indicator of the Open FPGA VI Reference function to the **FPGA VI Reference In** control on the Read/Write Control function.
11. Wire the **error out** indicator of the Open FPGA VI Reference function to the **error in** control of the Read/Write Control function.
12. Configure the Read/Write Control function by clicking the terminal section labeled `Unselected`, and selecting **IO Module/AO 0**.
13. Add the **IO Module/AI 0** I/O item to the Read/Write Control function by clicking the lower edge of the control node with the Positioning tool and dragging the edge down.
14. Wire a control to the input terminal of the **IO Module\AO 0** node.
15. Wire an Indicator from the output terminal of the **IO Module\AI 0** node.
16. Add the Close FPGA VI Reference function, located on the **FPGA Interface** palette, to the right of the While Loop on the block diagram.
17. Wire the **FPGA VI Reference Out** indicator of the Read/Write Control function to the **FPGA VI Reference In** control of the Close FPGA VI Reference function.
18. Wire the **error out** indicator of the Read/Write Control function to the **error in** control of the Close FPGA VI Reference function.

    Your block diagram should now resemble the block diagram in Figure 8.

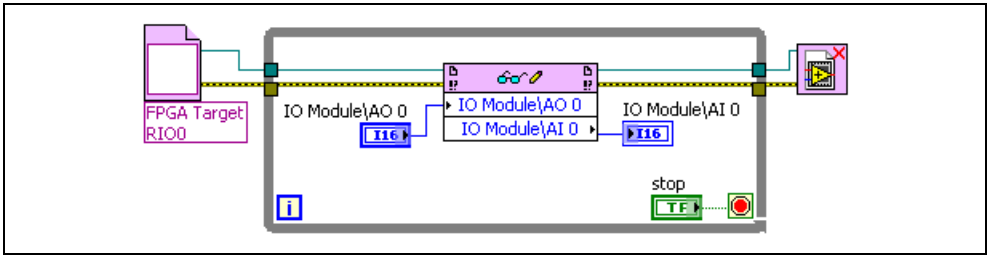


Figure 8. 5781SampleGen(Host).vi Block Diagram

19. Save the VI as `5781SampleGen(Host).vi`.

Running the Host VI

1. Using two MCX-MCX cables, make the following connections on the NI 5781R front panel. If these signals are already connected, proceed to step 2.
   - Connect AO CH0+ to AI CH0+
   - Connect AO CH0– to AI CH0–
2. Open the front panel of `5781SampleGen(Host).vi`.
3. Click the **Run** button to run the VI.
4. Enter a number into the **IO Module\AO 0** control to generate different values to AO CH 0. The IO Module\AI 0 indicator shows the input to AI CH 0. This data value is actively driven onto AI 0 and then read.

Note Full-scale AO data is 16 bits in I16 representation, while full-scale AI data is 14 bits in I16 representation. As a result, the AI indicator displays differently scaled data than the AO control for the same analog signal value.

5. Click the **STOP** button on the front panel and close the VI.

NI 5781 Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes a feature for HDL IP integration called CLIP. NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- User-defined CLIP allows users to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- NI FlexRIO devices also support socketed CLIP, which provides the same IP integration functionality of the user-defined CLIP, while also allowing the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

Figure 9 shows the relationship between an FPGA VI and CLIP.

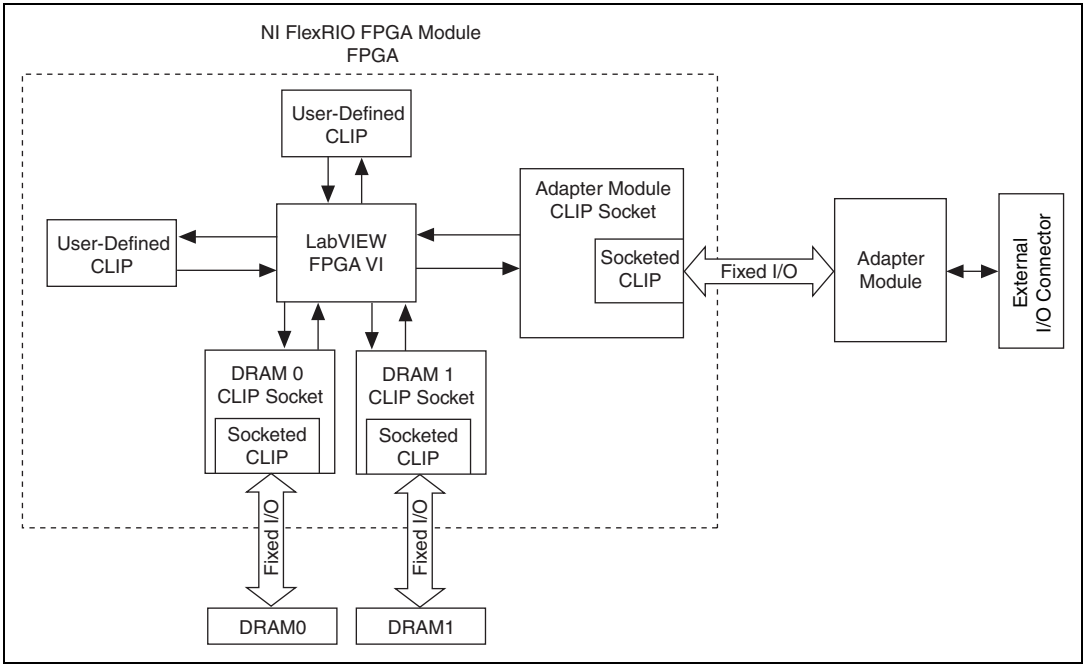


Figure 9. CLIP Relationship

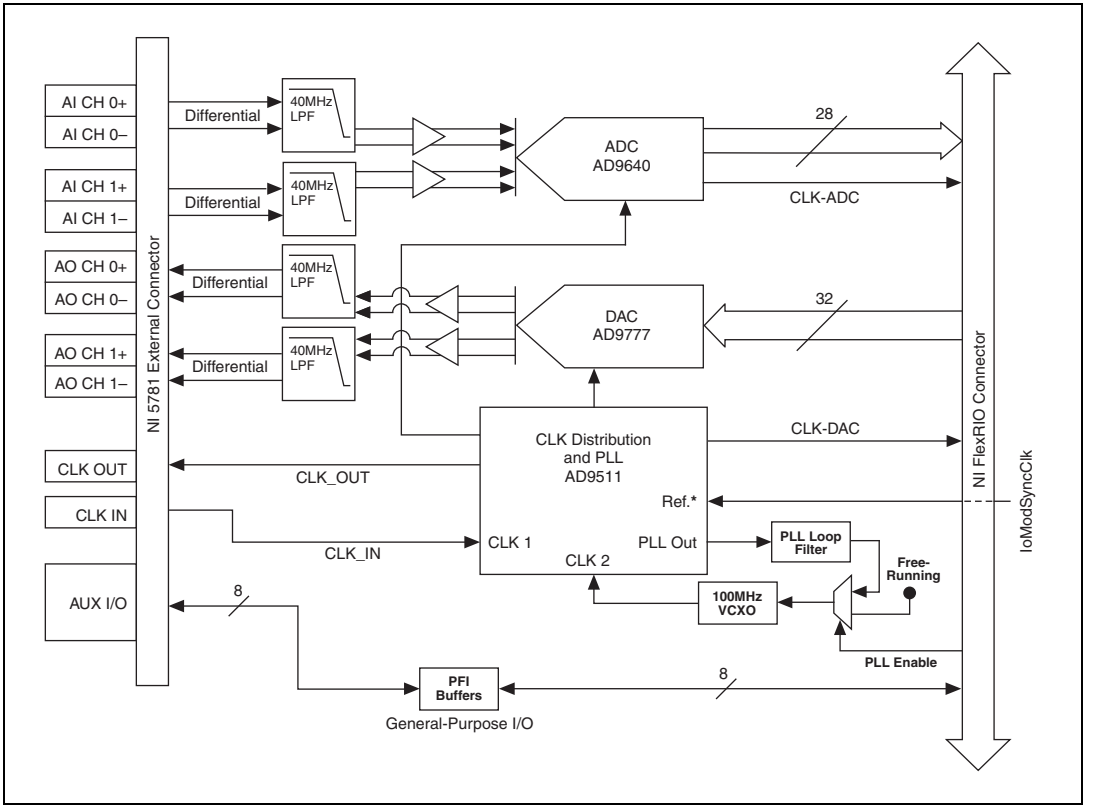
The NI 5781 ships with a socketed CLIP that is used to add module I/O to the LabVIEW project. The NI-developed NI 5781 CLIP provides access to four analog channels, eight PFI lines, one clock output, and an input clock selector. This CLIP also contains an engine to program the ADC, DAC, and clock, either through predetermined settings for an easier instrument setup or through raw SPI Address and Data signals for a more advanced setup.

Refer to the *NI FlexRIO Adapter Module Support* topic of the *LabVIEW Help* for more information regarding NI FlexRIO CLIP, configuring the NI 5781 with a socketed CLIP, and a list of available socketed CLIP and provided signals.

Specifications

This section lists the specifications of the National Instruments 5781 FlexRIO adapter module. Pair these specifications with the *NI FlexRIO FPGA Module Specifications*.

Caution To avoid permanent damage to the NI 5781, disconnect all signals connected to the NI 5781 before powering down the module, and only connect signals after the module has been powered on by the NI FlexRIO FPGA module.



* AD9511 Reference clock can be driven only by the NI PXIe-796*x*R FlexRIO FPGA modules, and it is limited to a 10 MHz clock.

Figure 10. NI 5781 Block Diagram

Typical values describe useful product performance that are not covered by warranty. Typical values cover the expected performance of units over ambient temperature ranges of 23 ±5 °C with a 90% confidence level, based on measurements taken during development or production.

All specifications are typical unless otherwise noted.

Note All graphs depicted in these specifications illustrate the performance of a representative module.

Analog Input (AI CH 0 and AI CH 1)

General Characteristics

Number of channels ..... Two, differential, simultaneously sampled

Connector ..... MCX

Input range (normal operating conditions)

- Differential ..... Fixed 2 V_{pk-pk}
  - Common mode input range ..... ±1 VDC
- Single-ended ..... Fixed 1 V_{pk-pk}

Absolute maximum input ..... ±2 V, per connector

Input impedance ..... 50 Ω, per connector

Input coupling ..... DC

Sample rate

- Internal Sample clock ..... 10 MHz to 100 MHz (100 MHz, default)
- External Sample clock ..... 20 MHz to 100 MHz
- Data rate (IOModClk0) ..... Sample rate

Digital data range ..... ±8,191

ADC part number ..... AD9640/105[1]; 14-bit resolution, dual ADC, multistage, differential pipelined architecture

[1] For additional information on the AD9640, refer to the Analog Devices device data sheet at `www.analog.com`.

Typical Specifications

Filter type.....Fixed 7th-order elliptical

Bandwidth (–3 dB)

Baseband.....40 MHz for each I and Q input

Complex baseband.....80 MHz when used with external I/Q demodulator

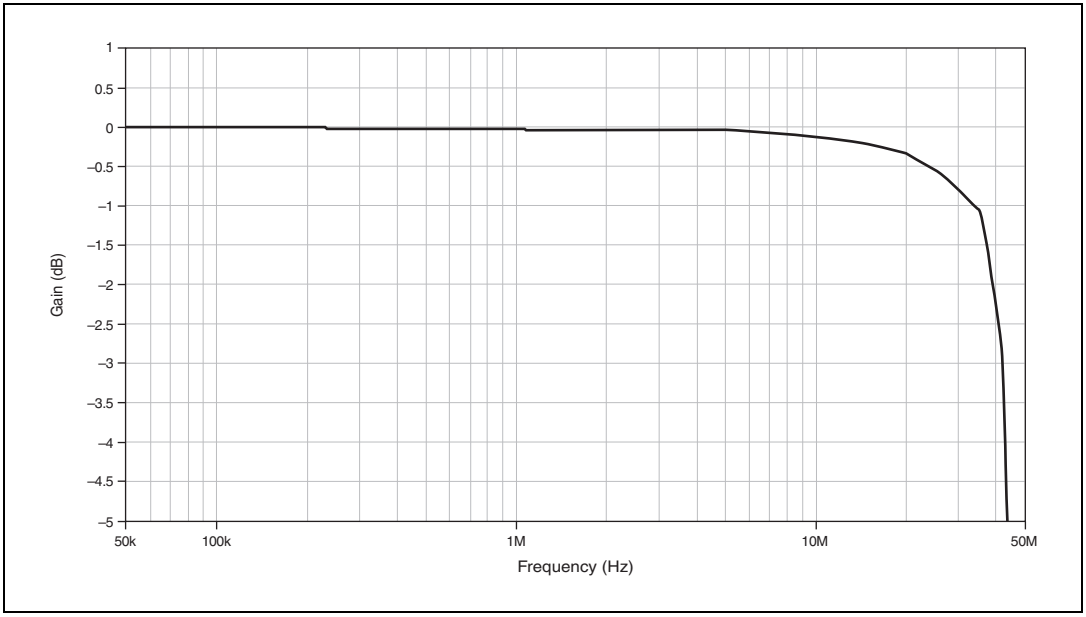


Figure 11. AI Bandwidth (Passband): Single-Ended Acquisition at 100 MS/s, 64 kS, Gain Referenced to Reading at 50 kHz

Spurious-free dynamic range (SFDR) and total harmonic distortion (THD)

The following table shows the SFDR and THD of the analog input with a source generating a differential 5 MHz sine wave at –1 dBFS input amplitude and the NI 5781 acquiring data at 100 MS/s. The SFDR measurement includes aliased and nonaliased harmonics, measured from DC to 50 MHz. The THD measurement includes the 2nd through 6th harmonics.

Generation Frequency (MHz)	SFDR (dBc)	THD (dBc)
5	70	–70

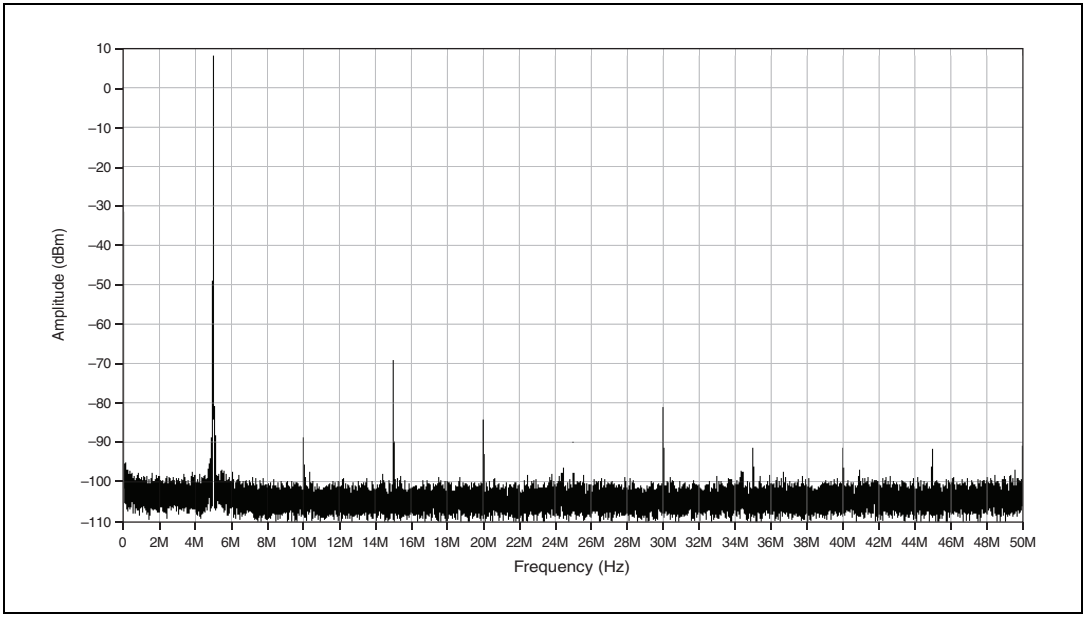


Figure 12. AI SFDR and THD: Differential Acquisition at 100 MS/s, 64 kS, Hanning Window, 10 Averages. Source Generating –1 dBFS Sine Wave at 5 MHz, with 5 MHz Low Pass Filters.

Third-order intermodulation distortion (IMD_3)

Generation Frequency (MHz)	IMD_3 (dBc)
20 and 21	–69

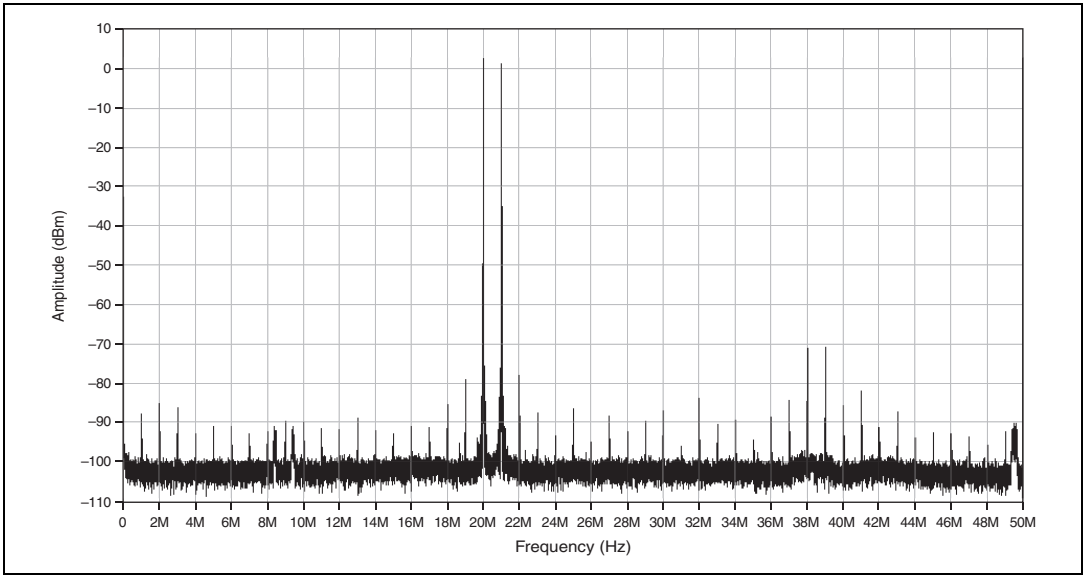


Figure 13. AI IMD_3 (Centered at 20.5 MHz): Differential Acquisition at 100 MS/s, 64 kS, Hanning Window, 10 Averages. Source Generating Two –7 dBFS Sine Tones at 20 MHz and 21 MHz.

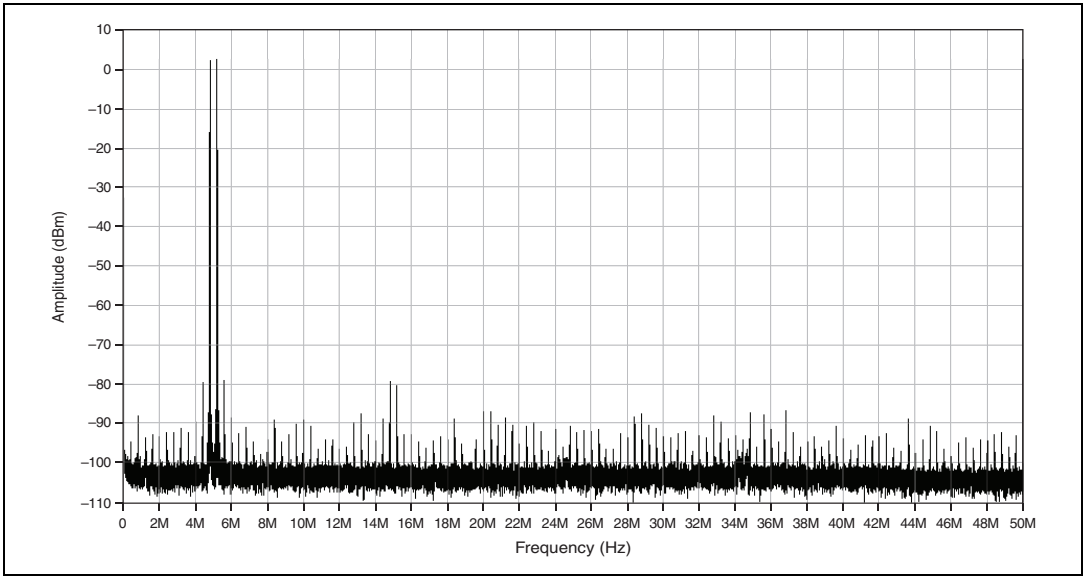


Figure 14. AI IMD_3 (Centered at 5 MHz): Differential Acquisition at 100 MS/s, 64 kS, Hanning Window, 10 Averages. Source Generating Two –7 dBFS Sine Tones at 4.8 MHz and 5.2 MHz.

Average noise density

Differential Amplitude Range		Average Noise Density		
V_{pk-pk}	dBm	$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz
2	10	35	–136	–146
Note: Average noise density from DC to 50 MHz, acquiring at 100 MS/s; inputs grounded through 50 Ω terminations.				

Phase noise density

Offset from Carrier (Hz)	Phase Noise (dBc/Hz)*
100	–114
1 k	–127
10 k	–138
* Measured on a 10 MHz tone using the free-running internal VCXO as the Sample clock. **Note**: The bandwidth of the PLL is 200 Hz when locking to IoModSyncClk.	

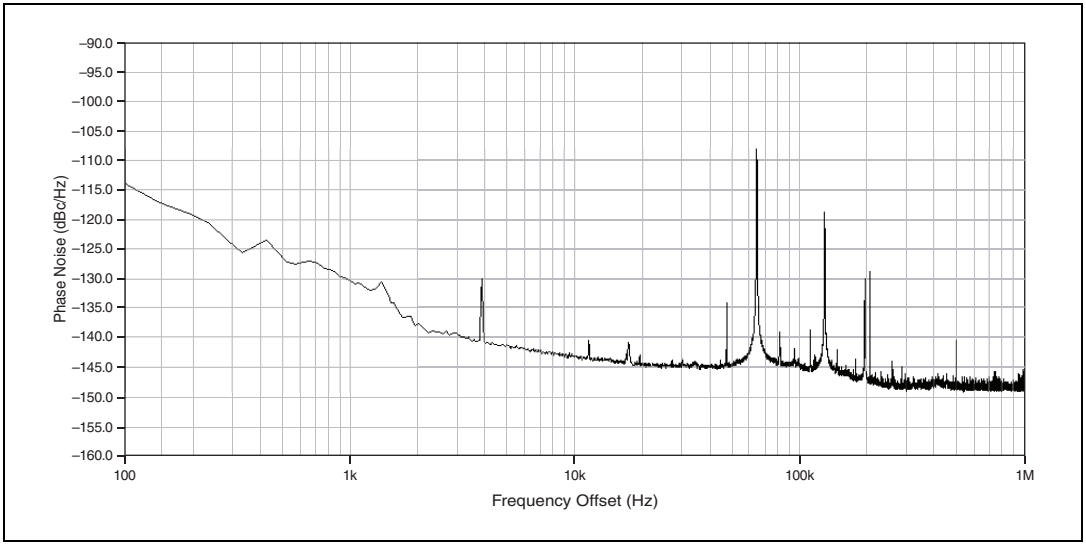


Figure 15. AI Phase Noise: Differential Acquisition at 100 MS/s, 2 MS, Hanning Window, 500 Averages, using Free-Running Internal VCXO as Sample Clock. Source Generating a Differential 10 MHz Tone.

DC absolute accuracy

Gain error.....±3.6% full-scale range (FSR)

Differential offset.....±15 mV

Note DC accuracy measured with a DMM. Differential gain and offset may be adjusted through waveform data. Offset is measured with differential inputs grounded through 50 Ω.

Analog Output (AO CH 0 and AO CH 1)

General Characteristics

Number of channels ..... Two, differential, simultaneously sampled

Connector ..... MCX

Output range

- Differential
  - Into 100 Ω ..... Fixed 2 V_{pk-pk}
  - Into High Z ..... Fixed 4 V_{pk-pk}
  - Common mode output voltage ..... 0 V, not adjustable
- Single-ended[1]
  - Into 50 Ω ..... Fixed 1 V_{pk-pk}
  - Into High Z ..... Fixed 2 V_{pk-pk}

Absolute maximum input ..... ±4 V per connector

Output impedance ..... 50 Ω, per connector

Output coupling ..... DC

Data rate (IOModClk1)

- Internal Sample clock ..... 10 MHz to 100 MHz (100 MHz, default)
- External Sample clock ..... 20 MHz to 100 MHz
- Sample rate ..... AO data rate × Interpolation factor
- Interpolation factors ..... 1×, 2×, 4× (default), 8×
- Maximum sample rate ..... 400 MS/s

Digital data range ..... ±32,767

DAC part number ..... AD9777[2]; 16-bit resolution, dual DAC, selectable interpolation rate

Note Output terminals support waveform summing. The outputs of multiple NI 5781 channels can be connected together.

[1] Both output terminals must be terminated to ground with the same impedance.

[2] For additional information about the AD9777, refer to the Analog Devices device data sheet at `www.analog.com`.

Typical Specifications

Filter type.....Fixed 7th-order elliptical

Bandwidth (–3 dB)

Baseband.....40 MHz for each I and Q output

Complex baseband.....80 MHz when used with external I/Q modulator

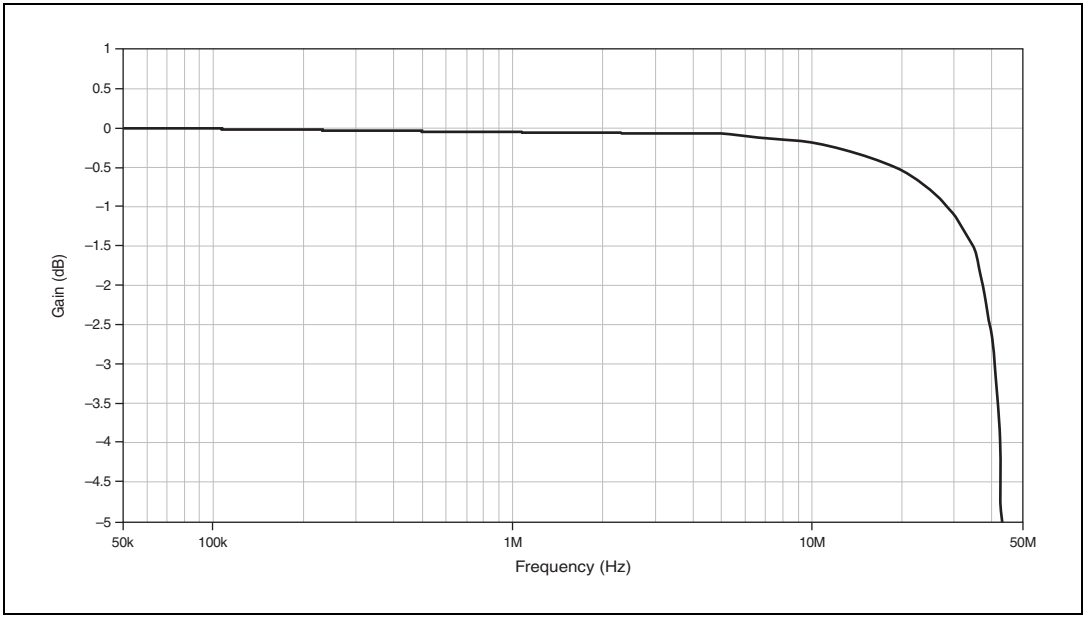


Figure 16. AO Bandwidth (Passband): Measured Single-Ended, AO Generating at 400 MS/s (100 MS/s Data Rate and 4× Interpolation), Gain Referenced to Reading at 50 kHz

Spurious-Free Dynamic Range (SFDR) and Total Harmonic Distortion (THD)

The following table shows the SFDR and THD of the analog output generating a 5 MHz sine wave at 400 MS/s (100 MS/s data rate and 4× interpolation) and −1 dBFS waveform data amplitude. The measurement is single-ended with both terminals terminated to ground through 50 Ω. The SFDR measurement includes aliased and nonaliased harmonics, measured from DC to 50 MHz. The THD measurement includes the 2nd through 6th harmonics.

Generation Frequency (MHz)	SFDR (dBc)	THD (dBc)
5	64	–64

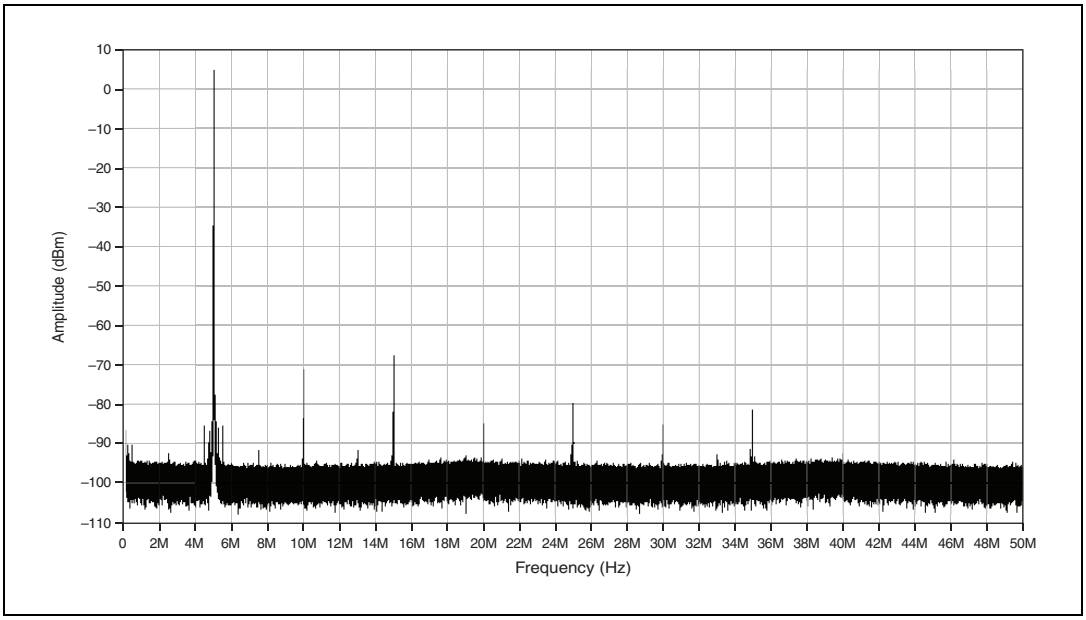


Figure 17. AO SFDR and THD: AO Generating a –1 dBFS 5 MHz Sine Wave with 100 MS/s Data Rate and 4× Interpolation. Measured Single-Ended using 10 Averages.

Third-Order Intermodulation Distortion (IMD_3)

Generation Frequency (MHz)	IMD_3 (dBc)
20 and 21	–58

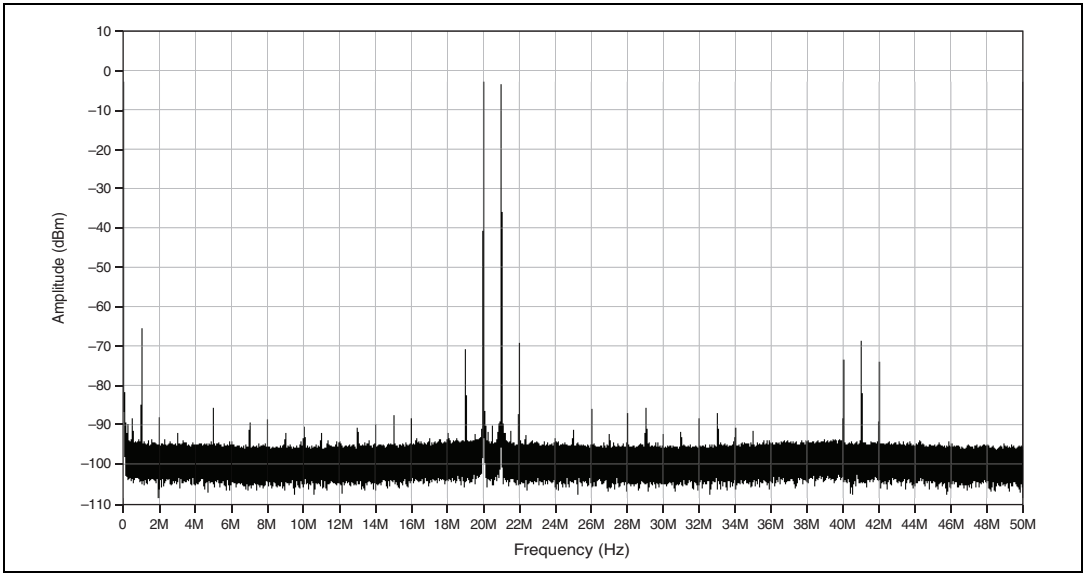


Figure 18. AO IMD_3 (Centered at 20.5 MHz): AO Generating Two –7 dBFS Sine Tones at 20 MHz and 21 MHz with 100 MS/s Data Rate and 4× Interpolation. Measured Single-Ended using 10 Averages.

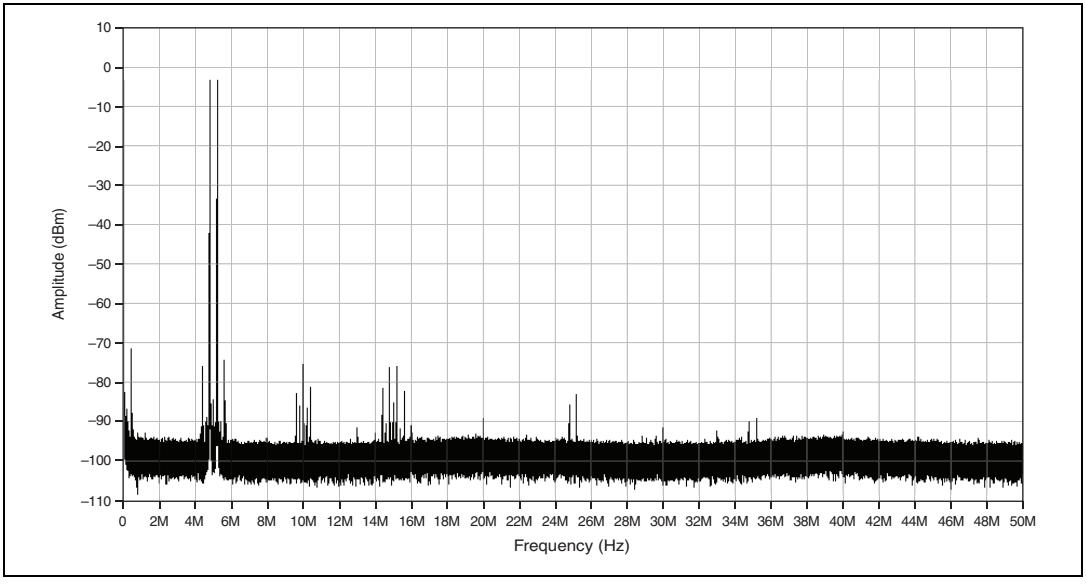


Figure 19. AO IMD_3 (Centered at 5 MHz): AO Generating Two –7 dBFS Sine Tones at 4.8 MHz and 5.2 MHz with 100 MS/s Data Rate and 4× Interpolation. Measured Single-Ended using 10 Averages.

Average Noise Density

	Amplitude Range		Average Noise Density		
	V_{pk-pk}	dBm	$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz
Single-ended	1	4	8	–149	–153
Differential	2	10	11	–146	–156

Note: The average noise density is measured from DC to 50 MHz. The AO generates 0 V DC at 400 MS/s (100 MS/s data rate and 4× interpolation).

Phase Noise Density

Offset from Carrier (Hz)	Phase Noise (dBc/Hz)*
100	–114
1 k	–127
10 k	–138

* Measured on a 10 MHz tone using the free-running internal VCXO as the Sample clock and the DAC using 4× interpolation and 100 MS/s data rate (400 MS/s).

Note: The bandwidth of the PLL is 200 Hz when locking to IoModSyncClk.

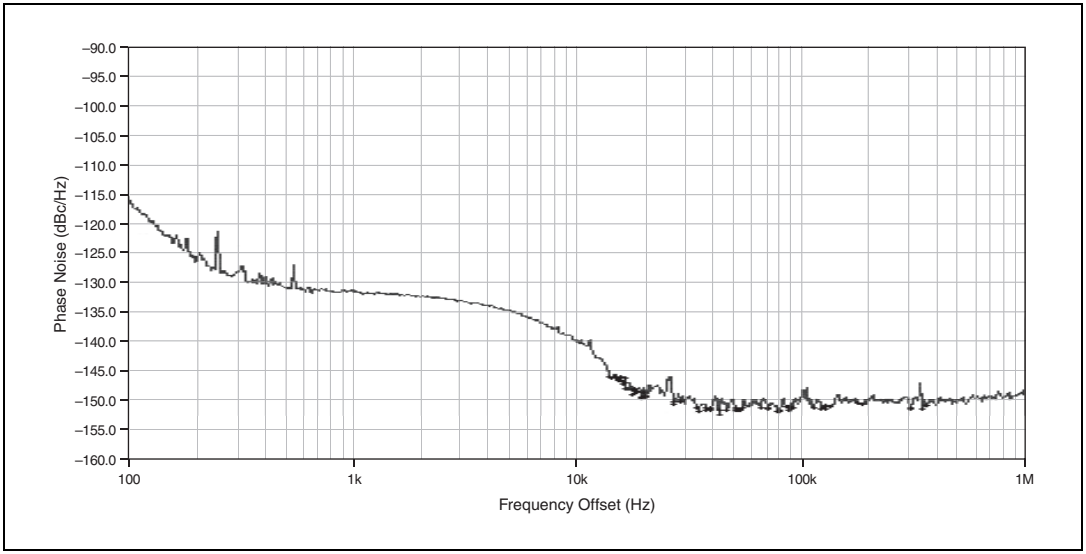


Figure 20. AO Phase Noise: AO Generating a 0 dBFS 20 MHz Sine Wave with 100 MS/s Data Rate and 4× Interpolation, using Free-Running Internal VCXO as the Sample Clock.

DC absolute accuracy (into high impedance)

Differential gain error ..... ±0.8% full-scale range (FSR)

Differential offset ..... ±15 mV

Common mode offset ..... ±5 mV

Note DC accuracy measured with a DMM. Differential gain and offset may be adjusted through waveform data. Measured with both terminals into high impedance.

Internal Sample Clock

General Characteristics

Oscillator type ..... VCXO

Frequency range ..... 100 MHz ±100 ppm

Clock distribution part number ..... AD9511[1]; clock distribution and on-chip PLL core

Reference clock sources ..... IoModSyncClk[2] (10 MHz from PXI backplane)

Typical Specifications

Frequency stability

Temperature ..... ±30 ppm over operating temperature range

Aging ..... ±5 ppm per year

CLK OUT

General Characteristics

Number of channels ..... 1, single-ended

Connector ..... MCX

Output range

Into 50 Ω ..... Fixed 1 V_{pk-pk}

Into High Z ..... Fixed 2 V_{pk-pk}

Absolute maximum input

DC ..... ±8 V

AC ..... 4 V_{pk-pk}

Output impedance ..... 50 Ω

Output coupling ..... AC

Frequency range ..... Sample clock/*N*; where *N* = 1, 2**M*; *M* = <1..16>

Clock distribution part number ..... AD9511[1]; clock distribution and on-chip PLL core

CLK IN

General Characteristics

Number of channels ..... 1, single-ended

Connector ..... MCX

[1] For additional information about the AD9511, refer to the Analog Devices device data sheet at `www.analog.com`.

[2] IoModSyncClk is available only on the NI PXIe-796*x*R FPGA module.

Input voltage range .....400 mV_{pk-pk} to 2 V_{pk-pk}

Absolute maximum input

DC .....±8 V

AC .....4 V_{pk-pk}

Input frequency range .....20 MHz to 100 MHz

Duty cycle requirements .....40% to 60%

Input impedance.....50 Ω

Input coupling .....AC

Clock distribution part number .....AD9511[1]; clock distribution and on-chip PLL core

PFI<0..7>

General Characteristics

Number of channels .....8; 5 output, 2 input, 1 bidirectional

Note PFI Out 4 and PFI In 7/PFI Out 7are available for interfacing with an I^2C bus. Refer to Table 2 for more information.

Connector type .....9-pin DIN with shield

Interface logic .....3.3 V LVTTL

V_{IH}.....≥2 V

V_{IL}.....≤0.8 V

Z_{in}.....5 kΩ

V_{OH}.....≥2.4 V

V_{OL}.....≤0.6 V

Z_{out} .....50 Ω

Absolute maximum input.....–1 V to +5 V per channel

Maximum toggle frequency.....5 MHz

EEPROM Map

Byte Address	Size (Bytes)	Field Name
0x0	2	Vendor ID
0x2	2	Product ID
0x4	4	Serial Number
0x8	116	Reserved
0x7C	132	User Space

Caution *Only* write to *User Space*. Writing to any other offset may cause the NI 5781 to stop functioning.

[1] For additional information on the AD9511, refer to the Analog Devices device data sheet at `www.analog.com`.

Power

Total power, typical operation[1] ..... 5.5 W

Physical

Dimensions ..... 12.9 × 2.0 × 12.1 cm
(5.1 × 0.8 × 4.7 in.)

Weight ..... 284 g (10 oz)

Front panel connectors ..... 10 MCX and one 9-pin DIN with shield

Environmental

The NI 5781 is intended for indoor use only.

Operating environment ..... 0 °C to 55 °C,
tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range ..... 10% to 90%, noncondensing,
tested in accordance with IEC-60068-2-56.

Altitude ..... 2,000 m at 25 °C ambient temperature.

Pollution Degree 2

Storage environment

Ambient temperature range ..... –20 °C to 70 °C,
tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range ..... 5% to 95%, noncondensing,
tested in accordance with IEC-60068-2-56.

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

[1] 100 MHz DAC data rate, 4× interpolation ON, and DAC modulation OFF.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

Note For EMC compliance, you must install two ferrites per cable, on the 9-pin DIN and CLK OUT cables (NI part number 711849-01 for CLK OUT, and NI part number 711627-01 for the 9-pin DIN cable). For best results, snap the ferrites onto the cables as close as possible to the plug at each end. For more information about how to use the cable ferrites with the NI 5781, refer to the *Attaching Ferrites to Your Cables Note to Users* included in your kit.

Note For EMC compliance, operate this device with shielded cables and according to the documentation.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

National Instruments is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

Where to Go From Here

The following resources contain information for writing applications and taking measurements with the NI 5781R.

Software Documentation

- LabVIEW FPGA documentation:
  - *Getting Started with LabVIEW FPGA 8.x*—This KnowledgeBase, available at `ni.com/kb`, provides links to the top resources that can be used to assist in getting started with programming in LabVIEW FPGA.
  - *FPGA Module* book in the *LabVIEW Help*—Select **Help»Search the LabVIEW Help** in LabVIEW to view the *LabVIEW Help*. Browse the **FPGA Module** book in the **Contents** tab for information about how to use the FPGA Module to create VIs that run on the NI PXI-5781R.
  - *LabVIEW FPGA Module Release and Upgrade Notes*—Contains information about installing the LabVIEW FPGA Module, describes new features, and provides upgrade information. To access this document, refer to `ni.com/manuals`. In LabVIEW 8.0 or later, you can also view the LabVIEW Manuals directory that contains this document by selecting **Start» All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.
- *National Instruments Example Finder*—LabVIEW contains an extensive library of VIs and example programs for use with NI FlexRIO devices. To access the NI Example Finder, open LabVIEW and select **Help»Find Examples**, then select **Hardware Input and Output»FlexRIO**.

  You can also access device-specific examples by selecting **Add device** from the **Hardware** pull-down menu in the NI Example Finder window.
- *NI FlexRIO Reference and Procedures*—This book provides instructions for using LabVIEW and the LabVIEW FPGA Module with NI FlexRIO devices. This document is located in the *FPGA Module* in the *LabVIEW Help*.

Device-Specific Documentation

- *NI FlexRIO FPGA Module Specifications*—Lists the specifications of your NI FlexRIO FPGA module. To access, refer to `ni.com/manuals`.

Additional Resources

- *LabVIEW FPGA IPNet*—Offers resources for browsing, understanding, and downloading LabVIEW FPGA functions or IP (Intellectual Property). Use this resource to acquire IP that you need for your application, download examples to help learn programming techniques, and explore the depth of IP offered by the LabVIEW FPGA platform. To access the LabVIEW FPGA IPNet, visit `ni.com/ipnet`.
- `ni.com/flexrio`—Contains product information, and helpful links to the NI FlexRIO forum and the NI community for NI FlexRIO devices.

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At `ni.com/support` you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at `ni.com/support` and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, contact your local branch office:

Australia 1800 300 800, Austria 43 662 457990-0, Belgium 32 (0) 2 757 0020,
Brazil 55 11 3262 3599, Canada 800 433 3488, China 86 21 5050 9800,
Czech Republic 420 224 235 774, Denmark 45 45 76 26 00,
Finland 358 (0) 9 725 72511, France 01 57 66 24 24, Germany 49 89 7413130,
India 91 80 41190000, Israel 972 3 6393737, Italy 39 02 41309277,
Japan 0120-527196, Korea 82 02 3451 3400, Lebanon 961 (0) 1 33 28 28,
Malaysia 1800 887710, Mexico 01 800 010 0793,
Netherlands 31 (0) 348 433 466, New Zealand 0800 553 322,
Norway 47 (0) 66 90 76 60, Poland 48 22 328 90 10, Portugal 351 210 311 210,
Russia 7 495 783 6851, Singapore 1800 226 5886, Slovenia 386 3 425 42 00,
South Africa 27 0 11 805 8197, Spain 34 91 640 0085,
Sweden 46 (0) 8 587 895 00, Switzerland 41 56 2005151,
Taiwan 886 02 2377 2222, Thailand 662 278 6777, Turkey 90 212 279 3031,
United Kingdom 44 (0) 1635 523545

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