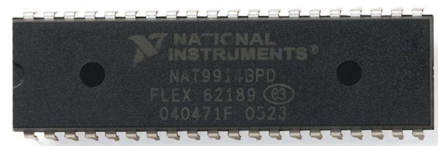
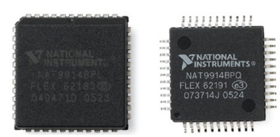
IEEE 488.2 Controller Chip

NAT9914

- Available as RoHS-compliant
- Pin compatible with TI TMS9914A
- Software compatible with NEC μPD7210 or TI TMS9914A controller chips
- Low power consumption
- Meets all IEEE 488.2 requirements
  - Bus line monitoring
  - Preferred implementation of requesting service
  - Will not send messages when there are no Listeners
- Performs all IEEE 488.1 interface functions
- Programmable data transfer rate (T1 delays of 350 ns, 500 ns, 1.1 μs, and 2 μs)
- Automatic EOS and/or NL message detection
- Direct memory access (DMA)
- Automatically processes IEEE 488 commands and reads undened commands
- TTL-compatible CMOS device
- Programmable clock rate 20 MHz maximum
- Reduces driver overhead
- Does not lose a data byte if ATN is asserted while transmitting data





RoHS

Description

The NAT9914 IEEE 488.2 controller chip can perform all the interface functions dened by the IEEE Standard 488.1-1987, and also meets the additional requirements and recommendations of the IEEE Standard 488.2-1987. Connected between the processor and the IEEE 488 bus, the NAT9914 provides high-level management of the IEEE 488 bus, signicantly increases the throughput of driver software, and simplifies both the hardware and software design. The NAT9914 performs complete IEEE 488 Talker, Listener, and Controller functions. In addition to its numerous improvements, the NAT9914 is also completely pin compatible with the TI TMS 9914A and software compatible with the NEC μPD7210 and TI TMS9914A controller chips.

IEEE 488.2 Overview

The IEEE 488.2 standard removes the ambiguities of IEEE 488.1 by standardizing the way instruments and controllers operate. It defines data formats, status reporting, error handling, and common configuration commands to which all IEEE 488.2 instruments must respond in a precise manner. It also denes a set of controller requirements. With IEEE 488.2, you gain the benets of reduced development time and cost because systems are more compatible and reliable. The NAT9914 brings the full power of IEEE 488.2 to the design engineer along with numerous other design and performance benefits, while retaining the 40-pin and 44-pin hardware congurations of the TI TMS 9914A.

General

The NAT9914 manages the IEEE 488 bus. You program the IEEE 488 bus by writing control words into the appropriate registers. CPU-readable status registers supply operational feedback. The NAT9914 mode determines the function of these registers. On power up or reset, the NAT9914 registers resemble those of the TMS9914A set, with additional registers that supply extra functionality and IEEE 488.2 compatibility. In this mode, the NAT9914 is completely pin compatible with the TI TMS9914A. If you enable the 7210 mode, the registers resemble those of the NEC μPD7210 set, with additional registers that supply extra functionality and IEEE 488.2 compatibility. This mode is not pin compatible with the NEC μPD7210. Figure 4 shows the key components of the NAT9914.

RoHS Compliance

The NAT9914 is currently available from NI both in a standard package and as a RoHS-compliant chip. The chips can be ordered using the part numbers shown in the Ordering Information box below. The RoHS-compliant parts are identified through the added “F” at the end of the part number and the chip itself is marked with an e3 inside an ellipse to indicate a matte pure tin finish on the leads, in accordance with the marking recommendations defined in JEDEC JESD97.

The RoHS-compliant NAT9914 meets industry requirements for baking and maximum solder reflow temperature. The baking requirements are outlined in JEDEC J-STD-033, and

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NI recommends using the solder reflow profile as shown in IPC/JEDEC J-STD-020C with a peak temperature of 260 °C, the maximum temperature they can withstand. The Moisture Sensitivity Level (MSL) for the RoHS-compliant surface mount NAT9914 ASICs is 3 (the MSL is not applicable to the NAT9914BPDF through-hole device).

Ordering Information

NI NAT9914BPD (40-pin DIP package)

RoHS-compliant	NAT9914BPDF-9
Non RoHS-compliant	NAT9914BPD-9
Sample kit (RoHS-compliant, 2 ASICs)	776730-01

NI NAT9914BPL (44-pin PLCC package)

RoHS-compliant	NAT9914BPLF-27
Non RoHS-compliant	NAT9914BPL-27
Sample kit (RoHS-compliant, 2 ASICs)	776730-02

NI NAT9914BPQ (44-pin QFP package)

RoHS-compliant	NAT9914BPQF-84
Non RoHS-compliant	NAT9914BPQ-84
Sample kit (RoHS-compliant, 4 ASICs)	776730-03

Visit ***ni.com*** for a detailed reference manual & specifications.

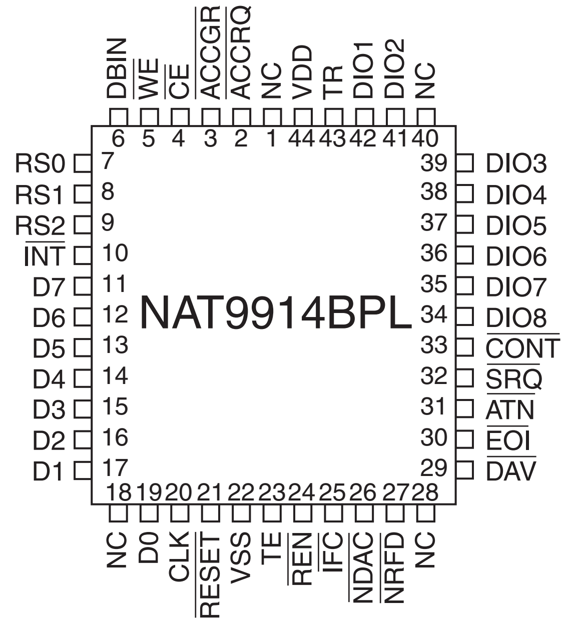

Figure 2. NAT9914BPL Pin Conguration

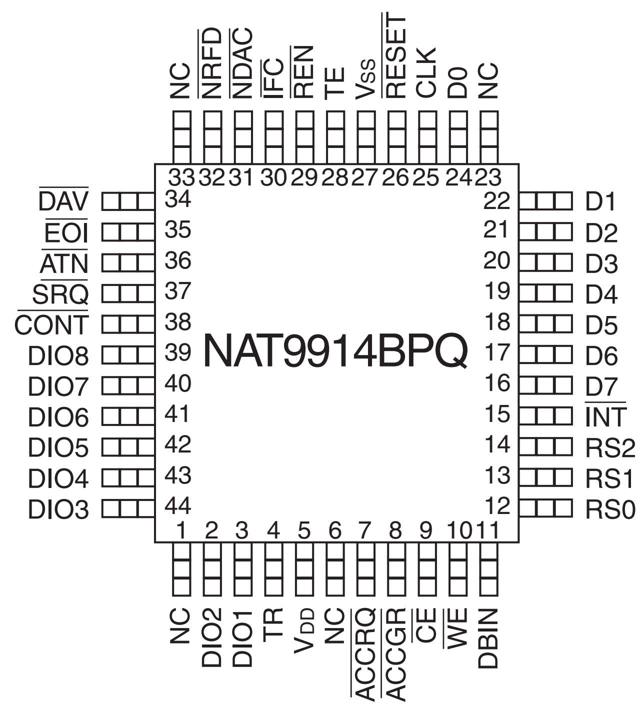

Figure 3. NAT9914BPQ Pin Conguration

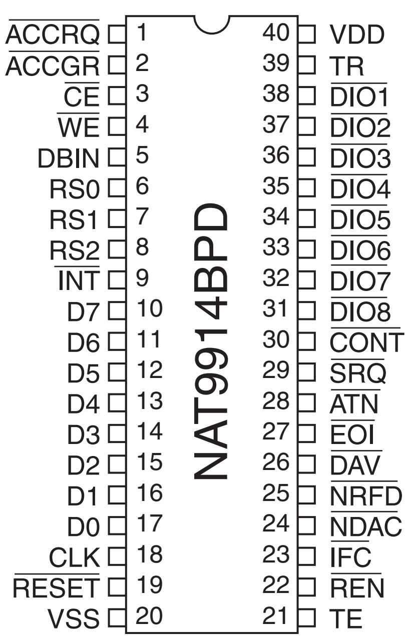

Figure 1. NAT9914BPD Pin Conguration

Pin Identication

Pin Number			Mnemonic	Type	Description
PLCC	DIP	QFP			
11, 12, 13, 14, 15, 16, 17, 19	10, 11, 12, 13, 14, 15, 16, 17	16, 17, 18, 19, 20, 21, 22, 24	D(7-0)	I/O†	Bidirectional 3-state data bus transfers commands, data, and status between the NAT9914 and the CPU. **D0 is the most significant bit.**
4	3	9	CE*	I	Chip Enable gives access to the register selected by a read or write operation, and the register selects RS(2-0).
6	5	11	DBIN	I†	With the Data Bus Input, you can place the contents of the register selected by RS(2-0) and CE* onto the data bus D(7-0). The polarity of DBIN is reversed for DMA operation.
5	4	10	WE*	I	The Write input latches the contents of the data bus D(7-0) into the register selected by RS(2-0).
3	2	8	ACCGR*	I†	The Access Grant signal selects the DIR or CDOR for the current read or write cycle.
2	1	7	ACCRQ*	O	The Access Request output asserts to request a DMA Acknowledge cycle.
20	18	25	CLK	I†	The CLK input can be up to 20 MHz.
21	19	26	RESET*	I†	Asserting the RESET* input places the NAT9914 in an initial, idle state.
10	9	15	INT* (OC)	O	The Interrupt output asserts when one of the unmasked interrupt conditions is true. The NAT9914 does not drive INT* high. The INT* pin must be pulled up by an external resistor.
9, 8, 7	8, 7, 6	14, 13, 12	RS(2-0)	I†††	The Register Selects determine which register to access during a read or write operation.
25	23	30	IFC*	I/O†,†† (OC)	Bidirectional control line initializes the IEEE 488 interface functions.
24	22	29	REN*	I/O† (OC)	Bidirectional control line selects either remote or local control of devices.
31	28	36	ATN*	I/O†	Bidirectional control line indicates whether data on the DIO lines is an interface or device-dependent message.
32	29	37	SRQ*	I/O†	Bidirectional control line requests service from the controller.
34, 35, 36, 37, 38, 39, 41, 42	31, 32, 33, 34, 35, 36 37, 38	39, 40, 41, 42, 43, 44, 2, 3	DIO(8-1)*	I/O†	8-bit bidirectional IEEE 488 data bus
29	26	34	DAV*	I/O†	Handshake line indicates that the data on the DIO(8-1)* lines is valid.
27	25	32	NRFD*	I/O†	Handshake line indicates that the device is ready for data.
26	24	31	NDAC*	I/O†	Handshake line indicates the completion of a message reception.
30	27	35	EOI*	I/O†	Bidirectional control line indicates the last byte of a data message or executes a parallel poll.
23	21	28	TE	O†	Talk Enable controls the direction of the IEEE 488 data transceiver.

Pin Number			Mnemonic	Type	Description
PLCC	DIP	QFP			
43	39	4	TR	O†	Trigger asserts when one of the trigger conditions is satisfied.
33	30	38	CONT*	O†	Controller asserts when the NAT9914 is Controller-In-Charge.
44	40	5	VDD	–	Power pin – +5 V (±5%)
22	20	27	VSS	–	Ground pin – 0 V
1, 18, 28,40	–	1, 6, 23, 33	NC	–	No connect

OC= Open collector.

† The pin contains an internal pull-up resistor of 25 kΩ to 100 kΩ.

* Active low.

†† In controller applications where the CLK signal frequency is > 8 MHz, IFC* should be pulled up with a 4.7 kΩ resistor.

††† RS0 and RS1 contain an internal pull-up resistor of 25 kΩ to 100 kΩ. RS2 does not contain an internal pull-up or pull-down resistor.

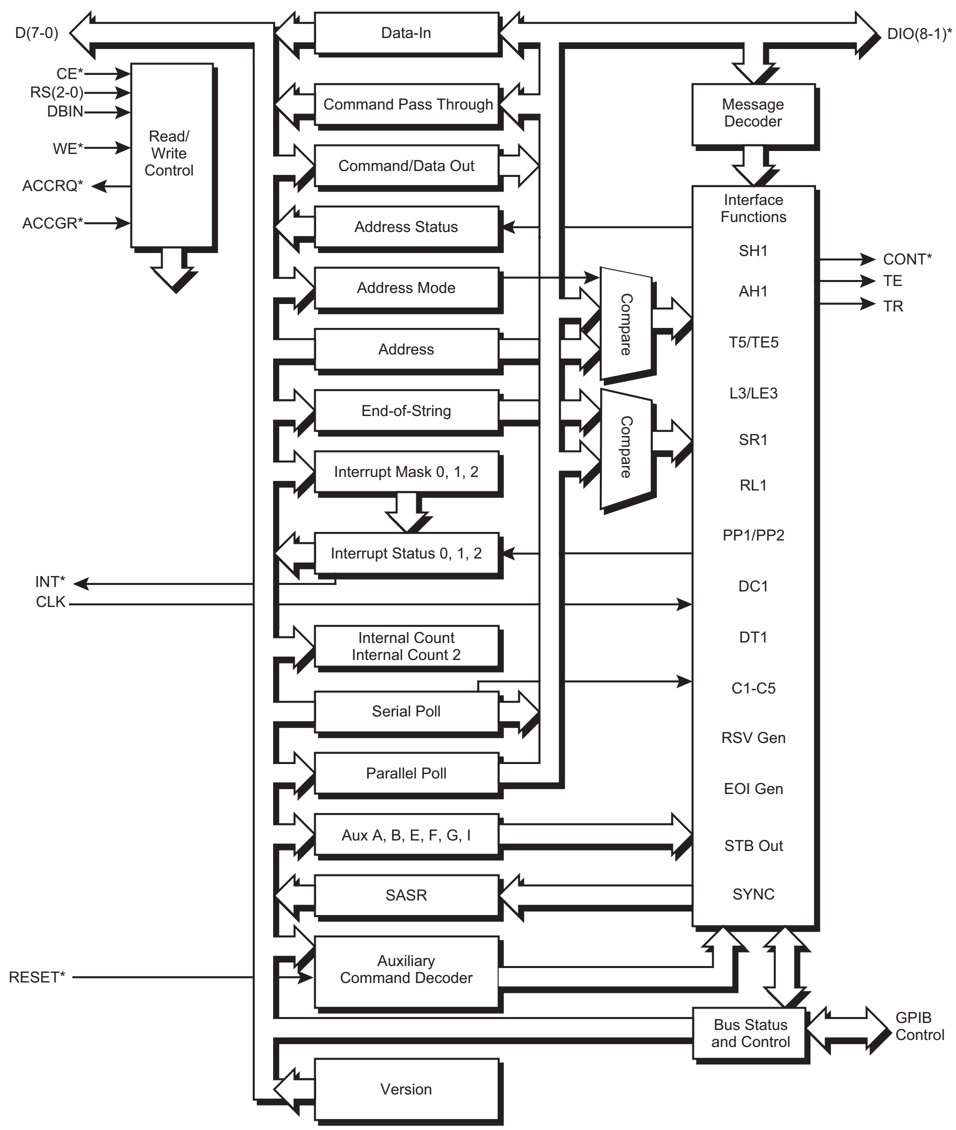

Figure 4. NAT9914 Block Diagram

9914 Mode Registers

In 9914 mode, the NAT9914 registers consist of all the TI TMS9914A registers and two types of additional registers – newly dened registers and paged-in registers. The NAT9914 maps the newly dened registers into the unused portion of the 9914 address space. Each paged-in register appears at Offset 2 immediately after you issue an auxiliary page-in command, and it remains there until you page another register into the same space or you issue a reset. The table below lists all the registers in the 9914 register set. See the *NAT9914 Reference Manual* available at ni.com for more information.

9914 Register Set

Register	PAGE-IN	RS(2-0)			WE*	DBIN	CE*	ACCGR*
Interrupt Status 0	U	0	0	0	1	1	0	1
Interrupt Mask 0	U	0	0	0	0	0	0	1
Interrupt Status 1	U	0	0	1	1	1	0	1
Interrupt Mask 1	U	0	0	1	0	0	0	1
Address Status	U	0	1	0	1	1	0	1
Interrupt Mask 2†	P	0	1	0	0	0	0	1
End-of-String†	P	0	1	0	0	0	0	1
Bus Control†	P	0	1	0	0	0	0	1
Accessory†	P	0	1	0	0	0	0	1
Bus Status	U	0	1	1	1	1	0	1
Auxiliary Command	U	0	1	1	0	0	0	1
Interrupt Status 2†	P	1	0	0	1	1	0	1
Address	U	1	0	0	0	0	0	1
Serial Poll Status†	P	1	0	1	1	1	0	1
Serial Poll Mode	U	1	0	1	0	0	0	1
Command Pass Through	U	1	1	0	1	1	0	1
Parallel Poll	U	1	1	0	0	0	0	1
Data-In	U	1	1	1	1	1	0	1
Data-In	U	X	X	X	X	0	X	0
Command/Data Out	U	1	1	1	0	0	0	1
Command/Data Out	U	X	X	X	0	1	X	0

The † symbol denotes features (such as registers and auxiliary commands) that are not available in the TMS9914A.

Notes for the PAGE-IN column:

U = Page-in auxiliary commands do not affect the register offset.

P = The register offset is valid only after a page-in auxiliary command.

7210 Mode Registers

The NAT9914 registers include all the NEC µPD7210 registers plus two types of additional registers – extra auxiliary registers and paged-in registers. You write the extra auxiliary registers the same as standard µPD7210 auxiliary registers. On issuing an auxiliary page-in command, the paged-in registers appear at the same offsets as existing µPD7210 registers. At the end of the next CPU access, the chip pages out the paged-in registers. The following table lists all the registers in the 7210 mode register set. See the *NAT9914 Reference Manual* available at ni.com for more information.

7210 Register Set

Register	PAGE-IN	A(2-0)			WE*	DBIN	CE*	ACCGR*
Data-In	U	0	0	0	1	1	0	1
Data-In	X	X	X	X	X	0	X	0
Command/Data Out	U	0	0	0	0	0	0	1
Command/Data Out	X	X	X	X	0	1	X	0
Interrupt Status 1	U	0	0	1	1	1	0	1
Interrupt Mask 1	U	0	0	1	0	0	0	1
Interrupt Status 2	U	0	1	0	1	1	0	1
Interrupt Mask 2	U	0	1	0	0	0	0	1
Serial Poll Status	N	0	1	1	1	1	0	1
Serial Poll Mode	N	0	1	1	0	0	0	1
Version	P	0	1	1	1	1	0	1
Internal Counter 2	P	0	1	1	0	0	0	1
Address Status	U	1	0	0	1	1	0	1
Address Mode	U	1	0	0	0	0	0	1
Command Pass Through	N	1	0	1	1	1	0	1
Auxiliary Mode	U	1	0	1	0	0	0	1
Source/Acceptor Status†	P	1	0	1	1	1	0	1
Address 0	N	1	1	0	1	1	0	1
Address	N	1	1	0	0	0	0	1
Interrupt Status 0†	P	1	1	0	1	1	0	1
Interrupt Mask 0†	P	1	1	0	0	0	0	1
Address 1	N	1	1	1	1	1	0	1
End-of-String	N	1	1	1	0	0	0	1
Bus Status†	P	1	1	1	1	1	0	1
Bus Control†	P	1	1	1	0	0	0	1

The † symbol denotes features (such as registers and auxiliary commands) that are not available in the NEC7210.

Notes for the PAGE-IN column:

U = The page-in auxiliary command does not affect the register.

N = The register offset is always valid except for immediately after a page-in auxiliary command.

P = The register is valid only immediately after a page-in auxiliary command.

Preliminary DC Characteristics

T_A 0 to 70 °C; V_{CC} = 5 V ±5%

		Limits			Test
Parameter	Symbol	Min	Max	Unit	Condition
Voltage input low	V_{IL}	-0.5	+0.8	V	–
Voltage input high	V_{IH}	+2.0	V_{CC}	V	–
Voltage output low	V_{OL}	0	0.4	V	–
Voltage output high	V_{OH}	+2.4	VCC	V	–
Input/output Leakage current	–	-10	+10	µA	without internal pull-up
Input/output Leakage current	–	-200	+200	µA	with internal pull-up
Supply current	–	–	45	mA	–
Output current low All pins except ACCRQ	I_{OL}	2	–	mA	0.4 V @ I_{OL}
ACCRQ	I_{OL}	4	–	mA	0.4 V @ I_{OL}
Input current low	I_{IL}	–	- 0.5	mA	–
Supply voltage	V_{DD}	4.75	5.25	V	–

Capacitance

T_A 0 to 70 °C; V_{CC} = 5 V ±5%

		Limits			Test
Parameter	Symbol	Min	Max	Unit	Condition
Input capacitance	C_{IN}	–	10	pF	–
Output capacitance	C_{OUT}	–	10	pF	–
I/O capacitance	$C_{I/O}$	–	10	pF	–

Absolute Maximum Ratings

Property	Range
Supply voltage, V_{DD}	-0.5 to +7.0 V
Input voltage, V_I	-0.5 to V_{DD} +0.5 V
Operating temperature, T_{OPR}	0 to +70° C
Storage temperature, T_{STG}	-40 to +125° C
Comment: Exposing the device to stresses above those listed could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section. Exposure to absolute maximum rating conditions for extended periods may affect reliability.	

AC Characteristics

T_A 0 to 70 °C; V_{CC} = 5 V ±5%

		Limits			Test
Parameter	Symbol	Min	Max	Unit	Condition
Address hold from $\overline{CE}$, $\overline{WE}$,and DBIN	t_{AH}	0	–	ns	–
Address setup to $\overline{CE}$, $\overline{WE}$, and DBIN	t_{AS}	0	–	ns	–
Data float from $\overline{CE}$ or DBIN	t_{DF}	–	20	ns	–
Data delay from DBIN↓	t_{DR}	–	75	ns	$\overline{ACCGR}$=0
$\overline{ACCRQ}$ unassertion	t_{DU}	–	20	ns	–
Data delay from $\overline{CE}$↓	t_{RD}	–	80	ns	$\overline{ACCGR}$=1
$\overline{CE}$ recovery width	t_{RR}	80	–	ns	–
$\overline{CE}$ pulse width	t_{RW}	80	–	ns	–
Data hold from $\overline{WE}$↑	t_{WH}	0	–	ns	–
Data setup to $\overline{WE}$↑	t_{WS}	60	–	ns	–

Notes

- t_{AS} is the setup time to $\overline{CE}$↓ or $\overline{WE}$↓ , whichever is later.
- t_{AH} is the hold time from $\overline{WE}$↑ or $\overline{CE}$↑, whichever is earlier.

Timing Waveforms

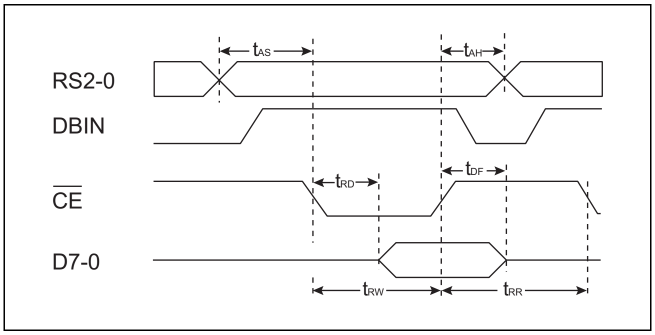

Figure 5. CPU Read

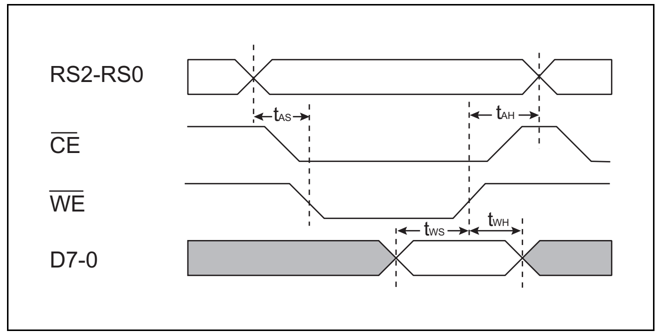

Figure 7. CPU Write

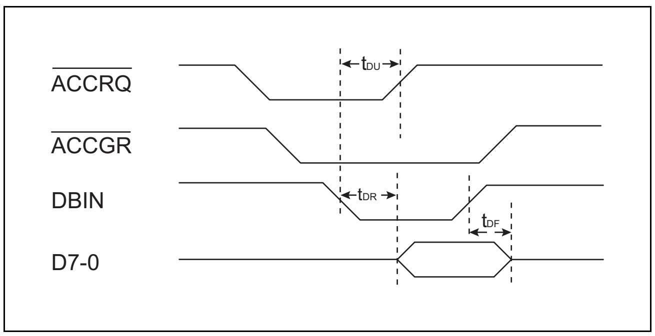

Figure 6. DMA Read

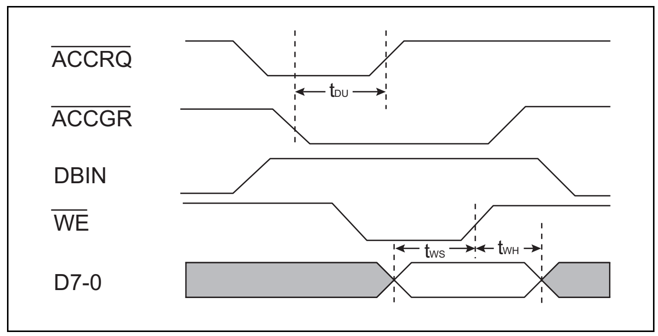

Figure 8. DMA Write

Source Handshake

Parameter	Symbol	Limits (ns)		Test
		Min	Max	Condition
$\overline{\text{NDAC}}$↑ to $\overline{\text{DAV}}$↑	t_{ND}	–	40	–
$\overline{\text{NDAC}}$↑ to $\overline{\text{INT}}$↓ or $\overline{\text{ACCRQ}}$↓	t_{NI}	–	40	INT(DOIE Bit=1) ACCGR (DMAO Bit=1)
$\overline{\text{WE}}$↑ to $\overline{\text{DAV}}$↓	t_{WD}	2000	2180	2 µs T1, 5MHz
$\overline{\text{WE}}$↑ to $\overline{\text{DAV}}$↓	t_{WD}	1200	1380	1.1 µs T1, 5MHz
$\overline{\text{WE}}$↑ to $\overline{\text{DAV}}$↓	t_{WD}	600	780	500 ns T1, 5MHz
$\overline{\text{WE}}$↑ to $\overline{\text{DAV}}$↓	t_{WD}	400	580	350 ns T1, 5MHz

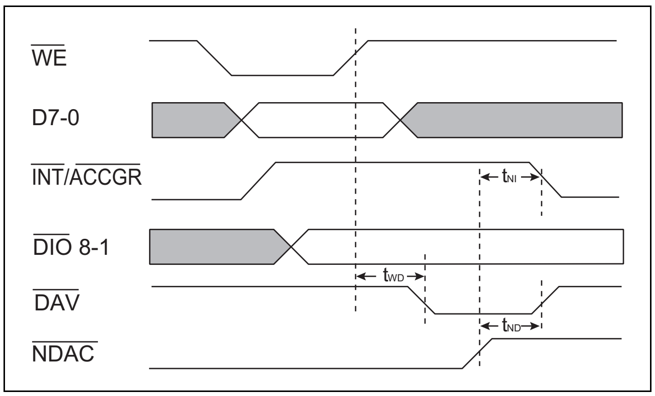

Figure 9. Source Handshake Timing

Acceptor Handshake

Parameter	Symbol	Limits (ns)		Test
		Min	Max	Condition
$\overline{\text{DAV}}$↓ to $\overline{\text{NDAC}}$↑	t_{DD}		35+3T	
$\overline{\text{DAV}}$↑ to $\overline{\text{NDAC}}$↓	t_{DF}		25	
$\overline{\text{DAV}}$↓ to $\overline{\text{INT}}$↓ or $\overline{\text{ACCRQ}}$↓	t_{DI}		50+2T	INT(DIIE Bit=1), ACCGR (DMAI Bit=1)
$\overline{\text{DAV}}$↓ to $\overline{\text{NRFD}}$↓	t_{DR}		20	
DBIN↑ to $\overline{\text{NRFD}}$↑	t_{NR}		35	Read of DIR, not in Holdoff state

Note: T = one clock period

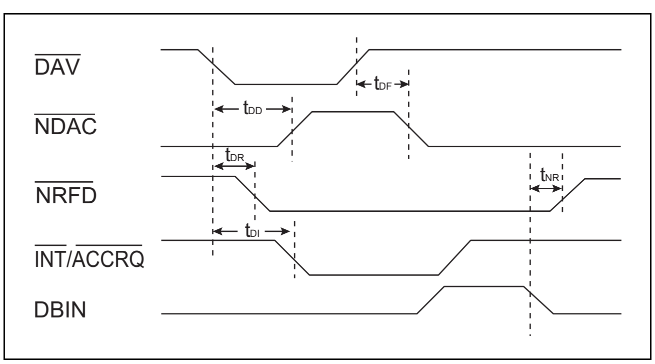

Figure 10. Acceptor Handshake Timing

Response to ATN

Parameter	Symbol	Limits (ns)		Test
		Min	Max	Condition
$\overline{\text{ATN}}$↑ to $\overline{\text{NRFD}}$↓	t_{AF}		35	Acceptor handshake holdoff
$\overline{\text{ATN}}$↓ to $\overline{\text{NDAC}}$↓	t_{AN}		35	AIDS → ANRS
$\overline{\text{ATN}}$↓ to TE↓	t_{AT}		30	TACS → TADS

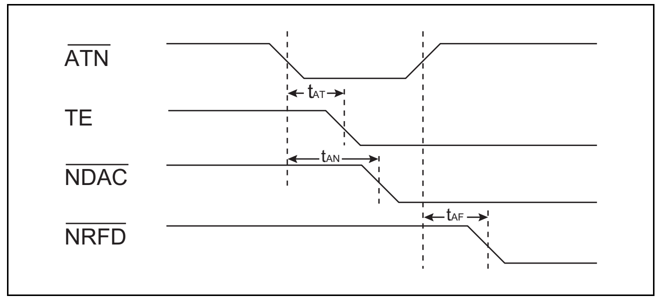

Figure 11. ATN Response Timing

Parallel Poll

Parameter	Symbol	Limits (ns)		Test
		Min	Max	Condition
$\overline{\text{EOI}}$↓ to $\overline{\text{DIO}}$↓ valid	t_{ED}		90	PPSS → PPAS
$\overline{\text{EOI}}$↓ to TE↑	t_{ET}		30	PPSS → PPAS
$\overline{\text{EOI}}$↑ to TE↓	t_{TE}		30	PPAS → PPSS

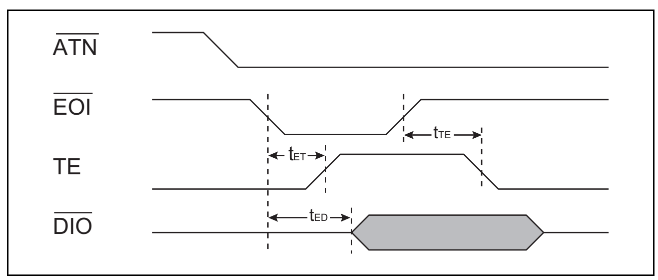

Figure 12. Parallel Poll Response Timing

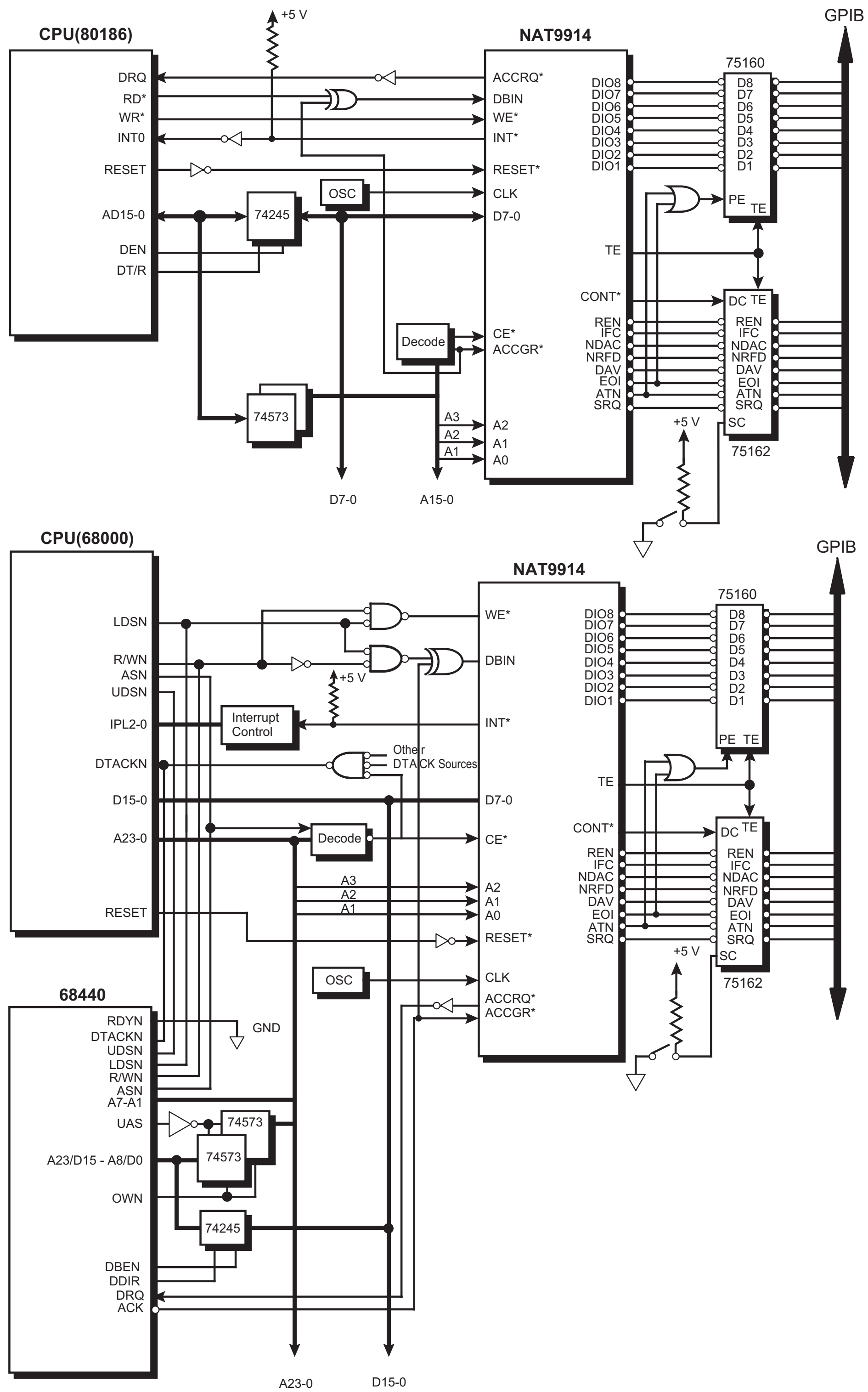

Figure 13. Typical CPU Systems with NAT9914

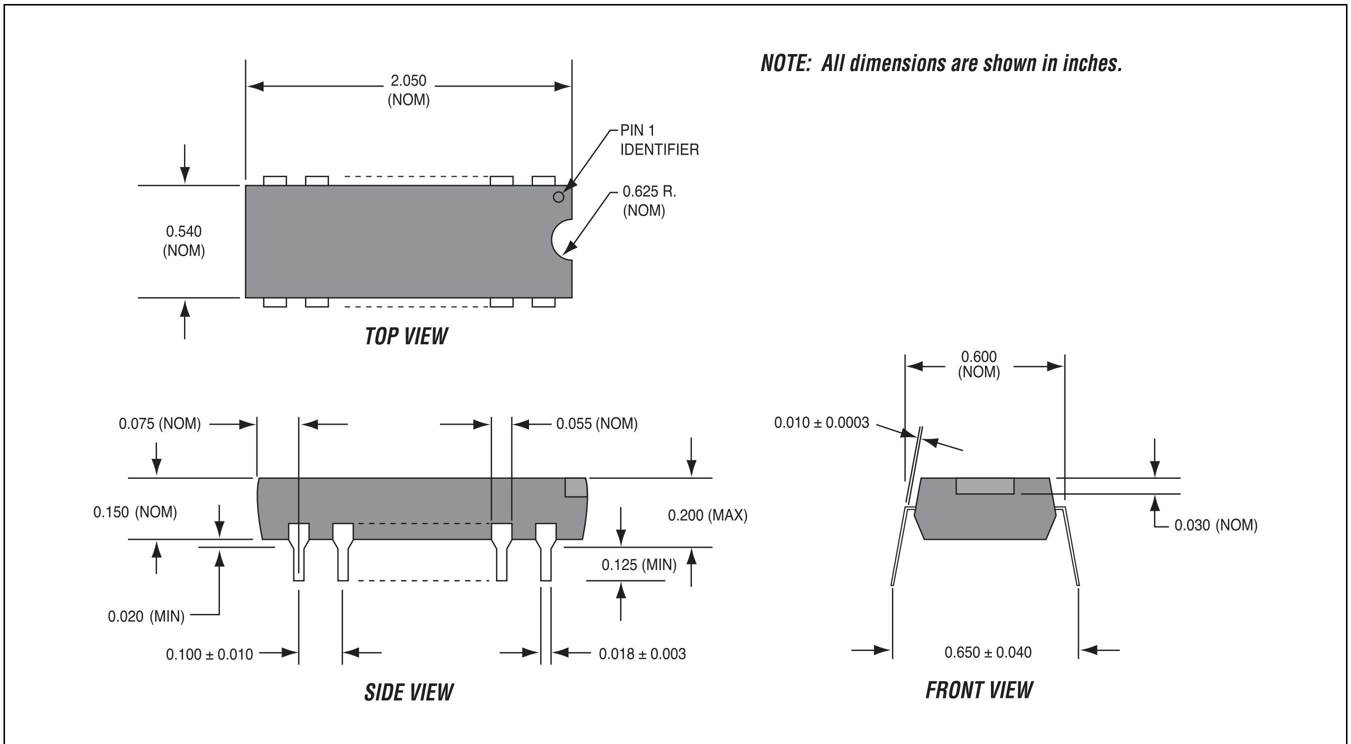

Figure 14. Mechanical Data 40-Pin Plastic DIP

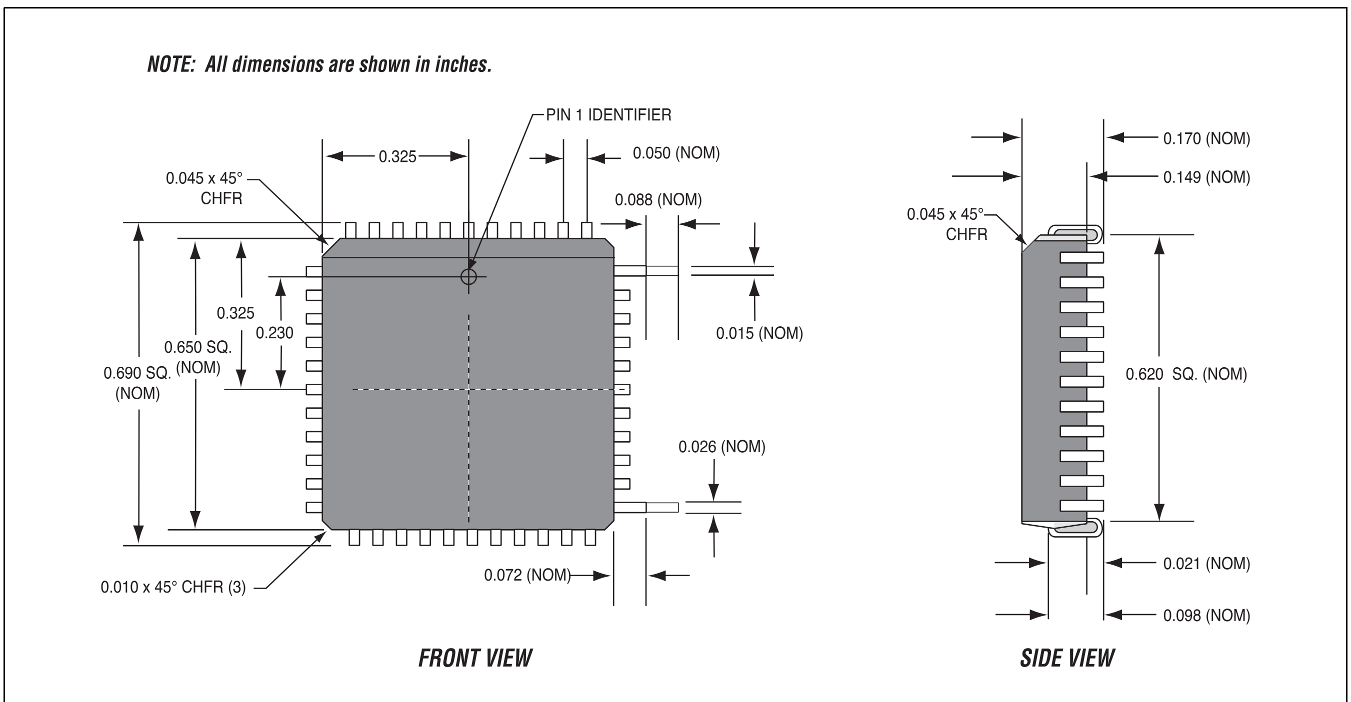

Figure 15. Mechanical Data 44-Pin PLCC

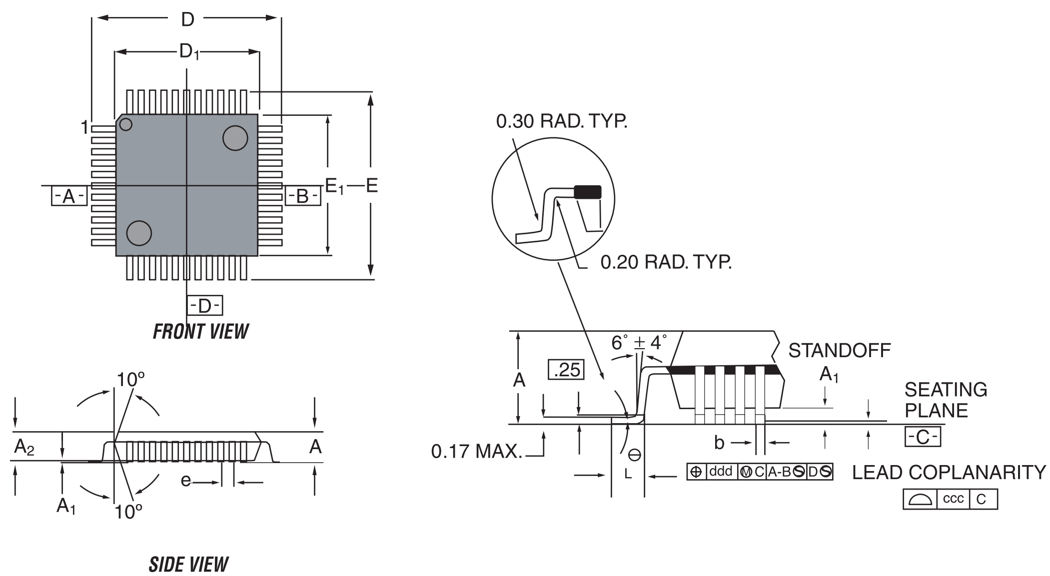

Figure 16. Mechanical 44-Pin QFP

Dimensions	Tolerance	Value (in mm)
A	max.	2.35
A_1	–	0.25 max.
A_2	+ 0.10/-0.05	2.00
D	± 0.25	17.20
D_1	± 0.10	14.00
E	± 0.25	17.20
E_1	± 0.10	14.00
L	+ 0.15/- 0.10	0.88
e	basic	1.00
b	± 0.05	0.35
θ	–	0 to 7°
ddd	–	0.20 nom.
ccc	max.	0.10

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Hardware Services

NI Factory Installation Services

NI Factory Installation Services (FIS) is the fastest and easiest way to use your PXI or PXI/SCXI combination systems right out of the box. Trained NI technicians install the software and hardware and configure the system to your specifications. NI extends the standard warranty by one year on hardware components (controllers, chassis, modules) purchased with FIS. To use FIS, simply configure your system online with ni.com/pxiadvisor.

Calibration Services

NI recognizes the need to maintain properly calibrated devices for high-accuracy measurements. We provide manual calibration procedures, services to recalibrate your products, and automated calibration software specifically designed for use by metrology laboratories. Visit ni.com/calibration.

Repair and Extended Warranty

NI provides complete repair services for our products. Express repair and advance replacement services are also available. We offer extended warranties to help you meet project life-cycle requirements. Visit ni.com/services.

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