Product Change Notification / SYST-18SSJO427

Date:

12-Jan-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

Errata - ATtiny417/814/816/817 Silicon Errata and Data Sheet Clarification Document Revision

Affected CPNs:

SYST-18SSJO427_Affected_CPN_01122021.pdf
SYST-18SSJO427_Affected_CPN_01122021.csv

Notification Text:

SYST-18SSJO427

Microchip has released a new Product Documents for the ATtiny417/814/816/817 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at ATtiny417/814/816/817 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
1) Initial document release

The content of the document has been restructured from:
a) ATtiny214/414/814 Silicon Errata and Data Sheet Clarification
b) ATtiny416/816 Silicon Errata and Data Sheet Clarification
c) ATtiny417/817 Silicon Errata and Data Sheet Clarification

to:
a) ATtiny417/814/816/817 Silicon Errata and Data Sheet Clarification (this document)
Refer to 4.2 Appendix - Obsolete Revision History for further details.
1) The following item is referring to changes between the latest revisions of the obsolete documents and this document:
a) Silicon revision A removed from Silicon issues summary, as this was never released to production

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 12 Jan 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATtiny417/ 814/ 816/ 817 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATTINY417-MF
ATTINY417-MN
ATTINY417-MNR
ATTINY417-MFR
ATTINY814-SSF
ATTINY814-SSN
ATTINY814-SSNR
ATTINY814-SSFR
ATTINY816-SF
ATTINY816-MF
ATTINY816-SN
ATTINY816-MN
ATTINY816-SNR
ATTINY816-MNR
ATTINY816-SFR
ATTINY816-MFR
ATTINY817-MF
ATTINY817-MN
ATTINY817-MNR
ATTINY817-MFR

ATtiny417/814/816/817

ATtiny417/814/816/817 Silicon Errata and Data Sheet Clarification

The ATtiny417/814/816/817 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002288), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny417/814/816/817 devices.

Notes:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002288) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. B[1]
Device	2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X
AC	2.3.1 Coupling Through AC Pins	X
	2.3.2 AC Interrupt Flag Not Set Unless Interrupt is Enabled	X
	2.3.3 False Triggers May Occur Under Certain Conditions	X
	2.3.4 False Triggering When Sweeping Negative Input of the AC When the Low-Power Mode is Disabled	X
ADC	2.4.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode	X
	2.4.2 Changing ADC Control Bits During Free-Running Mode not Working	X
	2.4.3 ADC Wake-Up with WCMP	X
	2.4.4 ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X
	2.4.5 ADC Performance Degrades with CLKADC Above 1.5 MHz and VDD < 2.7V	X
	2.4.6 Pending Event Stuck When Disabling the ADC	X
	2.4.7 ADC Interrupt Flags Cleared When Reading RESH	X
CCL	2.5.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'	X
	2.5.2 D-latch is Not Functional	X
	2.5.3 The CCL Must be Disabled to Change the Configuration of a Single LUT	X
RTC	2.6.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler	X
	2.6.2 Disabling the RTC Stops the PIT	X
TCA	2.7.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X
TCB	2.8.1 Minimum Event Duration Must Exceed the Selected Clock Period	X
	2.8.2 The TCB Interrupt Flag is Cleared When Reading CCMPH	X
	2.8.3 TCB Input Capture Frequency and Pulse-Width Measurement Mode Not Working with Prescaled Clock	X
	2.8.4 The TCA Restart Command Does Not Force a Restart of TCB	X
	2.8.5 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X

.....continued		
Peripheral	Short Description	Valid for Silicon Revision
		Rev. B(1)
TCD	2.9.1 TCD Auto-Update Not Working	X
	2.9.2 TCD Event Output Lines May Give False Events	X
	2.9.3 Asynchronous Input Events Not Working When TCD Counter Prescaler is Used	X
TWI	2.10.1 TIMEOUT Bits in the TWI.MCTRLB Register are Not Accessible	X
	2.10.2 TWI Smart Mode Gives Extra Clock Pulse	X
	2.10.3 TWI Host Mode Wrongly Detects the Start Bit as a Stop Bit	X
	2.10.4 The TWI Host Enable Quick Command is Not Accessible	X
USART	2.11.1 TXD Pin Override Not Released When Disabling the Transmitter	X
	2.11.2 Frame Error on a Previous Message May Cause False Start Bit Detection	X
	2.11.3 Full Range Duty Cycle Not Supported When Validating LIN Sync Field	X
	2.11.4 Open-Drain Mode Does Not Work When TXD is Configured as Output	X
	2.11.5 Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work Around

Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCK in CLKCTRL.OSC20MCALIBB to '1'.

Affected Silicon Revisions

Rev. B
X

2.3 AC - Analog Comparator

2.3.1 Coupling Through AC Pins

There is a capacitive coupling through the Analog Comparator. Toggling the selected positive AC pin may affect the selected negative input pin and vice versa.

Work Around

When the AC is disabled, configure AC.MUXCTRLA.MUXNEG to DAC or internal reference.

Affected Silicon Revisions

Rev. B
X

2.3.2 AC Interrupt Flag Not Set Unless Interrupt is Enabled

ACn.STATUS.CMP is not set if the ACn.INTCTRL.CMP is not set.

Work Around

Enable ACn.INTCTRL.CMP or use ACn.STATUS.STATE for polling.

Affected Silicon Revisions

Rev. B

X

2.3.3 False Triggers May Occur Under Certain Conditions

False triggers may occur on falling input pin:

- If the slew rate on the input signal is greater than 2 V/µs for common-mode voltage below 0.5V
- If the slew rate on the input signal is greater than 10 V/µs for common-mode voltage above 0.5V
- If the slew rate on the input signal is greater than 10 V/µs for any common-mode voltage and Low-Power mode is enabled

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.3.4 False Triggering When Sweeping Negative Input of the AC When the Low-Power Mode is Disabled

A false trigger may occur if sweeping the negative input of the AC with a negative slope, and the AC has Low-Power mode disabled.

Work Around
Enable Low-Power mode in AC.CTRLA.LPMODE.

Affected Silicon Revisions

Rev. B
X

2.4 ADC - Analog-to-Digital Converter

2.4.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work Around
Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. B
X

2.4.2 Changing ADC Control Bits During Free-Running Mode not Working

If control signals are changed during Free-Running mode, the new configuration is not properly taken into account in the next measurement. This is valid for the ADC.CTRLB, ADC.CTRLC, ADC.SAMPCTRL registers, and the ADC.MUXPOS, ADC.WINLT, and ADC.WINHT registers.

Work Around
Disable ADC Free-Running mode before updating the ADC.CTRLB, ADC.CTRLC, ADC.SAMPCTRL, ADC.MUXPOS, ADC.WINLT, or ADC.WINHT registers.

Affected Silicon Revisions

Rev. B
X

2.4.3 ADC Wake-Up with WCMP

When waking up from Standby sleep mode with ADC WCMP interrupt, the ADC is disabled for a few cycles before the device enters Active mode. A new INITDLY is required before the next conversion.

Work Around
Use INITDLY before the next conversion.

Affected Silicon Revisions

Rev. B
X

2.4.4 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

Work Around
If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

Affected Silicon Revisions

Rev. B
X

2.4.5 ADC Performance Degrades with CLK_{ADC} Above 1.5 MHz and VDD < 2.7V

The ADC INL performance degrades if CLK_{ADC} > 1.5 MHz and ADCn.CALIB.DUTYCYC set to '0' for VDD < 2.7V.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.4.6 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work Around
Clear ADC.EVCTRL.STARTEI and wait for the conversion to complete before disabling the ADC.

Affected Silicon Revisions

Rev. B
X

2.4.7 ADC Interrupt Flags Cleared When Reading RESH

ADCn.INTFLAGS.RESRDY and ADCn.INTFLAGS.WCOMP are cleared when reading ADCn.RESH.

Work Around

In 8-bit mode, read ADCn.RESH to clear the flag or clear the flag directly.

Affected Silicon Revisions

Rev. B
X

2.5 CCL - Configurable Custom Logic

2.5.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'

Connecting the LUTs in linked mode requires LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

Work Around

Use an event channel to link the LUTs, or do not use the corresponding I/O pin for other purposes.

Affected Silicon Revisions

Rev. B
X

2.5.2 D-latch is Not Functional

The CCL D-latch is not functional.

Work Around

None.

Affected Silicon Revisions

Rev. B
X

2.5.3 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure a LUT, the CCL peripheral must be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around

None

Affected Silicon Revisions

Rev. B
X

2.6 RTC - Real-Time Counter

2.6.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the 15-bit prescaler resulting in a longer period on the current count or period.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.6.2 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

Work Around
Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

Rev. B
X

2.7 TCA - Timer/Counter A

2.7.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to the NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset direction to default. The default is counting upwards.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.8 TCB - Timer/Counter B

2.8.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

Work Around
Ensure that the high/low period of input events is equal to or longer than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

Affected Silicon Revisions

Rev. B
X

2.8.2 The TCB Interrupt Flag is Cleared When Reading CCMPH

TCBn.INTFLAGS.CAPT is cleared when reading TCBn.CCMPH instead of CCMPL.

Work Around
Read both TCBn.CCMPL and TCBn.CCMPH.

Affected Silicon Revisions

Rev. B
X

2.8.3 TCB Input Capture Frequency and Pulse-Width Measurement Mode Not Working with Prescaled Clock

The TCB Input Capture Frequency and Pulse-Width Measurement mode may lock to Freeze state if CLKSEL in TCB.CTRLA is set to any other value than `0x0`.

Work Around
Only use CLKSEL equal to `0x0` when using Input Capture Frequency and Pulse-Width Measurement mode.

Affected Silicon Revisions

Rev. B
X

2.8.4 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is restarted only after a TCA OVF.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.8.5 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '`0x7`'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

Work Around
Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. B
X

2.9 TCD - Timer/Counter D

2.9.1 TCD Auto-Update Not Working

The TCD auto-update feature is not working.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.9.2 TCD Event Output Lines May Give False Events

The TCD event output lines can give false events.

Work Around
Use the delayed event functionality with a minimum of one cycle delay.

Affected Silicon Revisions

Rev. B
X

2.9.3 Asynchronous Input Events Not Working When TCD Counter Prescaler is Used

When the TCD is configured to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0' events can be missed.

Work Around
Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. B
X

2.10 TWI - Two-Wire Interface

2.10.1 TIMEOUT Bits in the TWI.MCTRLB Register are Not Accessible

The TIMEOUT bits in the TWI.MCTRLB register are not accessible from the software.

Work Around
When initializing TWI, BUSSTATE in TWI.MSTATUS must be brought into an IDLE state by writing `0x1` to it.

Affected Silicon Revisions

Rev. B
X

2.10.2 TWI Smart Mode Gives Extra Clock Pulse

TWI Host with Smart mode enabled gives an extra clock pulse on the SCL line after sending NACK.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.10.3 TWI Host Mode Wrongly Detects the Start Bit as a Stop Bit

If TWI is enabled in Host mode followed by an immediate write to the MADDR register, the bus monitor recognizes the Start bit as a Stop bit.

Work Around
Wait for a minimum of two clock cycles from TWI.MCTRLA.ENABLE until TWI.MADDR is written.

Affected Silicon Revisions

Rev. B
X

2.10.4 The TWI Host Enable Quick Command is Not Accessible

TWI.MCTRLA.QCEN is not accessible from the software.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.11 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.11.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '`0`' while the USART receiver is disabled (RXEN in USART.CTRLB is '`0`')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '`0`'

Work Around

There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. B
X

2.11.2 Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

Work Around

Wait for the RXD pin to go high before reading RXDATA, for instance, by polling the bit in PORTn.IN where the RXD pin is located.

Affected Silicon Revisions

Rev. B
X

2.11.3 Full Range Duty Cycle Not Supported When Validating LIN Sync Field

For the LIN sync field, the USART is validating each bit to be within ±15% instead of the time between falling edges as described in the LIN specification, which allows a minimum duty cycle of 43.5% and a maximum duty cycle of 57.5%.

Work Around

None.

Affected Silicon Revisions

Rev. B
X

2.11.4 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. B
X

2.11.5 Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'

The Start-of-Frame Detector can unintentionally be enabled when the device is in Active mode and when the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is '0'. If the Receive Data (RXDATA) registers are read while receiving new data, RXCIF is cleared, and the Start-of-Frame Detector will be enabled and falsely detects the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode, and no interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Enable it again by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. B
X

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002288).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 None

There are no known data sheet clarifications as of this publication date.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
A	12/2020	• Initial document release The content of the document has been restructured from: • ATtiny214/414/814 Silicon Errata and Data Sheet Clarification • ATtiny416/816 Silicon Errata and Data Sheet Clarification • ATtiny417/817 Silicon Errata and Data Sheet Clarification to: • **ATtiny417/814/816/817 Silicon Errata and Data Sheet Clarification (this document)** Refer to 4.2 Appendix - Obsolete Revision History for further details. • The following item is referring to changes between the latest revisions of the obsolete documents and this document: – Silicon revision A removed from Silicon issues summary, as this was never released to production

4.2 Appendix - Obsolete Revision History

Notes: Due to document structure change from pin organized documents, the following document history is provided as a reference.

- ATtiny214/414/814 Silicon Errata and Data Sheet Clarification (DS40002115C)
- ATtiny416/816 Silicon Errata and Data Sheet Clarification (DS40002116C)
- ATtiny417/817 Silicon Errata and Data Sheet Clarification (DS40002117B)

4.2.1 Obsolete Document DS40002115C

Doc. Rev.	Date	Comments
C	11/2020	• Added die revision C for ATtiny214 and ATtiny414 • Updated *Affected Silicon Revisions* for *ADC Interrupt Flags Cleared When Reading RESH* • Added new errata: – Device: *Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values* – CCL: *The CCL Must be Disabled to Change the Configuration of a Single LUT* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – TCD: *Asynchronous Input Events Not Working When TCD Counter Prescaler is Used* – USART: • *Full Range Duty Cycle Not Supported When Validating LIN Sync Field* • *Open-Drain Mode Does Not Work When TXD is Configured as Output* • *Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'*

.....continued

Doc. Rev.	Date	Comments
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten
A	06/2019	Initial document release

4.2.2 Obsolete Document DS40002116C

Doc. Rev.	Date	Comments
C	11/2020	• Added die revision C for ATtiny416 • Updated *Affected Silicon Revisions* for *ADC Interrupt Flags Cleared When Reading RESH* • Added new errata: – Device: *Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values* – CCL: *The CCL Must be Disabled to Change the Configuration of a Single LUT* – TCA: *Restart Will Reset Counter Direction in NORMAL and FRQ Mode* – TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode* – TCD: *Asynchronous Input Events Not Working When TCD Counter Prescaler is Used* – USART: • *Full Range Duty Cycle Not Supported When Validating LIN Sync Field* • *Open-Drain Mode Does Not Work When TXD is Configured as Output* • *Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'*
B	10/2019	• Updated document template • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten
A	06/2019	Initial document release

4.2.3 Obsolete Document DS40002117B

Doc Rev.	Date	Comments
B	10/2019	• Updated document template. • The ADC errata, **ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions**, has been split into two separate erratas and rewritten. • Added clarifications for: – Missing Memory Map – Missing ADC Block Diagram
A	06/2019	• Initial document release.

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