

Product Change Notification / SYST-17ZKFY392

Date:

18-Dec-2020

Product Category:

Analog Multiplexer/Switch ICs

PCN Type:

Document Change

Notification Subject:

Data Sheet - HV2607/2707/2708 Data Sheet Data Sheet Document Revision

Affected CPNs:

SYST-17ZKFY392_Affected_CPN_12182020.pdf SYST-17ZKFY392_Affected_CPN_12182020.csv

Notification Text:

SYST-17ZKFY392

Microchip has released a new Product Documents for the HV2607/2707/2708 Data Sheet of devices. If you are using one of these devices please read the document located at HV2607/2707/2708 Data Sheet.

Notification Status: Final

Description of Change: 1. Updated the Block Diagram. 2. Added the Negative Supply Voltage throughout Section 1.0 "Electrical Characteristics". 3. Updated Figure 2-1. 4. Updated Table 2-1 with the Negative Supply Voltage pin. 5. Updated all the figures in Section 3.0 "Test Circuit Examples". 6. Updated Section 5.4 "Power-up/Down Sequence and Decoupling Capacitor" and Section 5.5 "Layout Considerations".

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 18 Dec 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

HV2607/2707/2708 Data Sheet

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HV2607T-C/R8X HV2707T-C/R8X HV2708T-C/R8X



No High-Voltage Bias, Low Harmonic Distortion, 16-Channel, High-Voltage Analog Switch

Features

- 16-Channel High-Voltage Analog Switch
- Analog Signal Voltage Up to ±100V
- Only +5V Bias Supply Required
- 3.3V and 5V CMOS Input Logic Level
- 66 MHz Data Shift Clock Frequency
- Ultra-Low Quiescent Current < 10 µA
- · Low Parasitic Capacitance
- Low Harmonic Distortion
- DC to 100 MHz Analog Small Signal Frequency
- 200 kHz to 50 MHz Large Signal Frequency
- · -76 dB Typical Off Isolation at 5.0 MHz
- · Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Integrated Bleed Resistors on the Outputs (both sides for HV2707, one side for HV2708)

Application

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT) Metal Flaw Detection
- Piezoelectric Transducer Drivers
- · Inkjet Printer Head
- · Optical MEMS Module

General Description

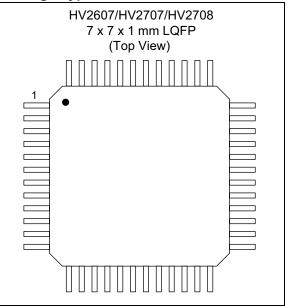
HV2607/HV2707/HV2708 devices are low harmonic distortion, low charge injection, 16-channel, high-voltage analog switches without high-voltage supplies. They are intended for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, driving piezoelectric transducers and printers.

The HV2707 has integrated bleed resistors at both sides of the switches. The HV2708 has integrated bleed resistors at the SWA side only. The HV2607 has no bleed resistors. The bleed resistor eliminates voltage build up on capacitive loads, such as piezoelectric transducers.

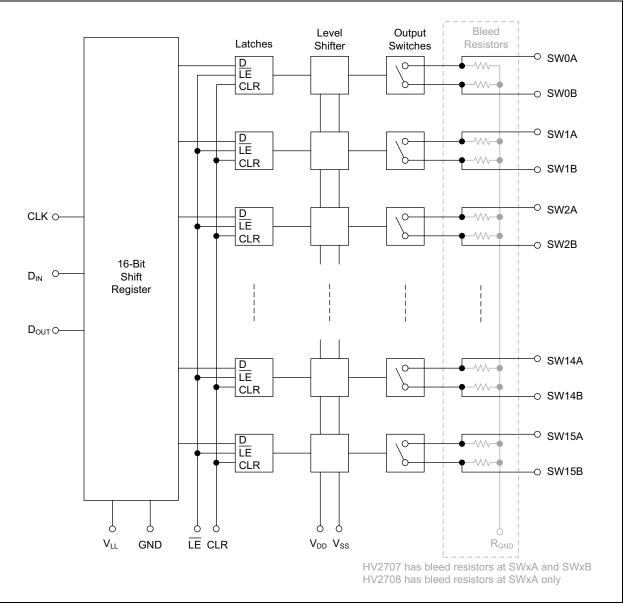
The HV2607/HV2707/HV2708 devices require no high-voltage supplies and require only +5V or +6V bias supply. The analog input voltage range is up to $\pm 100V$, even though there are no high-voltage supplies.

The HV2607/HV2707/HV2708 devices are offered in a 48-pin LQFP package, which is pin-to-pin compatible with HV2601/HV2701 and HV2605/HV2705 devices, except power supply pins.

Package Types



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings[†]

Logic Supply Voltage (V11)	-0.5V to 6.6V
Positive Supply Voltage (V _{DD})	-0.5V to 6.6V
Negative Supply Voltage (V _{SS})	
Logic Input Voltage (VIN)	0.5V to V ₁₁ + 0.3V
Analog Signal Range (V _{SIG})	110V to +110V
Peak Analog Signal Current/Channel (IPK)	

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS^(1,2,3)

Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions
Logic Supply Voltage	V _{LL}	3	—	5.5	V	
Positive Supply Voltage	V _{DD}	4.5	—	6.3	V	
Negative Supply Voltage	V _{SS}	-6.3	—	-4.5	V	Or floating
High-Level Input Voltage	V _{IH}	0.9 V _{LL}	_	V _{LL}	V	
Low-Level Input Voltage	VIL	0	—	0.1 V _{LL}	V	
Analog Signal Voltage Peak-to-Peak	V _{SIG}	-100	_	100	V	

Note 1: Power-up sequence is V_{LL} first and then V_{DD}/V_{SS} . Power-down sequence is the reverse of power-up.

2: V_{SIG} must be GND $\leq V_{SIG} \leq V_{DD}$ or floating during power-up/down transition.

3: Rise and fall times of power supplies, V_{LL} , V_{SS} and V_{DD} , should be greater than 1.0 ms.

DC ELECTRICAL CHARACTERISTICS

Boldface specifications apply over	1	· · · · ·	1	1	1	
Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions/Comments
Small Signal Switch On-Resistance	R _{ONS}		14	23	Ω	I _{SIG} = 5 mA
		—	14.5	23	Ω	$I_{SIG} = 200 \text{ mA}$
Small Signal Switch On-Resistance Matching	ΔR _{ONS}	—	5	20	%	I _{SIG} = 5 mA
Large Signal Switch On-Resistance	R _{ONL}	—	12	—	Ω	V _{SIG} = 90V, R _{LOAD} = 70Ω (Note 1)
Value of Output Bleed Resistor (HV2707/HV2708 only)	R _{INT}	20	35	50	kΩ	I _{RINT} = 0.1 mA
Switch Off Leakage per Switch	I _{SOL}	—	—	10	μA	V _{SIG} = +100V, 500 µs pulse, see Figure 3-1
		—	-	10	μA	V _{SIG} = -100V, 100 μs pulse, see Figure 3-1 (Note 1)
			HV2	607		
Switch Off Bias per Switch	I _{SOB}	—	—	3	μA	V _{SIG} = +100V, 500 µs pulse, see Figure 3-2
		—	—	100	μA	V _{SIG} = -100V, 100 μs pulse, see Figure 3-2 (Note 1)
	-	-	HV2	707	-	-
Switch Off Bias of All SWA and SWB Switches	I _{SOB}	_	-	3	μA	V _{SIG} = +100V, 500 µs pulse, see Figure 3-2
		_	_	3	mA	V _{SIG} = -100V, 100 μs pulse, see Figure 3-2 (Note 1)
			HV2	708		
Switch Off Bias of All SWA (with Bleed Resistor) Switches	I _{SOB}	—	-	3	μA	V _{SIG} = +100V, 500 μs pulse, see Figure 3-2
		—	-	1.5	mA	V _{SIG} = -100V, 100 μs pulse, see Figure 3-2 (Note 1)
Switch Off Bias per SWB (without Bleed Resistor) Switch		—	-	3	μA	V _{SIG} = +100V, 500 μs pulse, see Figure 3-2
		—	-	100	μA	V _{SIG} = -100V, 100 μs pulse, see Figure 3-2 (Note 1)
Switch Off DC Offset	V _{OS}	—	1	10	mV	R_{LOAD} = 25 kΩ (HV2607)/50 kΩ (HV2708),
Switch On DC Offset		—	1	10		no load (HV2707), see Figure 3-3 (Note 1)
Quiescent V _{DD} Supply Current	I _{DDQ}		_	10	μA	All switches off
			—	10		All switches on, V _{SW} = 1V
			—	20		All switches off, V _{SS} = -5V (Note 1)
			_	20		All switches on, V_{SW} = 1V, V_{SS} = -5V (Note 1)
Quiescent V _{SS} Supply Current	I _{SSQ}	—	—	20	μA	V _{SS} = -5V (Note 1)
Quiescent V _{LL} Supply Current	I _{LLQ}		1	10	μA	All logic inputs are GND
Switch Output Peak Current	I _{SW}	1.3	1.9		Α	V _{SIG} duty cycle < 0.1% (Note 1)
Output Switching Frequency	f _{SW}	—		50	kHz	Duty cycle = 50% (Note 1)
Average V _{DD} Supply Current	I _{DD}		3.7	6	mA	All output switches are turning on and off at 50 kHz with no load
			3	5	mA	All output switches are turning on and off at 50 kHz with no load, V _{SS} = -5V(Note 1)

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, V_{LL} = +5V, V_{DD} = +5V, V_{SS} = NC, T_A = +25°C. Boldface specifications apply over the full operating temperature range.									
Parameter Sym. Min. Typ. Max. Units Conditions/Comments									
Average V _{LL} Supply Current	ILL	_	0.3	0.5	mA	f _{CLK} = 5.0 MHz, f _{DIN} = 2.5 MHz			
Data Out Source Current	I _{SOR}	10	—	_	mA	$V_{OUT} = V_{LL} - 0.7V$			
Data Out Sink Current I_{SINK} 10 — — mA $V_{OUT} = 0.7V$									
Logic Input Capacitance C _{IN} – 8 – pF Note 2									

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{LL} = +5V, V_{DD} = +5V, V_{SS} = NC, t_R = $t_F \le 5.0$ ns, 50% duty cycle, T_A = +25°C. **Boldface** specifications apply over the full operating temperature range.

Boldface specifications apply ove	r the full ope	rating te	mperat	ure rang	ge.	
Parameter	Sym.	Min.	Тур.	Max.	Units	Conditions/Comments
Setup Time Before LE Rises	t _{SD}	25	—	_	ns	Note 1
Time Width of LE	t _{WLE}	12	—	—	ns	Note 1
Clock Delay Time to Data Out	t _{DO}	_	_	13.5	ns	
Time Width of CLR	t _{WCLR}	55	—	_	ns	Note 1
Setup Time Data to Clock	t _{SU}	1.5		—	ns	Note 1
Hold Time Data from Clock	t _H	1.5		—	ns	Note 1
Clock Frequency	f _{CLK}		—	66	MHz	50% duty cycle, f _{DIN} = (1/2)f _{CLK} , C _{DOUT} = 20 pF (Note 1)
Clock Rise and Fall Times	t _R , t _F			50	ns	
Turn-On Time	t _{ON}		—	5	μs	V_{SIG} = 5V, R_{LOAD} = 550 Ω , see Figure 3-4
Turn-Off Time	t _{OFF}	-	—	5	μs	V_{SIG} = 5V, R_{LOAD} = 550 Ω , see Figure 3-4
Input Large Signal Pulse Width	t _{PW}	_	_	2.5	μs	V _{PULSE} = 0V to ±100V, measured at 90% amplitude, see Figure 3-5 (Note 1)
Maximum V _{SIG} Slew Rate	dV/dt	_	_	20	V/ns	Note 1
Analog Small Signal Frequency	f _{BWS}		100	_	MHz	Note 1
Off Isolation	K _O		-64	-60	dB	f = 5.0 MHz,1.0 kΩ//15 pF load, see Figure 3-6 (Note 1)
		_	-76	-70	dB	f = 5.0 MHz, 50Ω load, see Figure 3-6 (Note 1)
Switch Crosstalk	K _{CR}		-70	-60	dB	f = 5.0 MHz, 50Ω load, see Figure 3-7 (Note 1)
Off Capacitance SW to GND	C _{SG(OFF)}		9	—	pF	V _{SIG} = 50 mV @1_MHz, no load (Note 1)
On Capacitance SW to GND	C _{SG(ON)}	_	17	—	pF	V _{SIG} = 50 mV @ 1 MHz, no load (Note 1)
Output Voltage Spike at SWA, SWB	V _{SPK}		—	50	mVpp	R_{LOAD} = 50 Ω , see Figure 3-8 (Note 1)
Charge Injection	QC	_	110	—	рС	See Figure 3-8 (Note 1)
Second Harmonic Distortion	HD2		-64	—	dBc	V _{SIG} = 1.5V @ 5 MHz, 50Ω load (Note 1)
		_	-60	-	dBc	V _{SIG} = 1.5V @ 5 MHz, 1 kΩ//15 pF load (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATION

Parameters	Sym	Min	Тур	Max	Units	Conditions
Temperature Range						
Operating Temperature	T _A	0	—	+70	°C	
Storage Temperature	Τ _S	-65	—	+150	°C	
Maximum Junction Temperature	TJ	—	—	+125	°C	
Package Thermal Resistance	·					
Thermal Resistance, LQFP	Θ _{JA}	_	52	_	°C/W	

TABLE 1-1: TRUTH TABLE^(1,2,3,4,5,6)

D0	D1		D7	D8		D15	LE	CLR	SW0	SW1		SW7	SW8		SW15
L	—					—	L	L	OFF	—			_		—
Н	—		_	_		_	L	L	ON	_		_	_		
—	L					_	L	L	—	OFF					
—	Н						L	L	—	ON					
—	—					_	L	L	—	—					
—	_					_	L	L	—	—					
—	_		L	-			L	L	—	—		OFF			
—	—		Н	-		_	L	L	—	—		ON			
—	_			L		_	L	L	—	—			OFF		
—	_			Н		—	L	L	—	—			ON		
—	—					_	L	L	—	—					
—	_					_	L	L	—	—					
—	_					L	L	L	—	—					OFF
—	_					Н	L	L		—		_			ON
Х	Х	Х	Х	Х	Х	Х	Н	L		Н	old Pf	REVIOL	IS STAT	ΓE	
Х	Х	Х	Х	Х	Х	Х	Х	Н			ALL SV	VITCHE	S OFF		

Note 1: The 16 switches operate independently.

- 2: Serial data are clocked in on the L to H transition of the CLK.
- **3:** All 16 switches go to a state retaining their latched condition at the rising edge of LE. When LE is low, the shift registers' data flow through the latch.
- **4:** D_{OUT} is high when the data in Register 15 are high.
- 5: Shift register clocking has no effect on the switch states if LE is high.
- 6: The CLR (clear) input overrides all of the inputs.

1.1 Typical Timing Diagram

Figure 1-1 shows the timing of AC characteristic parameters graphically.

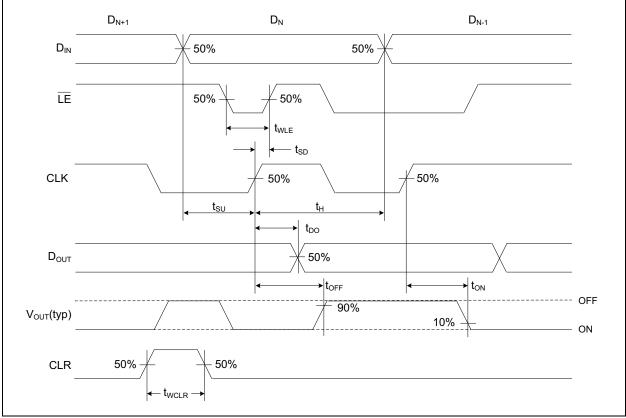


FIGURE 1-1: Logic Input Timing Diagram.

2.0 PIN DESCRIPTION

This section details the pin description for the 48-Lead LQFP package (Figure 2-1). The descriptions of the pins are listed in Table 2-1.

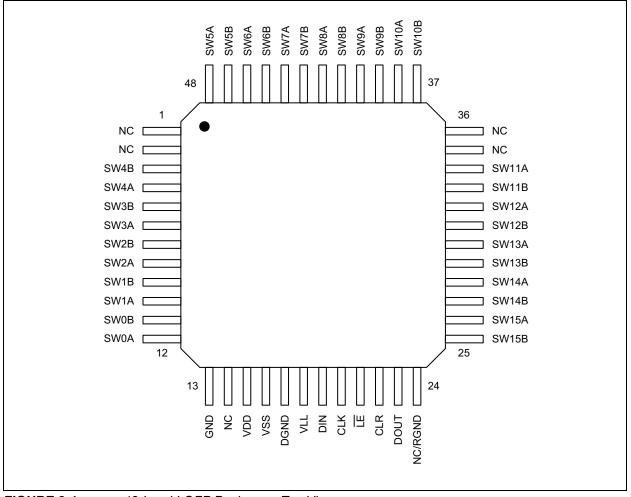


FIGURE 2-1:

48-Lead LQFP Package – Top View.

IABLE 2-1:			
Pin Number		ymbol	Description
	HV2607	HV2707/HV2708	
1	NC	NC	No Connection
2	NC	NC	No Connection
3	SW4B	SW4B	Analog Switch 4 Terminal B
4	SW4A	SW4A	Analog Switch 4 Terminal A
5	SW3B	SW3B	Analog Switch 3 Terminal B
6	SW3A	SW3A	Analog Switch 3 Terminal A
7	SW2B	SW2B	Analog Switch 2 terminal B
8	SW2A	SW2A	Analog Switch 2 Terminal A
9	SW1B	SW1B	Analog Switch 1 Terminal B
10	SW1A	SW1A	Analog Switch 1 Terminal A
11	SW0B	SW0B	Analog Switch 0 Terminal B
12	SW0A	SW0A	Analog Switch 0 Terminal A
13	GND	GND	Ground
14	NC	NC	No Connection
15	V _{DD}	V _{DD}	Positive Supply Voltage
16	V _{SS}	V _{SS}	Negative Supply Voltage. Connect -5V or floating.
17	DGND	DGND	Digital Ground
18	V _{LL}	V _{LL}	Logic Supply Voltage
19	D _{IN}	D _{IN}	Data In Logic Input
20	CLK	CLK	Clock Logic Input for Shift Register
21	LE	LE	Latch Enable Logic Input, Low Active
22	CLR	CLR	Latch Clear Logic Input
23	D _{OUT}	D _{OUT}	Data Out Logic Output
24	NC	RGND	No Connection/Ground for Bleed Resistor
25	SW15B	SW15B	Analog Switch 15 Terminal B
26	SW15A	SW15A	Analog Switch 15 Terminal A
27	SW14B	SW14B	Analog Switch 14 Terminal B
28	SW14A	SW14A	Analog Switch 14 Terminal A
29	SW13B	SW13B	Analog Switch 13 Terminal B
30	SW13A	SW13A	Analog Switch 13 Terminal A
31	SW12B	SW12B	Analog Switch 12 Terminal B
32	SW12A	SW12A	Analog Switch 12 Terminal A
33	SW11B	SW11B	Analog Switch 11 Terminal B
34	SW11A	SW11A	Analog Switch 11 Terminal A
35	NC	NC	No Connection
36	NC	NC	No Connection
37	SW10B	SW10B	Analog Switch 10 Terminal B
38	SW10A	SW10A	Analog Switch 10 Terminal A
39	SW9B	SW9B	Analog Switch 9 Terminal B
40	SW9A	SW9A	Analog Switch 9 Terminal A
41	SW8B	SW8B	Analog Switch 8 Terminal B
42	SW8A	SW8A	Analog Switch 8 Terminal A
43	SW7B	SW7B	Analog Switch 7 Terminal B
44	SW7A	SW7A	Analog Switch 7 Terminal A
45	SW6B	SW6B	Analog Switch 6 Terminal B
46	SW6A	SW6A	Analog Switch 6 Terminal A
47	SW5B	SW5B	Analog Switch 5 Terminal B
	01100		

TABLE 2-1: PIN FUNCTION TABLE

3.0 TEST CIRCUIT EXAMPLES

This section details a few examples of test circuits.

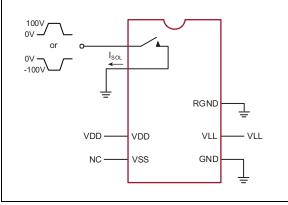


FIGURE 3-1: Switch Off Leakage per Switch.

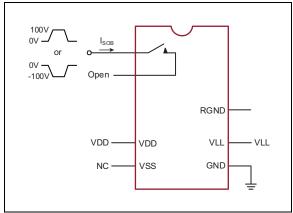


FIGURE 3-2:

Switch Off Bias per Switch.

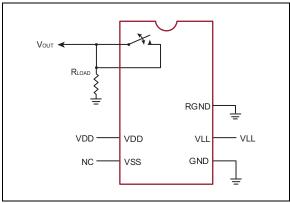


FIGURE 3-3:



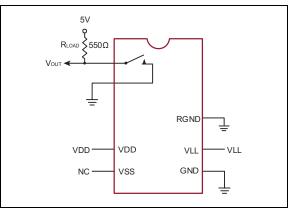


FIGURE 3-4:

T_{ON}/T_{OFF} Test Circuit.

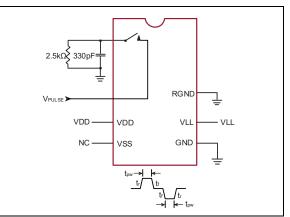


FIGURE 3-5: Tx Pulse Width.

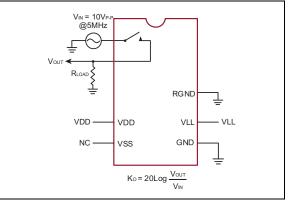
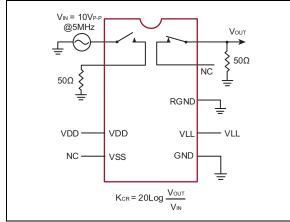


FIGURE 3-6: Off Isolation.





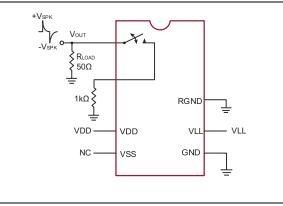
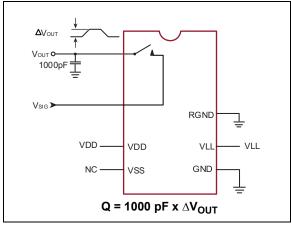


FIGURE 3-8:

Output Voltage Spike.





Charge Injection.

4.0 TYPICAL PERFORMANCE CURVES

Unless otherwise specified, V_{LL} = +5V, V_{DD} = +5V, T_A = +25°C.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

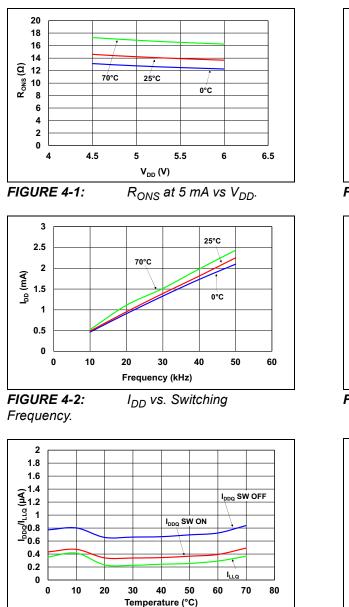
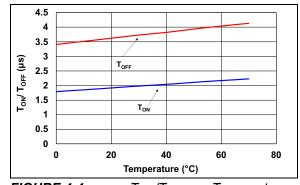


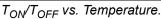
FIGURE 4-3:

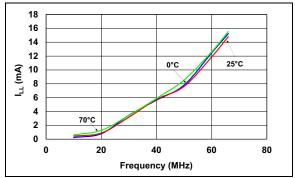
Note:

I_{DDQ}/I_{LLQ} vs. Temperature.



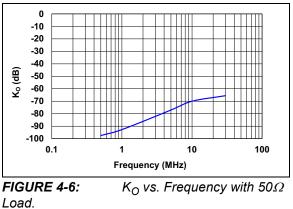












5.0 DETAILED DESCRIPTION AND APPLICATION INFORMATION

5.1 Device Overview

The HV2607/HV2707/HV2708 devices are low harmonic distortion, low charge injection, 16-channel, high-voltage analog switches without high-voltage supplies. The high-voltage analog switches are used for multiplexing a piezoelectric transducer array in a probe to multiple channel transmitter (Tx) arrays in a medical ultrasound system.

The HV2607/HV2707/HV2708 devices are distinguished by bleed resistors that eliminate voltage build-up in capacitance load, such as piezoelectric transducers. These devices can pass $\pm 100V$ high-voltage pulses without high-voltage bias, such as $\pm 100V$. These devices have typical 14 Ω on-resistance and 100 MHz bandwidth for small signals.

Figure 5-1 shows a typical medical ultrasound image system consisting of 64 channels of transmit pulsers, 64 channels of receivers (LNA and ADC) and 64 channels of T/R switches connecting to 192 elements of an ultrasound probe via a HV2XXX high-voltage analog switch array.

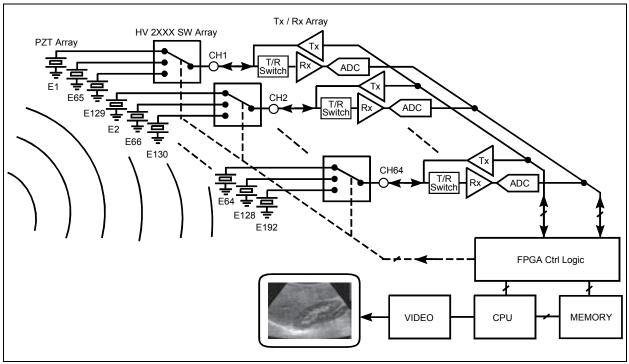


FIGURE 5-1: Typical Medical Ultrasound Imaging System.

5.2 Logic Input Timing

The HV2607/HV2707/HV2708 devices have a digital serial interface consisting of Data In (D_{IN}), Clock (CLK), Data Out (D_{OUT}), Latch Enable (LE) and Clear (CLR) to control 16 switches individually. The digital circuits are supplied by V_{LL} and connected to DGND. The serial clock frequency is up to 66 MHz.

The switch state configuration data are shifted into the shift registers on the rising edge (low-to-high transition) of the clock. The switch Configuration bit of SW15 is shifted in first and the Configuration bit of SW0 is shifted in last. To change all the switch states at the same time, the Latch Enable ($\overline{\text{LE}}$) input should remain high while the 16-bit Data In signal is shifted into the 16-bit register. After the valid 16-bit data complete shifting into the shift registers, the high-to-low transition of the $\overline{\text{LE}}$ signal transfers the contents of

the shift registers into the latches. Finally, setting the $\overline{\text{LE}}$ high again allows all the latches to keep the current state, while new data can now be shifted into the shift registers without disturbing the latches.

It is recommended to change all the latch states at the same time through this method to avoid possible clock feed through noise (see Figure 5-2 for details).

When the CLR input is set high, it resets the data of all 16 latches to low. Consequently, all the high-voltage switches are set to the OFF state. However, the CLR signal does not affect the contents of the shift register, so the shift register can operate independently of the CLR signal. Therefore, when the CLR input is low, the shift register still retains the previous data.

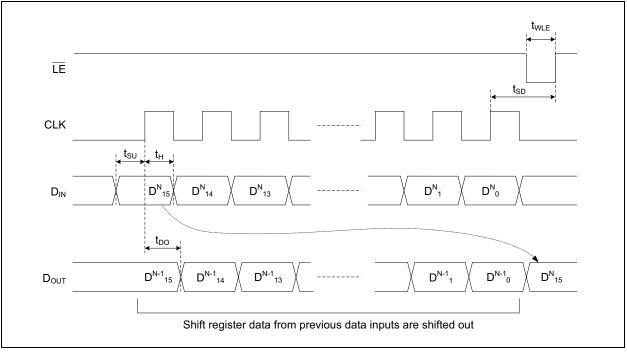


FIGURE 5-2: Latch Enable Timing Diagram.

5.3 Multiple Devices Connection

The serial input interface of the HV2607/HV2707/HV2708 allows multiple devices to daisy-chain together. In this configuration, the D_{OUT} of a device is connected to the D_{IN} of the subsequent device, and so forth. The last D_{OUT} of the daisy-chained HV2607/HV2707/HV2708 can either be floating or fed back to an FPGA to check the previously stored shift register data.

To control all the high-voltage analog switch states in daisy-chained N devices, N-times 16 clocks and N-times 16 bits of data are shifted into shift registers, while \overline{LE} remains high and CLR remains low. After all the data finish shifting in, one single negative pulse of \overline{LE} transfers the data from all shift registers to all the latches simultaneously. Consequently, all N-times 16 high-voltage analog switches change states simultaneously.

5.4 Power-Up/Down Sequence and Decoupling Capacitor

The recommended power-up sequence of the HV2607/HV2707/HV2708 is V_{LL} first, then V_{DD}/V_{SS}. The power-down sequence is in reverse order of power-up. During the power-up/down period, all the analog switch inputs should be within V_{DD} and GND or floating.

5.5 Layout Considerations

The HV2607/HV2707/HV2708 devices have two separate ground connections. DGND is the ground connection for digital circuitry and GND is the ground connection for substrate and analog switches. Since the analog switch passes large transient current from the pulser, the GND should be shared with the pulser output stage ground. It is important to have a good PCB layout which minimizes noise and ground bounce. It is recommended to use two separate ground planes in the PCB, connected together at the return terminal of the input power line, as shown in Figure 5-3. It is recommended that 0.1 µF or larger ceramic decoupling capacitors with low-ESR (Equivalent Series Resistance) and appropriate voltage ratings be connected between ground and power supplies, as shown in Figure 5-3. The decoupling capacitor of $V_{LL},\,V_{SS}$ and V_{DD} should be connected to DGND. These decoupling capacitors should be placed as close as possible to the device.

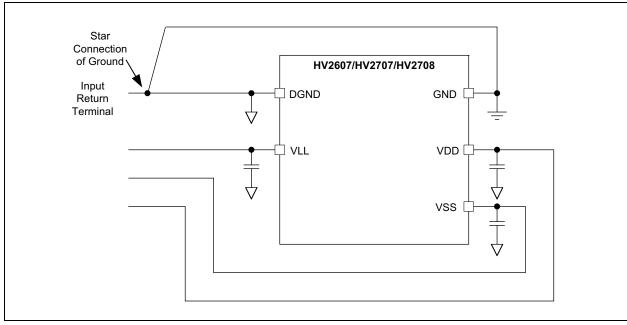
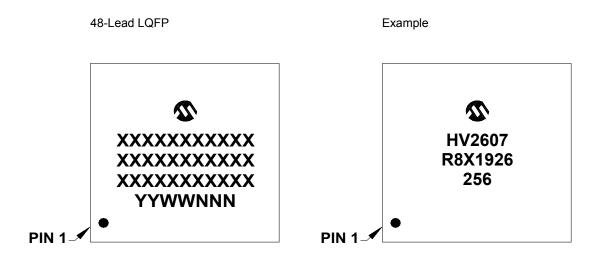


FIGURE 5-3: Layout Guidelines.

6.0 PACKAGING INFORMATION

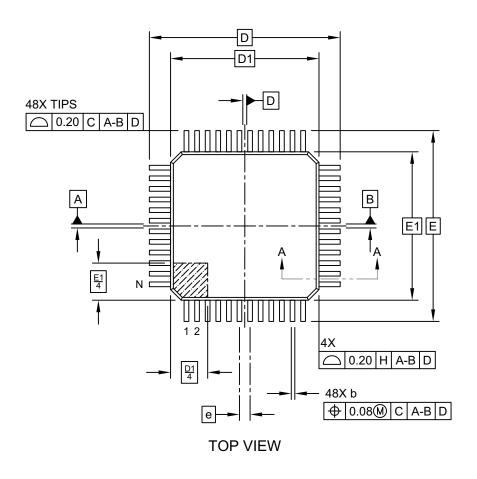
6.1 Package Marking Information

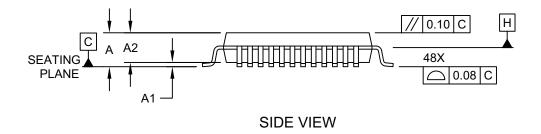


Legend:	XXX Y YY WW NNN	Product Code or Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code can be found on the outer packaging for this package.
t c	be carried	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available s for customer-specific information. Package may or may not include rate logo.

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

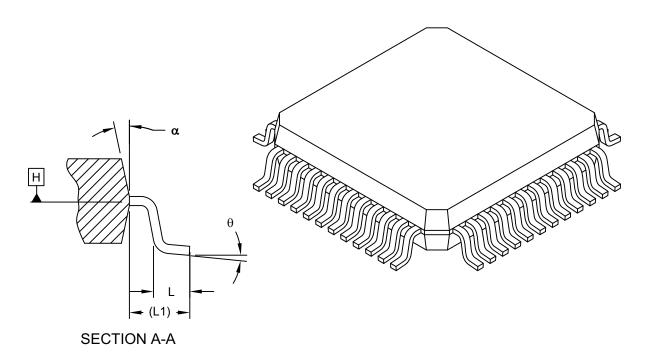




Microchip Technology Drawing C04-278 Rev A Sheet 1 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	N	ILLIMETER	S				
Dimension	MIN	NOM	MAX				
Number of Leads	Ν		48				
Lead Pitch	е		0.50 BSC				
Overall Height	Α	1.40	1.50	1.60			
Standoff	A1	0.05	0.10	0.15			
Molded Package Thickness	A2	1.35	1.40	1.45			
Foot Length	L	0.45	0.60	0.75			
Footprint	L1	1.00 REF					
Foot Angle	θ	0°	3.5°	7°			
Overall Width	Е		9.00 BSC				
Overall Length	D		9.00 BSC				
Molded Package Width	E1		7.00 BSC				
Molded Package Length	D1		7.00 BSC				
Lead Width	0.17	0.22	0.27				
Mold Draft Angle Top	α	11°	12°	13°			

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

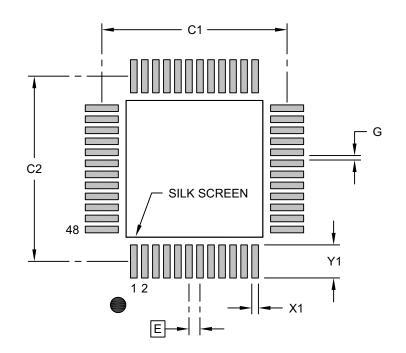
2. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-278 Rev A Sheet 2 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Contact Pitch	E		0.50 BSC		
Contact Pad Spacing	C1		8.40		
Contact Pad Spacing	C2		8.40		
Contact Pad Width (X48)	X1			0.30	
Contact Pad Length (X48)	Y1			1.50	
Contact Pad to Contact Pad (X44)	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2278 Rev A

APPENDIX A: REVISION HISTORY

Revision B (December 2020)

The following is the list of modifications:

- 1. Updated the Block Diagram.
- 2. Added the Negative Supply Voltage throughout **Section 1.0 "Electrical Characteristics"**.
- 3. Updated Figure 2-1.
- 4. Updated Table 2-1 with the Negative Supply Voltage pin.
- 5. Updated all the figures in Section 3.0 "Test Circuit Examples".
- 6. Updated Section 5.4 "Power-Up/Down Sequence and Decoupling Capacitor" and Section 5.5 "Layout Considerations".

Revision A (July 2020)

• Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X Tape and Reel	-X │ d Environmental	/XX Package		Example a) HV260	9 s: 7T-C/R8X:	No High-Voltage Bias, 16-Channel High-Voltage Analog Switch, 48-Lead LQFP package
Device:	HV2707:	No High-Voltage Bias, Analog Switch (Tape an No High-Voltage Bias, 1 Analog Switch with Blee of Switch (Tape and Re No High-Voltage Bias, 1 Analog Switch with Blee Switch (Tape and Reel)	nd Reel) 16-Channel High-Volta ed Resistor at Both Sic el) 16-Channel High-Volta ed Resistor at One Side	ge tes ge			
Environmental:	C =	Lead (Pb)-Free/ROHS-0	Compliant Package		Note 1:	part numb ordering p package.	Reel identifier only appears in the catalog per description. This identifier is used for purposes and is not printed on the device Check with your Microchip Sales Office for
Package:	R8X=	Low Profile Plastic Qua 7x7 mm Body, 48-Lead				package a	availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- · Microchip products meet the specifications contained in their particular Microchip Data Sheet.
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- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not
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