TJA1442

High-speed CAN transceiver with Standby mode

Rev. 1 — 12 August 2020 **Product data sheet**

1 General description

The TJA1442 is a member of the TJA144x family of transceivers that provide an interface between a Controller Area Network (CAN) or CAN FD (Flexible Data rate) protocol controller and the physical two-wire CAN bus. TJA144x transceivers implement the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5, and are fully interoperable with high-speed Classical CAN and CAN FD transceivers. All TJA144x variants enable reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

The TJA1442 is intended as a simple replacement for high-speed Classical CAN and CAN FD transceivers, such as the TJA1042 or TJA1044GT from NXP. It offers pin compatibility and is designed to avoid changes to hardware and software design, allowing the TJA1442 to be easily retrofitted to existing applications.

An AEC-Q100 Grade 0 variant, the TJR1442, is available for high temperature applications, supporting operation at 150 °C ambient temperature.

1.1 TJA1442 variants

The TJA1442 comes in two variants, each available in an SO8 or HVSON8 package:

- The TJA1442A is a high-speed CAN transceiver with Normal and Standby modes and a VIO supply pin. The VIO pin allows for direct interfacing with 3.3 V- and 5 V-supplied microcontrollers.
- The TJA1442B is a high-speed CAN transceiver with Normal and Standby modes.

2 Features and benefits

2.1 General

- ISO 11898-2:2016, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- Standard CAN and CAN FD data bit rates up to 5 Mbit/s
- Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI)
- Qualified according to AEC-Q100 Grade 1
- TJA1442A only: VIO input for interfacing with 3.3 V to 5 V microcontrollers
- All variants are available in SO8 and leadless HVSON8 (3.0 mm x 3.0 mm) packages; HVSON8 with improved Automated Optical Inspection (AOI) capability.
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.2 Predictable and fail-safe behavior

- Undervoltage detection with defined handling on all supply pins

- Full functionality guaranteed from the undervoltage detection thresholds up to the maximum limiting voltage values
- Defined behavior below the undervoltage detection thresholds
- Transceiver disengages from the bus (high-ohmic) when the supply voltage drops below the Off mode threshold
- Internal biasing of TXD and mode selection input pins, to enable defined fail-safe behavior

2.3 Low-power management

- Very low-current Standby mode with host and bus wake-up capability
- TJA1442A only: CAN wake-up receiver powered by V_{IO} allowing V_{CC} to be shut down
- CAN wake-up pattern filter time of 0.5 μs to 1.8 μs, meeting Classical CAN and CAN FD requirements

2.4 Protection

- High ESD handling capability on the bus pins (8 kV IEC and HBM)
- Bus pins protected against transients in automotive environments
- Transmit Data (TXD) dominant time-out function
- Thermally protected

3 Quick reference data

Table 1. Quick reference data

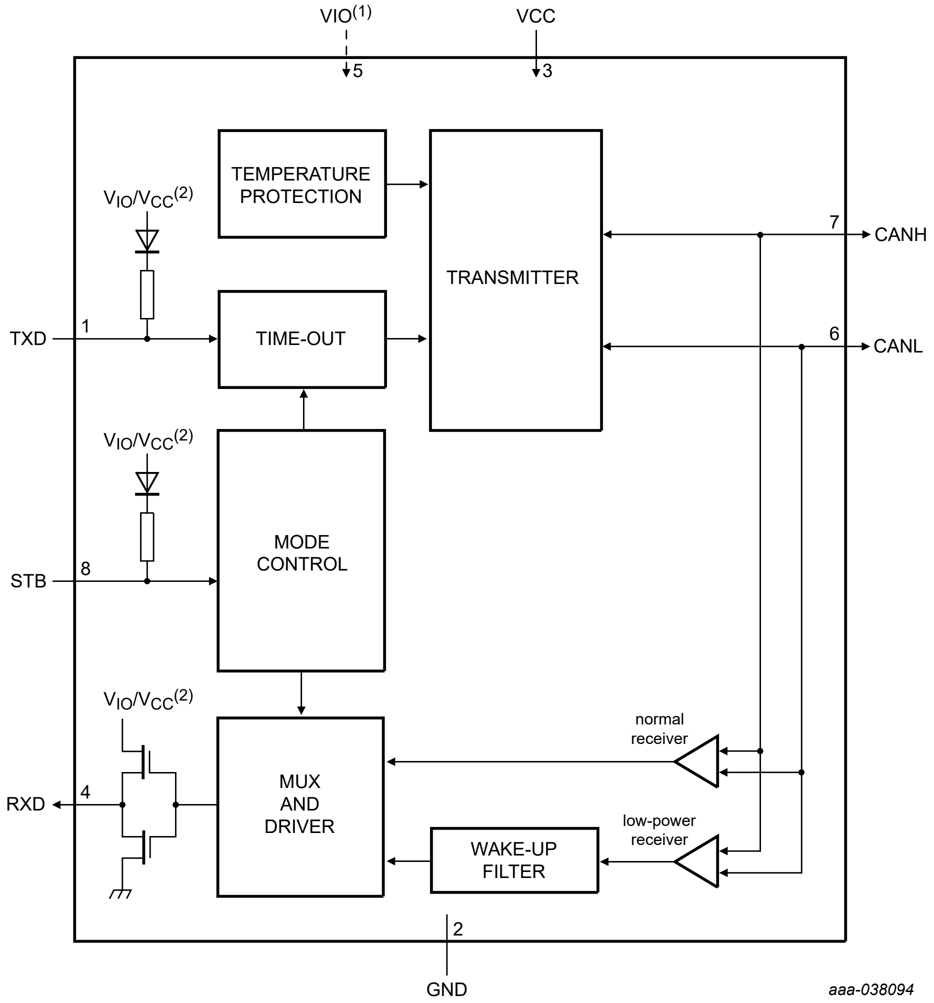
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
I_{CC}	supply current	Normal mode, dominant	-	38	60	mA
		Normal mode, recessive	-	4	7	mA
		Standby mode; TJA1442A	-	-	2	µA
		Standby mode; TJA1442B	-	8	12	µA
$V_{uvd(stb)(VCC)}$	standby undervoltage detection voltage on pin VCC		4	-	4.5	V
$V_{uvhys(stb)(VCC)}$	standby undervoltage hysteresis voltage on pin VCC		50	-	-	mV
$V_{uvd(swoff)(VCC)}$	switch-off undervoltage detection voltage on pin VCC	TJA1442B	2.65	-	2.95	V
V_{IO}	supply voltage on pin VIO		2.95	-	5.5	V
I_{IO}	supply current on pin VIO	Normal mode, dominant; V_{TXD} = 0 V	-	250	760	µA
		Normal mode, recessive; $V_{TXD} = V_{IO}$	-	150	460	µA
		Standby mode	-	8	11	µA
$V_{uvd(swoff)(VIO)}$	switch-off undervoltage detection voltage on pin VIO		2.65	-	2.95	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins CANH and CANL	-8	-	+8	kV
V_{CANH}	voltage on pin CANH	limiting value according to IEC 60134	-36	-	+40	V
V_{CANL}	voltage on pin CANL	limiting value according to IEC 60134	-36	-	+40	V
T_{vj}	virtual junction temperature		-40	-	+150	°C

4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1442AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJA1442BT			
TJA1442ATK	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT782-1
TJA1442BTK			

5 Block diagram



(1) V_{IO} is only available in the TJA1442A (pin 5 is not connected in the TJA1442B).

(2) V_{IO} in TJA1442A; V_{CC} in TJA1442B.

Figure 1. Block diagram

6 Pinning information

6.1 Pinning

TJA1442AT: SO8

TJA1442BT: SO8

TJA1442ATK: HVSON8

TJA1442BTK: HVSON8

Figure 2. Pin configuration diagrams

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
TXD	1	I	transmit data input; inputs data (from the CAN controller) to be written to the bus lines
GND[2]	2	G	ground
VCC	3	P	5 V supply voltage input
RXD	4	O	receive data output; outputs data read from the bus lines (to the CAN controller)
VIO	5	P	supply voltage input for I/O level adapter in TJA1442A
n.c.		-	not connected in TJA1442B
CANL	6	AIO	LOW-level CAN bus line
CANH	7	AIO	HIGH-level CAN bus line
STB	8	I	Standby mode control input; active-HIGH

[1] I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.

[2] HVSON package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

7 Functional description

7.1 Operating modes

The TJA1442 supports three operating modes, Normal, Standby and Off. The operating mode is selected via pin STB. See Table 4 for a description of the operating modes under normal supply conditions. Mode changes are completed after transition time $t_{t(moch)}$.

Table 4. Operating modes

Mode	Inputs		Outputs	
	Pin STB	Pin TXD	CAN driver	Pin RXD
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Standby	HIGH	X	biased to ground	follows BUS when wake-up detected
				HIGH when no wake-up detected
Off[1]	X	X	high-ohmic state	high-ohmic state

[1] Off mode is entered when the voltage on pin VIO (TJA1442A) or pin VCC (TJA1442B) is below the switch-off undervoltage detection threshold.

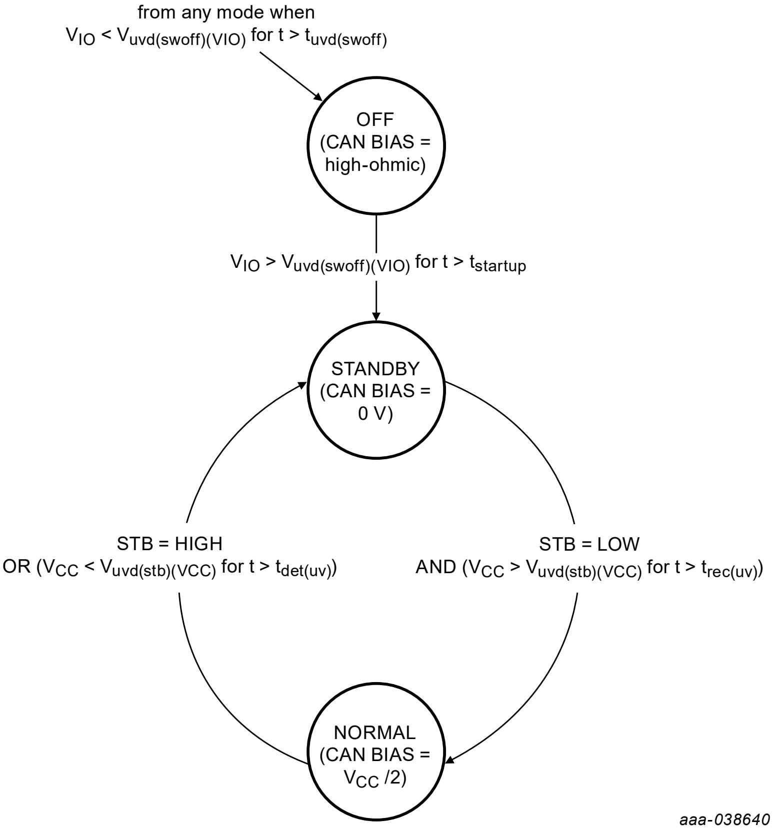


Figure 3. TJA1442A state diagram

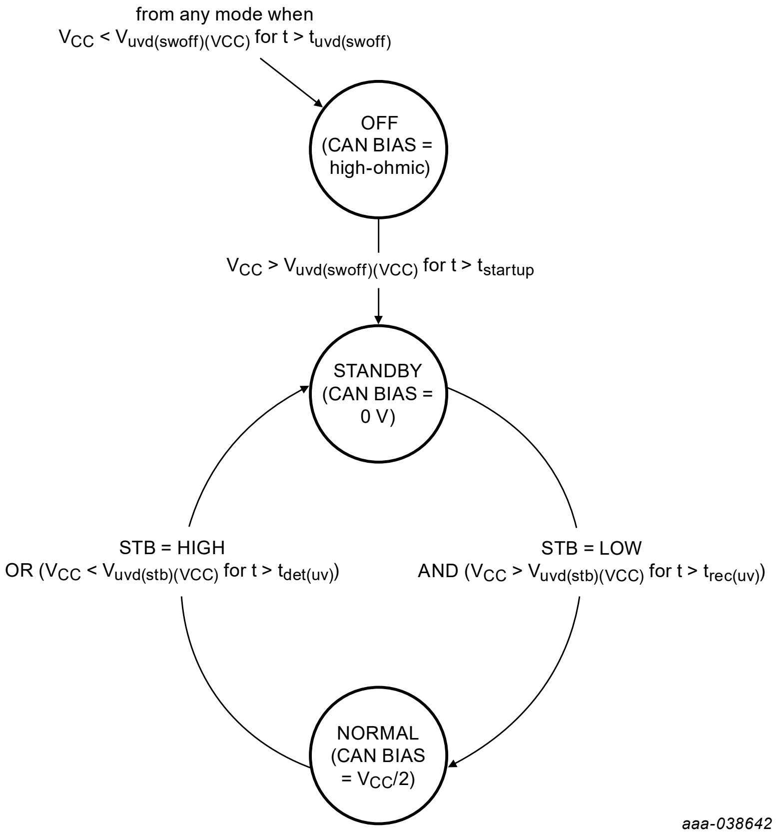


Figure 4. TJA1442B state diagram

7.1.1 Off mode

The TJA1442 switches to Off mode from any mode when the supply voltage (on pin VIO in the TJA1442A and VCC in the TJA1442B) falls below the switch-off undervoltage threshold ($V_{uvd(swoff)(VCC)}$ or $V_{uvd(swoff)(VIO)}$). This is the default mode when the supply is first connected.

In Off mode, the CAN pins and pin RXD are in a high-ohmic state.

7.1.2 Standby mode

When the supply voltage (V_{IO} for TJA1442A or V_{CC} for TJA1442B) rises above the switch-off undervoltage detection threshold, the TJA1442 starts to boot up, triggering an initialization procedure. The TJA1442 switches to the selected mode after $t_{startup}$.

Standby mode is selected when pin STB goes HIGH. In this mode, the transceiver is unable to transmit or receive data and a low-power receiver is activated to monitor the bus for a wake-up pattern. The transmitter and Normal-mode receiver blocks are switched off and the bus pins are biased to ground to minimize system supply current. Pin RXD follows the bus after a wake-up request has been detected.

A transition to Normal mode is triggered when STB is forced LOW (provided $V_{CC} > V_{uvd(stb)(VCC)}$ and $V_{IO} > V_{uvd(swoff)(VIO)}$ in the TJA1442A).

If V_{CC} is below $V_{uvd(stb)(VCC)}$ when STB goes LOW (with $V_{IO} > V_{uvd(swoff)(VIO)}$ in TJA1442A and $V_{CC} > V_{uvd(swoff)(VCC)}$ in TJA1442B), the TJA1442 will remain in Standby mode.

Pending wake-up events will be cleared and differential data on the bus pins converted to digital data via the low-power receiver and output on pin RXD.

In the TJA1442A, the low-power receiver is supplied from V_{IO} and can detect CAN bus activity when V_{IO} is above $V_{uvd(swoff)(VIO)}$ (even if V_{IO} is the only available supply voltage).

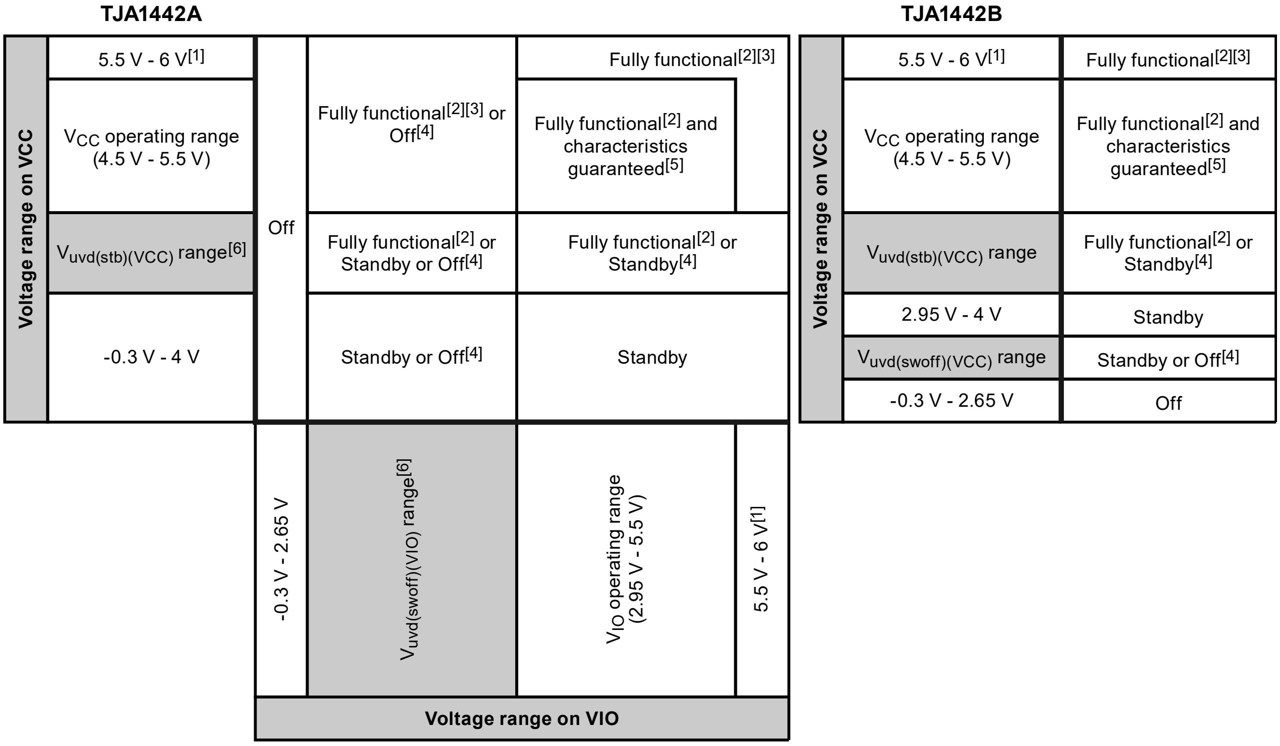
7.1.3 Normal mode

A LOW level on pin STB selects Normal mode, provided the supply voltage on pin VCC is above the standby undervoltage detection threshold, $V_{uvd(stb)(VCC)}$.

In this mode, the transceiver can transmit and receive data via bus lines CANH and CANL. Pin TXD must be HIGH at least once in Normal Mode before transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME. In recessive state, the output voltage on the bus pins is $V_{CC}/2$.

7.1.4 Operating modes and gap-free operation

Gap-free operation guarantees defined behavior at all voltage levels. Supply voltage-to-operating mode mapping is detailed in Figure 5 and in the state diagrams (Figure 3 and Figure 4).



[1] 6 V is the IEC 60134 Absolute Maximum Rating (AMR) for VCC and VIO (see Limiting values table). Above the AMR, irreversible changes in characteristics, functionality or performance may occur. Returning from above AMR to the operating range, datasheet characteristics and functionality cannot be guaranteed.

[2] Target transceiver functionality as described in this datasheet is applicable.

[3] Prolonged operation of the device outside the operating range may impact reliability over lifetime. Returning to the operating range, datasheet characteristics are guaranteed provided the AMR has not been exceeded.

[4] For a given value of V_{CC} (and V_{IO} in TJA1442A), a specific device will be in a single defined state determined by its undervoltage detection thresholds ($V_{uvd(stb)(VCC)}$, $V_{uvd(swoff)(VIO)}$ and $V_{uvd(swoff)(VCC)}$). The actual thresholds can vary between devices (within the ranges specified in this data sheet). To guarantee the device will be in a specific state, V_{IO} and V_{CC} must be either above the maximum or below the minimum thresholds specified for these undervoltage detection ranges.

[5] Datasheet characteristics are guaranteed within the V_{CC} and V_{IO} operating ranges. Exceptions are described in the Static and Dynamic characteristics tables.

[6] The following applies to TJA1442A:
- If both V_{CC} and V_{IO} are above the undervoltage threshold, the device is fully functional.
- If V_{CC} is below and V_{IO} above the undervoltage threshold, the device is in Standby mode.
- If V_{IO} is below the undervoltage threshold, the device is in Off mode, regardless of V_{CC}.

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Figure 5. Supply voltage ranges and gap-free operation

7.2 Remote wake-up (via the CAN bus)

The TJA1442 wakes up from Standby mode when a dedicated wake-up pattern (specified in ISO 11898-2: 2016) is detected on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

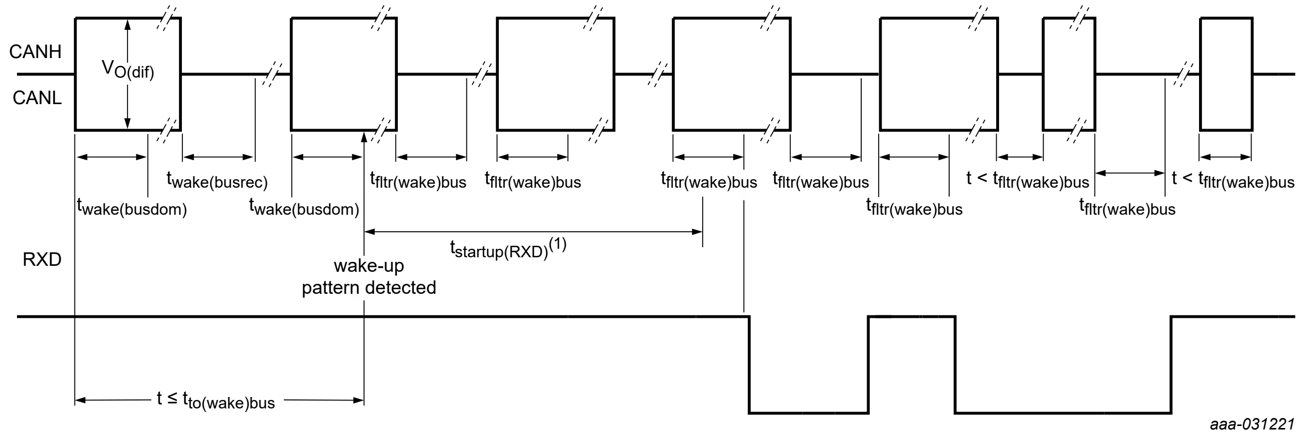
Dominant or recessive bits between the above mentioned phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 6). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.

After a wake-up sequence has been detected, the TJA1442 remains in Standby mode with the bus signals reflected on RXD after $t_{startup(RXD)}$. Note that dominant or recessive phases lasting less than $t_{fltr(wake)bus}$ will not be detected by the low-power differential receiver and will not be reflected on RXD in Standby mode.

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The device switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{CC} or V_{IO} switch-off undervoltage is detected ($V_{CC} < V_{uvd(swoff)(VCC)}$ or $V_{IO} < V_{uvd(swoff)(VIO)}$; see Section 7.3.3)



(1) During $t_{startup(RXD)}$, the low-power receiver is on but pin RXD is not active (i.e. HIGH/recessive). The first dominant pulse of width ≥ $t_{fltr(wake)bus}$ that ends after $t_{startup(RXD)}$ will trigger RXD to go LOW/dominant.

Figure 6. Wake-up timing

7.3 Fail-safe features

7.3.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH.

7.3.2 Internal biasing of TXD and STB input pins

Pins TXD and STB have internal pull-ups to V_{CC}/V_{IO} to ensure a safe, defined state in case one, or both, of these pins is left or becomes floating. Pull-up resistors are active on these pins in all states; they should be held at the V_{CC}/V_{IO} level in Standby mode to minimize supply current.

7.3.3 Undervoltage detection on pins VCC and VIO

If V_{CC} drops below the standby undervoltage detection threshold ($V_{uvd(stb)(VCC)}$) for $t_{det(uv)}$, the transceiver switches to Standby mode. The logic state of pin STB is ignored until V_{CC} has recovered.

In the TJA1442A, if V_{IO} drops below the switch-off undervoltage detection threshold ($V_{uvd(swoff)(VIO)}$) for $t_{uvd(swoff)}$, the transceiver switches to Off mode and disengages from the bus (high-ohmic) until V_{IO} has recovered.

In the TJA1442B, if V_{CC} drops below the switch-off undervoltage detection threshold ($V_{uvd(swoff)(VCC)}$) for $t_{uvd(swoff)}$, the transceiver switches to Off mode and disengages from the bus (high-ohmic) until V_{CC} has recovered.

7.3.4 Overtemperature protection

The device is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the CAN bus drivers are disabled. When the junction temperature drops below $T_{j(sd)rel}$, the CAN bus drivers recover once TXD has been reset to HIGH and Normal mode is selected (waiting for TXD to go HIGH prevents output driver oscillation due to small variations in temperature).

7.3.5 I/O levels

Pin VIO on the TJA1442A should be connected to the microcontroller supply voltage (see Figure 10). This adjusts the signal levels on pins TXD, RXD and STB to the I/O levels of the microcontroller, allowing for direct interfacing without additional glue logic. Pin VIO also provides the internal supply voltage for the low-power differential receiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin VCC.

All I/O levels are related to V_{CC} in the TJA1442B and are, therefore, compatible with 5 V microcontrollers. Spurious signals from the microcontroller on pin STB are filtered out with a filter time of $t_{fltr(IO)}$.

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	pins VCC, VIO (TJA1442A), TXD, STB	-0.3	+6	V
			-	+7[2]	V
		pins CANH, CANL	-36	+40	V
		pin RXD			
		TJA1442A	-0.3	V_{IO}+0.3[3]	V
		TJA1442B	-0.3	V_{CC}+0.3[3]	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-40	+40	V
V_{trt}	transient voltage	on pins CANH, CANL [4]			
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [5]			
		on pins CANH, CANL	-8	+8	kV
		Human Body Model (HBM)			
		on any pin [6]	-4	+4	kV
		on pins CANH, CANL [7]	-8	+8	kV
		Charged Device Model (CDM) [8]			
		on corner pins	-750	+750	V
		on any other pin	-500	+500	V
T_{vj}	virtual junction temperature	[9]	-40	+150	°C
T_{stg}	storage temperature		-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] The device can withstand voltages between 6 V and 7 V for a total of 20 s over the product lifetime.

[3] Subject to the qualifications detailed in Table notes 1 and 2 above for pins VCC, VIO, TXD and STB.

[4] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO7637.

[5] Verified by an external test house according to IEC TS 62228, Section 4.3.

[6] According to AEC-Q100-002.

[7] Pins stressed to reference group containing all ground and supply pins, emulating the application circuits (Figure 10 and Figure 11). HBM pulse as specified in AEC-Q100-002 used.

[8] According to AEC-Q100-011.

[9] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9 Thermal characteristics

Table 6. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO8	96	K/W
		HVSON8	57	K/W
$R_{th(j-c)}$	thermal resistance from junction to case[2]	HVSON8	19	K/W
$\Psi_{j\text{-}top}$	thermal characterization parameter from junction to top of package	SO8	9	K/W
		HVSON8	9	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 μm).

[2] Case temperature refers to the center of the heatsink at the bottom of the package.

10 Static characteristics

Table 7. Static characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJA1442A); R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	supply voltage		4.5	-	5.5	V
$V_{uvd(stb)}$	standby undervoltage detection voltage	[2]	4	-	4.5	V
$V_{uvhys(stb)}$	standby undervoltage hysteresis voltage		50	-	-	mV
$V_{uvd(swoff)}$	switch-off undervoltage detection voltage	TJA1442B [2]	2.65	-	2.95	V
I_{CC}	supply current	Normal mode				
		dominant; V_{TXD} = 0 V; t < $t_{to(dom)TXD}$	-	38	60	mA
		dominant; V_{TXD} = 0 V; short circuit on bus lines; -3 V < (V_{CANH} = V_{CANL}) < +40 V	-	-	125	mA
		recessive; V_{TXD} = V_{IO}[3]	-	4	7	mA
		Standby mode				
		TJA1442A; T_{vj} < 85 °C	-	-	2	μA
		TJA1442B; T_{vj} < 85 °C	-	8	12	μA
I/O level adapter supply; pin VIO (TJA1442A)						
V_{IO}	supply voltage		2.95	-	5.5	V
$V_{uvd(swoff)}$	switch-off undervoltage detection voltage	[2]	2.65	-	2.95	V
I_{IO}	supply current	Normal mode, dominant; V_{TXD} = 0 V	-	250	760	μA
		Normal mode, recessive; V_{TXD} = V_{IO}	-	150	460	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Standby mode; T_{vj} < 85 °C	-	8	11	μA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$[3]	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$[3]	V
$V_{hys(TXD)}$	hysteresis voltage on pin TXD		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	kΩ
C_i	input capacitance	[4]	-	-	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO}$[3] - 0.4 V	-10	-	-1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; bus dominant	1	-	10	mA
Standby control input; pin STB						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$[3]	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$[3]	V
V_{hys}	hysteresis voltage		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	kΩ
C_i	input capacitance	[4]	-	-	10	pF
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} ≥ 4.75 V				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; C_{SPLIT} = 4.7 nF; f_{TXD} = 250 kHz, 1 MHz or 2.5 MHz [4][5]	$0.9V_{CC}$	-	$1.1V_{CC}$	V
$V_{cm(step)}$	common mode voltage step	[4][5][6]	-150	-	+150	mV
$V_{cm(p-p)}$	peak-to-peak common mode voltage	[4][5][6]	-300	-	+300	mV
$V_{O(dif)}$	differential output voltage	dominant; Normal mode; V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} ≥ 4.75 V				
		R_L = 50 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω [4]	1.5	-	5	V
		recessive; no load				
		Normal mode; $V_{TXD} = V_{IO}$[3]	-50	-	+50	mV
		Standby mode	-0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	Normal mode; $V_{TXD} = V_{IO}$[3]; no load	2	2.5	3	V
		Standby mode; no load	-0.1	-	+0.1	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(RX)dif}$	differential receiver threshold voltage	$-12\ V \leq V_{CANH} \leq +12\ V$; $-12\ V \leq V_{CANL} \leq +12\ V$				
		Normal mode	0.5	-	0.9	V
		Standby mode	0.4	-	1.1	V
$V_{rec(RX)}$	receiver recessive voltage	$-12\ V \leq V_{CANH} \leq +12\ V$; $-12\ V \leq V_{CANL} \leq +12\ V$				
		Normal mode	-4	-	+0.5	V
		Standby mode	-4	-	+0.4	V
$V_{dom(RX)}$	receiver dominant voltage	$-12\ V \leq V_{CANH} \leq +12\ V$; $-12\ V \leq V_{CANL} \leq +12\ V$				
		Normal mode	0.9	-	9	V
		Standby mode	1.1	-	9	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	$-12\ V \leq V_{CANH} \leq +12\ V$; $-12\ V \leq V_{CANL} \leq +12\ V$; Normal mode	50	-	-	mV
$I_{O(sc)}$	short-circuit output current	$-15\ V \leq V_{CANH} \leq +40\ V$; $-15\ V \leq V_{CANL} \leq +40\ V$	-	-	115	mA
$I_{O(sc)rec}$	recessive short-circuit output current	$-27\ V \leq V_{CANH} \leq +32\ V$; $-27\ V \leq V_{CANL} \leq +32\ V$; Normal mode; $V_{TXD} = V_{IO}$[3]	-3	-	+3	mA
I_L	leakage current	$V_{CC} = V_{IO} = 0\ V$ or pins shorted to GND via 47 KΩ; $V_{CANH} = V_{CANL} = 5\ V$	-10	-	+10	μA
R_i	input resistance	$-2\ V \leq V_{CANL} \leq +7\ V$; $-2\ V \leq V_{CANH} \leq +7\ V$	25	40	50	kΩ
ΔR_i	input resistance deviation	$0\ V \leq V_{CANL} \leq +5\ V$; $0\ V \leq V_{CANH} \leq +5\ V$	-3	-	+3	%
$R_{i(dif)}$	differential input resistance	$-2\ V \leq V_{CANL} \leq +7\ V$; $-2\ V \leq V_{CANH} \leq +7\ V$	50	80	100	kΩ
$C_{i(cm)}$	common-mode input capacitance	[4]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[4]	-	-	10	pF
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	[4]	180	-	200	°C
$T_{j(sd)rel}$	release shutdown junction temperature	[4]	175	-	195	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.

[3] V_{CC} in TJA1442B

[4] Not tested in production; guaranteed by design.

[5] The test circuit used to measure the bus output voltage symmetry and the common-mode voltages (which includes C_{SPLIT}) is shown in Figure 13.

[6] See Figure 9

11 Dynamic characteristics

Table 8. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJA1442A); R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN timing characteristics; $t_{bit(TXD)} \geq 200$ ns; see Figure 7, Figure 8 and Figure 12						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	-	102.5	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	-	102.5	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal mode	-	-	127.5	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal mode	-	-	127.5	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	230	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	230	ns
CAN FD timing characteristics according to ISO 11898-2:2016; see Figure 8 and Figure 12						
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns	155	-	210	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	-65	-	+40	ns
		$t_{bit(TXD)}$ = 200 ns	-45	-	+15	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns	120	-	220	ns
Dominant time-out time; pin TXD						
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode [2] [3]	0.8	-	9	ms
Bus wake-up times; pins CANH and CANL; Figure 6						
$t_{wake(busdom)}$	bus dominant wake-up time	Standby mode [2] [4]	0.5	-	1.8	μs
$t_{wake(busrec)}$	bus recessive wake-up time	Standby mode [2] [4]	0.5	-	1.8	μs
$t_{to(wake)bus}$	bus wake-up time-out time	Standby mode [2] [3]	0.8	-	9	ms
$t_{fltr(wake)bus}$	bus wake-up filter time	Standby mode [2]	-	-	1.8	μs
Mode transitions						
$t_{t(moch)}$	mode change transition time	[2]	-	-	50	μs
$t_{startup}$	start-up time	[2]	-	-	1	ms
$t_{startup(RXD)}$	RXD start-up time	to Standby mode after wake-up [2] [5]	4	-	20	μs
IO filter; pin STB						
$t_{fltr(IO)}$	IO filter time	[6]	1	-	5	μs
Undervoltage detection; Figure 3 and Figure 4						
$t_{det(uv)}$	undervoltage detection time	on pin VCC [2]	-	-	30	μs
$t_{uvd(swoff)}$	switch-off undervoltage detection time	on pin VCC; TJA1442B [2]	-	-	30	μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		on pin VIO; TJA1442A [2]			30	μs
$t_{rec(uv)}$	undervoltage recovery time	on pin VCC [2]	-	-	50	μs

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] Not tested in production; guaranteed by design.

[3] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

[4] A dominant/recessive phase shorter than the min value is guaranteed not be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.

[5] When a wake-up is detected, RXD start-up time is between the min and max values. RXD cannot be relied on below the min value; RXD can be relied on above the max value; see Figure 6.

[6] Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.

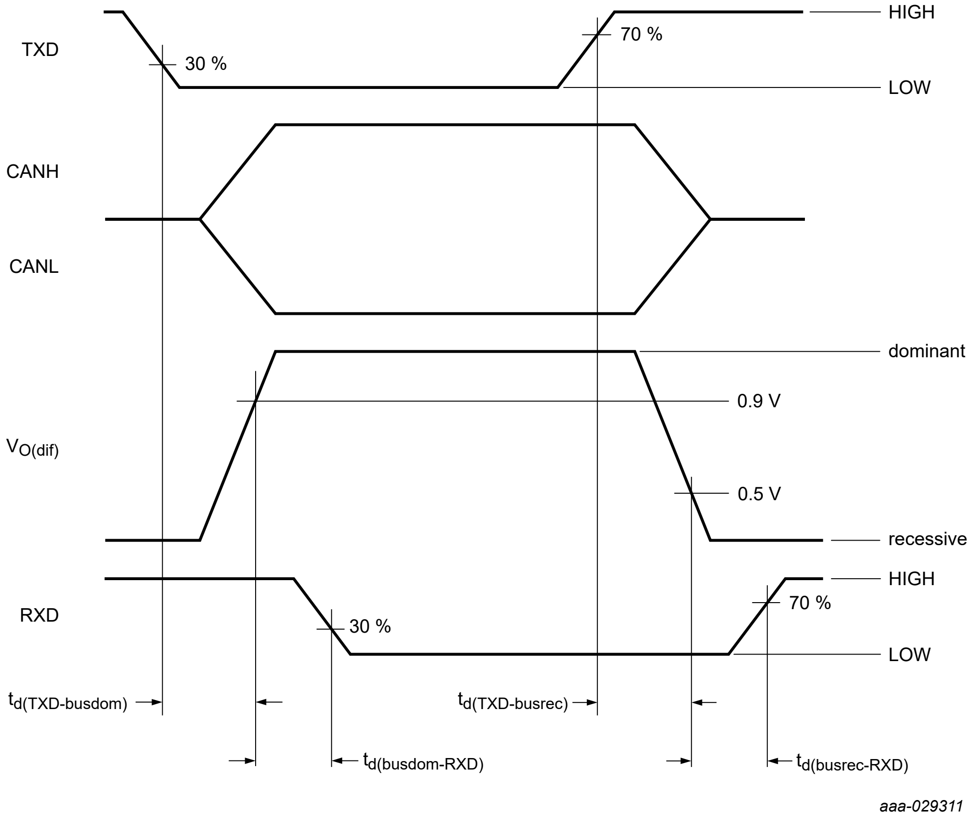


Figure 7. CAN transceiver timing diagram

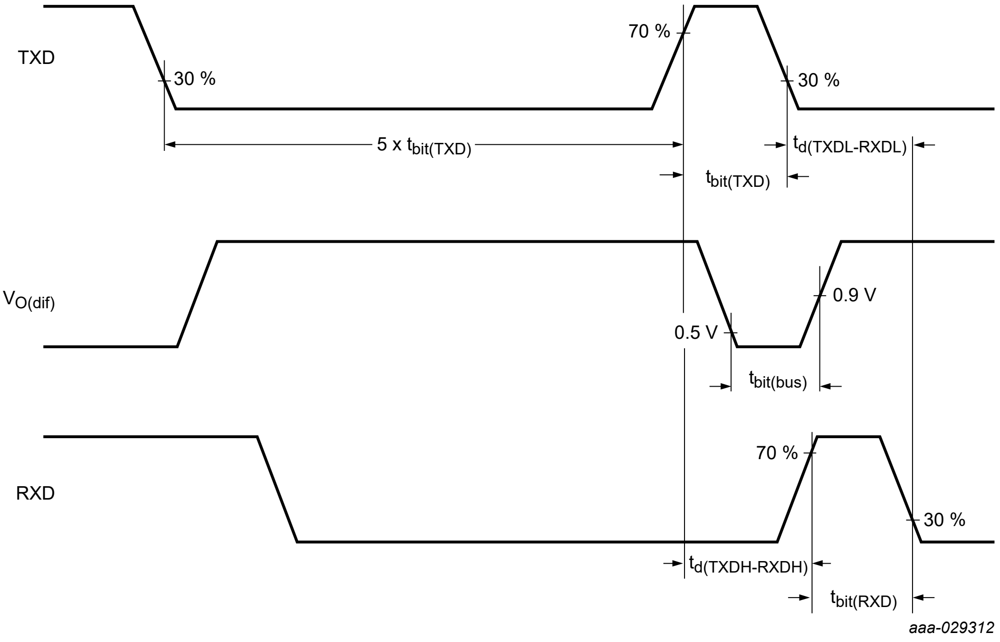


Figure 8. CAN FD timing definitions according to ISO 11898-2:2016

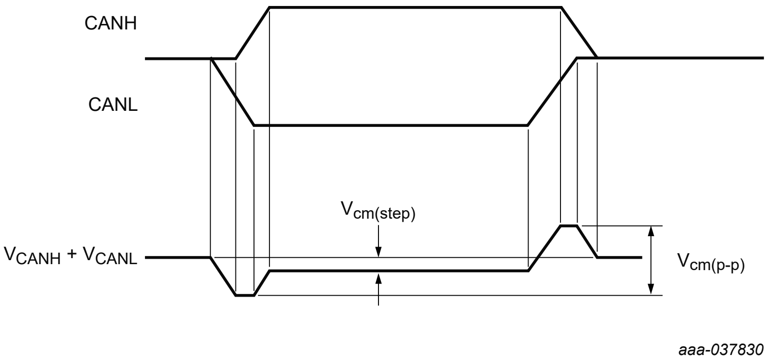
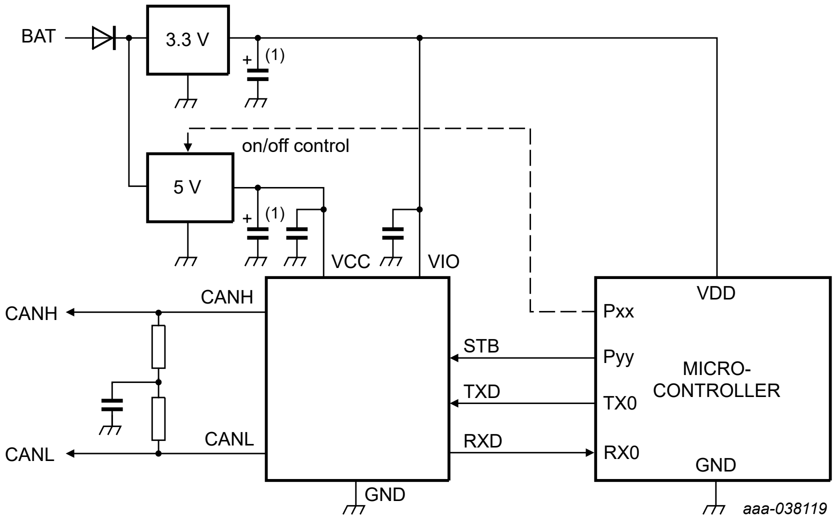


Figure 9. CAN bus common-mode voltage

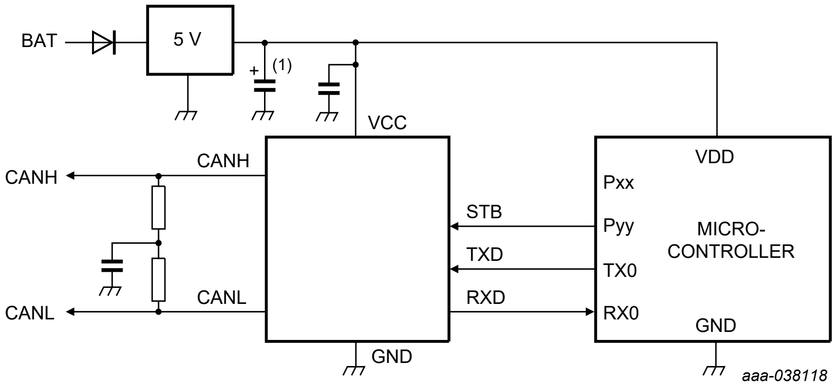
12 Application information

12.1 Application diagrams



(1) Optional, depends on regulator.

Figure 10. Typical TJA1442A application with a 3.3 V microcontroller



(1) Optional, depends on regulator.

Figure 11. Typical TJA1442B application with a 5 V microcontroller

12.2 Application hints

Further information on the application of the TJA1442 can be found in NXP application hints AH2002 '*TJx144x/TJx146x Application Hints*', available on request from NXP Semiconductors.

13 Test information

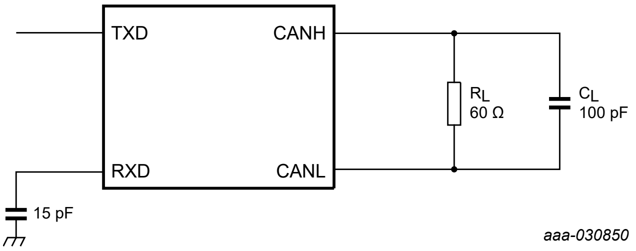


Figure 12. CAN transceiver timing test circuit

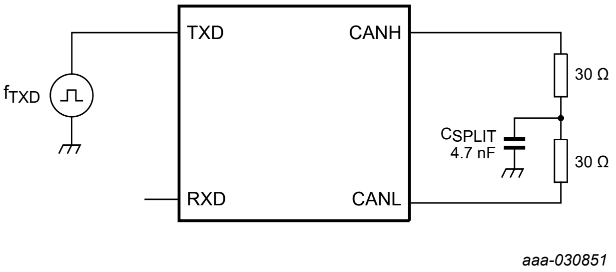


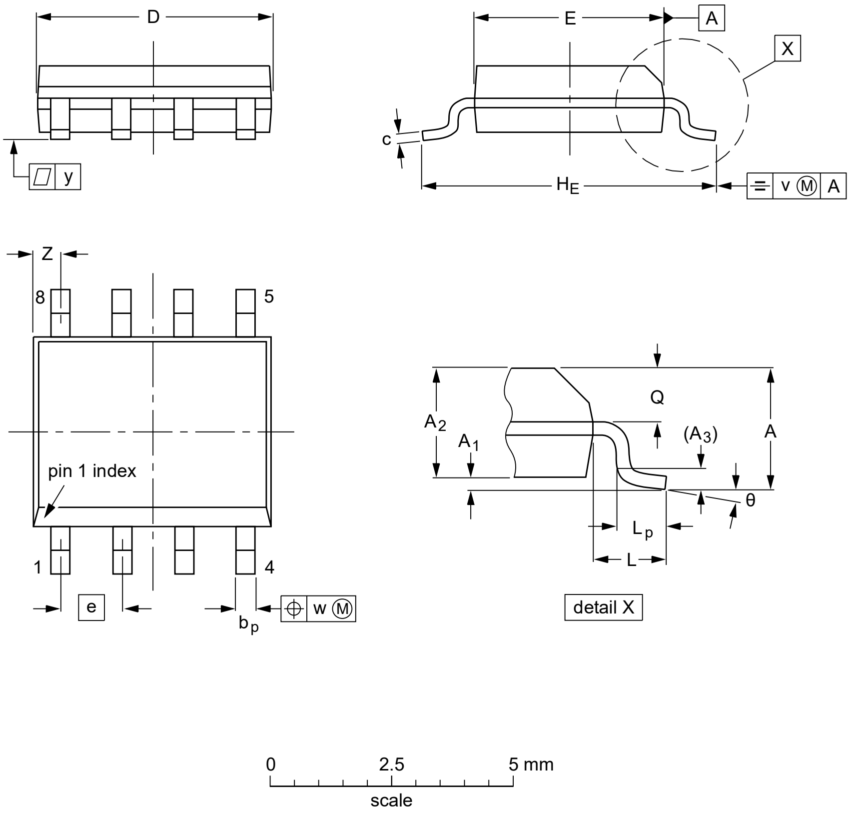
Figure 13. Test circuit for measuring transceiver driver symmetry

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-H - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

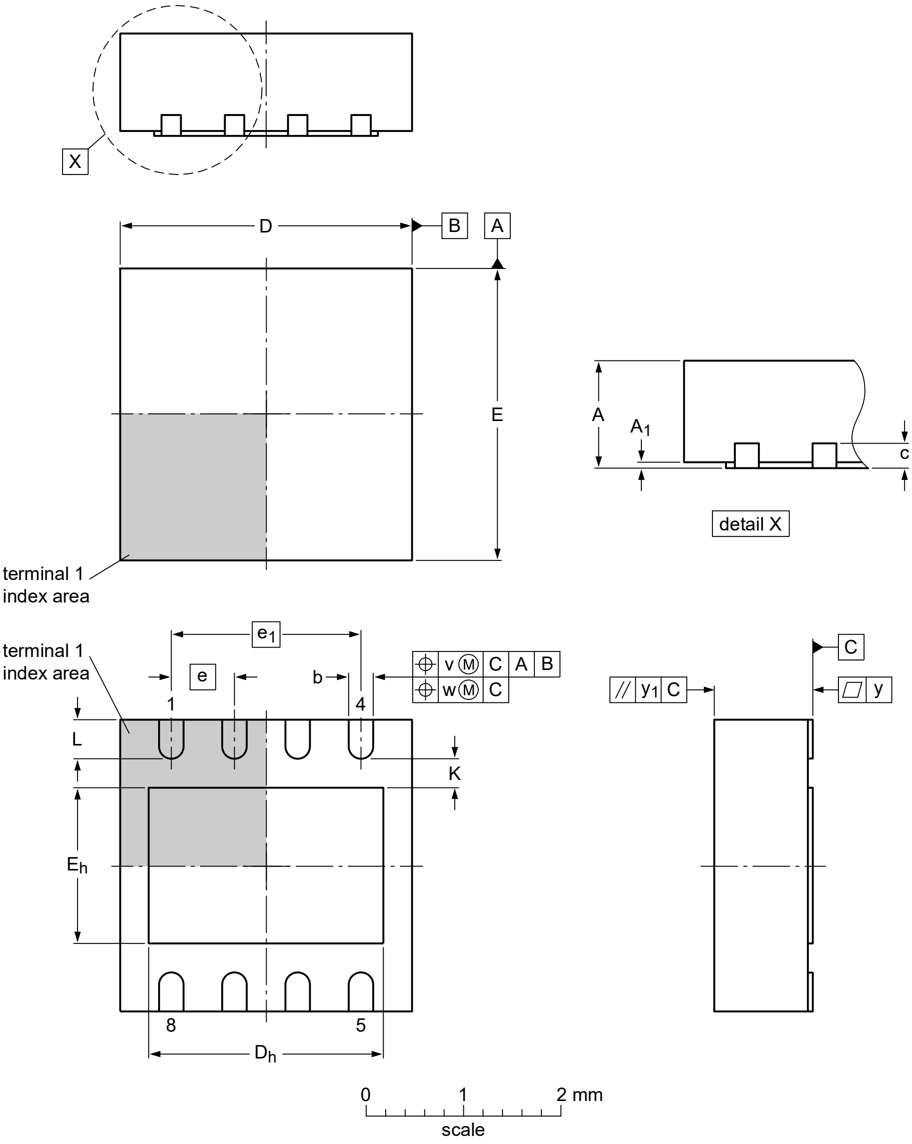
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 14. Package outline SOT96-1 (SO8)

**HVSON8: plastic thermal enhanced very thin small outline package; no leads;
8 terminals; body 3 x 3 x 0.85 mm** **SOT782-1**



Dimensions

Unit(1)		A	A1	b	c	D	Dh	E	Eh	e	e1	K	L	v	w	y	y1
mm	max	1.00	0.05	0.35		3.10	2.45	3.10	1.65			0.35	0.45				
	nom	0.85	0.03	0.30	0.2	3.00	2.40	3.00	1.60	0.65	1.95	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		2.90	2.35	2.90	1.55			0.25	0.35				

Note
1. Plastic or metal protrusions of 0.075 maximum per side are not included.

sot782-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT782-1	- - -	MO-229	- - -			~~09-08-25~~ 09-08-28

Figure 15. Package outline SOT782-1 (HVSON8)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and Table 10

Table 9. SnPb eutectic process (from J-STD-020D)

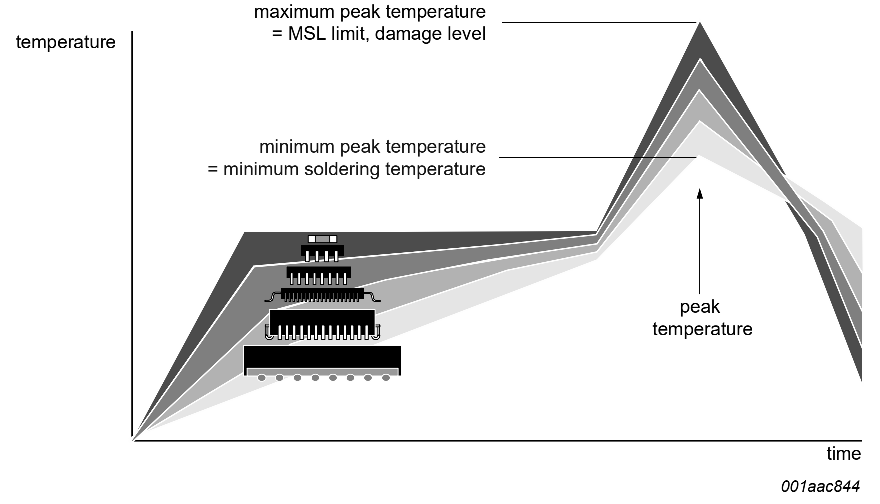
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Figure 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

17 Soldering of HVSON packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can be found in the following application note:

- AN10365 “Surface mount reflow soldering description”

18 Appendix: ISO 11898-2:2016 parameter cross-reference list

Table 11. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{SYM}	V_{TXsym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)}$	short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
Optional HS-PMA transmit dominant time-out			
Transmit dominant time-out, long	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant time-out, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_i	input resistance
Matching of internal resistance	MR	ΔR_i	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}	receiver timing symmetry
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating VCAN_H and VCAN_L			
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA bus biasing control timings			
CAN activity filter time, long	t_{Filter}	$t_{wake(busdom)}$[1] $t_{wake(busrec)}$	bus dominant wake-up time bus recessive wake-up time
CAN activity filter time, short			
Wake-up time-out, short	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up time-out, long			

[1] $t_{fltr(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality

19 Legal information

19.1 Data sheet status

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Contents

Date of release: 12 August 2020
Document identifier: TJA1442