Product Change Notification / SYST-08FUMQ885

Date:

16-Feb-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-08FUMQ885_Affected_CPN_02162021.pdf
SYST-08FUMQ885_Affected_CPN_02162021.csv

Notification Text:

SYST-08FUMQ885

Microchip has released a new Product Documents for the PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:1) Added Module 8.1. Other minor corrections.
2) Data Sheet Clarifications: Removed previous Module 1 as it was added to the data sheet and is no longer needed in this document.
3) Added new Module 1: Nonvolatile Memory (NVM) Control.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 16 Feb 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.

If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

PIC18F25K83-E/ML
PIC18F25K83-E/MLVAO
PIC18F25K83-E/MX
PIC18F25K83-E/SO
PIC18F25K83-E/SP
PIC18F25K83-E/SS
PIC18F25K83-E/SSVAO
PIC18F25K83-I/ML
PIC18F25K83-I/MX
PIC18F25K83-I/SO
PIC18F25K83-I/SP
PIC18F25K83-I/SS
PIC18F25K83T-E/SO
PIC18F25K83T-E/SS
PIC18F25K83T-I/ML
PIC18F25K83T-I/MX
PIC18F25K83T-I/SO
PIC18F25K83T-I/SS
PIC18F26K83-E/5NVAO
PIC18F26K83-E/ML
PIC18F26K83-E/MLVAO
PIC18F26K83-E/MX
PIC18F26K83-E/SO
PIC18F26K83-E/SP
PIC18F26K83-E/SS
PIC18F26K83-E/SSVAO
PIC18F26K83-I/ML
PIC18F26K83-I/MX
PIC18F26K83-I/SO
PIC18F26K83-I/SP
PIC18F26K83-I/SS
PIC18F26K83T-E/5NVAO
PIC18F26K83T-I/ML
PIC18F26K83T-I/MX
PIC18F26K83T-I/SO
PIC18F26K83T-I/SS
PIC18F26K83T-I/SS020
PIC18LF25K83-E/ML
PIC18LF25K83-E/MX
PIC18LF25K83-E/SO
PIC18LF25K83-E/SP
PIC18LF25K83-E/SS
PIC18LF25K83-I/ML
PIC18LF25K83-I/MX
PIC18LF25K83-I/SO
PIC18LF25K83-I/SP

PIC18LF25K83-I/SS
PIC18LF25K83T-I/ML
PIC18LF25K83T-I/MX
PIC18LF25K83T-I/SO
PIC18LF25K83T-I/SS
PIC18LF26K83-E/ML
PIC18LF26K83-E/MX
PIC18LF26K83-E/SO
PIC18LF26K83-E/SP
PIC18LF26K83-E/SS
PIC18LF26K83-I/ML
PIC18LF26K83-I/MX
PIC18LF26K83-I/SO
PIC18LF26K83-I/SP
PIC18LF26K83-I/SS
PIC18LF26K83T-I/ML
PIC18LF26K83T-I/MX
PIC18LF26K83T-I/SO
PIC18LF26K83T-I/SS

PIC18(L)F25/26K83

PIC18(L)F25/26K83 Family
Silicon Errata and Data Sheet Clarification

The PIC18(L)F25/26K83 family devices that you have received conform functionally to the current Device Data Sheet (DS40001943**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18(L)F25/26K83 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18(L)F25/26K83 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID<13:0>(1), (2)	Revision ID for Silicon Revision	
		A2	A3
PIC18F25K83	6EE0h	A002	A003
PIC18F26K83	6EC0h	A002	A003
PIC18LF25K83	6F20h	A002	A003
PIC18LF26K83	6F00h	A002	A003

Note 1: The Revision ID is located in addresses 3FFFFCh-3FFFFDh and Device ID is located in addresses 3FFFFEh-3FFFFFh.

2: Refer to the "PIC18(L)F25/26K83 *Memory Programming Specification*" (DS40001886) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revisions(1)	
				A2	A3
Electrical Specifications	SMBus 3.0	1.1	SMBus 3.0 logic levels.	X	X
	Fixed Voltage Reference (FVR) Accuracy	1.2	FVR output tolerance may be higher than specified at temperatures below 20°C.	X	X
Direct Memory Access (DMA) Specifications	DMA in Doze mode	2.1	DMA transfers may not work when CPU is in Doze mode.	X	
Analog-to-Digital Converter Computation (ADC2)	Burst Average mode Double Sampling	3.1	The ADC^2 does not trigger the second conversion when operated in non-continuous double-sampling Burst Average mode.	X	
Nonvolatile Memory (NVM) Control	WRERR bit Functionality	4.1	WRERR bit cannot be cleared in hardware after being set once.	X	
Windowed Watchdog Timer (WWDT)	WWDT Operation in Doze mode	5.1	Window violation occurs when WWDT is operated in Doze mode.	X	
Power-Saving Operation Modes	Low-Power Sleep mode	6.1	Low-Power Sleep mode does not operate at 3.1V <V_{DD} <3.3V.	X	
Program Flash Memory	Endurance of PFM Cell for LF Devices	7.1	Endurance of PFM cell is lower than specified.	X	X
In-Circuit Debugging (ICD)	Software Breakpoints	8.1	Software breakpoints are not available.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: Electrical Specifications

1.1 SMBus 3.0

The SMBus 3.0 V_{IL} specification (Parameter D305) is temperature and V_{DD} dependent. Refer to the table below.

Temperature	V_{DD}	D305 SMBus 3.0 V_{IL} Specification
-40°C	1.8V	0.6V
-40°C	5.5V	0.8V
25°C	1.8V	0.6V
25°C	5.5V	0.8V
85°C	1.8V	0.6V
85°C	5.5V	0.6V
125°C	1.8V	0.5V
125°C	5.5V	0.6V

Work around

None.

Affected Silicon Revisions

A2	A3						
X	X						

1.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A2	A3						
X	X						

2. Module: Direct Memory Access (DMA) Specifications

2.1 DMA in Doze Mode 3.0

When the CPU is operated in Doze mode, DMA transfers may not work as expected.

Work around

None.

Affected Silicon Revisions

A2	A3						
X							

3. Module: Analog-to-Digital Converter Computation (ADC^2)

3.1 Burst Average Mode Double Sampling

When the ADC^2 is operated in Burst Average mode (MD = 0b011 in the ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = 0 in the ADCON0 register and DSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond 0b1 toward the value in the ADRPT register.

Work around

When operating the ADC^2 in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = 1 in the ADCON0 register) and set the Stop-On-Interrupt bit (SOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and re-trigger ADC^2 as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC^2 in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = 0 in the ADCON1 register), compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in software.

Affected Silicon Revisions

A2	A3						
X							

4. Module: Nonvolatile Memory (NVM) Control

4.1 WRERR Bit Functionality

When a Reset is issued while an NVM high-voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again, regardless of whether an NVM operation is in progress or not.

Work around

None.

Affected Silicon Revisions

A2	A3						
X							

5. Module: Windowed Watchdog Timer (WWDT)

5.1 WWDT Operation in Doze Mode

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT, even though the window is open and armed.

Work around

Do not operate the WWDT in Doze mode.

Affected Silicon Revisions

A2	A3						
X							

6. Module: Power-Saving Operation Modes

6.1 Low-Power Sleep Mode in F Devices

When the CLRWDT instruction is issued in Doze mode, a window violation error occurs in WWDT, even though the window is open and armed.

Work around

a) If wake-up from Sleep is needed at 3.1V < V_{DD} <3.3V, operate the F device in Normal Power mode (VREGPM = 0).

b) If wake-up from Sleep is needed at 3.1V <V_{DD} <3.3V, enable the Fixed Voltage Reference (EN = 1 in the FVRCON register). This increases the current in Sleep mode by typically 7 μA.

Affected Silicon Revisions

A2	A3						
X							

7. Module: Program Flash Memory

7.1 Endurance of PFM Cell for LF Devices

The Flash memory cell endurance specification (Parameter MEM30) for this device family is 1K cycles.

Work around

None.

Affected Silicon Revisions

A2	A3						
X	X						

8. Module: In-Circuit Debugging (ICD)

8.1 Software Breakpoints

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

A2	A3						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001943**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Nonvolatile Memory (NVM) Control

Section 13.2 incorrectly states the writing access for User IDs. The corrected Section 13.2 is shown below with changes highlighted in **bold**.

13.2.2 Writing Access

Only the User IDs and CONFIG words have write access enabled. The user can write to these blocks by setting the REG bits to 0b01 or0b11. The WREN bit in NVMCON1 must be set to enable writes. This prevents accidental writes to the CONFIG words due to errant (unexpected) code execution. The WREN bit should be kept clear at all times, except when updating the CONFIG words. The WREN bit is not cleared by hardware. The WR bit will be inhibited from being set unless the WREN bit is set.

13.2.2.1 Writing to User IDs

The user needs to load the TBLPTR and TABLAT registers with the address and data byte respectively. **Writing to the User IDs does not include an implicit erase cycle like the EEPROM/CONFIG words; hence, the user needs to clear the memory location pointed by TBLPTR, first by setting the FREE bit and executing the write command**. An unlock sequence is required before setting the **writing command**. **A single User ID byte is cleared at once (set to 0xFF). CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set and the CPU resumes operation.**

Once the User ID byte is cleared, the user can now write the new value to that location. To do this, the user needs to execute TBLWT instruction, followed by executing the write command. An unlock sequence is required before setting the writing command. A single User ID byte is written at once. CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set. The new User ID value takes effect when the CPU resumes operation.

During the above operations, if TBLPTR points to an invalid address location (see Table 13-1), WR bit is cleared without any effect and WRERR is set.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev D Document (2/2021)

Added Module 8.1. Other minor corrections.

Data Sheet Clarifications:

Removed previous Module 1 as it was added to the data sheet and is no longer needed in this document.

Added new Module 1: Nonvolatile Memory (NVM) Control.

Rev C Document (1/2020)

Removed Module 1.2, renumbered Module 1.3 and updated; Updated Table 2.

Data Sheet Clarifications:

Added Module 1.

Rev B Document (2/2019)

Added silicon revision A3.

Added Module 1.3: Fixed Voltage Reference (FVR) Accuracy. Added Module 2: Direct Memory Access (DMA). Added Module 3: Analog-to-Digital Converter with Computation (ADC^2). Added Module 4: Nonvolatile Memory (NVM) Control. Added Module 5: Windowed Watchdog Timer (WWDT). Added Module 6: Power-Saving Operation Modes. Added module 7: Program Flash Memory.

Rev A Document (11/2017)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

ISBN: 978-1-5224-7549-1

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820