Product Change Notification / SYST-10BNQU415

Date:

11-Mar-2021

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-10BNQU415_Affected_CPN_03112021.pdf
SYST-10BNQU415_Affected_CPN_03112021.csv

Notification Text:

SYST-10BNQU415

Microchip has released a new Product Documents for the PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:
1. Removed A5 from the Affected Silicon Revisions table in silicon errata issue 4 (Primary XT and HS Oscillator (POSC) because this issue only affects silicon revisions A3 and A4.
2. The I2C standard uses the terminology “Master” and “Slave.” The equivalent Microchip terminology used in this document is “Host” and “Client”, respectively.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 11 March 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC24FJ128GA702-E/ML
PIC24FJ128GA702-E/MV
PIC24FJ128GA702-E/SO
PIC24FJ128GA702-E/SS
PIC24FJ128GA702-I/ML
PIC24FJ128GA702-I/MV
PIC24FJ128GA702-I/SO
PIC24FJ128GA702-I/SS
PIC24FJ128GA702T-I/ML
PIC24FJ128GA702T-I/MV
PIC24FJ128GA702T-I/SO
PIC24FJ128GA702T-I/SS
PIC24FJ128GA704-E/PT
PIC24FJ128GA704-I/PT
PIC24FJ128GA704-I/PTC01
PIC24FJ128GA704T-I/PT
PIC24FJ128GA704T-I/PTC01
PIC24FJ128GA705-E/M4
PIC24FJ128GA705-E/PT
PIC24FJ128GA705-I/M4
PIC24FJ128GA705-I/PT
PIC24FJ128GA705T-I/M4
PIC24FJ128GA705T-I/PT
PIC24FJ256GA702-E/ML
PIC24FJ256GA702-E/MV
PIC24FJ256GA702-E/SO
PIC24FJ256GA702-E/SP
PIC24FJ256GA702-E/SS
PIC24FJ256GA702-I/ML
PIC24FJ256GA702-I/MV
PIC24FJ256GA702-I/SO
PIC24FJ256GA702-I/SP
PIC24FJ256GA702-I/SS
PIC24FJ256GA702T-I/ML
PIC24FJ256GA702T-I/MV
PIC24FJ256GA702T-I/SO
PIC24FJ256GA702T-I/SS
PIC24FJ256GA704-E/PT
PIC24FJ256GA704-E/PTC02
PIC24FJ256GA704-I/PT
PIC24FJ256GA704T-E/PTC02
PIC24FJ256GA704T-I/PT
PIC24FJ256GA705-E/M4
PIC24FJ256GA705-E/PT
PIC24FJ256GA705-I/M4
PIC24FJ256GA705-I/PT

PIC24FJ256GA705-I/PTC03
PIC24FJ256GA705T-I/M4
PIC24FJ256GA705T-I/PT
PIC24FJ64GA702-E/ML
PIC24FJ64GA702-E/MV
PIC24FJ64GA702-E/SO
PIC24FJ64GA702-E/SS
PIC24FJ64GA702-I/ML
PIC24FJ64GA702-I/MV
PIC24FJ64GA702-I/SO
PIC24FJ64GA702-I/SS
PIC24FJ64GA702T-I/ML
PIC24FJ64GA702T-I/MV
PIC24FJ64GA702T-I/SO
PIC24FJ64GA702T-I/SS
PIC24FJ64GA704-E/PT
PIC24FJ64GA704-I/PT
PIC24FJ64GA704T-I/PT
PIC24FJ64GA705-E/M4
PIC24FJ64GA705-E/PT
PIC24FJ64GA705-I/M4
PIC24FJ64GA705-I/PT
PIC24FJ64GA705T-E/M4
PIC24FJ64GA705T-I/M4
PIC24FJ64GA705T-I/PT

PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ256GA705 family devices that you have received conform functionally to the current Device Data Sheet (DS30010118**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ256GA705 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on Page 12, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ256GA705 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A3	A4	A5			A3	A4	A5
PIC24FJ64GA705	0x7507	0x03	0x04	0x05	PIC24FJ256GA704	0x750D	0x03	0x04	0x05
PIC24FJ128GA705	0x750B				PIC24FJ64GA702	0x7506			
PIC24FJ256GA705	0x750F				PIC24FJ128GA702	0x750A			
PIC24FJ64GA704	0x7505				PIC24FJ256GA702	0x750E			
PIC24FJ128GA704	0x7509				—				

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJ256GA705 Family Flash Programming Specification"* (DS30010102) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A3	A4	A5
I2C	Address Hold	1.	In Host mode when AHEN = 1 (Address Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.	X	X	X
Reset	Trap Conflict	2.	The TRAPR bit is not getting set when a hard trap conflict occurs.	X	X	X
I2C	Data Hold	3.	In Client mode when DHEN = 1 (Data Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of data reception, then a client interrupt will not occur after the 8th clock.	X	X	X
Primary XT and HS Oscillator (POSC)	Primary Oscillator Start-up Timer (OST)	4.	OST may indicate oscillator is ready for use too early.	X	X	
Power	Retention Sleep	5.	When the device wakes up from Retention Sleep mode (RETEN bit (RCON[12]) = 1, $\overline{\text{LPCFG}}$ bit (FPOR[2]) = 0), a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.	X		
Power	Power BOR	6.	The main BOR may not function on some devices.	X		
I2C	Client Mode	7.	Bus data can get corrupted when it matches with one of the client addresses connected to the bus.	X	X	X
I2C	Client Mode	8.	In 10-Bit Addressing Client mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence.	X	X	X
I2C	Client Receive Mode	9.	The Acknowledge Time Status bit (ACKTIM) is asserted only if the Address Hold Enable (AHEN) or Data Hold Enable (DHEN) bit is enabled.	X	X	X
I2C	Bus Collisions	10.	In Client mode, false bus collision triggers are generated when bus collision is enabled (SBCDE = 1).	X	X	X
I2C	Hold Time	11.	Minimum hold time of 300 ns is not achieved when the SDAx Hold Time Selection bit (SDAHT) is set.	X	X	X
I2C	Client Mode	12.	In Client mode, the Bus Collision Detect bit (BCL) cannot be cleared when bus collision detection is enabled (SBCDE = 1).	X	X	X
I2C	Client Mode	13.	In Client mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).	X	X	X
UART	Break Character Transmission	14.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.	X	X	X
ADC	Differential Nonlinearity	15.	Increase DNL specification on the positive side.	X	X	X
ADC	Current	16.	ADC draws additional current when enabled.	X	X	
Oscillator	FSCM	17.	RESET instruction in oscillator trap causes abnormal behavior.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A3	A4	A5
CCP	32-Bit Mode	18.	MCCP timer in 32-bit mode cannot be cleared by writing a zero to the Timer register.	X	X	X
Oscillator	FSCM	19.	When FSCM is enabled and selected clock fails, an oscillator trap may not occur.	X	X	
Oscillator	96 MHz PLL Mode	20.	PLL in 96 MHz mode may not operate under certain conditions.	X	X	
I^2C	Multiple Client Mode	21.	In applications with multiple I^2C Client and General Call enabled, unexpected behavior is observed in the unaddressed Client.	X	X	X
I^2C	Client Transmit	22.	Client transmits 0xFF if ACKDT bit is set prior to transmission.	X	X	X
Oscillator	OSCFDIV	23.	OSCFDIV oscillator may not function under certain conditions.	X	X	
CCP	Timer Interrupt	24.	Timer interrupt in Capture mode may not occur.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: I²C

In Client mode when AHEN = 1 (Address Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.

Work around

In Client mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

2. Module: Reset

If a lower priority address error trap occurs while a higher priority oscillator failure trap is being processed, the TRAPR bit (RCON[15]) is not set. A Trap Conflict Reset does not occur as expected and the device may stop executing code.

Work around

None. However, a $\overline{\text{MCLR}}$/POR Reset will recover the device.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

3. Module: I²C

In Client mode when DHEN = 1 (Data Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of data reception, then the client interrupt will not occur after the 8th clock.

Work around

In Client mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

4. Module: Primary XT and HS Oscillator (POSC)

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize the POSC.
3. Switch to the POSC source.

Example 1 shows a work around for the device power-on and Example 2 explains the work around when the device wakes from Sleep.

EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma config FNOSC = FRC            // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
int     main()
{
    // configure REFO to request POSC
    REFOCONLbits.ROSEL = 2;           // POSC
    REFOCONLbits.ROOUT = 0;           // disable output
    REFOCONLbits.ROEN = 1;            // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    {   // delay for 9 ms
        unsigned int delayms = 9;
        while(delayms--) asm volatile("repeat #(8000000/1000/2) \n nop");
    }

    // switch to POSC = 2
    __builtin_write_OSCCONH(2);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch
```

EXAMPLE 2: USING POSC WHEN WAKING FROM SLEEP

```
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
    // switch to FRC = 0 before entering sleep
    __builtin_write_OSCCONH(0);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch

    // enter sleep mode
    Sleep();

    // configure REFO to request POSC
    REFOCONLbits.ROSEL = 2;           // POSC
    REFOCONLbits.ROOUT = 0;           // disable output
    REFOCONLbits.ROEN = 1;            // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    {   // delay for 9 ms
        unsigned int delayms = 9;
        while(delayms--) asm volatile("repeat #(8000000/1000/2) \n nop");
    }

    // switch to POSC = 2
    __builtin_write_OSCCONH(2);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch
```

Affected Silicon Revisions

A3	A4	A5					
X	X						

5. Module: Power

When the device wakes up from Retention Sleep mode (RETEN bit (RCON[12]) = 1, $\overline{\text{LPCFG}}$ bit (FPOR[2]) = 0), occasionally a device reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.

Work around

To provide a consistent behavior when the device wakes up from Retention Sleep mode, a software RESET instruction (RESET) should be inserted following the SLEEP instruction. In this case, a Reset will be always be generated when the device wakes up from Retention Sleep. Example 3 shows the software RESET instruction implementation:

EXAMPLE 3: SOFTWARE RESET AFTER SLEEP INSTRUCTION

```
// ENTER SLEEP MODE.
asm volatile ("pwrsav #0");
// SOFTWARE RESET RIGHT AFTER SLEEP.
asm volatile("reset");
```

Affected Silicon Revisions

A3	A4	A5					
X							

6. Module: Power

The main BOR may not occur when the operating voltage drops below the BOR trip voltage.

Work around

Ensure the device operating voltage does not violate the specified values. Use an external supervisor circuit to reset the device if the operating voltage can be outside the specified values.

Affected Silicon Revisions

A3	A4	A5					
X							

7. Module: I²C

In applications with multiple I²C clients, bus data can become corrupted when the data payload sent to an addressed client device matches the bus address of another (unaddressed) client device.

Work around

Keep track of the bus address and data phases in software. When Address Hold Enable is used (the AHEN bit is set), the application can assert a NACK for any of the received bytes (invalid addresses and data bytes for other client devices) until a Stop bit is received.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

8. Module: I²C

In I²C 10-Bit Client Addressing mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence. This issue is not seen during the reception of the lower address byte (A7 to A0) and data bytes. The hardware asserts the ACKTIM bit on the falling edge of the eighth clock and deasserts on the rising edge of the ninth clock. In this case, ACKTIM is not asserted on upper address byte reception. When AHEN = 1, the clock is stretched after the 8th falling edge and the ACKTIM bit is asserted until the clock is released. If AHEN = 0, the clock is not stretched and ACKTIM is asserted during the Acknowledgment sequence, which is of a short duration. Therefore, the user application can see this issue of the ACKTIM bit not getting asserted when AHEN = 1.

Work around

Instead of polling for ACKTIM to be asserted, poll for the RBF flag.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

9. Module: I²C

In I²C Client Receive mode, the Acknowledge Time Status bit (ACKTIM) has no effect if the Address Hold Enable (AHEN) and Data Hold Enable (DHEN) bits are disabled (AHEN = 0 and DHEN = 0). The Acknowledge Time Status bit (ACKTIM) is asserted only if the Address Hold Enable (AHEN) or Data Hold Enable (DHEN) bit is enabled.

Work around

Instead of polling for the ACKTIM bit to be asserted, poll for the RBF flag.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

10. Module: I²C

In Client mode, false bus collision triggers are generated when the bus collision is enabled (SBCDE = 1).

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

11. Module: I²C

A minimum hold time of 300 ns on SDAx, after the falling edge of SCLx, is not achieved when the SDAx Data Hold Time Selection bit (SDAHT) is set.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

12. Module: I²C

In Client mode, the Bus Collision Detect bit (BCL) cannot be cleared when bus collision detection is enabled (SBCDE = 1).

Work around

Disable the I²C module and then re-enable the module.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

13. Module: I²C

In Client mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

14. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.

For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA[11]), to be cleared instead of the TRMT bit (U1STA[8]) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

15. Module: ADC

As shown in the following table, the ADC Differential Nonlinearity (DNL) specification on the positive side changes (changes shown in **bold**).

TABLE 32-24: A/D MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
A/D Accuracy							
AD22B	DNL	Differential Nonlinearity	—	—	**< +2** **< -1**	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

16. Module: ADC

On some devices, the current drawn may increase when the ADC is enabled. The power-saving modes or ADC configuration cannot stop the additional current being drawn. However, the additional current does not affect the performance of either the ADC or the device.

Work around

Disable the ADC when it is not used in the application.

Affected Silicon Revisions

A3	A4	A5					
X	X						

17. Module: Oscillator

When the device is clocked from the Primary Oscillator with PLL (XT+PLL, HS+PLL or EC+PLL), it may not recover from the oscillator failure (Fail-Safe Clock Monitor event) if a `RESET` instruction is executed in the oscillator trap. The device will stop responding.

Work around

In the application code, the device should be started from FRC (defined in the Configuration bits). Then the clock should be switched to the Primary Oscillator with PLL.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

18. Module: CCP

The MCCP timer in 32-bit mode cannot be cleared by writing a zero to the Timer register.

Work around

Switch to 16-bit mode, clear both low and high words and then return to 32-bit mode.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

19. Module: Oscillator

If a clock failure event occurs when the Fail-Safe Clock Monitor (FSCM) is enabled, the oscillator trap may not occur. Instead of the oscillator trap, a clock failure condition can result in instruction misexecution with other traps or Resets generated.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X						

20. Module: Oscillator

The PLL in 96 MHz mode may not function when the device starts up and the capacitor on the V_{CAP} pin is discharged. This condition is applicable in both Two-Speed Oscillator Start-up and clock switching at run time.

Work around

1. The 8x/6x/4x PLL modes are functional and available for use.
2. If 96 MHz PLL mode is required for application, connect a 1 µF capacitor between V_{DD} and V_{CAP} to precharge the V_{CAP} capacitor.

Affected Silicon Revisions

A3	A4	A5					
X	X						

21. Module: I²C

In applications with multiple I²C clients and General Call (GCEN (I2CxCONL[7]) = 1) is enabled, unexpected behavior is observed in the unaddressed client when the data payload of the addressed client matches the General Call address (00h).

When the issue occurs, unexpected data might be received in the unaddressed client. If Address Hold is enabled (AHEN (I2CxCONH[1]) = 1), then I²C will erroneously ACK the byte.

Work around

If Address Hold is enabled (I2CxCONH[1] = 1), Acknowledge Data (ACKDT (I2CxCONL[5]) = 1) should be set during initialization.

Instead of a client interrupt, poll the Receive Buffer Full Status bit and read the receive buffer to clear the unwanted data.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

22. Module: I²C

When the client is transmitting data, if Acknowledge Data (ACKDT (I2CxCONL[5]) = 1) is set before the client starts transmission, then the second data transmitted will be 0xFF, irrespective of the actual data in I2CxTRN.

Work around

Clear the ACKDT bit before client transmission.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

23. Module: Oscillator

On start-up with the VCAP capacitor discharged, the OSCFDIV oscillator may not function. This condition is applicable in both Two-Speed Oscillator Start-up and clock switching at run time. If the OSCFDIV oscillator is selected by default in the FNOSC Configuration bits, the device may not start.

Work around

Use another clock source option, such as FRC.

Affected Silicon Revisions

A3	A4	A5					
X	X						

24. Module: CCP

The CCP timer interrupt will not occur in Capture mode (CCSEL = 1) with the timer time base prescale set to anything other than zero (TMRPS[1:0] ≠ 0).

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30010118**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Power-Saving Features

The VREGS column in Table 10-1: Low-Power Sleep Modes of the device data sheet should be read as the one given in the following table. .

TABLE 10-1: LOW-POWER SLEEP MODES

RETEN	VREGS	MODE	Relative Power
0	**0**	Sleep	A Few µA Range
0	**1**	Fast Wake-up	100 µA Range
1	**0**	Retention Sleep	Less than 1 µA
1	**1**	Fast Retention	A Few µA Range

2. Module: Oscillator

If POSC is disabled/not present, then PLLSS should be set to FRC. PLLSS = PRI is an invalid configuration when POSC is not present.

On any Reset:

The PLL clock source will get selected by the PLLSS configuration option.

By default, in FOSC configuration, it is set to Primary, and if the Primary clock source is not selected (POSCMD = None) or not available, then the device may stop responding as a clock switch to the PLL clock source will not happen after Reset.

So in such a scenario, the user must take care of the PLLSS option and select PLLSS = FRC.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2016)

Initial release of this document; issued for Revision A3.

Rev B Document (12/2016)

Added silicon errata issue 5 (Power).

Rev C Document (6/2017)

Added silicon errata issue 6 (Power).

Added data sheet clarifications 1 (Referenced Sources), 2 (Device Overview), 3 (Power-Saving Features), 4 (Capture/Compare/PWM/Timer Modules (MCCP)), 5 (Serial Peripheral Interface), 6 (Serial Peripheral Interface), 7 (Comparator Voltage Reference), 8 (High/Low-Voltage Detect (HLVD)), 9 (High/Low-Voltage Detect (HLVD)), 10 (Electrical Characteristics) and 11 (Packaging Information.

Rev D Document (3/2018)

Rev D is updated for the silicon revision A4.

Added silicon errata issues 7 (I^2C), 8 (I^2C), 9 (I^2C), 10 (I^2C), 11 (I^2C), 12 (I^2C), 13 (I^2C), 14 (UART) and 15 (ADC).

Incorporated all data sheet clarifications into the *"PIC24FJ256GA705 Family Data Sheet"* (DS30010118**C**).

Rev E Document (2/2019)

Added silicon errata issue 16 (ADC)

Added data sheet clarifications 1 (Power-Saving Features), 2 (Flash Program Memory) 3 (Memory Organization) and 4 (Capture/Compare/PWM/Timer Modules (MCCP)).

Rev F Document (8/2020)

Added silicon errata issues 17 (Oscillator), 18 (CCP), 19 (Oscillator), 20 (Oscillator), 21 (I^2C) and 22 (I^2C).

Removed data sheet clarifications 2 (Flash Program Memory), 3 (Memory Organization) and 4 (Capture/Compare/PWM/Timer Modules (MCCP)) because these were corrected in the current device data sheet.

Added data sheet clarification 2 (Oscillator).

Rev G Document (2/2021)

Rev G is updated for the silicon revision A5.

Added silicon errata issues 23 (Oscillator) and 24 (CCP).

Rev H (3/2021

Removed A5 from the Affected Silicon Revisions table in silicon errata issue 4 (Primary XT and HS Oscillator (POSC) because this issue only affects silicon revisions A3 and A4.

The I^2C standard uses the terminology "Master" and "Slave." The equivalent Microchip terminology used in this document is "Host" and "Client", respectively.

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