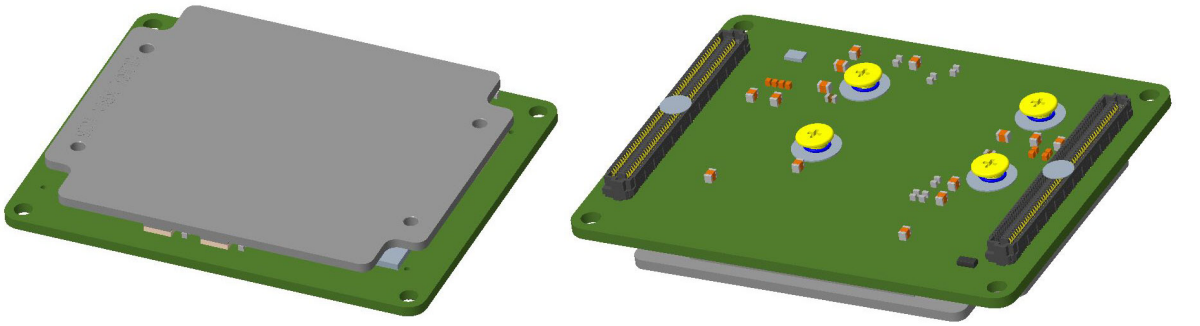
Overview

Module Description

The Xilinx® Kria™ K26 system-on-module (SOM) is a compact embedded platform that integrates a custom-built Zynq® UltraScale+™ MPSoC that runs optimally (and exclusively) on the K26 SOM with DDR memory, nonvolatile storage devices, a security module, and an aluminum thermal heat spreader. The SOM is designed to be plugged into a carrier card with solution-specific peripherals. Key target applications include smart city, machine vision, industrial robotics, and AI/ML computing. The following figure shows the top-side and bottom-side connector view.

Figure 1: **K26 SOM**



X25044-013121

Ordering Information

Table 1: **Ordering Information**

Part Number	Device	Temperature Grade	Encryption	Description
SM-K26-XCL2GC	XCK26-C	Commercial	Enabled	K26C SOM
SM-K26-XCL2GC-ED	XCK26-C	Commercial	Disabled	K26C SOM with encryption disabled
SM-K26-XCL2GI	XCK26-I	Industrial	Enabled	K26I SOM
SM-K26-XCL2GI-ED	XCK26-I	Industrial	Disabled	K26I SOM with encryption disabled

Functional Overview and Block Diagram

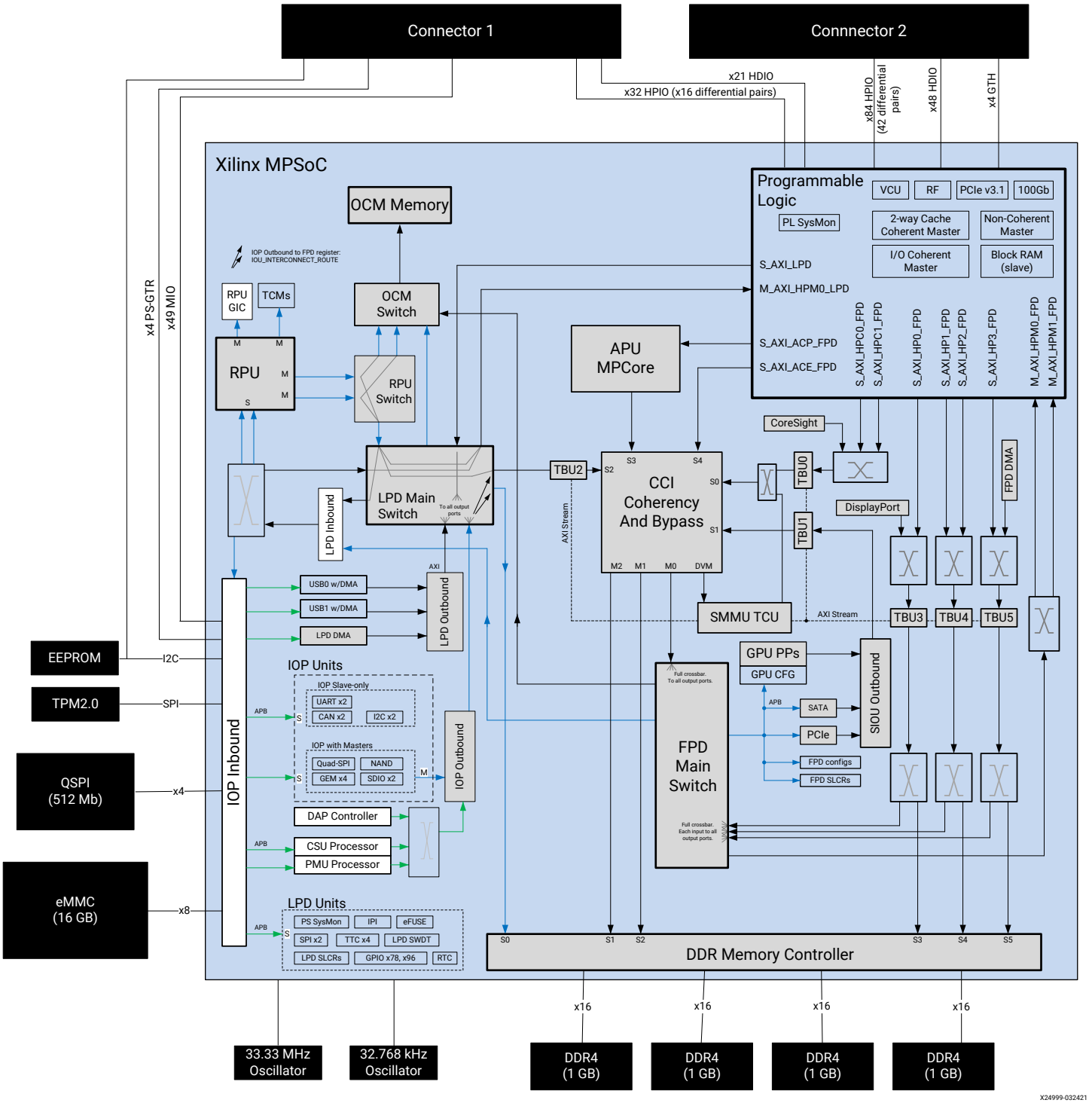
The K26 SOM leverages the XCK26-SFVC784-2LV-C/I, a custom-built Zynq UltraScale+ MPSoC that runs optimally (and exclusively) on the SOM. It provides an embedded processing system (PS) with tightly integrated programmable logic and a rich set of configurable I/O capabilities. The SOM hardware features include:

- Zynq UltraScale+ MPSoC (XCK26 in commercial (C) grade or industrial (I) grade)
- 4 GB 64-bit wide DDR4 memory
- Integrated non-volatile memory devices
  - 512 Mb QSPI
  - 16 GB eMMC
  - 64 Kb EEPROM
- TPM2.0 security module
- Two 240-pin connectors with access to user-configurable I/O:
  - PS MIO
  - PS-GTR transceivers
  - PS I2C platform control bus
  - PL HPIO
  - PL HDIO
  - PL GTH transceivers
  - Sideband platform signals
  - Power and power sequencing signals
- Integrated and flexible power design
  - SOC power supplies derived from a single +5V input
  - PL I/O supplies customized through carrier card defined power rails
- Compact mechanical size with integrated thermal heat spreader

The following sections provide a more detailed description of:

- Functional interfaces and input/output
- MPSoC processing system (PS)
- MPSoC programmable logic (PL)
- Boot sources and storage devices
- Security features and module

Figure 2: **K26 SOM Block Diagram**



Functional Interfaces

The K26 SOM provides a combination of fixed and user-defined functional interfaces. Each interface is implemented with one of the major systems within the MPSoC. The following table is a summary of the interfaces, and system association (PS or PL), with a description of their use.

Table 2: **Interfaces Summary**

Interface	Linked Subsystem	Functional Description
MIO 500 – QSPI	PS	SOM QSPI memory
MIO 500 – SD	PS	SOM eMMC memory
MIO 500 – I2C	PS	SOM power management, EEPROM, and carrier card extensible I2C bus
MIO 500 – SPI	PS	Isolated SPI interface for TPM 2.0 security module
MIO 501	PS	3 PMU power management pins, 23 user-defined multiplexed CPU connected I/O pins or power management pins
MIO 502	PS	26 user-defined multiplexed CPU connected I/O pins
MIO 504 – DDR memory controller	PS	SOM DDR4 memory
HDA – HDIO bank 45	PL	21 user-defined high-density input/output pins
HDB – HDIO bank 43	PL	24 user-defined high-density input/output pins
HDC – HDIO bank 44	PL	24 user-defined high-density input/output pins
HPA – HPIO bank 66	PL	16 user-defined high-performance input/output differential pin pairs
HPB – HPIO bank 65	PL	21 user-defined high-performance input/output differential pin pairs
HPC – HPIO bank 64	PL	21 user-defined high-performance input/output differential pin pairs
PS-GTR transceivers	PS	Four lanes of user-defined high-speed serial transceivers
GTH transceivers	PL	Four lanes of user-defined high-speed serial transceivers

The K26 SOM provides a large number of flexible user-defined I/O that can be configured for various I/O standards and voltage levels. Voltage levels for each HDIO and HPIO bank can be customized by the SOM carrier card to provide the application-required voltage rails to the corresponding I/O banks. See the Supported I/O Standards section for the I/O voltage rail pin definitions and corresponding decoupling requirements.

The K26 SOM provides PS-GTR and GTH transceivers to implement various high-speed protocols. The supported protocols are listed in the protocol tables of the *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925), and are described in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) and *Zynq UltraScale+ MPSoC: Software Developers Guide* (UG1137). The transceivers are configured via the Vivado® Design Suite.

Processing System

This section outlines the processing system (PS) resources. It includes:

- **APU:** Arm® Cortex®-A53 based application processing unit (APU) consisting of quad-core Cortex-A53 processors, L2 cache, SIMD, VFP4 floating point, and cryptography extensions.
- **RPU:** Arm Cortex-R5F based real-time processing unit (RPU) consisting of dual-core Cortex-R5F processors with floating point unit support, able to operate in stand-alone and lock-step functions.

- **PMU:** Platform management unit for dedicated SOM power and subsystem management functions.
- **Dynamic memory controller (DDRC):** DDR4 memory controller with configurable quality-of-service configuration capabilities.
- **GPU:** Arm Mali™-400 MP2 based graphics processing unit.
- **System Monitor:** Built-in analog-digital-converter (ADC) with threshold checks for monitoring and reporting power supply and temperature conditions.
- **RTC:** Real-time clock for maintaining an accurate time base with optional battery backup through a carrier card pin.

The PS provides access to a number of integrated peripherals through multiplexed input/output (MIO) banks. The MPSoC has a total of three MIO banks. The SOM uses the first bank for the onboard peripherals, while the other two MIO banks are customizable and available through the SOM connector interface. All three MIO banks are powered by the SOM with a 1.8V power rail.

Table 3: **MIO Banks**

PS MIO Bank	Description
MIO500	Onboard SOM peripherals including QSPI, SPI, I2C, and eMMC devices.
MIO501	PMU power management I/O and user-defined I/O.
MIO502	User-defined I/O.

A number of peripherals are available within the MIO. The following is a summary of the interfaces that can be configured for your applications.

- **PS-GTR transceivers (x4):** Four dedicated PS-GTR receivers and transmitters with up to 6.0 Gb/s data rates supporting SGMII, tri-speed Ethernet, PCI Express® Gen2, serial ATA (SATA), USB3.0, and DisplayPort
- **Gigabit Ethernet MAC (GEM):** Four 10/100/1000 tri-speed GEM peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
- **DisplayPort controller:** Provides a flexible display output with direct memory access (DMA), centralized buffer manager, rendering block, and audio mixer block.
- **CAN controller:** Two full CAN 2.0B, CAN 2.0A, and ISO 118981-1 standards compliant CAN bus interfaces.
- **USB controller:** Two USB 3.0/2.0 device, host, or OTG peripherals, each supporting up to 12 endpoints.
- **PCI Expresscontroller:** Compliant with the PCI Express base specification 2.1 with support for x1, x2, or x4 line width at Gen1 (2.5 GT/s) or Gen2 (5 GT/s) rates.
- **SD/SDIO/eMMC controller:** One SD/SDIO 2.0/eMMC4.51 compliant controller.
- **UART controller:** One high-speed UART (up to 1Mb/s)
- **SPI controller:** One full-duplex SPI port with three peripheral chip selects.
- **SATA Host controller:** Supports up to two channels at 1.5, 3.0, and 6.0 Gb/s data rates as defined by the SATA specification, revision 3.1

- **I2C controller:** Master and slave I2C interface with support for multi-master designs and clock rates up to 400 Kb/s.

The PS hosts the SOM I2C platform management bus for interfacing with supporting SOM peripherals. These devices are summarized in the following table. The PS I2C bus interface can be extended on a carrier card, but must not introduce address conflicts. The following table defines the K26 SOM I2C device addresses in 7-bit format.

Table 4: **SOM I2C Interface Addresses**

I2C 7-bit Address	Description
0x50, 0x58	SOM EEPROM
0x30, 0x31	DA9062 PMIC
0x32	DA9130 PMIC
0x33	DA9131 PMIC
0x68	PL power domain monitor
0x70	PS power domain monitor

Programmable Logic

The K26 SOM includes a custom-built Zynq UltraScale+ MPSoC (XCK26), that runs optimally (and exclusively) on the K26 SOM and includes a flexible and extensible programmable logic system (PL), an integrated video codec (VCU), and 12.5 Gb/s high-speed transceivers (GTH). The PL resources are summarized in the following table.

Table 5: **PL Resources**

Resource	K26 SOM	Description
System logic cells	256,200	Programmable logic cells for available
CLB flip-flops	234,240	Configurable logic block (CLB): Total number of flip-flops
CLB LUTs	117,120	Configurable logic block: Total number of look-up tables
Distributed RAM (Mb)	3.5	Distributed memory
Block RAM	144	Number of 36 Kb block RAMs
Block RAM (Mb)	5.1	Total block RAM memory footprint
UltraRAM blocks	64	288 Kb dual-port, 72-bit-wide memory with error correction
DSP slices	1,248	27 x 18 signed multiplier with 48-bit adder/accumulator
GTH transceivers	4	12.5 Gb/s serial transceivers
Video Codec	1	H.264 and H.265 supported simultaneous encode/decode
HDIO	69	High-density I/O supports 1.2V to 3.3V rails
HPIO	58	High-performance I/O differential pairs supports 1.0V to 1.8V rails

Boot Sources and Storage Devices

The K26 SOM includes two nonvolatile storage boot devices, a QSPI flash memory, and an eMMC flash memory. The primary boot device is selected by tying the MODE[3:0] pins to the desired value on your carrier card. The boot-mode pins are made available at the SOM connector to allow flexibility in defining the boot device. The boot-mode configurations for using QSPI or eMMC are shown in the following table. Other boot-mode options can be introduced based on your carrier card design. See the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for the full set of boot-mode definitions. Reference the *Kria SOM Carrier Card Design Guide* (UG1091) for details on strapping the boot-mode resistors.

Table 6: **Boot Mode Pins and Location**

Boot Mode	PS_Mode Pins[3:0]	Physical Pin Location
Quad-SPI (32 bit)	0010	MIO[5:0]
eMMC	0110	MIO[22:13]

The K26 SOM provides two storage devices to enable a primary/secondary boot process with isolation between boot firmware and operating system (OS) storage, or similar device firmware segmentation. As an example of the supported hierarchical boot process, the SOM boot mode can be set to QSPI as the primary boot device, which contains the power-on boot firmware, and then the power-on boot loader (e.g., U-Boot) loads the OS from the eMMC secondary boot device.

Security Features

The K26 SOM provides two levels of security with dedicated hardware built into the MPSoC and an on-board trusted platform module (TPM) device. Together they enable implementation of tamper monitoring, secure boot, measured boot, and hardware accelerated cryptographic functions.

The K26 SOM includes the following security features:

- Encryption and authentication of configuration files (non-ED devices only)
- Hardened crypto-accelerators available for user applications (non-ED devices only)
- Secure methods for storing cryptographic keys via eFUSEs
- Methods for detecting and responding to device tamper events

MPSoCs have a dedicated configuration security unit (CSU), which is used for supporting secure boot, tamper monitoring, secure key storage, and cryptographic hardware acceleration. See the *Security* chapter in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085) for implementation details. The cryptographic accelerators available on the MPSoC are as follows:

- SHA-3/384
- AES-GCM-256
- RSA exponential multiplier

The CSU, an internal on-chip memory (OCM), and flexible key storage provide hardware root of trust mechanisms for implementing secure boot within the MPSoC. The hardware capabilities support authenticated and encrypted protections for boot and associated configuration files.

After ensuring the initial boot integrity of the device, the CSU then acts as a centralized tamper monitoring and response controller using the MPSoC integrated system monitor (SYSMON) for measuring and implementing voltage and temperature alarms and configurations. Various alarms and setpoints can be configured as defined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

The MPSoC includes a key management infrastructure supporting battery-backed RAM (BBRAM), eFUSE, embedded boot keys, PUF KEK, and device family keys. When BBRAM is required, battery backup must be provided on the carrier card. Additional details on the key management functions of the MPSoC are outlined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085).

The MPSoC contains a 96-bit unique, nonvolatile device identifier called the device DNA that is permanently programmed in the MPSoC. The SOM EEPROM also contains a unique identifier (UID), programmed at the time of SOM manufacturing. These unique identifiers support the implementation over-the-air (OTA) device enrollment and attestation functionality.

The MPSoC eFUSEs allow permanent enable or disable of specific features to protect deployed systems. A complete list of these capabilities is outlined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085). Two commonly used features are:

- **RSA_EN:** Forces every device boot to be authenticated via RSA
- **JTAG_DIS:** Disables JTAG

In addition to the MPSoC security features, the SOM includes an external TPM device, compliant with the trusted computing group (TCG) TPM 2.0 standard. The TPM 2.0 device enables hardware-based security for remote attestation, measured boot, and other secure cryptographic functions.

Electrical Specifications

This section describes the electrical interfaces and connections available on the SOM to use with your carrier card design.

SOM Connector Overview

The K26 SOM uses two 240-pin connectors to provide electrical connectivity between the SOM and the carrier card. These two connectors are referred to as SOM240_1 and SOM240_2.

The SOM240_1 and SOM240_2 connectors use the Samtec 0.635 mm AcceleRate HD high-density 4-row, 60 position connector set. The part number for the socket (ADF6-60-03.5-L-4-2-A) is used on the bottom side of the SOM. The part number for the terminal (ADM6-60-01.5-L-4-2-A) is for use on the carrier card. The SOM240_1 and SOM240_2 connectors provide support for following interfaces.

- Control and status signals
- Multiplexed I/O (MIO) bank
- PS-GTR high-speed serial transceiver signals
- High-performance I/O (HPIO) bank signals
- High-density I/O (HDIO) bank signals
- GTH high-speed serial transceiver signals
- Power system

Signal Naming Conventions

The SOM240 connectors adopt the naming conventions outlined in the following table.

Table 7: **SOM240 Signal Naming Conventions**

Signal	Description
Module (M)	The SOM, in this case the K26 SOM
Carrier card (C)	The board that the SOM is plugged into is called the carrier card
C2M	Signal names with `C2M` indicate that the signal is driven by the carrier card and received by the SOM
M2C	Signal names with `M2C` indicate that the signal is driven by the SOM and received by the carrier card
_P	The postfix `_P` on differential signal pairs indicates the positive component of a differential signal
_N	The postfix `_N` on differential signal pairs indicates the negative component of a differential signal
_L	The postfix `_L` on a single-ended signal indicates an active-Low signal. This is used for the connector pinouts only. The postfix _B is also used to indicate an active-Low signal.

Table 8: **Legend for Connector Pinouts**

Example	SOM240 Connector	Function
GND	Both SOM240_1 and SOM240_2	Ground pins
VCC_SOM	Both SOM240_1 and SOM240_2	Power connection pins
MIO35	SOM240_1	MIO 501 bank pins
MIO58	SOM240_1	MIO 502 bank pins
JTAG_TMS_C2M	SOM240_1	Configuration and control pins

Table 8: **Legend for Connector Pinouts** *(cont'd)*

Example	SOM240 Connector	Function
GTR_DP1_M2C_P	SOM240_1	PS-GTR transceiver pins
HPA04_P	SOM240_1	HPA pins
HDA00_CC	SOM240_1	HDA pins
HPB15_CC_P	SOM240_2	HPB pins
HPC07_P	SOM240_2	HPC pins
HDB12	SOM240_2	HDB pins
HDC00_CC	SOM240_2	HDC pins
GTH_DP2_C2M_P	SOM240_2	GTH transceiver pins

Supported I/O Standards

The K26 SOM supports all I/O standards supported by the respective bank that a signal is connected to with the exception of I/O standards that require a reference voltage (V_{REF}). For more information, refer to the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

SOM240_1 Connector Pinout

The SOM240_1 connector provides access to two MIO banks (MIO501, MIO502), HPIO bank 66 (HPA), HDIO bank 45 (HDA), and the PS-GTR transceivers (MIO505). It also provides sideband signals for configuration and operation of the board.

Table 9: **SOM240_1 Connector Pinout**

Connector Row/ Pin Number	A	B	C	D
1	VCC_BATT	HPA05_CC_P	GND	VCCO_HPA
2	GND	HPA05_CC_N	GND	VCCO_HPA
3	HPA06_P	GND	HPA00_CC_P	GND
4	HPA06_N	HPA04_P	HPA00_CC_N	HPA02_P
5	GND	HPA04_N	GND	HPA02_N
6	HPA_CLK0_P	GND	HPA03_P	GND
7	HPA_CLK0_N	HPA07_P	HPA03_N	HPA01_P
8	GND	HPA07_N	GND	HPA01_N
9	HPA12_P	GND	HPA08_P	GND
10	HPA12_N	HPA11_P	HPA08_N	HPA09_P
11	GND	HPA11_N	GND	HPA09_N
12	HPA13_P	GND	HPA10_CC_P	GND
13	HPA13_N	VCCO_HDA	HPA10_CC_N	HPA14_P
14	GND	VCCO_HDA	GND	HPA14_N
15	HDA09	GND	PS_POR_L	GND
16	HDA10	HDA03	PS_SRST_C2M_L	HDA00_CC
17	HDA11	HDA04	GND	HDA01

Table 9: **SOM240_1 Connector Pinout** *(cont'd)*

Connector Row/ Pin Number	A	B	C	D
18	GND	HDA05	HDA06	HDA02
19	VCCOEN_PS_M2C	GND	HDA07	GND
20	VCCOEN_PL_M2C	HDA15	HDA08_CC	HDA12
21	GND	HDA16_CC	GND	HDA13
22	JTAG_TMS_C2M	HDA17	HDA18	HDA14
23	JTAG_TDO_M2C	GND	HDA19	GND
24	JTAG_TDI_C2M	PS_ERROR_OUT_M2C	HDA20	PWRGD_FPD_M2C
25	JTAG_TCK_C2M	PS_ERROR_STATUS_M2C	GND	PWRGD_LPD_M2C
26	GND	PWROFF_C2M_L	MIO24_I2C_SCK	PWRGD_PL_M2C
27	MODE0_C2M	GND	MIO25_I2C_SDA	GND
28	MODE1_C2M	MIO35	MIO12_FWUEN_C2M_L	MIO26_WD_IN
29	MODE2_C2M	MIO36	GND	MIO27
30	MODE3_C2M	MIO37	MIO29	MIO28
31	Reserved	GND	MIO30	GND
32	Reserved	MIO38	MIO31_SHUTDOWN	MIO44
33	GND	MIO39	GND	MIO45
34	MIO41	MIO40	MIO47	MIO46
35	MIO42	GND	MIO48	GND
36	MIO43	MIO50	MIO49	MIO52
37	GND	MIO51	GND	MIO53
38	MIO61	Reserved	MIO55	MIO54
39	MIO62	GND	MIO56	GND
40	MIO63	MIO58	MIO57	MIO64
41	GND	MIO59	GND	MIO65
42	MIO73	MIO60	MIO67	MIO66
43	MIO74	GND	MIO68	GND
44	MIO75	MIO70	MIO69	MIO76
45	GND	MIO71	Reserved	MIO77
46	GND	MIO72	GND	Reserved
47	GTR_DP1_M2C_P	GND	GTR_REFCLK0_C2M_P	GND
48	GTR_DP1_M2C_N	GND	GTR_REFCLK0_C2M_N	GND
49	GND	GTR_REFCLK1_C2M_P	GND	GTR_DP3_C2M_P
50	GND	GTR_REFCLK1_C2M_N	GND	GTR_DP3_C2M_N
51	GTR_REFCLK3_C2M_P	GND	GTR_DP3_M2C_P	GND
52	GTR_REFCLK3_C2M_N	GND	GTR_DP3_M2C_N	GND
53	GND	GTR_DP2_C2M_P	GND	GTR_REFCLK2_C2M_P
54	GND	GTR_DP2_C2M_N	GND	GTR_REFCLK2_C2M_N
55	GTR_DP0_C2M_P	GND	GTR_DP1_C2M_P	GND
56	GTR_DP0_C2M_N	GND	GTR_DP1_C2M_N	GND
57	GND	GTR_DP0_M2C_P	GND	GTR_DP2_M2C_P

Table 9: **SOM240_1 Connector Pinout** *(cont'd)*

Connector Row/ Pin Number	A	B	C	D
58	GND	GTR_DP0_M2C_N	GND	GTR_DP2_M2C_N
59	VCC_SOM	GND	VCC_SOM	GND
60	VCC_SOM	VCC_SOM	VCC_SOM	VCC_SOM

SOM240_1 Signal Names and Descriptions

Table 10: **SOM240_1 Signal Pins**

Pin Number	Signal Name	Signal Description
Connector Row A		
A1	VCC_BATT	PS BBRAM and real-time clock (RTC) supply voltage, requires external battery. Connect to GND when battery is not used.
A2	GND	Ground
A3	HPA06_P	HPIO on bank 66
A4	HPA06_N	HPIO on bank 66
A5	GND	Ground
A6	HPA_CLK0_P	HPIO global clock pin on bank 66
A7	HPA_CLK0_N	HPIO global clock pin on bank 66
A8	GND	Ground
A9	HPA12_P	HPIO on bank 66
A10	HPA12_N	HPIO on bank 66
A11	GND	Ground
A12	HPA13_P	HPIO on bank 66
A13	HPA13_N	HPIO on bank 66
A14	GND	Ground
A15	HDA09	HDIO on bank 45
A16	HDA10	HDIO on bank 45
A17	HDA11	HDIO on bank 45
A18	GND	Ground
A19	VCCOEN_PS_M2C	Indication to turn on power for PS I/O peripherals on the carrier card
A20	VCCOEN_PL_M2C	Indication to turn on power for PL /IO peripherals on the carrier card
A21	GND	Ground
A22	JTAG_TMS_C2M	JTAG mode select, pulled up at 1.8V on the SOM
A23	JTAG_TDO_M2C	JTAG data out, pulled up at 1.8V on the SOM
A24	JTAG_TDI_C2M	JTAG data in, pulled up at 1.8V on the SOM
A25	JTAG_TCK_C2M	JTAG clock, pulled up at 1.8V on the SOM
A26	GND	Ground
A27	MODE0_C2M	PS mode bit 0, pulled up at 1.8V on the SOM
A28	MODE1_C2M	PS mode bit 1, pulled up at 1.8V on the SOM
A29	MODE2_C2M	PS mode bit 2, pulled up at 1.8V on the SOM
A30	MODE3_C2M	PS mode bit 3, pulled up at 1.8V on the SOM

Table 10: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
A31	Reserved	No connect on the SOM
A32	Reserved	No connect on the SOM
A33	GND	Ground
A34	MIO41	PS MIO signal on bank 501
A35	MIO42	PS MIO signal on bank 501
A36	MIO43	PS MIO signal on bank 501
A37	GND	Ground
A38	MIO61	PS MIO signal on bank 502
A39	MIO62	PS MIO signal on bank 502
A40	MIO63	PS MIO signal on bank 502
A41	GND	Ground
A42	MIO73	PS MIO signal on bank 502
A43	MIO74	PS MIO signal on bank 502
A44	MIO75	PS MIO signal on bank 502
A45	GND	Ground
A46	GND	Ground
A47	GTR_DP1_M2C_P	PS-GTR lane 1 TX
A48	GTR_DP1_M2C_N	PS-GTR lane 1 TX
A49	GND	Ground
A50	GND	Ground
A51	GTR_REFCLK3_C2M_P	PS-GTR REFCLK3 input
A52	GTR_REFCLK3_C2M_N	PS-GTR REFCLK3 input
A53	GND	Ground
A54	GND	Ground
A55	GTR_DP0_C2M_P	PS-GTR lane 0 RX
A56	GTR_DP0_C2M_N	PS-GTR lane 0 RX
A57	GND	Ground
A58	GND	Ground
A59	VCC_SOM	SOM main supply voltage, +5V
A60	VCC_SOM	SOM main supply voltage, +5V
Connector Row B		
B1	HPA05_CC_P	HPIO clock-capable pin on bank 66
B2	HPA05_CC_N	HPIO clock-capable pin on bank 66
B3	GND	Ground
B4	HPA04_P	HPIO on bank 66
B5	HPA04_N	HPIO on bank 66
B6	GND	Ground
B7	HPA07_P	HPIO on bank 66
B8	HPA07_N	HPIO on bank 66
B9	GND	Ground
B10	HPA11_P	HPIO on bank 66
B11	HPA11_N	HPIO on bank 66

Table 10: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
B12	GND	Ground
B13	VCCO_HDA	HDA I/O voltage rail, 1.2V to 3.3V
B14	VCCO_HDA	HDA I/O voltage rail, 1.2V to 3.3V
B15	GND	Ground
B16	HDA03	HDIO on bank 45
B17	HDA04	HDIO on bank 45
B18	HDA05	HDIO on bank 45
B19	GND	Ground
B20	HDA15	HDIO on bank 45
B21	HDA16_CC	HDIO clock-capable pin on bank 45
B22	HDA17	HDIO on bank 45
B23	GND	Ground
B24	PS_ERROR_OUT_M2C	PS error indication from SOM
B25	PS_ERROR_STATUS_M2C	PS error status from SOM
B26	PWROFF_C2M_L	Control signal to turn off all power rails on the SOM
B27	GND	Ground
B28	MIO35	PS MIO signal on bank 501. Optional use as PMU output.
B29	MIO36	PS MIO signal on bank 501
B30	MIO37	PS MIO signal on bank 501
B31	GND	Ground
B32	MIO38	PS MIO signal on bank 501
B33	MIO39	PS MIO signal on bank 501
B34	MIO40	PS MIO signal on bank 501
B35	GND	Ground
B36	MIO50	PS MIO signal on bank 501
B37	MIO51	PS MIO signal on bank 501
B38	Reserved	Not connected to SOM connector
B39	GND	Ground
B40	MIO58	PS MIO signal on bank 502
B41	MIO59	PS MIO signal on bank 502
B42	MIO60	PS MIO signal on bank 502
B43	GND	Ground
B44	MIO70	PS MIO signal on bank 502
B45	MIO71	PS MIO signal on bank 502
B46	MIO72	PS MIO signal on bank 502
B47	GND	Ground
B48	GND	Ground
B49	GTR_REFCLK1_C2M_P	PS-GTR REFCLK1 input
B50	GTR_REFCLK1_C2M_N	PS-GTR REFCLK1 input
B51	GND	Ground
B52	GND	Ground
B53	GTR_DP2_C2M_P	PS-GTR lane 2 RX

Table 10: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
B54	GTR_DP2_C2M_N	PS-GTR lane 2 RX
B55	GND	Ground
B56	GND	Ground
B57	GTR_DP0_M2C_P	PS-GTR lane 0 TX
B58	GTR_DP0_M2C_N	PS-GTR lane 0 TX
B59	GND	Ground
B60	VCC_SOM	SOM main supply voltage, +5V
Connector Row C		
C1	GND	Ground
C2	GND	Ground
C3	HPA00_CC_P	HPIO clock-capable pin on bank 66
C4	HPA00_CC_N	HPIO clock-capable pin on bank 66
C5	GND	Ground
C6	HPA03_P	HPIO on bank 66
C7	HPA03_N	HPIO on bank 66
C8	GND	Ground
C9	HPA08_P	HPIO on bank 66
C10	HPA08_N	HPIO on bank 66
C11	GND	Ground
C12	HPA10_CC_P	HPIO clock-capable pin on bank 66
C13	HPA10_CC_N	HPIO clock-capable pin on bank 66
C14	GND	Ground
C15	PS_POR_L	PS power-on reset driven by the carrier card. When deasserted, the PS begins the boot process
C16	PS_SRST_C2M_L	PS system reset driven by the carrier card. When asserted, forces the PS to enter the system reset sequence
C17	GND	Ground
C18	HDA06	HDIO on bank 45
C19	HDA07	HDIO on bank 45
C20	HDA08_CC	HDIO clock-capable pin on bank 45
C21	GND	Ground
C22	HDA18	HDIO on bank 45
C23	HDA19	HDIO on bank 45
C24	HDA20	HDIO on bank 45
C25	GND	Ground
C26	MIO24_I2C_SCK	PS I2C clock output
C27	MIO25_I2C_SDA	PS I2C serial data
C28	MIO12_FWUEN_C2M_L	Firmware user enable indication
C29	GND	Ground
C30	MIO29	PS MIO signal on bank 501. No connect on the SOM
C31	MIO30	PS MIO signal on bank 501. No connect on the SOM
C32	MIO31_SHUTDOWN	PS MIO signal on bank 501. Optional use as PMU input. Optional PMU library enabled input for hardware-initiated shutdown by the PMU.

Table 10: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
C33	GND	Ground
C34	MIO47	PS MIO signal on bank 501
C35	MIO48	PS MIO signal on bank 501
C36	MIO49	PS MIO signal on bank 501
C37	GND	Ground
C38	MIO55	PS MIO signal on bank 502
C39	MIO56	PS MIO signal on bank 502
C40	MIO57	PS MIO signal on bank 502
C41	GND	Ground
C42	MIO67	PS MIO signal on bank 502
C43	MIO68	PS MIO signal on bank 502
C44	MIO69	PS MIO signal on bank 502
C45	Reserved	NC on the SOM
C46	GND	Ground
C47	GTR_REFCLK0_C2M_P	PS-GTR REFCLK0 input
C48	GTR_REFCLK0_C2M_N	PS-GTR REFCLK0 input
C49	GND	Ground
C50	GND	Ground
C51	GTR_DP3_M2C_P	PS-GTR lane 3 TX
C52	GTR_DP3_M2C_N	PS-GTR lane 3 TX
C53	GND	Ground
C54	GND	Ground
C55	GTR_DP1_C2M_P	PS-GTR lane 1 RX
C56	GTR_DP1_C2M_N	PS-GTR lane 1 RX
C57	GND	Ground
C58	GND	Ground
C59	VCC_SOM	SOM main supply voltage, +5V
C60	VCC_SOM	SOM main supply voltage, +5V
Connector Row D		
D1	VCCO_HPA	HPA I/O voltage rail, 1.0V to 1.8V
D2	VCCO_HPA	HPA I/O voltage rail, 1.0V to 1.8V
D3	GND	Ground
D4	HPA02_P	HPIO on bank 66
D5	HPA02_N	HPIO on bank 66
D6	GND	Ground
D7	HPA01_P	HPIO on bank 66
D8	HPA01_N	HPIO on bank 66
D9	GND	Ground
D10	HPA09_P	HPIO on bank 66
D11	HPA09_N	HPIO on bank 66
D12	GND	Ground
D13	HPA14_P	HPIO on bank 66

Table 10: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
D14	HPA14_N	HPIO on bank 66
D15	GND	Ground
D16	HDA00_CC	HDIO clock-capable pin on bank 45
D17	HDA01	HDIO on bank 45
D18	HDA02	HDIO on bank 45
D19	GND	Ground
D20	HDA12	HDIO on bank 45
D21	HDA13	HDIO on bank 45
D22	HDA14	HDIO on bank 45
D23	GND	Ground
D24	PWRGD_FPD_M2C	Power good indication for PS FPD power rails
D25	PWRGD_LPD_M2C	Power good indication for PS LPD power rails
D26	PWRGD_PL_M2C	Power good indication for all PL power rails
D27	GND	Ground
D28	MIO26	PS MIO signal on bank 501. Optional use as PMU input.
D29	MIO27	PS MIO signal on bank 501. Optional use as PMU input.
D30	MIO28	PS MIO signal on bank 501. Optional use as PMU input.
D31	GND	Ground
D32	MIO44	PS MIO signal on bank 501
D33	MIO45	PS MIO signal on bank 501
D34	MIO46	PS MIO signal on bank 501
D35	GND	Ground
D36	MIO52	PS MIO signal on bank 502
D37	MIO53	PS MIO signal on bank 502
D38	MIO54	PS MIO signal on bank 502
D39	GND	Ground
D40	MIO64	PS MIO signal on bank 502
D41	MIO65	PS MIO signal on bank 502
D42	MIO66	PS MIO signal on bank 502
D43	GND	Ground
D44	MIO76	PS MIO signal on bank 502
D45	MIO77	PS MIO signal on bank 502
D46	Reserved	No connect on the SOM
D47	GND	Ground
D48	GND	Ground
D49	GTR_DP3_C2M_P	PS-GTR lane 3 RX
D50	GTR_DP3_C2M_N	PS-GTR lane 3 RX
D51	GND	Ground
D52	GND	Ground
D53	GTR_REFCLK2_C2M_P	PS-GTR REFCLK2 input
D54	GTR_REFCLK2_C2M_N	PS-GTR REFCLK2 input
D55	GND	Ground

Table 10: **SOM240_1 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
D56	GND	Ground
D57	GTR_DP2_M2C_P	PS-GTR lane 2 TX
D58	GTR_DP2_M2C_N	PS-GTR lane 2 TX
D59	GND	Ground
D60	VCC_SOM	SOM main supply voltage, +5V

SOM240_2 Connector Pinout

The SOM240_1 connector provides access to two HPIO bank 65 (HPB), HPIO bank 64 (HPC), HDIO bank43 (HDB, HDIO bank 44 (HDC), and the PL GTH Quad.

Table 11: **SOM240_2 Connector Pinout**

Connector Row/ Pin Number	A	B	C	D
1	GND	GTH_DP2_C2M_P	GND	GTH_DP1_C2M_P
2	GND	GTH_DP2_C2M_N	GND	GTH_DP1_C2M_N
3	GTH_DP3_C2M_P	GND	GTH_REFCLK0_C2M_P	GND
4	GTH_DP3_C2M_N	GND	GTH_REFCLK0_C2M_N	GND
5	GND	GTH_DP2_M2C_P	GND	GTH_DP3_M2C_P
6	GND	GTH_DP2_M2C_N	GND	GTH_DP3_M2C_N
7	GTH_REFCLK1_C2M_P	GND	GTH_DP1_M2C_P	GND
8	GTH_REFCLK1_C2M_N	GND	GTH_DP1_M2C_N	GND
9	GND	GTH_DP0_C2M_P	GND	GTH_DP0_M2C_P
10	GND	GTH_DP0_C2M_N	GND	GTH_DP0_M2C_N
11	HPB15_CC_P	GND	HPB09_P	GND
12	HPB15_CC_N	HPB10_CC_P	HPB09_N	HPB01_P
13	GND	HPB10_CC_N	GND	HPB01_N
14	HPB08_P	GND	HPB14_P	GND
15	HPB08_N	HPB07_P	HPB14_N	HPB00_CC_P
16	GND	HPB07_N	GND	HPB00_CC_N
17	HPB12_P	GND	HPB02_P	GND
18	HPB12_N	HPB05_CC_P	HPB02_N	HPB_CLK0_P
19	GND	HPB05_CC_N	GND	HPB_CLK0_N
20	HPB06_P	GND	HPB13_P	GND
21	HPB06_N	HPB11_P	HPB13_N	HPB04_P
22	GND	HPB11_N	GND	HPB04_N
23	HPB16_P	GND	HPB_18_P	GND
24	HPB16_N	HPB03_P	HPB_18_N	HPB17_P
25	GND	HPB03_N	GND	HPB17_N
26	HPB_19_P	GND	HPC07_P	GND
27	HPB_19_N	HPC06_P	HPC07_N	HPC09_P

Table 11: **SOM240_2 Connector Pinout** *(cont'd)*

Connector Row/ Pin Number	A	B	C	D
28	GND	HPC06_N	GND	HPC09_N
29	HPC17_P	GND	HPC05_CC_P	GND
30	HPC17_N	HPC13_P	HPC05_CC_N	HPC01_P
31	GND	HPC13_N	GND	HPC01_N
32	HPC19_P	GND	HPC08_P	GND
33	HPC19_N	HPC16_P	HPC08_N	HPC00_CC_P
34	GND	HPC16_N	GND	HPC00_CC_N
35	HPC14_P	GND	HPC11_P	GND
36	HPC14_N	HPC10_CC_P	HPC11_N	HPC02_P
37	GND	HPC10_CC_N	GND	HPC02_N
38	HPC15_CC_P	GND	HPC12_P	GND
39	HPC15_CC_N	HPC18_P	HPC12_N	HPC04_P
40	GND	HPC18_N	GND	HPC04_N
41	HPC03_P	GND	HPC_CLK0_P	GND
42	HPC03_N	VCCO_HPB	HPC_CLK0_N	VCCO_HPC
43	GND	GND	GND	GND
44	VCCO_HPB	HDB12	VCCO_HPC	HDB00_CC
45	GND	HDB13	GND	HDB01
46	HDB18	HDB14	HDB06	HDB02
47	HDB19	GND	HDB07	GND
48	HDB20	HDB15	HDB08_CC	HDB03
49	GND	HDB16_CC	GND	HDB04
50	HDB21	HDB17	HDB09	HDB05
51	HDB22	GND	HDB10	GND
52	HDB23	HDC12	HDB11	HDC00_CC
53	GND	HDC13	GND	HDC01
54	HDC18	HDC14	HDC06	HDC02
55	HDC19	GND	HDC07	GND
56	HDC20	HDC15	HDC08_CC	HDC03
57	GND	HDC16_CC	GND	HDC04
58	HDC21	HDC17	HDC09	HDC05
59	HDC22	VCCO_HDB	HDC10	VCCO_HDC
60	HDC23	VCCO_HDB	HDC11	VCCO_HDC

SOM240_2 Signal Names and Descriptions

Table 12: **SOM240_2 Signal Pins**

Pin Number	Signal Name	Signal Description
Connector Row A		
A1	GND	Ground
A2	GND	Ground
A3	GTH_DP3_C2M_P	GTH Lane 3 RX
A4	GTH_DP3_C2M_N	GTH Lane 3 RX
A5	GND	Ground
A6	GND	Ground
A7	GTH_REFCLK1_C2M_P	GTH REFCLK1 input
A8	GTH_REFCLK1_C2M_N	GTH REFCLK1 input
A9	GND	Ground
A10	GND	Ground
A11	HPB15_CC_P	HPIO clock-capable pin on bank 65
A12	HPB15_CC_N	HPIO clock-capable pin on bank 65
A13	GND	Ground
A14	HPB08_P	HPIO on bank 65
A15	HPB08_N	HPIO on bank 65
A16	GND	Ground
A17	HPB12_P	HPIO on bank 65
A18	HPB12_N	HPIO on bank 65
A19	GND	Ground
A20	HPB06_P	HPIO on bank 65
A21	HPB06_N	HPIO on bank 65
A22	GND	Ground
A23	HPB16_P	HPIO on bank 65
A24	HPB16_N	HPIO on bank 65
A25	GND	Ground
A26	HPB_19_P	HPIO on bank 65
A27	HPB_19_N	HPIO on bank 65
A28	GND	Ground
A29	HPC08_P	HPIO on bank 64
A30	HPC08_N	HPIO on bank 64
A31	GND	Ground
A32	HPC19_P	HPIO on bank 64
A33	HPC19_N	HPIO on bank 64
A34	GND	Ground
A35	HPC14_P	HPIO on bank 64
A36	HPC14_N	HPIO on bank 64
A37	GND	Ground
A38	HPC15_CC_P	HPIO clock-capable pin on bank 64
A39	HPC15_CC_N	HPIO clock-capable pin on bank 64

Table 12: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
A40	GND	Ground
A41	HPC03_P	HPIO on bank 64
A42	HPC03_N	HPIO on bank 64
A43	GND	Ground
A44	VCCO_HPB	HPB I/O voltage rail, 1.0V to 1.8V
A45	GND	Ground
A46	HDB18	HDIO on bank 43
A47	HDB19	HDIO on bank 43
A48	HDB20	HDIO on bank 43
A49	GND	Ground
A50	HDB21	HDIO on bank 43
A51	HDB22	HDIO on bank 43
A52	HDB23	HDIO on bank 43
A53	GND	Ground
A54	HDC18	HDIO on bank 44
A55	HDC19	HDIO on bank 44
A56	HDC20	HDIO on bank 44
A57	GND	Ground
A58	HDC21	HDIO on bank 44
A59	HDC22	HDIO on bank 44
A60	HDC23	HDIO on bank 44
Connector Row B		
B1	GTH_DP2_C2M_P	GTH Lane 2 RX
B2	GTH_DP2_C2M_N	GTH Lane 2 RX
B3	GND	Ground
B4	GND	Ground
B5	GTH_DP2_M2C_P	GTH Lane 2 TX
B6	GTH_DP2_M2C_N	GTH Lane 2 TX
B7	GND	Ground
B8	GND	Ground
B9	GTH_DP0_C2M_P	GTH Lane 0 RX
B10	GTH_DP0_C2M_N	GTH Lane 0 RX
B11	GND	Ground
B12	HPB10_CC_P	HPIO on bank 65
B13	HPB10_CC_N	HPIO on bank 65
B14	GND	Ground
B15	HPB07_P	HPIO on bank 65
B16	HPB07_N	HPIO on bank 65
B17	GND	Ground
B18	HPB05_CC_P	HPIO clock-capable pin on bank 65
B19	HPB05_CC_N	HPIO clock-capable pin on bank 65
B20	GND	Ground

Table 12: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
B21	HPB11_P	HPIO on bank 65
B22	HPB11_N	HPIO on bank 65
B23	GND	Ground
B24	HPB03_P	HPIO on bank 65
B25	HPB03_N	HPIO on bank 65
B26	GND	Ground
B27	HPC06_P	HPIO on bank 64
B28	HPC06_N	HPIO on bank 64
B29	GND	Ground
B30	HPC13_P	HPIO on bank 64
B31	HPC13_N	HPIO on bank 64
B32	GND	Ground
B33	HPC16_P	HPIO on bank 64
B34	HPC16_N	HPIO on bank 64
B35	GND	Ground
B36	HPC07_P	HPIO on bank 64
B37	HPC07_N	HPIO on bank 64
B38	GND	Ground
B39	HPC18_P	HPIO on bank 64
B40	HPC18_N	HPIO on bank 64
B41	GND	Ground
B42	VCCO_HPB	HPB I/O voltage rail, 1.0V to 1.8V
B43	GND	Ground
B44	HDB12	HDIO on bank 43
B45	HDB13	HDIO on bank 43
B46	HDB14	HDIO on bank 43
B47	GND	Ground
B48	HDB15	HDIO on bank 43
B49	HDB16_CC	HDIO clock-capable pin on bank 43
B50	HDB17	HDIO on bank 43
B51	GND	Ground
B52	HDC12	HDIO on bank 44
B53	HDC13	HDIO on bank 44
B54	HDC14	HDIO on bank 44
B55	GND	Ground
B56	HDC15	HDIO on bank 44
B57	HDC16_CC	HDIO clock-capable pin on bank 44
B58	HDC17	HDIO on bank 44
B59	VCCO_HDB	HDB I/O voltage rail, 1.2V to 3.3V
B60	VCCO_HDB	HDB I/O voltage rail, 1.2V to 3.3V
Connector Row C		
C1	GND	Ground

Table 12: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
C2	GND	Ground
C3	GTH_REFCLK0_C2M_P	GTH REFCLK0 input
C4	GTH_REFCLK0_C2M_N	GTH REFCLK0 input
C5	GND	Ground
C6	GND	Ground
C7	GTH_DP1_M2C_P	GTH Lane 1 TX
C8	GTH_DP1_M2C_N	GTH Lane 1 TX
C9	GND	Ground
C10	GND	Ground
C11	HPB09_P	HPIO on bank 65
C12	HPB09_N	HPIO on bank 65
C13	GND	Ground
C14	HPB14_P	HPIO on bank 65
C15	HPB14_N	HPIO on bank 65
C16	GND	Ground
C17	HPB02_P	HPIO on bank 65
C18	HPB02_N	HPIO on bank 65
C19	GND	Ground
C20	HPB13_P	HPIO on bank 65
C21	HPB13_N	HPIO on bank 65
C22	GND	Ground
C23	HPB_18_P	HPIO on bank 65
C24	HPB_18_N	HPIO on bank 65
C25	GND	Ground
C26	HPC17_P	HPIO on bank 64
C27	HPC17_N	HPIO on bank 64
C28	GND	Ground
C29	HPC10_CC_P	HPIO clock-capable pin on bank 64
C30	HPC10_CC_N	HPIO clock-capable pin on bank 64
C31	GND	Ground
C32	HPC11_P	HPIO on bank 64
C33	HPC11_N	HPIO on bank 64
C34	GND	Ground
C35	HPC12_P	HPIO on bank 64
C36	HPC12_N	HPIO on bank 64
C37	GND	Ground
C38	HPC05_CC_P	HPIO clock-capable pin on bank 64
C39	HPC05_CC_N	HPIO clock-capable pin on bank 64
C40	GND	Ground
C41	HPC_CLK0_P	HPIO global clock pin on bank 64
C42	HPC_CLK0_N	HPIO global clock pin on bank 64
C43	GND	Ground

Table 12: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
C44	VCCO_HPC	HPC I/O voltage rail, 1.0V to 1.8V
C45	GND	Ground
C46	HDB06	HDIO on bank 43
C47	HDB07	HDIO on bank 43
C48	HDB08_CC	HDIO clock-capable pin on bank 43
C49	GND	Ground
C50	HDB09	HDIO on bank 43
C51	HDB10	HDIO on bank 43
C52	HDB11	HDIO on bank 43
C53	GND	Ground
C54	HDC06	HDIO on bank 44
C55	HDC07	HDIO on bank 44
C56	HDC08_CC	HDIO clock-capable pin on bank 44
C57	GND	Ground
C58	HDC09	HDIO on bank 44
C59	HDC10	HDIO on bank 44
C60	HDC11	HDIO on bank 44
Connector Row D		
D1	GTH_DP1_C2M_P	GTH Lane 1 RX
D2	GTH_DP1_C2M_N	GTH Lane 1 RX
D3	GND	Ground
D4	GND	Ground
D5	GTH_DP3_M2C_P	GTH Lane 3 TX
D6	GTH_DP3_M2C_N	GTH Lane 3 TX
D7	GND	Ground
D8	GND	Ground
D9	GTH_DP0_M2C_P	GTH Lane 0 TX
D10	GTH_DP0_M2C_N	GTH Lane 0 TX
D11	GND	Ground
D12	HPB01_P	HPIO on bank 65
D13	HPB01_N	HPIO on bank 65
D14	GND	Ground
D15	HPB00_CC_P	HPIO on bank 65
D16	HPB00_CC_N	HPIO on bank 65
D17	GND	Ground
D18	HPB_CLK0_P	HPIO global clock pin on bank 65
D19	HPB_CLK0_N	HPIO global clock pin on bank 65
D20	GND	Ground
D21	HPB04_P	HPIO on bank 65
D22	HPB04_N	HPIO on bank 65
D23	GND	Ground
D24	HPB17_P	HPIO on bank 65

Table 12: **SOM240_2 Signal Pins** *(cont'd)*

Pin Number	Signal Name	Signal Description
D25	HPB17_N	HPIO on bank 65
D26	GND	Ground
D27	HPC09_P	HPIO on bank 64
D28	HPC09_N	HPIO on bank 64
D29	GND	Ground
D30	HPC01_P	HPIO on bank 64
D31	HPC01_N	HPIO on bank 64
D32	GND	Ground
D33	HPC00_CC_P	HPIO clock-capable pin on bank 64
D34	HPC00_CC_N	HPIO clock-capable pin on bank 64
D35	GND	Ground
D36	HPC02_P	HPIO on bank 64
D37	HPC02_N	HPIO on bank 64
D38	GND	Ground
D39	HPC04_P	HPIO on bank 64
D40	HPC04_N	HPIO on bank 64
D41	GND	Ground
D42	VCCO_HPC	HPC I/O voltage rail, 1.0V to 1.8V
D43	GND	Ground
D44	HDB00_CC	HDIO clock-capable pin on bank 43
D45	HDB01	HDIO on bank 43
D46	HDB02	HDIO on bank 43
D47	GND	Ground
D48	HDB03	HDIO on bank 43
D49	HDB04	HDIO on bank 43
D50	HDB05	HDIO on bank 43
D51	GND	Ground
D52	HDC00_CC	HDIO clock-capable pin on bank 44
D53	HDC01	HDIO on bank 44
D54	HDC02	HDIO on bank 44
D55	GND	Ground
D56	HDC03	HDIO on bank 44
D57	HDC04	HDIO on bank 44
D58	HDC05	HDIO on bank 44
D59	VCCO_HDC	HDC I/O voltage rail, 1.2V to 3.3V
D60	VCCO_HDC	HDC I/O voltage rail, 1.2V to 3.3V

Functional Signal Descriptions

Sideband Signals

The sideband signals consist of power, processor, and configuration signals. V_{CCO} for sideband signals is 1.80V.

- **JTAG:** The JTAG signals JTAG_TCK_C2M, JTAG_TMS_C2M, JTAG_TDI_C2M, and JTAG_TDO_M2C connect to the SOM Zynq UltraScale+ MPSoC JTAG port.
- **I2C:** The I2C signals I2C_SCK and I2C_SDA connect to an I2C master on MIO bank 500 of the SOM Zynq UltraScale+ MPSoC. The I2C I/O standard is 1.8V.
- **PS_MODE[3:0]:** The connector PS_MODE[3:0] pins connect to the SOM Zynq UltraScale+ MPSoC PS_MODE pins. All mode pins are pulled High to 1.8V through a resistor on the SOM.The carrier card boot mode is required to set the PS_MODE pins to a valid boot mode as defined in the *Zynq UltraScale+ Device Technical Reference Manual* (UG1085). To configure a PS_MODE pin to a logic 1, the pin must be left floating, to configure a logic 0, the PS_MODE pin must be connected to GND with a 0Ω resistor.
- **PS_POR_L:** During power up, a voltage monitor keeps PS_POB_L asserted (Low) until all SOM power rails are stabilized. Afterward, PS_POR_L is released and the boot process starts. A carrier card can use PS_POR_L to reset any on-board devices. The carrier card can also force PS_POR_L Low to extend the reset during power on to reset the system at any time.
- **PS_SRST_C2M_L:** The PS_SRST_C2M_L pin connects to PS_SRST_B signal on the SOM Zynq UltraScale+ MPSoC. PS_SRST_B input signal to the Zynq UltraScale+ MPSoC is the system reset signal, and it is commonly used during debug. PS_SRST_C2M_L is pulled High to 1.8V on the SOM.

Power Management Signals

- **PWROFF_ C2M_L:**
  - PWROFF_C2M_L is an active-Low signal to power down the SOM and pulled High to the +5V SOM input power rail.
  - When PWROFF_C2M_L is asserted, the SOM power regulators perform a full-power shutdown of the device following the correct regulator power-down sequence. This signal does not alert application software to the power shutdown.
  - Upon deassertion of PWROFF_C2M_L, the SOM power regulators initiate a power-on sequence.

  ***Note*:** Asserting PWROFF_C2M_L does not perform a software shutdown or notify the system of the shutdown. The power regulators will start to power down instantly. Use the MIO31_SHUTDOWN pin and PMU functionality to initiate a software shutdown.

- **PWRGD_LPD_M2C:** PWRGD_LPD_M2C is an active-High output signal from the SOM power system that indicates the power status of all SOM PS low-power domain (LPD) rails. PWRGD_LPD_M2C is pulled High to 1.80V on the SOM. A carrier card can use this signal to monitor LPD status.
- **PWRGD_FPD_M2C:** PWRGD_FPD_M2C is an active-High output signal from the SOM power system that indicates the power status of all SOM PS full-power domain (FPD) rails. PWRGD_FPD_M2C is pulled High to 1.80V on the SOM. A carrier card can use this signal to monitor FPD status.

  ***Note*:** The K26 SOM does not have split rails for LPD and FPD. PWRGD_LPD_M2C and PWRGD_FPD_M2C are tied together on the SOM.

- **PWRGD_PL_M2C:** PWRGD_PL_M2C is an active-High output signal from the SOM power system that indicates the power status of all SOM PL power rails. PWRGD_PL_M2C is pulled High to 1.80V on the SOM. A carrier card can use this signal to monitor PL power status.
- **VCCOEN_PS_M2C:** VCCOEN_PS_M2C is an active-High output signal from the SOM power system to enable the PS V_{CCO} rails that are supplied by the carrier card. A carrier card can use this signal as an indication to turn power on for all PS peripherals.
- **VCCOEN_PL_M2C:** VCCOEN_PL_M2C is an active-High output signal from the SOM power system to enable the PL V_{CCO} rails that are supplied by the carrier card. A carrier card can use this signal as an indication to turn power on for all PL peripherals.

MIO Banks

- MIO banks 501 and 502 signals are accessible through the SOM240_1 connector.
- MIO bank 501 contains the MIO[51:26] pins.

  ***Note*:** The MIO[34:32] pins of bank 501 are reserved for the MPSoC PMU processor for power management functions, they are not connected to the SOM240_1 connector.
- MIO bank 502 contains the MIO[77:52] pins.

A carrier card is not required to deliver V_{CCO} to the MIO banks. The V_{CCO} for MIO banks 501 and 502 is fixed at 1.8V and is supplied by the K26 SOM.

Platform Management Unit Signals

- The platform management unit (PMU) processor supports up to twelve GPIO pins that are configurable within MIO bank 501. MIO[31:26] can be configured as PMU inputs, and MIO[37:35] can be configured as PMU outputs.

  ***Note*:** MIO[34:32] are reserved on the K26 SOM for power management functions.
- The PMU GPIOs are used for a variety of critical systems functions like watchdog timers and power management related signals.
- When not used by the PMU, these signals can be used as regular MIO pins.

PS-GTR Transceivers

- PS-GTR transceivers are accessible through the SOM240_1 connector.
- GTR_DP[3:0]_M2C_P/N pins are transmit signals from the MPSoC.
- GTR_DP[3:0]_C2M_P/N pins are receive signals to the MPSoC.
- GTR_REFCLK[3:0]_P/N pins are REFCLKs inputs to the MPSoC.
- The carrier cards must supply the appropriate clock signals as required by the application.
- The PS-GTR transceivers support the following protocols:
  - PCIe Gen1/2
  - Serial ATA (SATA) 3.1
  - USB 3.0
  - DisplayPort 1.2

- 10M/100M/1G Ethernet MAC (GEM)

HPIO: HPA, HPB, and HPC Banks

This section describes the high-performance I/O (HPIO) banks. The HPIO bank HPA (bank 66) is accessible through the SOM240_1 connector. The HPIO banks HPB (bank 65) and HPC (bank 64) are accessible through the SOM240_2 connector.

- All signals in the HPIO banks are routed as differential pairs. Each HPIO bank supports one differential global clock input, namely HPA_CLK0_P/N, HPB_CLK0_P/N, and HPC_CLK0_P/N.
- V_{CCO} for the HP(x) bank is supplied by the carrier card through the VCCO_HP(x) pins where x = A, B, C.

HPIO bank connections are listed in the following table.

Table 13: **HPIO Bank Connections**

HPIO Bank	Connector	HPIO Signals	Clock-capable Pins	V_{CCO}
HPA bank 66	SOM240_1	HPA[14:00]_P/N, HPA_CLK0_P/N	HPA_CLK0_P/N	VCCO_HPA
HPB bank 65	SOM240_2	HPB[19:00]_P/N, HPB_CLK0_P/N	HPB_CLK0_P/N	VCCO_HPB
HPC bank 64	SOM240_2	HPC[19:00]_P/N, HPC_CLK0_P/N	HPC_CLK0_P/N	VCCO_HPC

MIPI Support

The differential signal pairs in HPIO banks HPA, HPB, and HPC are organized to support MIPI links with up to four lanes. A four lane MIPI link requires five differential HPIO signals, with the first signal pair supporting a clock-capable signal pair. Bank HPA can support three MIPI links. Banks HPB and HPC can support four MIPI links each. The following table lists the MIPI links.

Table 14: **Bank Organization**

	CLK	CSI0	CSI1	CSI2	CSI3
MIPIA0	HPA00_CC	HPA01	HPA02	HPA03	HPA04
MIPIA1	HPA05_CC	HPA06	HPA07	HPA08	HPA09
MIPIA2	HPA10_CC	HPA11	HPA12	HPA13	HPA14
MIPIB0	HPB00_CC	HPB01	HPB02	HPB03	HPB04
MIPIB1	HPB05_CC	HPB06	HPB07	HPB08	HPB09
MIPIB2	HPB10_CC	HPB11	HPB12	HPB13	HPB14
MIPIB3	HPB15_CC	HPB16	HPB17	HPB18	HPB19
MIPIC0	HPC00_CC	HPC01	HPC02	HPC03	HPC04
MIPIC1	HPC05_CC	HPC06	HPC07	HPC08	HPC09
MIPIC2	HPC10_CC	HPC11	HPC12	HPC13	HPC14
MIPIC3	HPC15_CC	HPC16	HPC17	HPC18	HPC19

HDIO: HDA, HDB, and HDC Banks

This section describes the high-density I/O (HDIO) banks. The HDIO bank HDA (bank 45) is accessible through the SOM240_1 connector. HDIO banks HDB (bank 43) and HDC (bank 44) are accessible through the SOM240_2 connector.

- The HDA bank supports 21 single-ended signals HDA[20:0]. Three signals (HDA00_CC, HDA08_CC, and HDA16_CC) are clock-capable inputs available on the MPSoC.
- The HDB and HDC bank supports 24 single-ended signals HDx[23:0]. Three signals (HDx00_CC, HDx08_CC, and HDx16_CC) are clock-capable inputs available on the MPSoC.
- V_{CCO} for the HD(x) bank is supplied by the carrier card through the VCCO_HD(x) pins where x = A, B, or C.

HDIO bank connections are listed in the following table.

Table 15: **HDIO Bank Connections**

HDIO Bank	Connector	HDIO Signals	Clock-capable Pins	V_{CCO}
HDA bank 45	SOM240_1	HDA[20:00]	HDA00, HDA08, HDA16	VCCO_HDA
HDB bank 43	SOM240_2	HDB[23:00]	HDB00, HDB08, HDB16	VCCO_HDB
HDC bank 44	SOM240_2	HDC[23:00]	HDC00, HDC08, HDC16	VCCO_HDC

GTH Transceivers

- The PL GTH transceiver lanes on bank 224 are accessible through the SOM240_2 connector.
- The GTH_DP[0:3]_M2C_P/N pins are transmit signals from the MPSoC.
- The GTH_DP[3:0]_C2M_P/N pins are receive signals to the MPSoC.
- The GTR_REFCLK[0:1]_P/N pins are REFCLK inputs to the MPSoC.
- The carrier cards must supply REFCLKs to the GTH_REFCLK[0:1]_P/N pins on the SOM240_2 connector.

See *UltraScale Architecture GTH Transceivers User Guide* (UG576) for more information on the GTH transceivers.

Power Management and Sequencing

The main power supply for the K26 SOM is a single +5V power rail that is supplied by the carrier card. The V_{CCO} power rails for the PL HPIO and HDIO banks are also powered by the carrier card. The carrier card can also supply an external battery power rail to the VCC_BATT pin for RTC battery-backup power.

SOM Connector Power Pins

The following table lists all power rails required for the proper operation of the K26 SOM. The carrier card designed for your application should provide these power rails based on the required peripheral I/O voltage. These supplies must be intentionally sequenced as outlined in the Power Sequencing section.

Table 16: **SOM Power Rails**

Power Rail Name	Supported Voltage Range	Maximum Current	Description
V_{CC_SOM}	5V (4.75V – 5.25V) 50 mV p-p maximum noise	4A	Main power input to the SOM. Supplies power to on-board power regulators.
V_{CC_BATT}	1.50V		External battery input for the RTC
V_{CCO_HPA}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 66
V_{CCO_HPB}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 65
V_{CCO_HPC}	1.00V – 1.80V	1.0A	Voltage rail for HPIO bank 64
V_{CCO_HDA}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 45
V_{CCO_HDB}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 43
V_{CCO_HDC}	1.20V – 3.30V	1.0A	Voltage rail for HDIO bank 44

For the selected I/O type, the supply voltage tolerance at the SOM connector must be within +3%/–2%. For example:

- If an HPIO bank is configured for the LVDS (1.8V) standard, the V_{CCO} at the SOM connector pin must be within 1.764V–1.854V.
- If an HDIO bank is configured for the LVDS_25 standard, the V_{CCO} at the SOM connector pin must be within 2.450V–2.575V.

Power Sequencing

The carrier card power management circuit for your application must use the following sequence to power on the K26 SOM. Your carrier card supplies the +5V SOM power rail (V_{CC_SOM}).

1. When the V_{CC_SOM} voltage level is within the specified range, the carrier card deasserts the POWER_OFF_C2M_L signal.
2. The K26 SOM initiates onboard power sequencing.
3. The K26 SOM asserts the VCCOEN_PS_M2C signal, indicating to the carrier card to turn on the supply rails for the PS peripheral devices.
4. The K26 SOM asserts the VCCOEN_PL_M2C signal, indicating to the carrier card to turn on the supply rails for the PL peripheral devices as well as all V_{CCO} rails for the HPIO and HDIO banks.

Device Firmware

The K26 SOM includes two memory devices that are used for nonvolatile storage of firmware and an EEPROM for SOM device configuration information.

Application-agnostic reference implementations of the SOM boot firmware and fixed peripheral board support package (BSP) are made available in the Xilinx tools and software repositories. The references include:

- First-stage boot loader (FSBL)
- Arm trusted firmware (ATF)
- U-Boot
- Platform management unit (PMU)

The reference implementations are available for you to use and modify for your unique product implementation.

EEPROM

The K26 SOM EEPROM is pre-programmed during manufacturing and provides device configuration, identification, and manufacturing data. The EEPROM content is protected as a read-only interface and organized per the IPMI specification. See the information on EEPROM data mapping in the *IPMI Platform Management FRU Information Storage Definition v1.0*, Revision 1.3, March 24, 2015.

The K26 SOM EEPROM includes the IPMI records defined in the following table. The addresses are expressed in EEPROM physical address offsets.

Table 17: **EEPROM Content Summary**

Record Area	IPMI Record Type	Record Start	Record End
Header and board area record	Board area record	0x00	0x67
DC load multi-record	OEM multi-record	0x68	0x79
MAC address multi-record	OEM multi-record	0x7A	0x89
Memory configuration multi-record	OEM multi-record	0x9B	0xF6

The following table defines the specific content of the EEPROM.

Table 18: **EEPROM Content**

Address	Byte Length	Format	Description
Header and Board Area Record			
0	1	Binary	Version
1	1	Binary	Internal user area
2	1	Binary	Chassis information area
3	1	Binary	Board area
4	1	Binary	Product information area
5	1	Binary	Multi-record area
6	1	Binary	Pad
7	1	Binary	Checksum
8	1	Binary	Version
9	1	Binary	Length
A	1	Binary	Language code
B	3	Binary	Manufacturing date starting on 1/1/1996 in minutes
E	1	Binary	Board manufacturer type-length
F	6	ASCII	Board manufacturer is Xilinx
15	1	Binary	Board product name type-length
16	16	ASCII	Board product name
26	1	Binary	Board serial type-length
27	16	ASCII	Board serial number (any printable ASCII character)
37	1	Binary	Board part number type-length
38	9	ASCII	Board part number

Table 18: **EEPROM Content** *(cont'd)*

Address	Byte Length	Format	Description
41	1	Binary	FRU file ID type-length
42	1	ASCII	FRU file ID (00)
43	1	Binary	Revision type-length
44	8	ASCII	Revision number
4C	1	Binary	PCIe information type/length byte
4D	8	Binary	PCIe information
55	1	Binary	UUID type-length byte
56	16	Binary	UUID
66	1	Binary	End of field
67	1	Binary	Board area checksum
DC Load Multi-record			
68	1	Binary	Record type (DC load)
69	1	Binary	Record format
6A	1	Binary	Length
6B	1	Binary	Record checksum
6C	1	Binary	Header checksum
6D	1	Binary	Output number
6E	2	Binary	Nominal voltage (10 mV): V_{CC_SOM} (5V)
70	2	Binary	Specified minimum voltage (10 mV)
72	2	Binary	Specified maximum voltage (10 mV)
74	2	Binary	Specified ripple and noise pk-pk 10 Hz to 30 MHz (mV)
76	2	Binary	Minimum current load (mA)
78	2	Binary	Maximum current load (mA)
MAC Address Multi-record			
7A	1	Binary	Record type (OEM)
7B	1	Binary	Type
7C	1	Binary	Length
7D	1	Binary	Record checksum
7E	1	Binary	Header checksum
7F	3	Binary	Xilinx internet assigned numbers authority (IANA) ID
82	1	Binary	Version number
83	6	Binary	MAC ID 0
Memory Configuration Multi-record			
9B	1	Binary	Record type (OEM)
9C	1	Binary	Record format
9D	1	Binary	Length
9E	1	Binary	Record checksum
9F	1	Binary	Header checksum
A0	3	Binary	Xilinx IANA ID
A3	8	ASCII	Memory
AB	12	ASCII	Primary boot device memory definition
B7	1	Binary	Memory type field end

Table 18: **EEPROM Content** *(cont'd)*

Address	Byte Length	Format	Description
B8	8	ASCII	Memory
C0	12	ASCII	SOM secondary boot device memory
CC	1	Binary	Memory type field end
CD	8	ASCII	Memory
D5	12	ASCII	SOM PS DDR memory
E1	1	Binary	Memory type field end
E2	8	ASCII	Memory
EA	12	ASCII	SOM PL DDR memory
F6	1	Binary	Memory type field end

QSPI

The K26 includes a 512 Mb (64 MB) QSPI flash memory device. It supports interface clock speeds up to 40 MHz, and can be used as the primary boot device for the MPSoC processing subsystem. The QSPI device is left blank during SOM manufacturing.

eMMC

The K26 SOM includes a 16 GB eMMC flash memory device. It supports interface clock speeds up to 50 MHz, and can be used as the primary or secondary boot device for the MPSoC processing subsystem. The eMMC device is left blank during SOM manufacturing.

Mechanical and Thermal

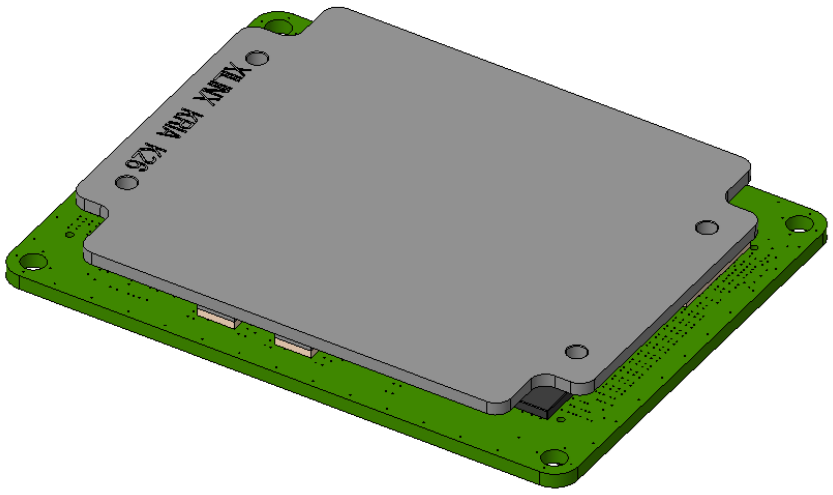
The production K26 SOM is available in both commercial and industrial temperature grades. The temperature specification is defined relative to the junction temperature of the MPSoC as measured by the integrated System Monitor. All the other components on the SOM should remain within their operating limits as long as temperature is maintained in the MPSoC. Your design is expected to have a thermal solution connected to the integrated heat spreader, this is to maintain the operating temperature within these limits under the operating conditions (i.e., ambient temperature, airflow, etc.) of your system.

Table 19: **K26 SOM Specifications**

K26 SOM	Operating Temperature
Commercial grade: K26C SOM	0°C to 85°C (as measured at MPSoC junction temperature)
Industrial grade: K26I SOM	–40°C to 100°C (as measured at MPSoC junction temperature)

The K26 SOM is supplied with an aluminum heat spreader. This heat spreader makes full contact with all the high-power active components, including the MPSoC, DDR4, eMMC, and power regulators. The primary function of the heat spreader is to transfer the non-uniform heat distribution of the module that is generated on the PCB assembly to the heat spreader, making the heat flux more uniform and spread over a larger surface area. This allows for more efficient heat transfer out of the package to an attached cooling device and simplifies thermal design. The user-defined system cooling solutions should be designed to directly attach to the heat spreader.

Figure 3: **K26 SOM**



IMPORTANT! *The thermal solution on your system must provide adequate cooling to maintain all the components on the PCB (including the K26 SOM) at below the maximum temperature specifications as detailed in Table 19: K26 SOM Specifications.*

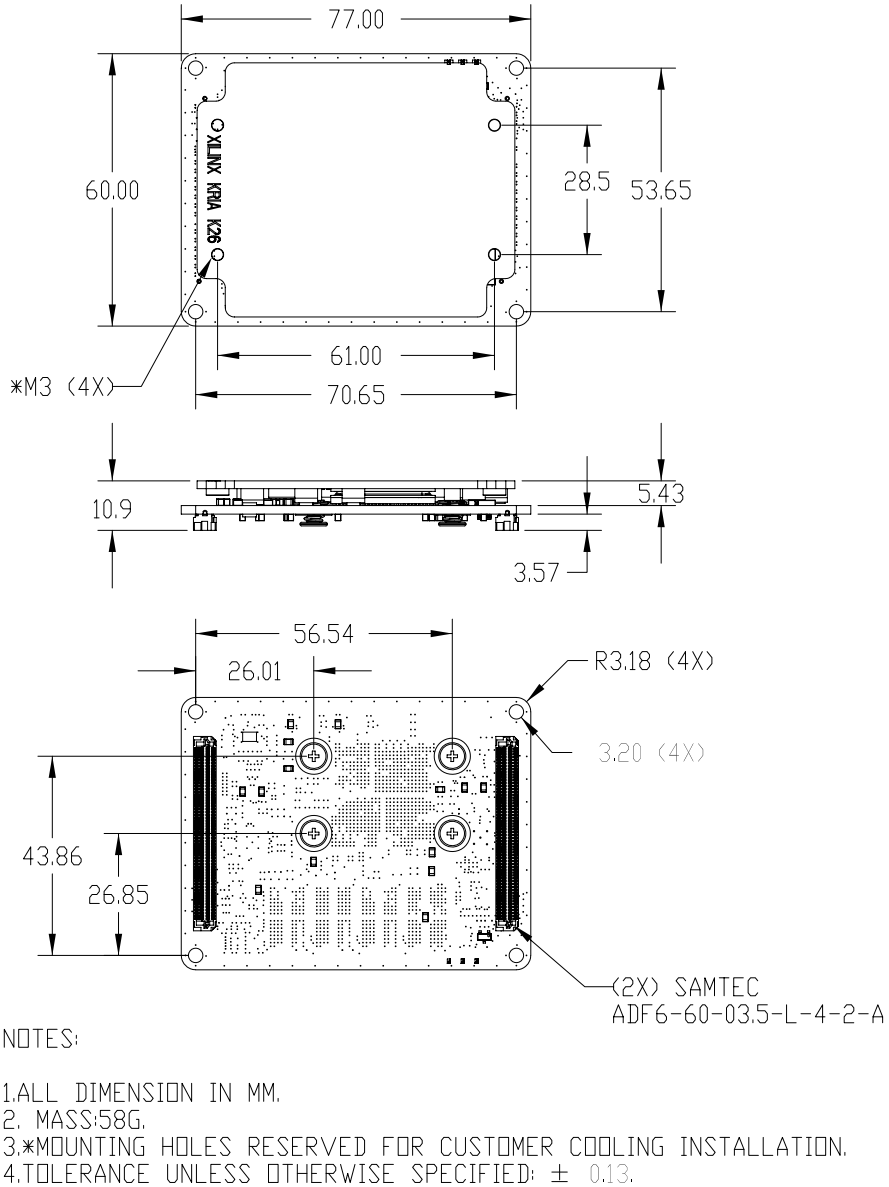
Mechanical Dimensions

The following table and figures define the mechanical specifications of the K26 SOM. The following mechanical drawing provides the detailed dimensions of the SOM.

Table 20: **K26 SOM Mechanical Specifications**

Parameter	Specification
SOM length	77 mm
SOM width	60 mm
SOM height	10.9 mm
Mass	58 grams

Figure 4: **K26 SOM Dimensions**



The K26 SOM 3D CAD files are available for your platform or carrier design reference. These files are design aides in your cooling mechanical design, system assembly interference and clearance reviews, and board-to-board (B2B) connector placement alignment checks.

SOM PCB Assembly

Figure 5: **Top PCBA Views**

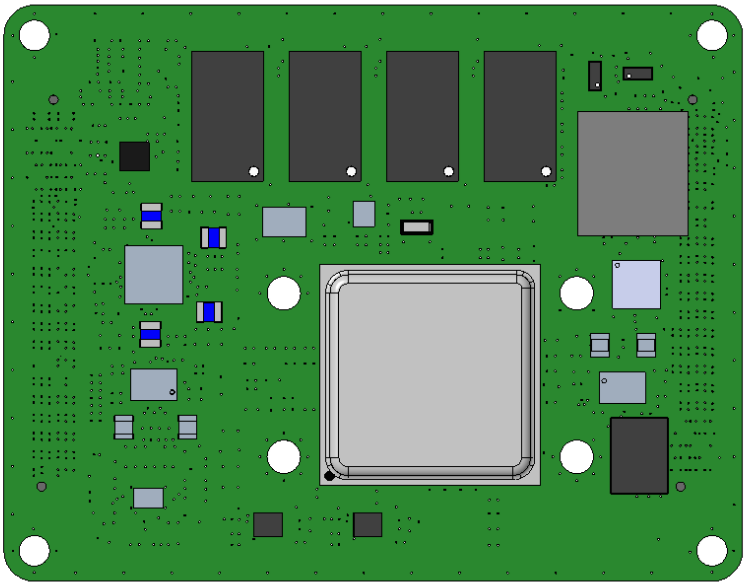
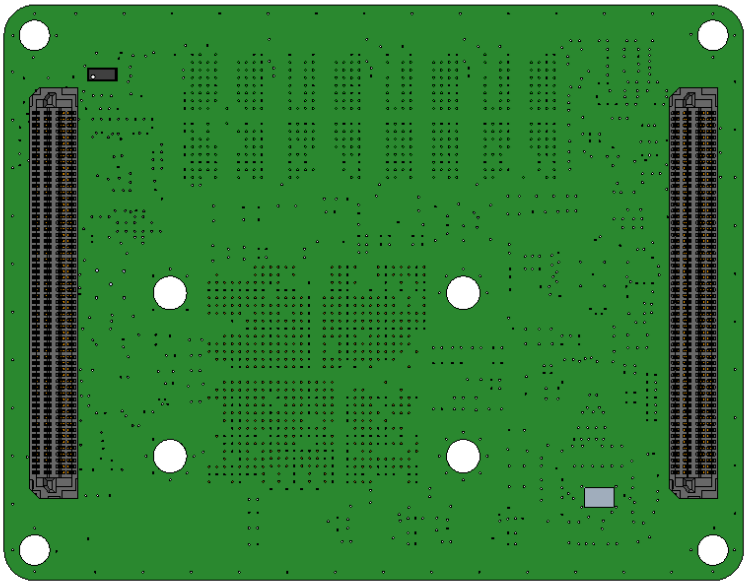


Figure 6: **Bottom PCBA Views**



Thermal

Operating Environment and Storage Temperature Conditions

The following table defines the temperature and humidity conditions for device operation and storage.

Table 21: **Operating Environment and Storage Temperatures and Humidity Conditions**

Specification	Condition
Operating environment temperature	Use case dependent
Storage temperature	–40°C to 75°C
Operating humidity, non-condensing	8% to 90%, and a dew point of –12°C
Storage humidity, non-condensing	5% to 95%

Thermal Design

The K26 SOM is built with a thermal interface plate that for most deployed applications is not a full thermal solution. It is your responsibility to integrate the SOM into a system-level thermal solution that can dissipate the application-specific thermal load of the SOM while maintaining it within specified temperature limits. The *Kria K26 SOM Thermal Design Guide* (UG1090) provides documentation to support the integration of the SOM into your application system thermal and mechanical solutions including thermal modeling and detailed design specifications.

Regulatory Compliance Statements

Safety

The following safety standards apply to all products listed in this document.

IEC 62368-1, 2nd Edition, 2014/A11:2017, *Information technology equipment – Safety, Part 1: General requirements*

EN 62368-1, 2nd Edition, 2014/A11:2017, *Information technology equipment – Safety, Part 1: General requirements*

FCC Class A Products

The following is a list of the products covered by this data sheet:

- SM-K26-XCL2GC
- SM-K26-XCL2GI
- SM-K26-XCL2GC-ED
- SM-K26-XCL2GI-ED

Regulatory Compliance Statements are valid for the production version of the K26 SOM.

Safety Compliance

The following safety standards apply to all products listed above.

UL 62368-1, 2nd Edition, 2014/A11:2017 (Information Technology Equipment - Safety - Part 1: General Requirements)

CSA C22.2 No. 60950-1-07, 2nd Edition, 2014/A11:2017 (Information Technology Equipment - Safety - Part 1: General Requirements)

EU LVD Directive 2014/35/EU

EN/IEC-62368-12014/A11:2017

EMC Compliance

Class A Products

The following standards apply:

- FCC Part 15 – Radiated & Conducted Emissions (USA)
- CAN ICES-3(A)/NMB-3(A) – Radiated & Conducted Emissions (Canada)
- CISPR 32 – Radiated & Conducted Emissions (International)
- EN55032: 2015 – Radiated & Conducted Emissions (European Union)
- EN55035:2017 – Immunity (European Union)
- EMC Directive 2014/30/EU
- VCCI (Class A)– Radiated & Conducted Emissions (Japan)
- CNS13438 – Radiated & Conducted Emissions (Taiwan)
- CNS 15663 - RoHS (Taiwan)
- AS/NZS CISPR 32 – Radiated and Conducted Emissions (Australia/New Zealand)
- Article 58-2 of Radio Waves Act, Clause 3 (Korea)

Regulatory Compliance Markings

When required, these products are provided with the following product certification markings:

- UL Listed Accessories Mark for the USA and Canada
- CE mark
- FCC markings
- VCCI marking
- Australian RCM mark
- Korea MSIP mark
- Taiwan BSMI mark

- German GS mark

FCC Class A User Information

The Class A products listed above comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

CAUTION! *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at their own expense.*

ATTENTION! *Cet équipement a été testé et jugé conforme à la Class A digital device, conformément à la règle 15 du standard FCC. Ces limites sont conçues pour fournir des protections contre des interférences nuisibles lorsque l'équipement est utilisé dans un environnement commercial. Cet équipement génère, utilise et peut émettre des énergies de radio-fréquence et, s'il n'est pas installé et utilisé conformément aux instructions, peut nuire aux communications radio. L'exploitation de cet équipement dans une zone résidentielle est susceptible de causer des interférences nuisibles, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates à ses propres frais.*

VORSICHT! *Dieses Gerät wurde getestet und entspricht den Grenzwerten für digitale Geräte der Klasse A gemäß Teil 15 der FCC-Bestimmungen. Diese Grenzwerte bieten einen angemessenen Schutz gegen schädliche Interferenzen, wenn das Gerät in einer gewerblichen Umgebung betrieben wird. Dieses Gerät erzeugt und verwendet Hochfrequenzenergie und kann diese abstrahlen. Wenn es nicht gemäß den Anweisungen installiert und verwendet wird, kann dies Funkstörungen verursachen. Der Betrieb dieses Geräts in einem Wohngebiet kann schädliche Interferenzen verursachen. In diesem Fall muss der Benutzer die Interferenz auf eigene Kosten beheben.*

CAUTION! *If the device is changed or modified without permission from Xilinx, the user may void their authority to operate the equipment.*

ATTENTION! *Si l'appareil est modifié sans l'autorisation de Xilinx, l'utilisateur peut annuler son abilité à utiliser l'équipement.*

VORSICHT! *Wenn das Gerät ohne Erlaubnis von Xilinx geändert wird, kann der Benutzer seine Berechtigung zum Betrieb des Geräts verlieren.*

Canadian Compliance (Industry Canada)

CAN ICES-3(A)/NMB-3(A)

RoHS Compliance

- RoHS Directive 2011/65/EU
- RoHS 3 Directive 2015/863

- SJ/T 11363-2006, 11364-2006, and GB/T 26572-2011 (China RoHS)

VCCI Class A Statement

この装置は、クラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。
この場合には使用者が適切な対策を構ずるよう要求されることがあります。 VCCI-A

KCC Notice Class A (Republic of Korea Only)

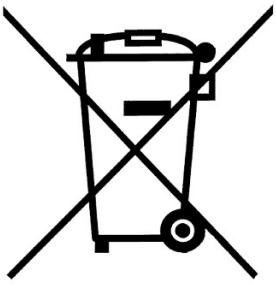
A급 기기 (업무용 방송통신기기) **CLASS A device** (commercial broadcasting and communication equipment	이 기기는 업무용(A급)으로 전자파적합등록을 한 기기이오니 판매자 또는 사용자는 이 점을 주의하시기 바라며, 가정외의 지역에서 사용하는 것을 목적으로 합니다. This device has been appoved by EMC registration. Distributors or users pay attention to this point. This device is usually aimed to be used in other area except at home

BSMI Class A Notice (Taiwan)

警告使用者:

此為甲類資訊技術設備，於居住環境中使用時，可能會造成射頻擾動，在此種情況下，使用者會被要求採取某些適對當的對策。

EU WEEE Logo



[redacted]

Manufacturer Declaration European Community

Manufacturer Declaration

Xilinx declares that the equipment described in this document is in conformance with the requirements of the European Council Directives listed below:

- Low Voltage Directive 2014/35/EU
- EMC Directive 2014/30/EU
- RoHS 3 Directive 2011/65/EU, 2015/863
- China RoHS Declaration: Standards SJ/T 11363-2006, 11364-2006, and GB/T 26572-2011
- Reach Regulation 1907/2006
- POP Regulation 2019/1021

These products follow the provisions of the European Directive 2014/53/EU.

Dette produkt er i overensstemmelse med det europæiske direktiv 2014/53/EU.

Dit product is in navolging van de bepalingen van Europees Directief 2014/53/EU.

Tämä tuote noudattaa EU-direktiivin 2014/53/EU määräyksiä.

Ce produit est conforme aux exigences de la Directive Européenne 2014/53/EU.

Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2014/53/EU.

Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2014/53/EU.

Questo prodotto è conforme alla Direttiva Europea 2014/53/EU.

Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 2014/53/EU.

Este produto cumpre com as normas da Diretiva Européia 2014/53/EU.

Este producto cumple con las normas del Directivo Europeo 2014/53/EU.

Denna produkt har tillverkats i enlighet med EG-direktiv 2014/53/EU.

This declaration is based upon compliance of the Class A products listed above to the following standards:

EN 55032 (CISPR 32 Class A) RF Emissions Control

EN 55035:2017 (CISPR 35) Electromagnetic compatibility of multimedia equipment – Immunity requirements

EN 62368-1, 2nd Edition, 2014/A11:2017 *Information technology equipment – Safety, Part 1: General Requirements*

EN 50581:2012 - Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances.

CAUTION! *In a domestic environment, Class A products could cause radio interference, in which case the user may be required to take adequate measures.*

ATTENTION! *Dans un environnement domestique, les produits de Classe A peuvent causer des interférences radio, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates.*

VORSICHT! *In einer häuslichen Umgebung können Produkte der Klasse A Funkstörungen verursachen. In diesem Fall muss der Benutzer möglicherweise geeignete Maßnahmen ergreifen.*

Responsible Party

Xilinx, Inc.
2100 Logic Drive, San Jose, CA 95124
United States of America
Phone: (408) 559-7778

References

These documents provide supplemental material useful with this guide:

1. *Kria SOM Carrier Card Design Guide* (UG1091)
2. *Zynq UltraScale+ Device Technical Reference Manual* (UG1085)
3. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
4. *UltraScale Architecture and Product Data Sheet: Overview* (DS890)
5. *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925)
6. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
7. *UltraScale Architecture PCB Design User Guide* (UG583)
8. *Zynq UltraScale+ MPSoC: Software Developers Guide* (UG1137)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
4/20/2021 Version 1.0	
Initial release.	N/A

Please Read: Important Legal Notices

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos.

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

Copyright