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MDT0400EIS-MIPI	480 x 480	MIPI Interface	TFT Module

Specification

Version: 1	Date: 24/06/2020

Revision

1	22/06/2020	First issue

* Please note: Midas Displays are able to provide a wide range of MIPI interface TFT displays. There are many more sizes available, with a range of different features. Get in touch for more information.

Display Features	
Display Size	4.0”
Resolution	480 x 480
Orientation	Square
Appearance	RGB
Logic Voltage	2.8V
Interface	MIPI
Brightness	500 cd/m^2
Touchscreen	---
Module Size	78.80 x 82.95 x 4.77mm
Operating Temperature	-30°C ~ +80°C
Pinout	24 way FFC
Pitch	0.5mm

RoHS compliant

Box Quantity	Weight / Display
---	---

* - For full design functionality, please use this specification in conjunction with the ST7701S specification.(Provided Separately)

Display Accessories

Part Number	Description

Optional Variants

Appearances	Voltage

Summary

TFT 4.0” is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This TFT LCD has a 4.0 (1:1) inch diagonally
measured active display area with 480x480 (480 horizontal by 480 vertical pixel) resolution.

General Specifications

- Size: 4.0 inch
- Dot Matrix: 480× 3(RGB) × 480 dots
- Module dimension: 78.8(H) * 82.95 (W) *4.77 mm
- Active area: 71.856(H)*70.176 (V) mm
- Dot pitch: 0.1497(H)*0.1462(V) mm
- LCD type: TFT, Normally Black, Transmissive
- View Direction: 80/80/80/80
- Aspect Ratio: 1:1
- Interface: 2-Lanes MIPI
- Driver IC: ST7701S
- Backlight Type: LED ,Normally White
- With /Without TP: Without TP
- Surface: Glare

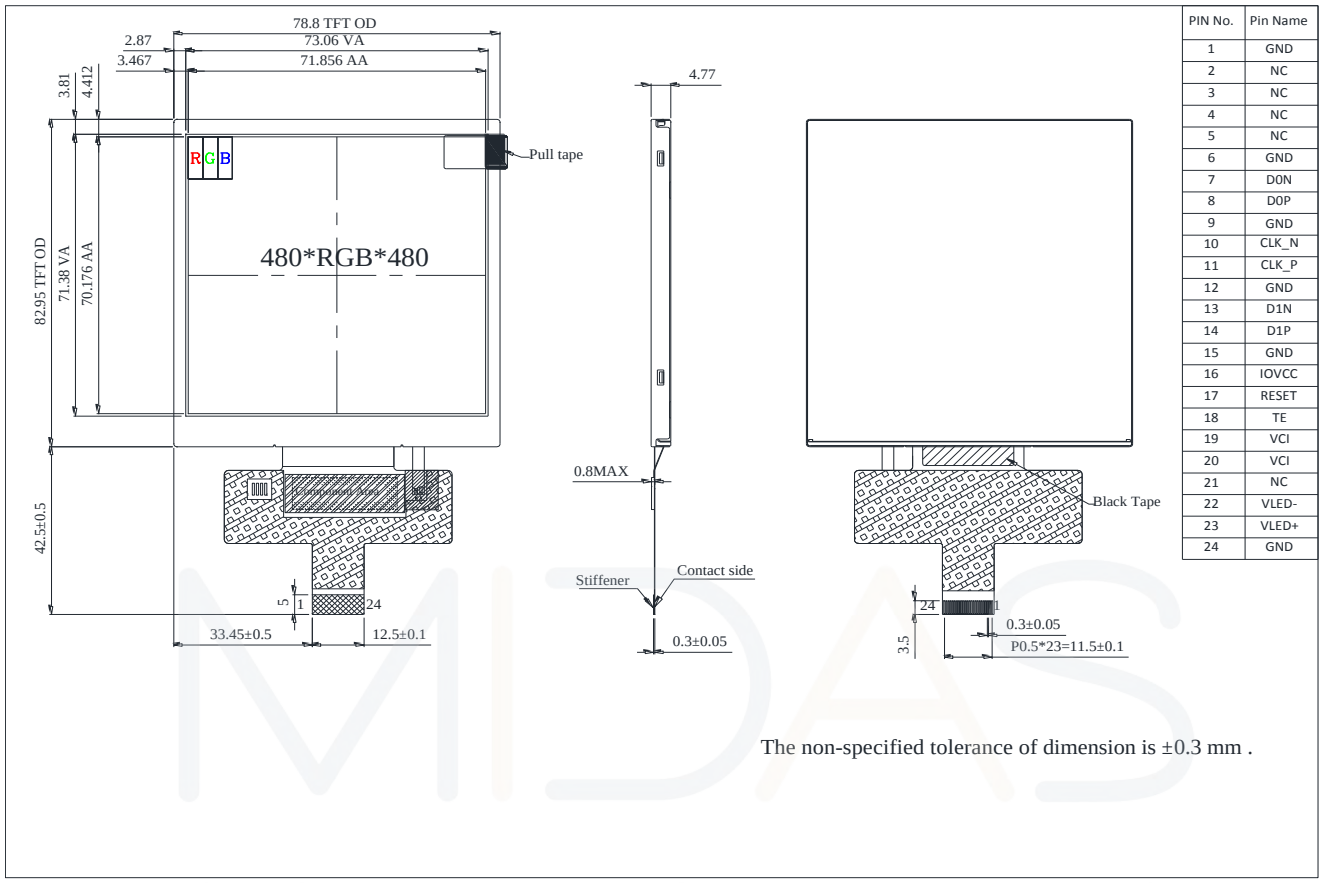
*Color tone slight changed by temperature and driving voltage.

Interface

1. LCM PIN Definition

Pin	Symbol	Function
1	GND	Power ground
2-5	NC	No connect
6	GND	Power ground
7	D0N	MIPI DSI differential data pair (Data lane 0)
8	D0P	
9	GND	Power ground
10	CLK_N	MIPI DSI differential clock pair
11	CLK_P	
12	GND	Power ground
13	D1N	MIPI DSI differential data pair(Data lane 1)
14	D1P	
15	GND	Power ground
16	IOVCC	I/O and interface power supply (1.8V)
17	RESET	Reset input
18	TE	Tearing effect output pin.
19	VCI	Analog power supply
20	VCI	Analog power supply
21	NC	No connect
22	VLED-	Power for LED backlight cathode
23	VLED+	Power for LED backlight anode
24	GND	Power ground

Contour Drawing



PIN No.	Pin Name
1	GND
2	NC
3	NC
4	NC
5	NC
6	GND
7	D0N
8	D0P
9	GND
10	CLK_N
11	CLK_P
12	GND
13	D1N
14	D1P
15	GND
16	IOVCC
17	RESET
18	TE
19	VCI
20	VCI
21	NC
22	VLED-
23	VLED+
24	GND

The non-specified tolerance of dimension is ±0.3 mm .

Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-30	—	+80	℃
Storage Temperature	TST	-30	—	+80	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≦60℃, 90% RH MAX. Temp.＞60℃, Absolute humidity shall be less than 90% RH at 60℃

Electrical Characteristics

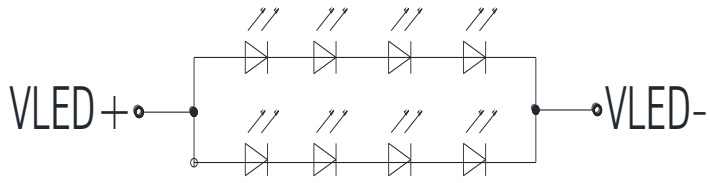
1. Typical Operation Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Interface Supply Voltage	VCI	2.5	2.8	3.6	V	
Power voltage	IOVCC	1.65	1.8	3.3	V	
Current for Driver(White)	IDD	-	11	16.5	mA	

2. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	ILED	-	100	-	mA	
LED voltage	VLED+	10.8	12.4	13.6	V	Note 1
LED Life Time		50,000	-	-	Hr	Note 2,3,4

Note 1 : There are 1 Groups LED



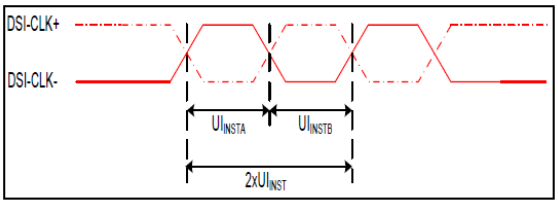
CIRCUIT DIAGRAM

Note 2 : Ta = 25 ℃
Note 3 : Brightness to be decreased to 50% of the initial value
Note 4 : The single LED lamp case.

Interface Timing

1. MIPI Interface Characteristics

High Speed Mode



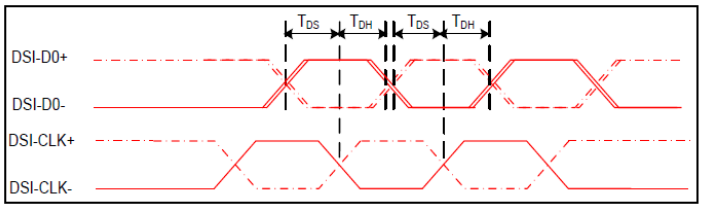


Figure 1 DSI clock channel timing

Figure 2 Rising and falling time on clock and data channel

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	UI = UI_{INSTA}= UI_{INSTB}
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Table 1 Mipi Interface-High SpeedMode Timing Characteristics

Lowe Power Mode

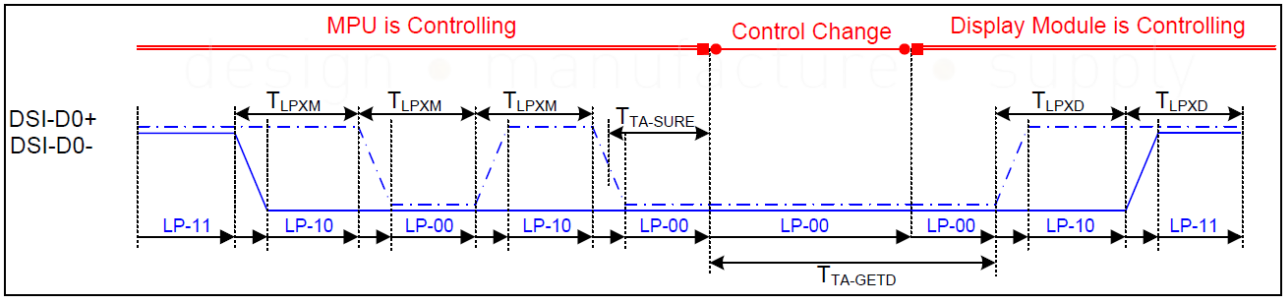


Figure 3 Bus Turnaround (BTA) from display module to MPU Timing

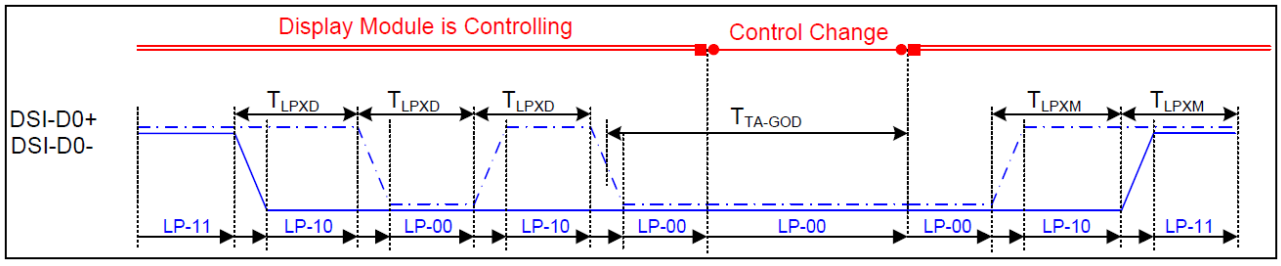


Figure 4 Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

Table 2 Mipi Interface Low Power Mode Timing Characteristics

DSI Bursts Mode

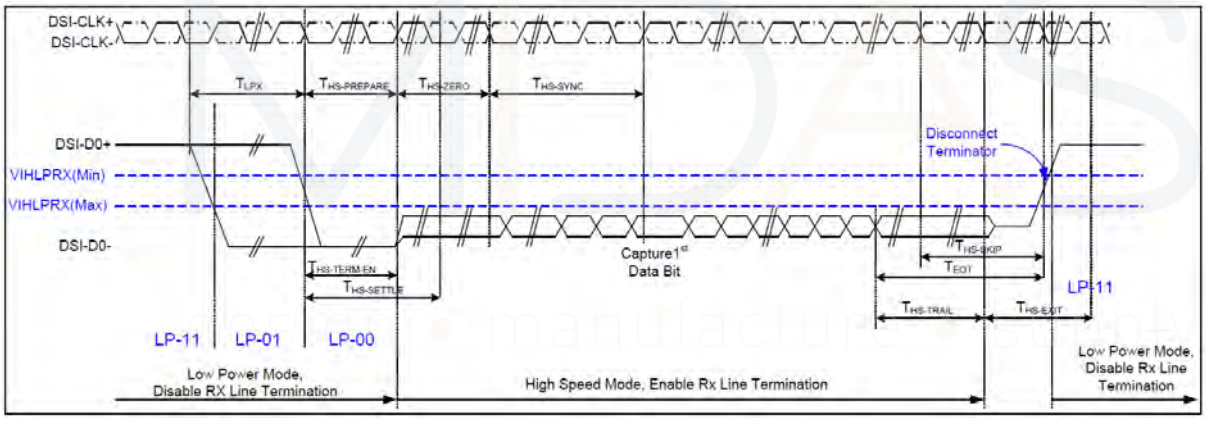


Figure 5 Data lanes-Low Power Mode to/from High Speed Mode Timing

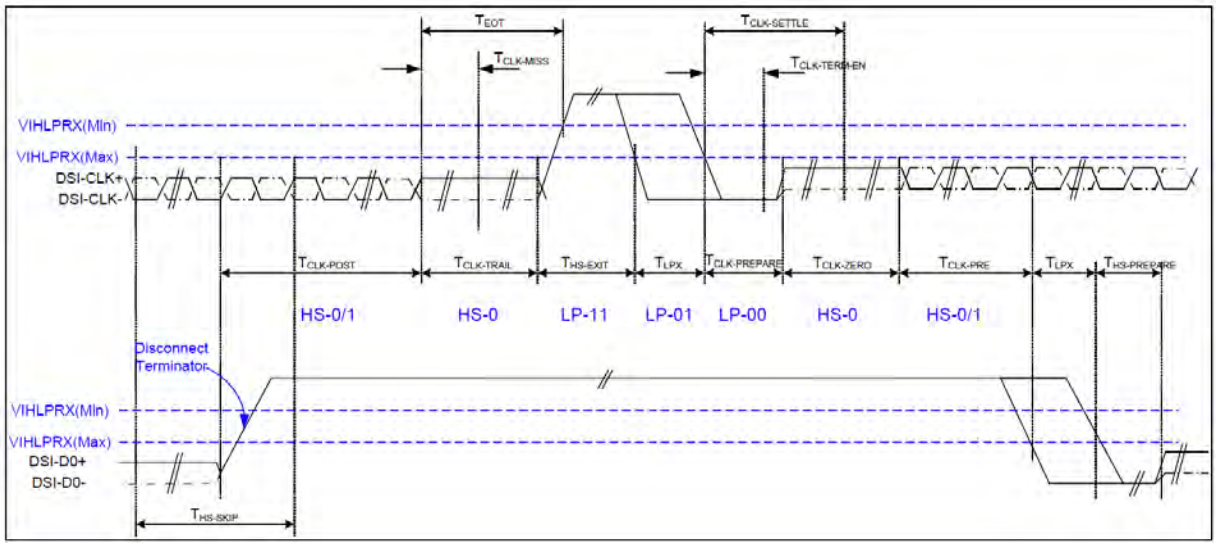


Figure 6 Clock lanes- High Speed Mode to/from Low Power Mode Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	–	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

Reset Timing

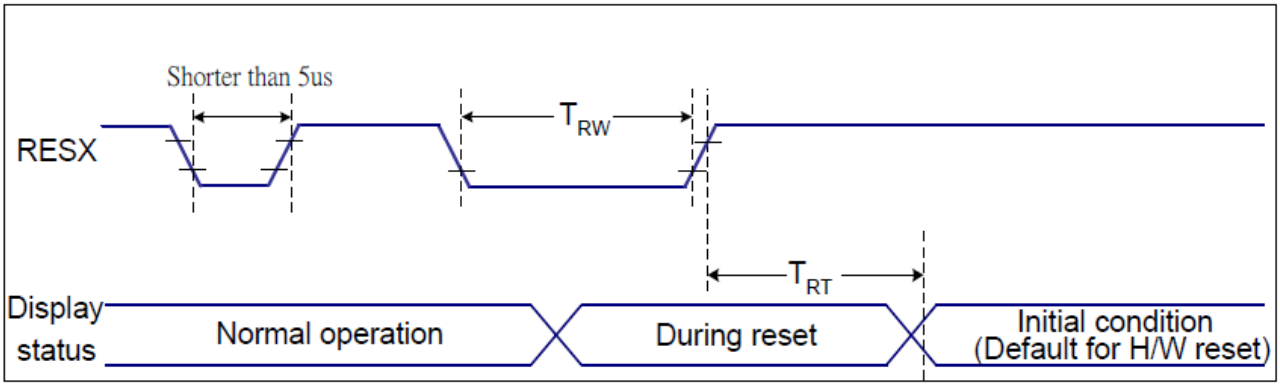


Figure 6 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

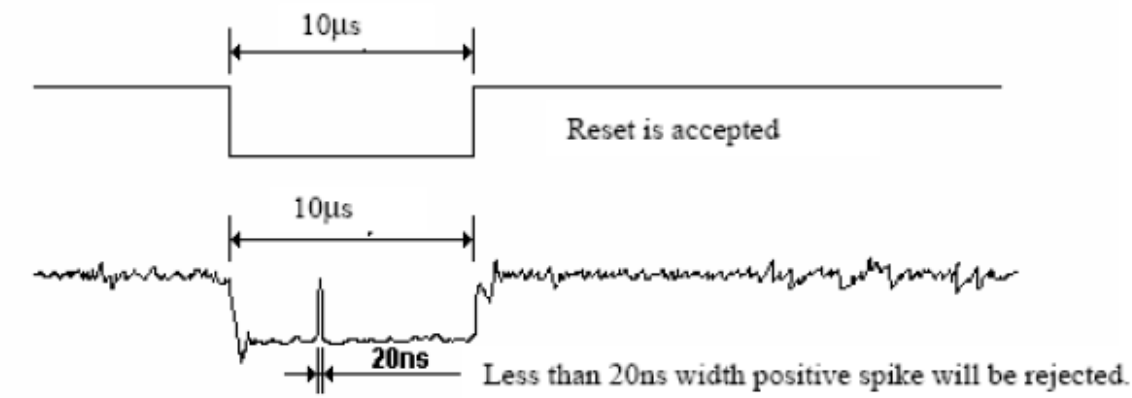
Table 3 Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr+ Tf	θ=0°、Φ=0°	-	25	35	.ms	Note 3
Contrast ratio		CR	At optimized viewing angle	640	800	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.251	0.301	0.351		Note 2,6,7
		Wy		0.277	0.327	0.377		
Viewing angle	Hor.	ΘR	CR≧10	70	80	-	Deg.	Note 1
		ΘL		70	80	-		
	Ver.	ΦT		70	80	-		
		ΦB		70	80	-		
Brightness		-	-	400	500	-	cd/m^2	Center of display
Uniformity		(U)	-	75	-	-	%	Note 5

Ta=25±2℃

Note 1: Definition of viewing angle range

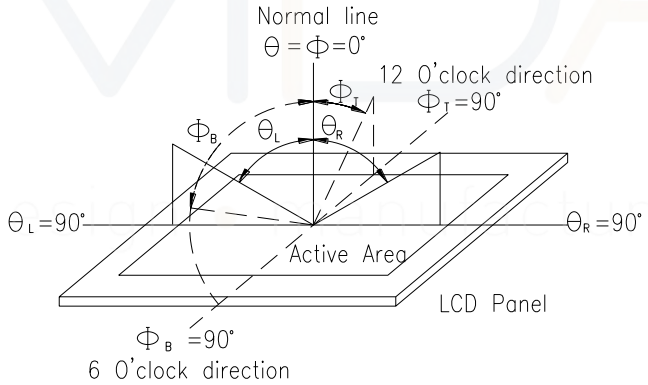


Fig. 9.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7or BM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

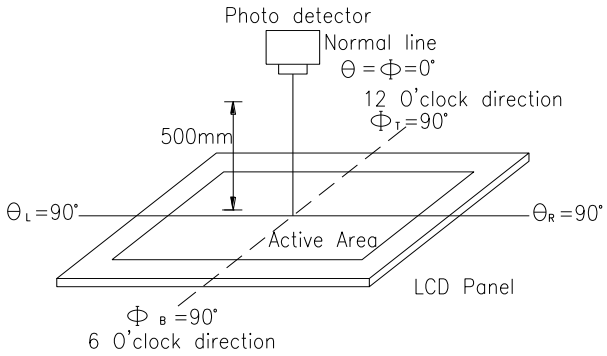
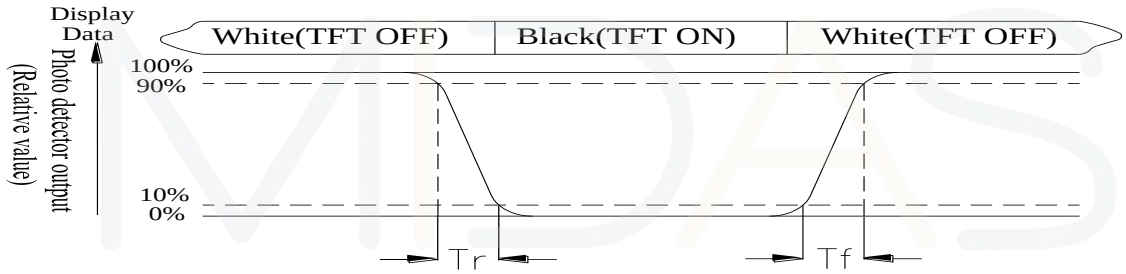


Fig. 9.2. Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.
Luminance Uniformity (U) = Lmin/Lmax x100%
L = Active area length
W = Active area width

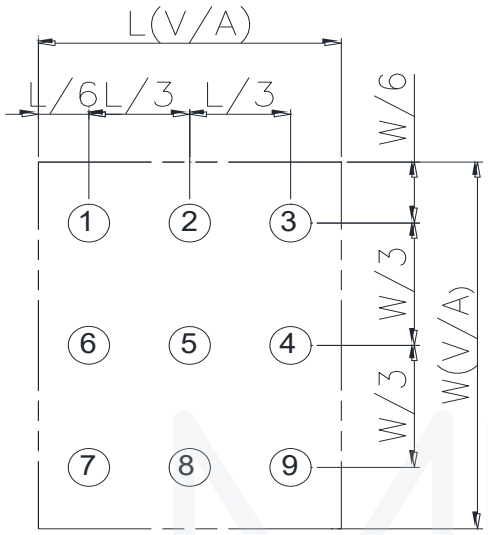


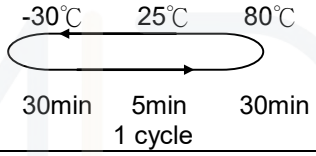
Fig 9.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Reliability

Content of Reliability Test (Super Wide temperature, -30℃~80℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	80℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30℃ 200hrs	1
High Temperature/ Humidity storage	The module should be allowed to stand at 60℃,90%RH max	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation  1 cycle	-30℃/80℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	**3**
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact) ,±800v(air), RS=330Ω CS=150pF 10 times	——

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

Initial Code For Reference

External system porch setting:125>VBP≧17, VFP≧20
Two data lanes / maximum speed 550Mbps

```
Void ST7701S_PanelInitialCode(void)
{
//-------------------------------------Reset Sequence-------------------------------------//
LCD_Nreset(1);
Delayms (1); //Delay 1ms
LCD_Nreset(0);
Delayms (1); //Delay 1ms
LCD_Nreset(1);
Delayms (120); //Delay 120ms
WriteComm (0x11);
Delayms (120); //Delay 120ms

//-----------------------------------Initial setting-----------------------------------------//
WriteComm (0xFF);
WriteData (0x77);
WriteData (0x01);
WriteData (0x00);
WriteData (0x00);
WriteData (0x10);

WriteComm (0xC0);
WriteData (0x3B);
WriteData (0x00);

WriteComm (0xC1);
WriteData (0x0D);
WriteData (0x02);

WriteComm (0xC2);
WriteData (0x21);
WriteData (0x08);

WriteComm (0xCC);
WriteData (0x10);

WriteComm (0xB0);
WriteData (0x00);
WriteData (0x05);
WriteData (0x0F);
WriteData (0x0D);
WriteData (0x13);
WriteData (0x07);
WriteData (0x01);
```

```
WriteData (0x08);
WriteData (0x09);
WriteData (0x1E);
WriteData (0x05);
WriteData (0x12);
WriteData (0x10);
WriteData (0xA7);
WriteData (0x2F);
WriteData (0x18);

WriteComm (0xB1);
WriteData (0x00);
WriteData (0x0F);
WriteData (0x17);
WriteData (0x0C);
WriteData (0x0D);
WriteData (0x05);
WriteData (0x01);
WriteData (0x08);
WriteData (0x08);
WriteData (0x1E);
WriteData (0x05);
WriteData (0x13);
WriteData (0x11);
WriteData (0xA7);
WriteData (0x2F);
WriteData (0x18);

WriteComm (0xFF);
WriteData (0x77);
WriteData (0x01);
WriteData (0x00);
WriteData (0x00);
WriteData (0x11);

WriteComm (0xB0);
WriteData (0x4D);

WriteComm (0xB1);
WriteData (0x4F);

WriteComm (0xB2);
WriteData (0x07);

WriteComm (0xB3);
WriteData (0x80);

WriteComm (0xB5);
```

```
WriteData (0x47);

WriteComm (0xB7);
WriteData (0x85);

WriteComm (0xB8);
WriteData (0x21);

WriteComm (0xB9);
WriteData (0x10);

WriteComm (0xC1);
WriteData (0x78);

WriteComm (0xC2);
WriteData (0x78);

WriteComm (0xD0);
WriteData (0x88);

Delayms (100);

WriteComm (0xE0);
WriteData (0x00);
WriteData (0x00);
WriteData (0x02);

WriteComm (0xE1);
WriteData (0x08);
WriteData (0x00);
WriteData (0x0A);
WriteData (0x00);
WriteData (0x07);
WriteData (0x00);
WriteData (0x09);
WriteData (0x00);
WriteData (0x00);
WriteData (0x33);
WriteData (0x33);

WriteComm (0xE2);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
```


```
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);

WriteComm (0xE3);
WriteData (0x00);
WriteData (0x00);
WriteData (0x33);
WriteData (0x33);

WriteComm (0xE4);
WriteData (0x44);
WriteData (0x44);

WriteComm (0xE5);
WriteData (0x0E);
WriteData (0x2D);
WriteData (0xA0);
WriteData (0xA0);
WriteData (0x10);
WriteData (0x2D);
WriteData (0xA0);
WriteData (0xA0);
WriteData (0x0A);
WriteData (0x2D);
WriteData (0xA0);
WriteData (0xA0);
WriteData (0x0C);
WriteData (0x2D);
WriteData (0xA0);
WriteData (0xA0);

WriteComm (0xE6);
WriteData (0x00);
WriteData (0x00);
WriteData (0x33);
WriteData (0x33);

WriteComm (0xE7);
WriteData (0x44);
WriteData (0x44);

WriteComm (0xE8);
WriteData (0x0D);
WriteData (0x2D);
```

```
WriteData (0xA0);
WriteData (0xA0);
WriteData (0x0F);
WriteData (0x2D);
WriteData (0xA0);
WriteData (0xA0);
WriteData (0x09);
WriteData (0x2D);
WriteData (0xA0);
WriteData (0xA0);
WriteData (0x0B);
WriteData (0x2D);
WriteData (0xA0);
WriteData (0xA0);

WriteComm (0xEB);
WriteData (0x02);
WriteData (0x01);
WriteData (0xE4);
WriteData (0xE4);
WriteData (0x44);
WriteData (0x00);
WriteData (0x40);

WriteComm (0xEC);
WriteData (0x02);
WriteData (0x01);

WriteComm (0xED);
WriteData (0xAB);
WriteData (0x89);
WriteData (0x76);
WriteData (0x54);
WriteData (0x01);
WriteData (0xFF);
WriteData (0xFF);
WriteData (0xFF);
WriteData (0xFF);
WriteData (0xFF);
WriteData (0xFF);
WriteData (0x10);
WriteData (0x45);
WriteData (0x67);
WriteData (0x98);
WriteData (0xBA);

WriteComm (0xFF);
WriteData (0x77);
```

```
WriteData (0x01);
WriteData (0x00);
WriteData (0x00);
WriteData (0x00);

WriteComm (0x11);

WriteComm (0x36);
WriteData (0x00);

WriteComm (0x29);

}
```