150MHz Differential Twisted Pair Driver

The EL2141 is a very high bandwidth amplifier whose output is in differential form, and is thus primarily targeted for applications such as driving twisted pair lines, or any application where common mode injection is likely to occur. The input signal can be in either single-ended or differential form, but the output is always in differential form.

On the EL2141, two feedback inputs provide the user with the ability to set the device gain, (stable at minimum gain of two).

The output common mode level is set by the reference pin (V_{REF}), which has a -3dB bandwidth of over 100MHz. Generally, this pin is grounded, but it can be tied to any voltage reference.

The transmission of ADSL/HDSL signals requires very low distortion amplification, so this amplifier was designed with this as a primary goal. The actual signal distortion levels depend upon input and output signal amplitude, as well as the output load impedance. (See distortion data inside.)

Both outputs (V_{OUT}, V_{OUTB}) are short circuit protected to withstand temporary overload condition.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL2141CS	8-pin SOIC	-	MDP0027
EL2141CS-T7	8-pin SOIC	7"	MDP0027
EL2141CS-T13	8-pin SOIC	13"	MDP0027
EL2141CSZ (See Note)	8-pin SOIC (Pb-free)	-	MDP0027
EL2141CSZ-T7 (See Note)	8-pin SOIC (Pb-free)	7"	MDP0027
EL2141CSZ-T13 (See Note)	8-pin SOIC (Pb-free)	13"	MDP0027

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
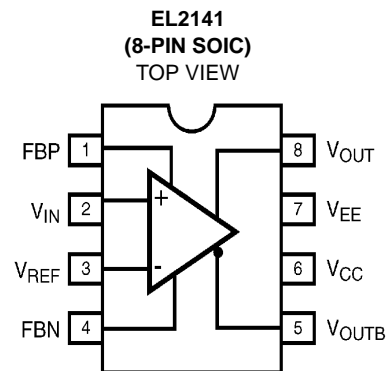
Features

- Fully differential inputs, outputs, and feedback
- Differential input range ±2.3V
- 150MHz 3dB bandwidth
- 800V/μs slew rate
- -55dB distortion at 3MHz
- -75dB distortion at 100kHz
- ±5V supplies or +6V single supply
- 50mA minimum output current
- Output swing (200Ω load) to within 1.5V of supplies (14V_{PKPK} differential)
- Low power-11mA typical supply current
- Pb-free available (RoHS compliant)

Applications

- Twisted pair driver
- Differential line driver
- VGA over twisted pair
- ADSL/HDSL driver
- Single ended to differential amplification
- Transmission of analog signals in a noisy environment

Pinout

EL2141
(8-PIN SOIC)
TOP VIEW

Pin	Name	Pin	Name
1	FBP	8	V_{OUT}
2	V_{IN} (+)	7	V_{EE}
3	V_{REF} (-)	6	V_{CC}
4	FBN	5	V_{OUTB}

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage V_S+ and GND . . . . +12.6V
Maximum Output Current. . . . . ±60mA
Storage Temperature Range . . . . -65°C to +150°C
Operating Junction Temperature . . . . +150°C

Recommended Operating Temperature . . . . -40°C to 85°C
V_IN, V_INB, V_REF. . . . . V_EE+0.8V (MIN) to V_CC-0.8V (MAX)
V_IN–V_INB . . . . ±5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications   V_CC = +5V, V_EE = -5V, T_A = 25°C, V_IN = 0V, R_L = 200, unless otherwise specified.

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_SUPPLY	Supply Operating Range (V_CC–V_EE)	±3.0	±5.0	±6.3	V
I_S	Power Supply Current (No Load)		11	14	mA
V_OS	Input Referred Offset Voltage	-25	10	40	mV
I_IN	Input Bias Current (V_IN, V_INB, V_REF)	-20	6	20	μA
Z_IN	Differential Input Impedance		400		kΩ
V_DIFF	Differential Input Range	±2.0	±2.3		V
A_VOL	Open Loop Voltage Gain		75		dB
V_OUT(200)	Output Voltage Swing (200Ω load, V_OUT to V_OUTB)	±3.4	±3.6		V
V_OUT(100)	Output Voltage Swing (100Ω Load, V_OUT to V_OUTB)	±2.9	±3.1		V
V_N	Input Referred Voltage Noise		36		nV/√Hz
V_REFOS	Output Offset Relative to V_REF	-60	-25	+60	mV
PSRR	Power Supply Rejection Ratio	60	70		dB
I_OUT(min)	Minimum Output Current	50	60		mA
R_OUT	(V_OUT = V_OUTB = 0V) Output Impedance		0.1		Ω

AC Electrical Specifications   V_CC = +5V, V_EE = -5V, T_A = 25°C, V_IN = 0V, R_LOAD = 200, unless otherwise specified

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
BW(-3dB)	-3dB Bandwidth (@ gain of 2)		150		MHz
SR	Differential Slewrate		800		V/μs
Tstl	Settling Time to 1%		15		ns
GBW	Gain Bandwidth Product		400		MHz
V_REFBW(-3dB)	V_REF -3dB Bandwidth		130		MHz
V_REFSR	V_REF Slewrate		100		V/μs
THDf1	Distortion at 100kHz (Note 1)		-75		dB
dP	Differential Phase @ 3.58MHz		0.16		°
dG	Differential Gain @ 3.58MHz		0.24		%

NOTE:

1. Distortion measurement quoted for V_OUT–V_OUTB = 12V pk-pk, R_LOAD = 200Ω, V_GAIN = 8

Pin Descriptions

EL2141	PIN NAME	FUNCTION
2	V_{IN}	Non-inverting Input
1	FBP	Non-inverting Feedback Input. Resistor R1 must be Connected from this Pin to V_{OUT}.
4	FBN	Inverting Feedback Input. Resistor R3 must be Connected from this pin to V_{OUTB}.
3	V_{REF}	Output Common-mode Control. The Common-mode Voltage of V_{OUT} and V_{OUTB} will Follow the Voltage on this Pin. Note that on the EL2141, this pin is also the V_{INB} pin.
5	V_{OUTB}	Inverting Output
6	V_{CC}	Positive Supply
7	V_{EE}	Negative Supply
8	V_{OUT}	Non-inverting Output

Typical Performance Curves
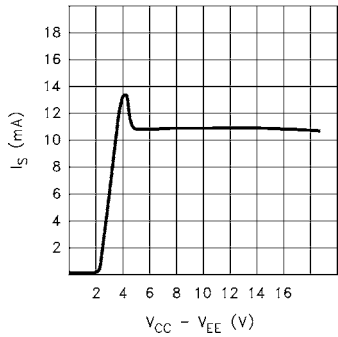
FIGURE 1. I_S vs SUPPLY VOLTAGE
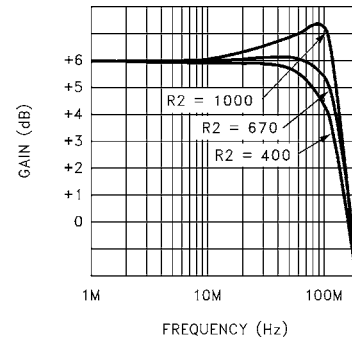
FIGURE 2. FREQUENCY RESPONSE vs RESISTOR R2
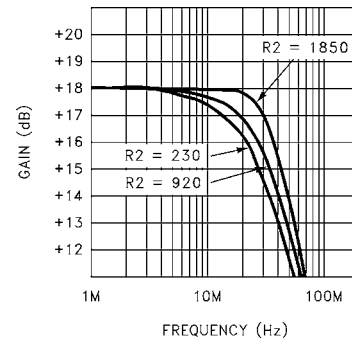(GAIN = 2)
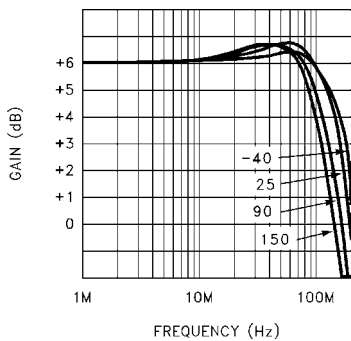
FIGURE 3. FREQUENCY RESPONSE vs TEMPERATURE

FIGURE 4. FREQUENCY RESPONSE vs RESISTOR R2
(GAIN = 8)

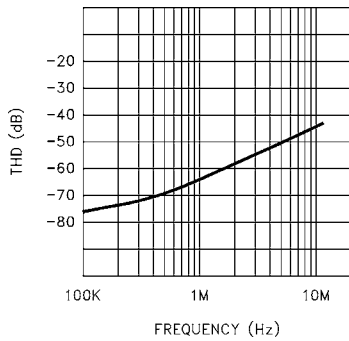*intersil*

Typical Performance Curves (Continued)

FIGURE 5. DISTORTION vs FREQUENCY
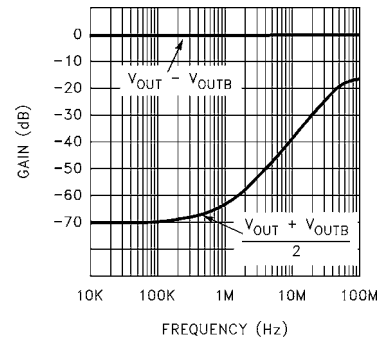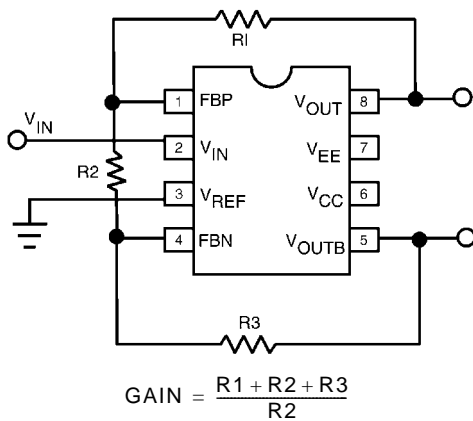**(GAIN = 6, R_{LOAD} = 200Ω) V_{IN} = 2V_{PK-PK}**

FIGURE 6. OUTPUT SIGNAL AND COMMON MODE SIGNAL
vs FREQUENCY

Applications Information

$$GAIN = \frac{R1 + R2 + R3}{R2}$$

Choice of Feedback Resistor

There is little to be gained from choosing resistor R2 values below 400Ω and, in fact, it would only result in increased power dissipation and signal distortion. Above 400Ω, the bandwidth response will develop some peaking (for a gain of two), but substantially higher resistor R2 values may be used for higher voltage gains, such as up to 2kΩ at a gain of eight before peaking will develop. R1 and R3 are selected as needed to set the voltage gain, and while R1 = R3 is suggested, the gain equation above holds for any values (see distortion for further suggestions).

Capacitance Considerations

As with many high bandwidth amplifiers, the EL2141 prefers not to drive highly capacitive loads. It is best if the capacitance on V_{OUT} and V_{OUTB} is kept below 10pF if the user does not want gain peaking to develop.

In addition, on the EL2141, the two feedback nodes FBP and FBN should be laid out so as to minimize stray capacitance, else an additional pole will potentially develop in the response with possible gain peaking.

The amount of capacitance tolerated on any of these nodes in an actual application will also be dependent on the gain setting and the resistor values in the feedback network.

Distortion Considerations

The harmonics that these amplifiers will potentially produce are the 2nd, 3rd, 5th, and 6th. Their amplitude is application dependent. All other harmonics should be negligible by comparison. Each should be considered separately:

H2 The second harmonic arises from the input stage, and the lower the applied differential signal amplitude, the lower the magnitude of the second harmonic. For practical considerations of required output signal and input noise levels, the user will end up choosing a circuit gain. Referring to Figure 1, it is best if the voltage at the negative feedback node tracks the V_{REF} node, and the voltage at the positive feedback node tracks the V_{IN} node respectively. This would theoretically require that R1 + R2 = R3, although the lowest distortion is found at about R3 = R1 + (0.7*R2). With this arrangement, the second harmonic should be suppressed well below the value of the third harmonic.

H3 The third harmonic should be the dominant harmonic and is primarily affected by output load current which, of course, is unavoidable. However, this should encourage the user not to waste current in the gain setting resistors, and to use values that consume only a small proportion of the load current, so long as peaking does not occur. The more load current, the worse the distortion, but depending on the frequency, it may be possible to reduce the amplifier gain so that there is more internal gain left to cancel out any distortion.

H5 The fifth harmonic should always be below the third, and will not become significant until heavy load currents are drawn. Generally, it should respond to the same efforts applied to reducing the third harmonic.

H6 The sixth harmonic should not be a problem and is the result of poor power supply decoupling. While 100nF chip capacitors may be sufficient for some applications, it would be insufficient for driving full signal swings into a twisted pair line at 100kHz. Under these conditions, the addition of 4.7μF tantalum capacitors would cure the problem.
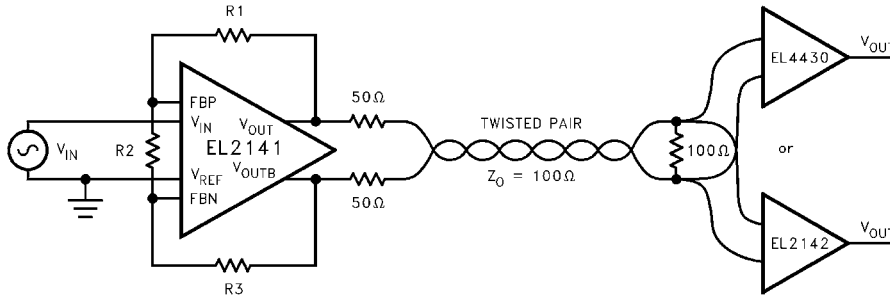
Typical Applications Circuits
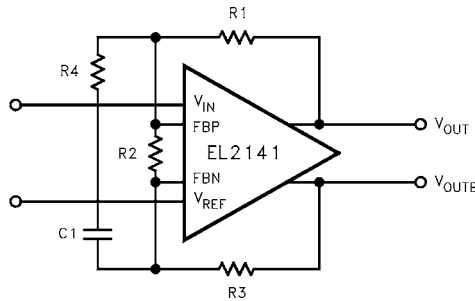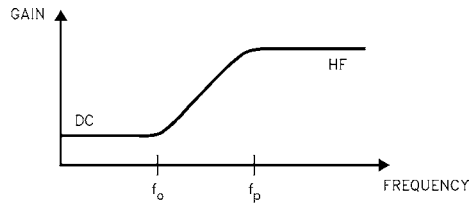

FIGURE 7. TYPICAL TWISTED PAIR APPLICATION

FIGURE 8. DIFFERENTIAL LINE DRIVER WITH EQUALIZATION

$$DCGain = \frac{R1 + R2 + R3}{R2}(See Figure9)$$

$$(HF)Gain = \frac{R1 + (R2/R4) + R3}{(R2/R4)}(See Figure9)$$

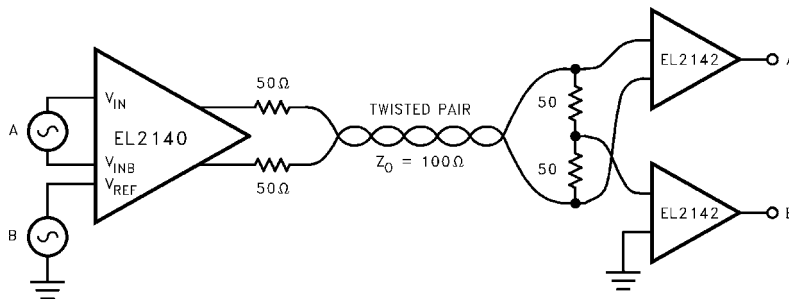$$where F_O = \frac{1}{2\pi C_1 R_2}$$

$$and F_P = \frac{1}{2\pi C_1 R_4}$$

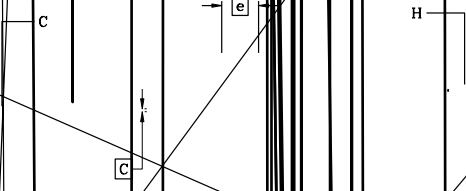**FIGURE 9. DUAL SIGNAL TRANSMISSION CIRCUIT**

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C — e — H

		SO16 (0.150")	SO16 (0.300")	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	
		0.068	0.068	0.104	0.104		0.104	
M		0.006	0.006	0.007	0.007		0.007	
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
		0.017	0.017	0.017	0.017		0.017	+
		0.009	0.009	0.011	0.011		0.011	
D		0.341	0.390	0.406	0.504		0.704	− − 0.009
E		0.236	0.236	0.406	0.406		0.406	
E1		0.154		0.295	0.295		0.295	
		0.050	0.050	0.050	0.050		0.050	Basic
		0.025	0.025	0.030	0.030		0.030	− 0.009
		0.041		0.056	0.056		0.056	Basic
L		0.013	0.013	0.020	0.020	0.020	0.020	Reference
		14	16	16	20		28	Reference

SMALL OUTLINE (SOL PACKAGE) FAMILY

Units: Inches

Notes:
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.

(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

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