MAX40023/MAX40024 Low-Noise, Low-Power, Low-Bias-Current Amplifiers

General Description

The MAX40023/MAX40024 are single and dual amplifiers optimized for power-sensitive applications that require low noise and very low-leakage input current (bias current).

The MAX40023/MAX40024 amplifiers consume less than 17μA (typ) of supply current per channel, but also feature incredibly low noise as low as 32nV/√Hz. The input bias current is <1pA at room temperature.

These amplifiers are available in a space-saving, 6-bump wafer-level package (WLP) with a 0.4mm bump pitch (single), 9-bump WLP (dual), 6-pin SOT23 (single), and 10-pin TDFN (dual). They are designed for use as a sensor interface in wearable medical and industrial sensor applications.

The MAX40023/MAX40024 amplifiers operate from a 1.6V to 3.6V power supply voltage and are specified over the -40°C to +125°C operating temperature range.

Applications

- Wearable Medical
- Industrial Sensors
- Battery-Powered Devices

Benefits and Features

- Ultra-Low <1pA Input Bias Current
- Low 17μA Quiescent Current (per Op Amp)
- Low 32nV/√Hz Input-Voltage Noise
- Internal EMI Rejection
- Supply Voltage Range: 1.6V to 3.6V
- Power-Saving Shutdown Mode
- Available in 6-Bump WLP and 6-Pin SOT23 (Single) and 9-Bump WLP and 10-Pin TDFN (Dual)

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram

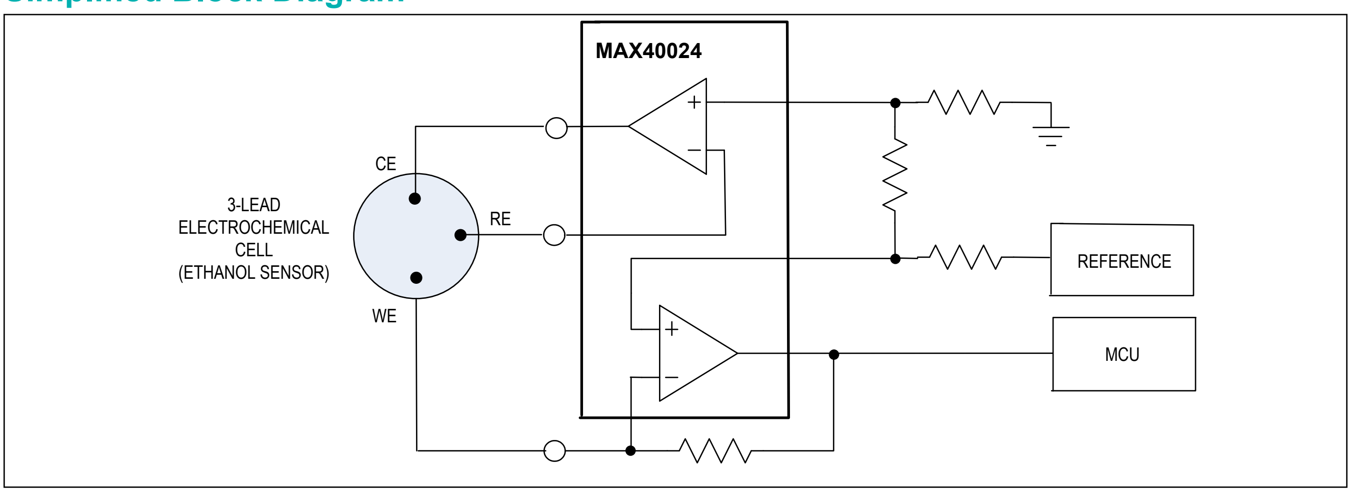


TABLE OF CONTENTS

Absolute Maximum Ratings

V_{DD} to GND.. -0.3V to +4V
IN+ to IN- .... -0.3V to V_{DD} + 0.3V
OUT to GND .... -0.3V to V_{DD} + 0.3V
IN+, IN- to GND .... -0.3V to V_{DD} + 0.3V
Continuous Current into Any Input/Output Pin 10mA
Output Short-Circuit Duration to Either V_{DD} or GND ..Continuous
Operating Temperature Range ....-40°C to 125°C
Junction Temperature .... +150°C
Storage Temperature Range ....-40°C to +150°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

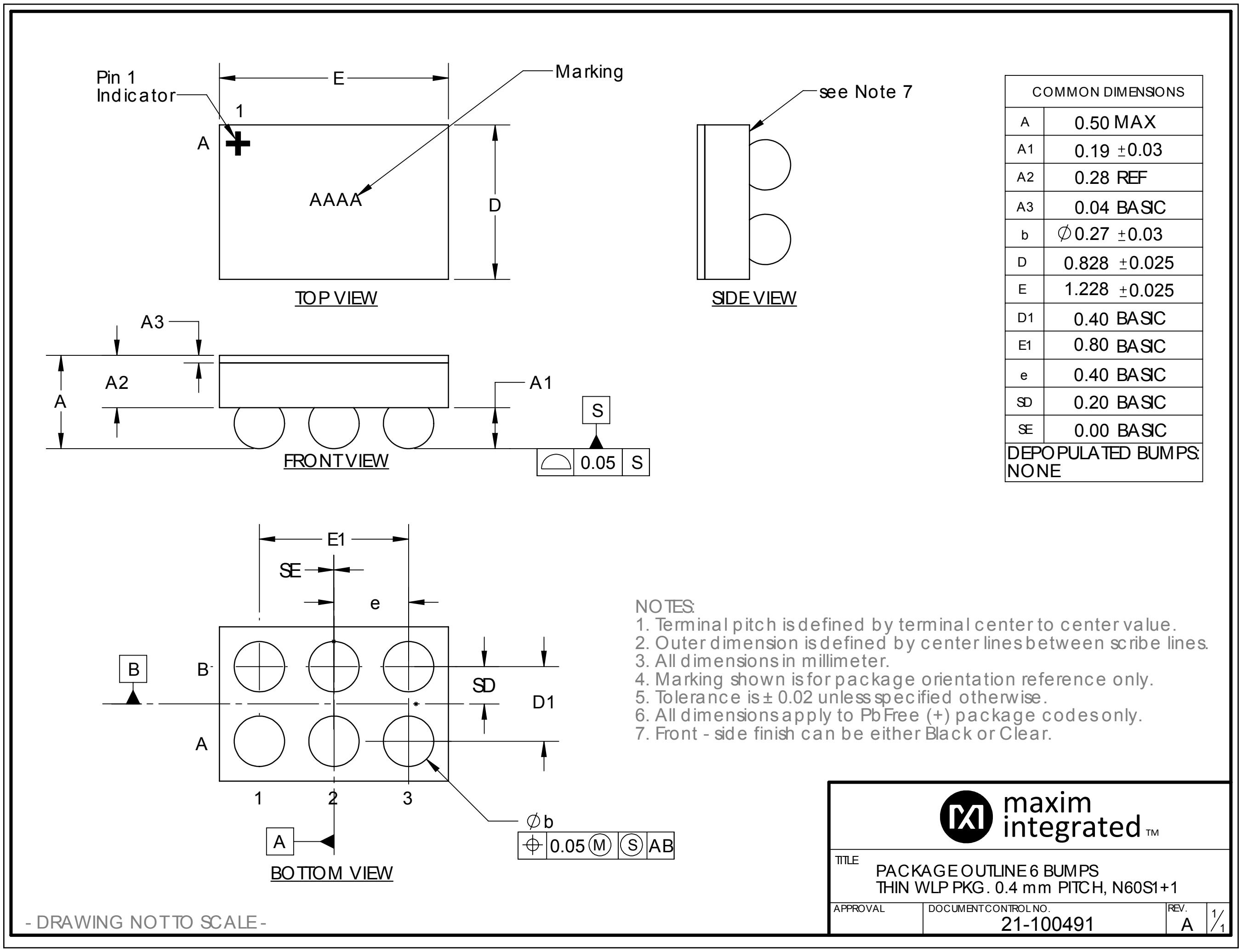
Package Information

6 WLP

Package Code	N60S1+1
Outline Number	21-100491
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	N/A
Junction to Case (θ_{JC})	N/A
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	95.15°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

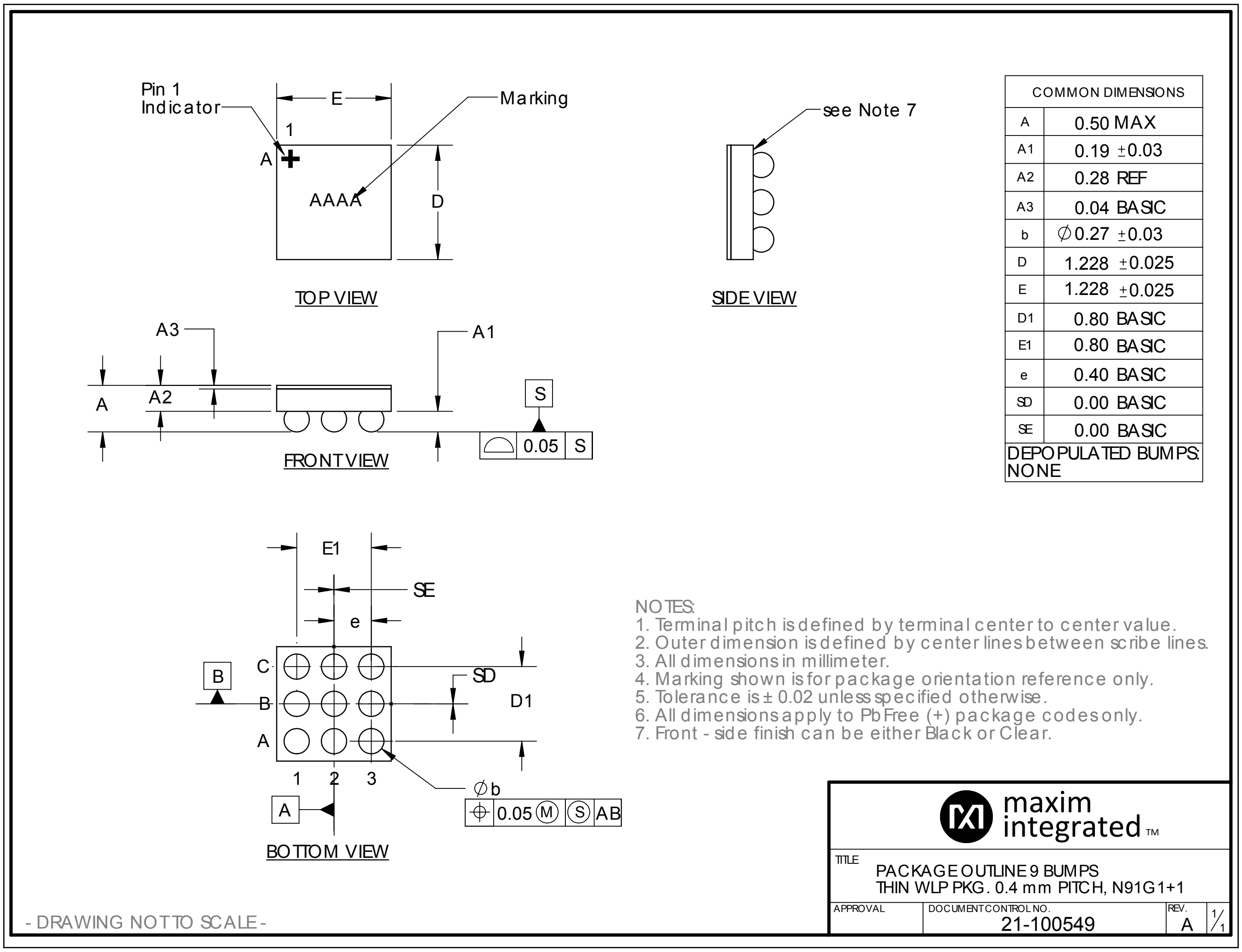


9 WLP

Package Code	N91G1+1
Outline Number	21-100549
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	N/A
Junction to Case (θ_{JC})	N/A
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	83.98°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a *four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.*

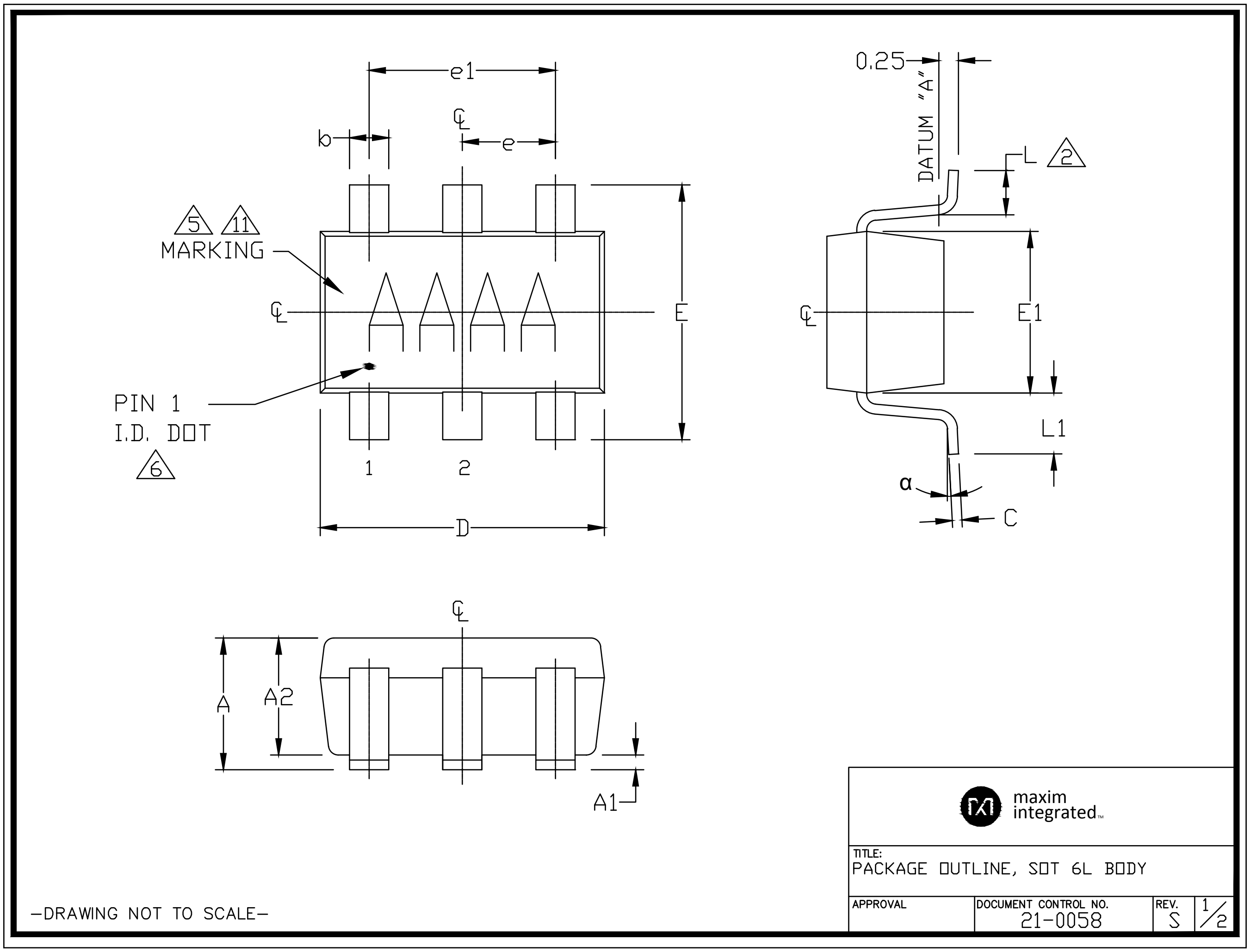


6 SOT23

Package Code	U6+1C
Outline Number	21-0058
Land Pattern Number	90-0175
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	N/A
Junction to Case (θ_{JC})	N/A
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	230°C/W
Junction to Case (θ_{JC})	76°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different *suffix character, but the drawing pertains to the package regardless of RoHS status.*

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHER SPECIFIED.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT.
6. PIN 1 I.D. DOT IS Ø0.3mm MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1mm.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1		0.60 REF.	
e1		1.90 BSC.	
e		0.95 BSC.	
α	0°	2.5°	10°

PKG CODES:
U6-1, U6-1A, U6-2, U6-4, U6-4A, U6-5, U6-5A, U6CN-2, U6F-6, U6SN-1, U6-8, U6-9, U6-1C

** U6-9 TO BE USED FOR RF50 PARTS ONLY WHICH USES A Si SPACER
** U6-5 USES LOW STRESS MOLD COMPOUND

-DRAWING NOT TO SCALE-

maxim integrated

TITLE: PACKAGE OUTLINE, SOT 6L BODY

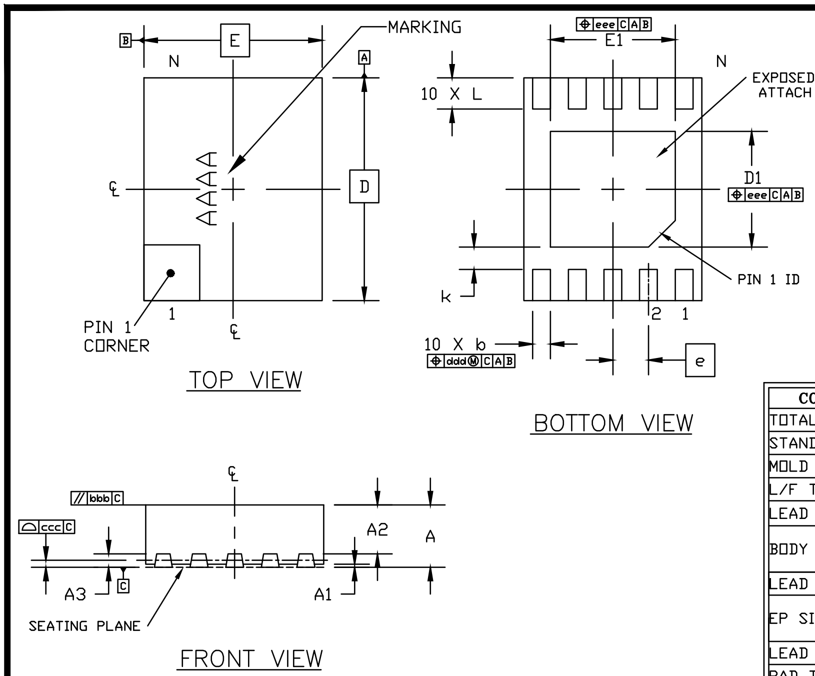
APPROVAL | DOCUMENT CONTROL NO. 21-0058 | REV. S | 2/2

10 TDFN

Package Code	T102A2+2C
Outline Number	21-100013
Land Pattern Number	90-100007
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	N/A
Junction to Case (θ_{JC})	N/A
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	102°C/W
Junction to Case (θ_{JC})	2.9°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a *four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.*



COMMON DIMENSION		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	Y	D	2.5 BSC		
	X	E	2 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	Y	D1	1.2	1.3	1.4
	X	E1	1.3	1.4	1.5
LEAD LENGTH		L	0.3	0.35	0.4
PAD TO LEAD		k	0.25 MIN		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. ALL DIMENSIONS APPLY TO PbFREE (+) PKG. CODE.
9. PACKAGE CODE: T102A2+1 T102A2+1C T102A2+2C

-DRAWING NOT TO SCALE-

maxim integrated

TITLE: PACKAGE OUTLINE, 10L, TDFN, EXPOSED PAD, 2.5X2.0x0.75 mm

APPROVAL | DOCUMENT CONTROL NO. 21-100013 | REV. C | 1/1

Electrical Characteristics

(V_{DD} = 1.8V, V_{CM} = V_{DD}/2, R_{LOAD} = 10kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40° to +125°C. Typical values are at +25°C, unless otherwise noted. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC SPECIFICATIONS							
Input Offset Voltage	V_{OS}	T_A = +25°C			100	400	µV
Input Offset Drift	TCV_{OS}				1	4	µV/°C
Input Bias Current	I_B	(*Note 2*)	0°C ≤ T_A ≤ +50°C		0.1	5	pA
			-40°C ≤ T_A ≤ +85°C			30	
			-40°C ≤ T_A ≤ +125°C			550	
Input Offset Current	I_{OS}				0.5		pA

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{CM} = V_{DD}/2, R_{LOAD} = 10kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40° to +125°C. Typical values are at +25°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Resistance	R_{IN}	0°C ≤ T_A ≤ +50°C			15,000		GΩ
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR		-0.1		V_{DD} + 0.1V	V
Common-Mode Rejection Ratio	CMRR	-40°C ≤ T_A ≤ +125°C	-0.1V ≤ V_{CM} ≤ V_{DD} + 0.1V	75	100		dB
			0V ≤ V_{CM} ≤ V_{DD} + 0.1V	75	100		
		0°C ≤ T_A ≤ +50°C	0V ≤ V_{CM} ≤ V_{DD} + 0.1V	75	100		
Power Supply Rejection Ratio	PSRR	V_{IN+} = V_{IN-} = 0V		84	100		dB
Open-Loop Gain	A_{OL}	150mV - GND ≤ V_{OUT} ≤ V_{DD} - 150mV, R_{LOAD} = 10kΩ to V_{DD}/2		90	110		dB
Output Voltage Swing High	V_{OH}	V_{DD} - V_{OUT}	R_{LOAD} = 10kΩ to V_{DD}/2			10	mV
Output Voltage Swing Low	V_{OL}	V_{OUT} - GND	R_{LOAD} = 10kΩ to V_{DD}/2			10	mV
Short-Circuit Current	I_{SC}				10		mA
AC SPECIFICATIONS							
Gain Bandwidth Product	GBW				80		kHz
Slew Rate	SR				0.02		V/µs
Input Voltage-Noise Density	V_N	f = 1kHz			32		nV/√Hz
Input Voltage Noise		0.1Hz to 10Hz			1.5		$µV_{P-P}$
Input Current-Noise Density	I_N	f = 1kHz			10		fA/√Hz
EMI Rejection Ratio	EMIRR	V_{RFpeak} = 100mV$_P$, f = 400MHz, 900MHz, both IN+ and IN-			>70		dB
		V_{RFpeak} = 100mV$_P$, f = 1800MHz, 2400MHz, both IN+ and IN-			>110		
Phase Margin	PM	C_{LOAD} = 20pF			60		degrees
Capacitive Loading Stability					50		pF
Crosstalk		Buffer with G = 1V/V, IN1+ = 100mV$_{P-P}$, f = 100Hz, test V_{OUT2} (MAX40024 only)			90		dB
POWER SUPPLY							
Supply Voltage	V_{DD}	Guaranteed by PSRR, -40°C < T_A < +125°C		1.6		3.6	V
Supply Current	I_{DD}	0°C ≤ T_A ≤ +50°C			17	20	µA
		-40°C ≤ T_A ≤ +125°C				25	
Power-Up Time	t_{ON}	V_{DD} = 0 to 1.8V step, A_V = 1V/V	Measured at 90% of nominal final value		80		µs

Electrical Characteristics (continued)

(V_{DD} = 1.8V, V_{CM} = V_{DD}/2, R_{LOAD} = 10kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40° to +125°C. Typical values are at +25°C, unless otherwise noted. (Note 1))

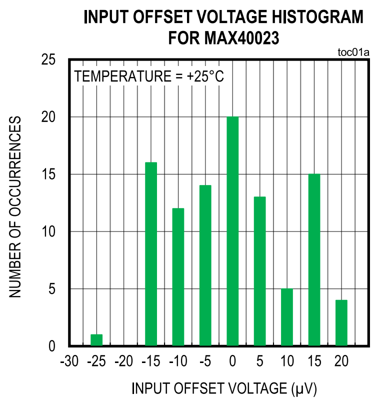
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Supply Current	$I_{\overline{SHDN}}$	T_A = +25°C			55	100	nA
		-40°C ≤ T_A ≤ +125°C			55	400	
Turn-On Time from Shutdown	t_{ONSD}	V_{DD} = 1.8V, $V_{\overline{SHDN}}$ = 0 to 1.8V step, A_V = 1V/V	Measured at 90% of final value		60		µs
LOGIC INPUT DC CHARACTERISTICS							
Input Low Level	V_{IL}	Active level				0.3 x V_{DD}	V
Input High Level	V_{IH}			0.7 x V_{DD}			V
Input Leakage Current	I_L					100	nA

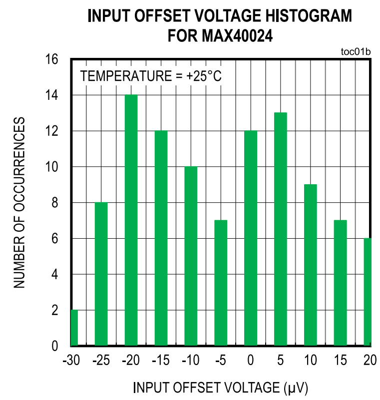
Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

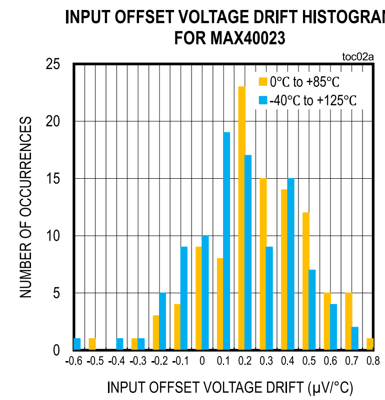
Note 2: Not production tested, guaranteed by design and bench characterization.

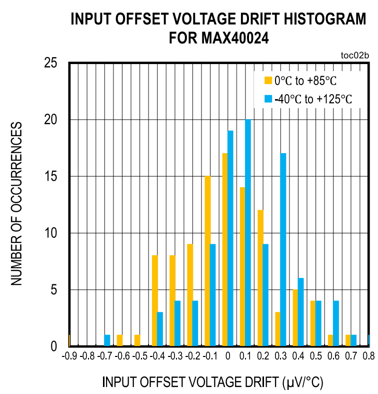
Typical Operating Characteristics

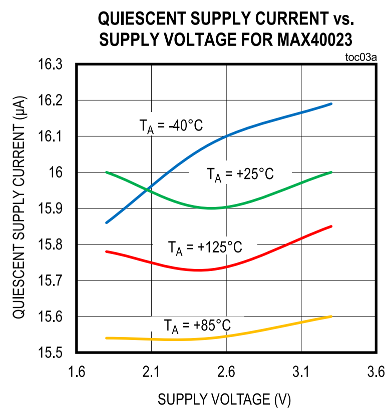
(V_{DD} = +1.8V, GND = 0V, V_{IN-} = V_{IN+} = V_{DD}/2 = 0.9V; $V_{\overline{SHDN}}$ = V_{DD}, R_{LOAD} = 10kΩ to V_{DD}/2, T_A = +25°C)

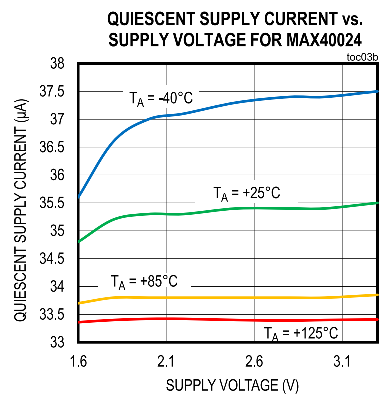


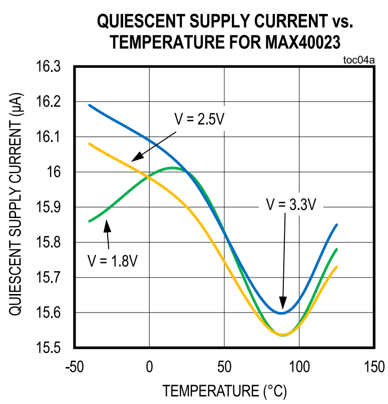


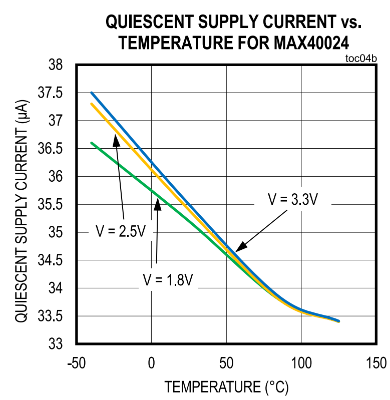


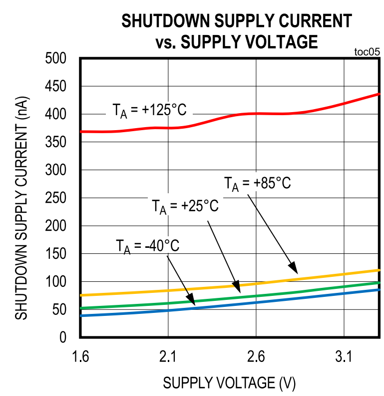








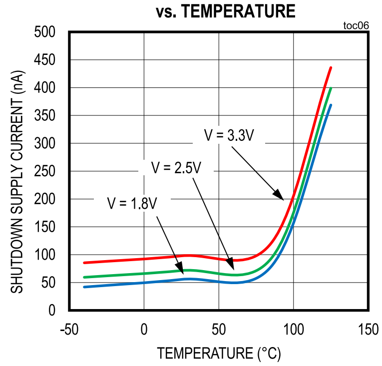




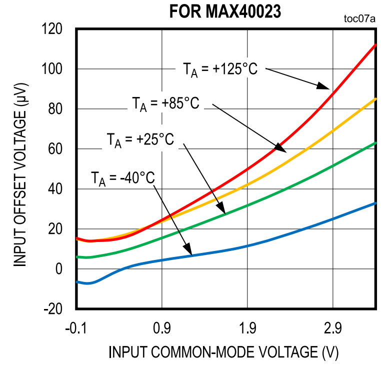
Typical Operating Characteristics (continued)

(V_{DD} = +1.8V, GND = 0V, V_{IN-} = V_{IN+} = V_{DD}/2 = 0.9V; $V_{\overline{SHDN}}$ = V_{DD}, R_{LOAD} = 10kΩ to V_{DD}/2, T_A = +25°C)

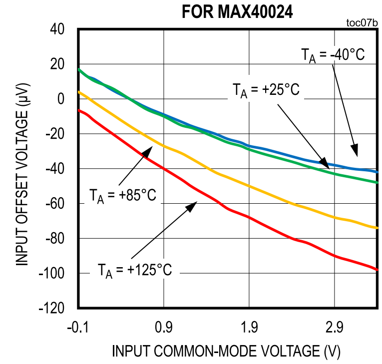
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



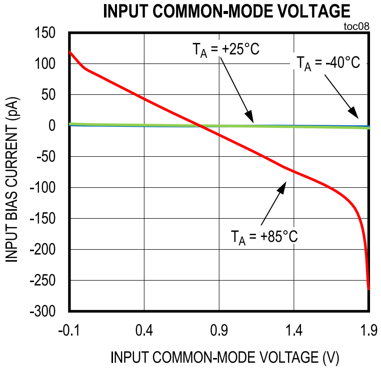
INPUT OFFSET VOLTAGE vs. INPUT COMMON-MODE VOLTAGE FOR MAX40023



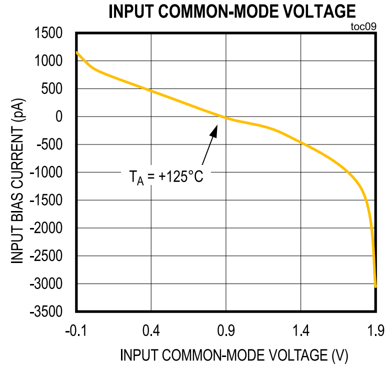
INPUT OFFSET VOLTAGE vs. INPUT COMMON-MODE VOLTAGE FOR MAX40024



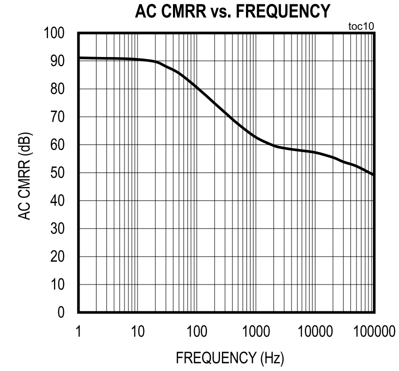
INPUT BIAS CURRENT vs. INPUT COMMON-MODE VOLTAGE



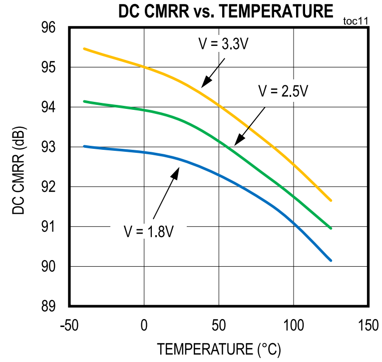
INPUT BIAS CURRENT vs. INPUT COMMON-MODE VOLTAGE



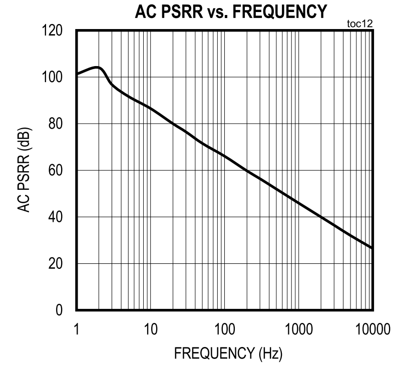
AC CMRR vs. FREQUENCY



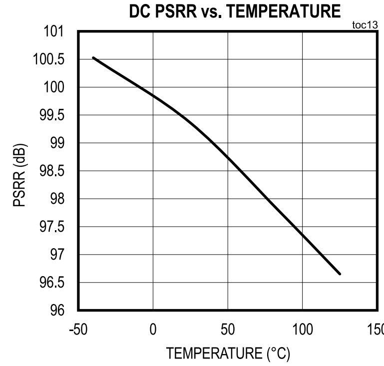
DC CMRR vs. TEMPERATURE



AC PSRR vs. FREQUENCY



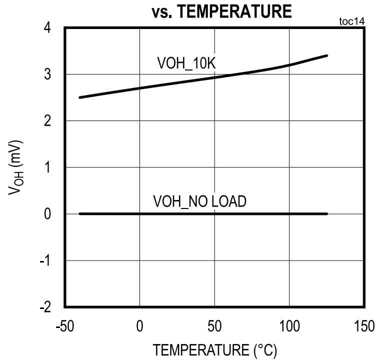
DC PSRR vs. TEMPERATURE



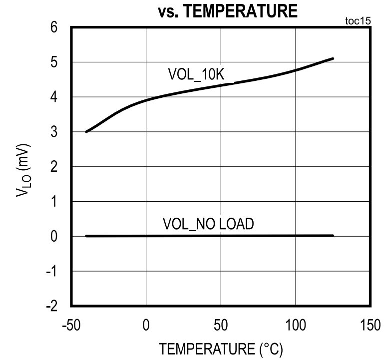
Typical Operating Characteristics (continued)

(V_{DD} = +1.8V, GND = 0V, V_{IN-} = V_{IN+} = $V_{DD}/2$ = 0.9V; $V_{\overline{SHDN}}$ = V_{DD}, R_{LOAD} = 10kΩ to $V_{DD}/2$, T_A = +25°C)

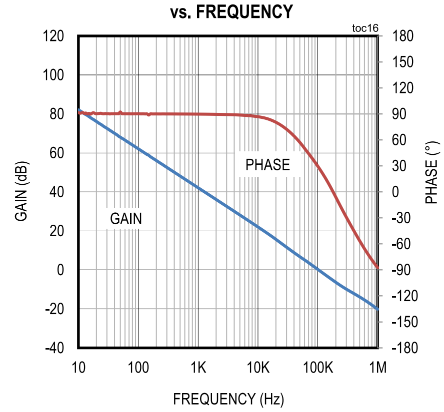
OUTPUT VOLTAGE SWING HIGH vs. TEMPERATURE



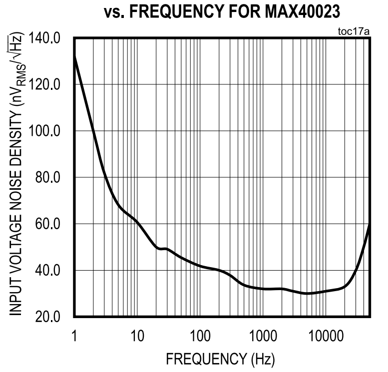
OUTPUT VOLTAGE SWING LOW vs. TEMPERATURE



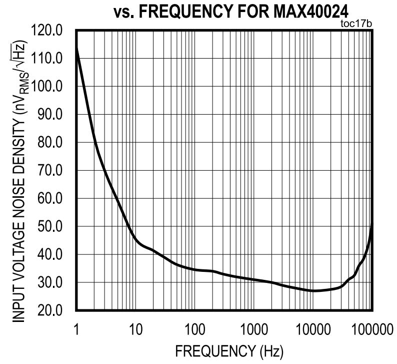
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



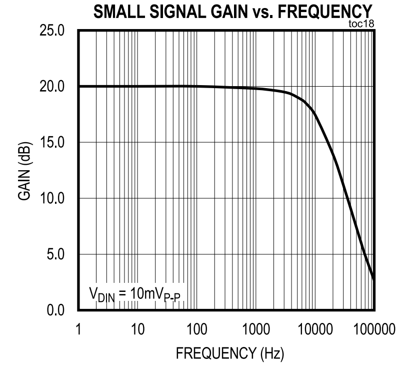
VOLTAGE NOISE DENSITY vs. FREQUENCY FOR MAX40023



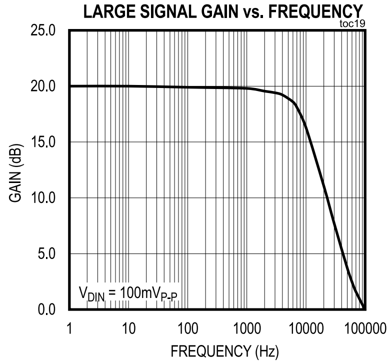
VOLTAGE NOISE DENSITY vs. FREQUENCY FOR MAX40024



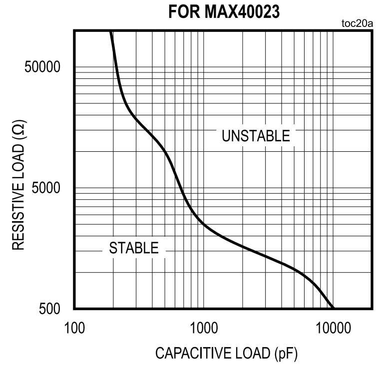
SMALL SIGNAL GAIN vs. FREQUENCY



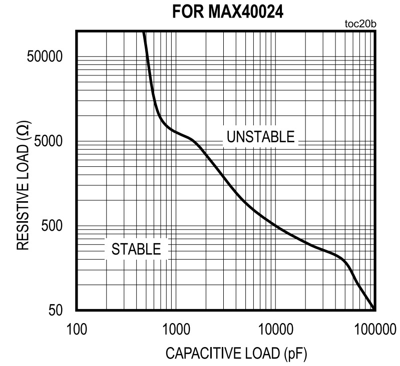
LARGE SIGNAL GAIN vs. FREQUENCY



STABILITY vs. CAPACITIVE LOAD AND RESISTIVE LOAD FOR MAX40023



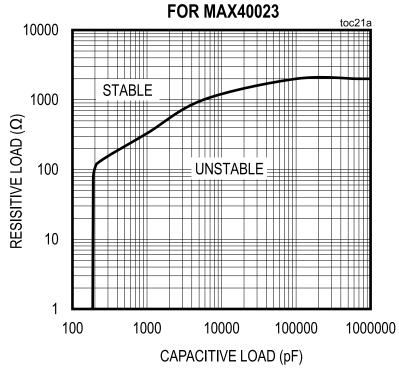
STABILITY vs. CAPACITIVE LOAD AND RESISTIVE LOAD FOR MAX40024



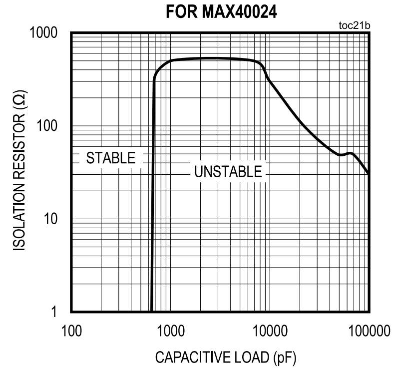
Typical Operating Characteristics (continued)

(V_{DD} = +1.8V, GND = 0V, V_{IN-} = V_{IN+} = V_{DD}/2 = 0.9V; $V_{\overline{SHDN}}$ = V_{DD}, R_{LOAD} = 10kΩ to V_{DD}/2, T_A = +25°C)

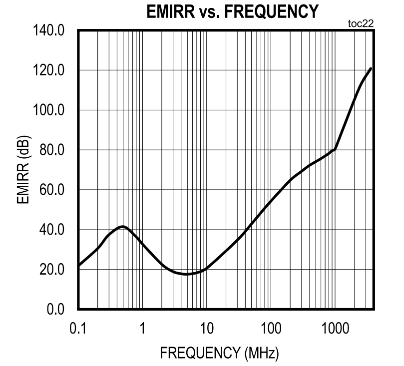
STABILITY vs. CAPACITIVE LOAD AND ISOLATION RESISTOR FOR MAX40023



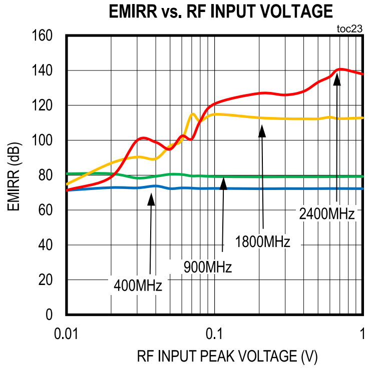
STABILITY vs. CAPACITIVE LOAD AND ISOLATION RESISTOR FOR MAX40024



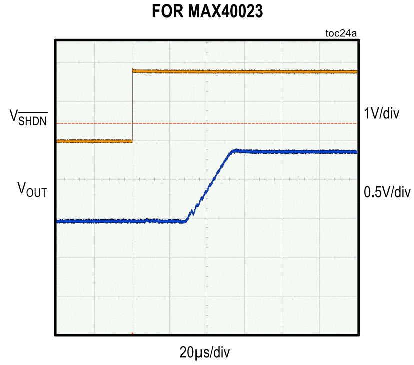
EMIRR vs. FREQUENCY



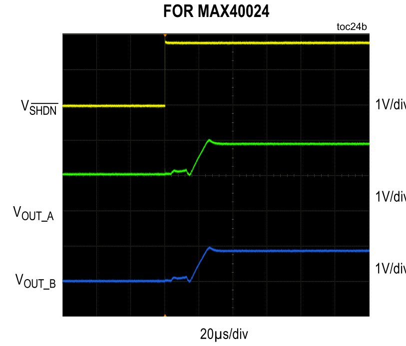
EMIRR vs. RF INPUT VOLTAGE



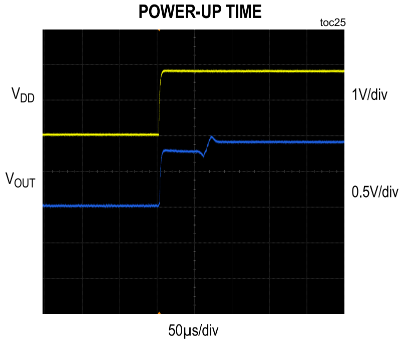
SHUTDOWN ENABLE RESPONSE FOR MAX40023



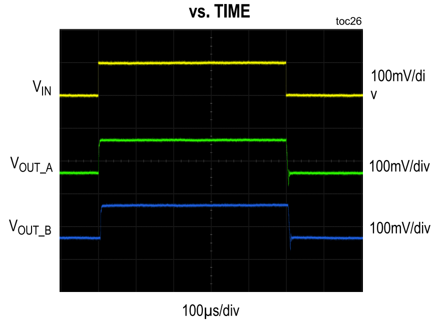
SHUTDOWN ENABLE RESPONSE FOR MAX40024



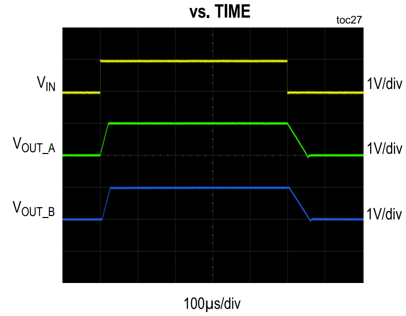
POWER-UP TIME



SMALL SIGNAL STEP RESPONSE vs. TIME

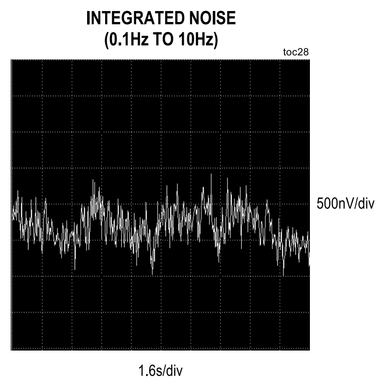


LARGE SIGNAL STEP RESPONSE vs. TIME



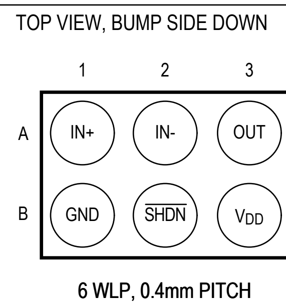
Typical Operating Characteristics (continued)

(V_{DD} = +1.8V, GND = 0V, V_{IN-} = V_{IN+} = $V_{DD}/2$ = 0.9V; $V_{\overline{SHDN}}$ = V_{DD}, R_{LOAD} = 10kΩ to $V_{DD}/2$, T_A = +25°C)

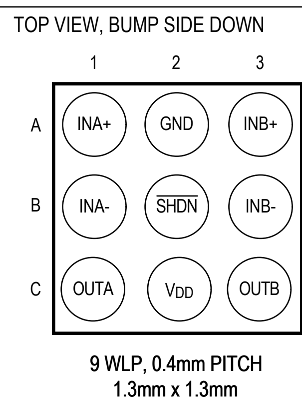


Pin Configurations

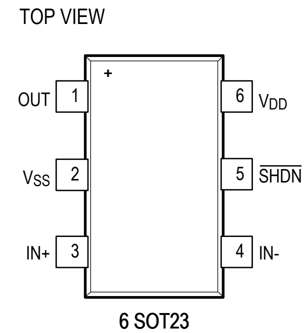
WLP Single



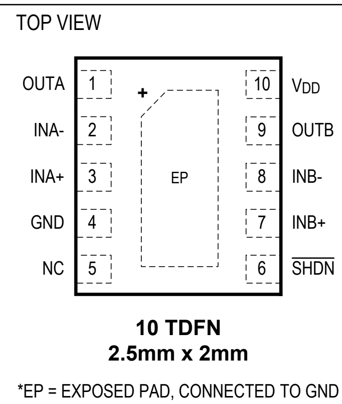
WLP Dual



SOT23 Single



TDFN Dual



Pin Description

PIN				NAME	FUNCTION
WLP Single	WLP Dual	SOT23 Single	TDFN Dual		
A1	A1, A3	3	3, 7	IN+	Noninverting Input
B1	A2	2	4	GND	Ground
A2	B1, B3	4	2, 8	IN-	Inverting Input
B3	C2	6	10	V_{DD}	Positive Supply
A3	C1, C3	1	1, 9	OUT	Output
B2	B2	5	6	$\overline{SHDN}$	Shutdown (active low)
—	—	—	5	NC	Do Not Connect
—	—	—	EP	EP	Exposed Pad. Connect to GND.

Detailed Description

The MAX40023/MAX40024 feature a combination of low input current and voltage noise, rail-to-rail input and output voltage swing, low supply voltage, and low-power operation. High-impedance inputs on the MAX40023/MAX40024 make them ideal for use as transimpedance amplifiers and high-impedance sensor interface front-ends in medical and industrial applications. The MAX40023/MAX40024 can interface with small signals from either current sources or high-output impedance voltage sources. Applications include photodiode interfaces, pH sensors, capacitive pressure sensors, chemical analysis equipment, smoke detectors, and humidity sensors.

Low quiescent supply current and low power supply make the MAX40023/MAX40024 compatible with portable systems and applications that operate under tight power budgets. The MAX40023/MAX40024 achieve rail-to-rail performance at the input through the use of a low-noise charge pump. The rail-to-rail input maximizes the amplifier input dynamic range when it is operating at its minimum supply voltage of 1.6V. This also ensures a glitch-free, common-mode input-voltage range extending from the negative supply rail up to the positive supply rail, eliminating crossover distortion common to traditional n-channel/p-channel CMOS pair inputs. The charge pump requires no external components, and in most applications it is entirely transparent to the user. The operating frequency is well beyond the unity-gain frequency of the amplifier, avoiding aliasing or other signal integrity issues in sensitive applications.

Shutdown Operation

The device features an active-low shutdown mode that reduces the quiescent current to a typical value of 55nA. In shutdown mode, the inputs and output are high impedance. This allows multiple devices to be multiplexed onto a single line without the use of external buffers. Pull $\overline{SHDN}$ high for normal operation. The shutdown high (V_{IH}) and low (V_{IL}) threshold voltages are designed for ease of integration with digital controls like microcontroller outputs. See the *Typical Operating Characteristics* for output voltage response to a shutdown disable signal.

Low-Current, Low-Noise Input Stage

The MAX40023/MAX40024 feature a MOS-input stage with only 0.1pA (typ) of input bias current and a low 32nV/$\sqrt{Hz}$ (typ) input voltage-noise density. The low-frequency input voltage noise is a low 1.5μV_{P-P} (typ). The MAX40023/MAX40024 feature rail-to-rail CMOS inputs; the input stage accepts a wide common-mode range, extending from (GND - 0.1V) to (V_{CC} + 0.1V). The low input offset voltage, CMOS inputs, and absence of 1/f noise allow for optimization of sensor interfaces, particularly for sensors that operate with low voltage and at a low frequency.

Applications Information

Overview

The MAX40023/MAX40024 low-power, low-noise, precision op amps are designed for applications that interface with sensors like the ones found in portable medical devices, such as ECGs and blood glucose meters, as well as industrial equipment.

Power-Up Settling Time and Shutdown Enable Response

The MAX40023/MAX40024 typically require 80µs to power up. During this startup time, the output is indeterminate. The application circuit should allow for this initial delay. See the *Typical Operating Characteristics* for the Power-Up Time curve. The MAX40023/MAX40024 typically requires 60µs to respond from shutdown mode; the application circuit should allow for this delay.

Power Supplies

The MAX40023/MAX40024 operate either with a single supply from +1.6V to +3.6V with respect to ground or with dual supplies from ±0.8V to ±1.8V. Bypass both supplies with a bypass capacitor to ground when used with dual supplies; bypass V_{DD} with a bypass capacitor to ground when used with a single supply.

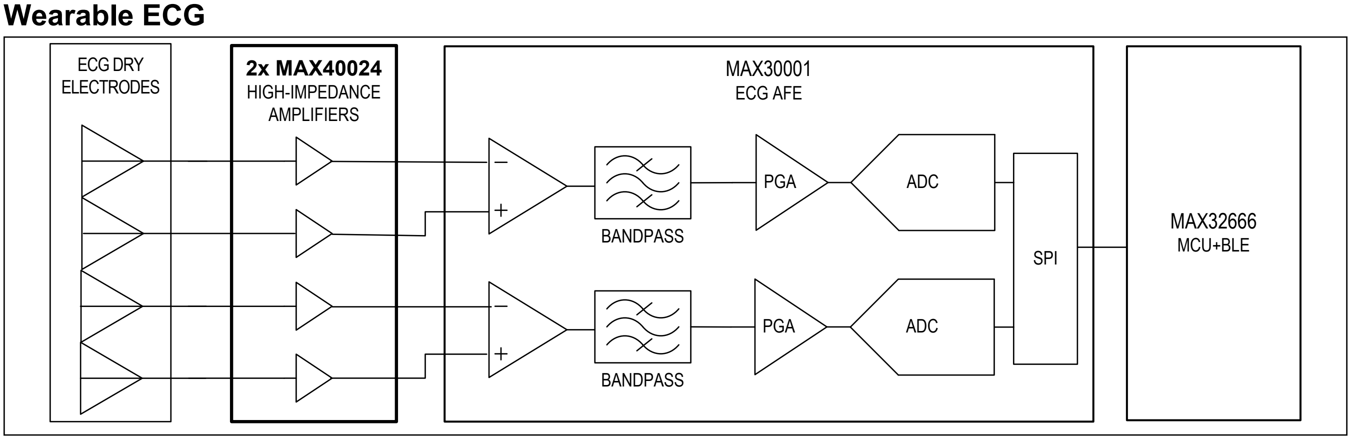
Layout Techniques

A good layout is critical to obtaining high performance, especially when interfacing with high-impedance sensors. Use shielding techniques to guard against parasitic leakage paths. For transimpedance applications, for example, surround the inverting input and the traces connecting to it with a buffered version of its own voltage. A convenient source of this voltage is the noninverting input pin.

Take care to also decrease the amount of stray capacitance at the op amp's inputs to improve stability. To achieve this, minimize trace lengths and resistor leads by placing external components as close as possible to the package. If the sensor is inherently capacitive, or is connected to the amplifier through a long cable, use a low-value feedback capacitor to control high-frequency gain and peaking to stabilize the feedback loop.

Typical Application Circuits

Wearable ECG



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING
MAX40023ANT+	-40°C to +125°C	6 WLP	+BH
MAX40023AUT+T*	-40°C to +125°C	6 SOT23	ACWH+
MAX40024ANL+	-40°C to +125°C	9 WLP	+AA
MAX40024ATB+T*	-40°C to +125°C	10 TDFN	+AZP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/21	Initial release	—