Product/Process Change Notification

N° 2021-080-A

Dear customer,

please find attached our Infineon Technologies AG PCN:

Datasheet update for products TLE9180x and TLE9183QK

Important information for your attention:

- Please respond to this PCN by indicating your decision on the approval form, sign it and return to your sales partner before 2021-08-02.
- Infineon aligns with the widely-recognized JEDEC STANDARD “JESD46“, which stipulates:
  “Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change.”
  Notwithstanding the aforesaid individual agreements shall prevail.

Your prompt reply will help Infineon to assure a smooth and well-executed transition. If Infineon does not hear from your side by the due date, we will assume your full acceptance to this proposed change and its implementation.

Your attention and response to this matter is greatly appreciated.

On 16 April 2020, Infineon acquired Cypress.
We are now in the process of merging and consolidating our tools and processes for PCN, Information Notes, Errata and Product Discontinuance. We ask for your patience in the meantime. For further details, please visit our website:
https://www.infineon.com/cms/en/about-infineon/company/cypress-acquisition/

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Product/Process Change Notification

N° 2021-080-A

Products affected	Please refer to attached affected product list 1_cip21080_A

Detailed change information

Subject:	Datasheet update for products TLE9180x and TLE9183QK
Reason/Motivation:	Datasheet update.

Description	**Old**	**New**
DATA SHEET: Change of datasheet parameters/electrical specification (min./max./typ. values) and/or AC/DC specification	TLE9180-xxQK: datasheet rev. 1.72 TLE9180C-xxQK: datasheet rev. 1.01 TLE9180D-x1QK: datasheet rev. 1.10 TLE9180D-26QK: datasheet rev. 1.01 TLE9180D-32QK: datasheet rev. 1.01 TLE9183QK: datasheet rev. 1.01	TLE9180-xxQK: datasheet rev. 1.80 TLE9180C-xxQK: datasheet rev. 1.10 TLE9180D-x1QK: datasheet rev. 1.20 TLE9180D-26QK: datasheet rev. 1.10 TLE9180D-32QK: datasheet rev. 1.10 TLE9183QK: datasheet rev. 1.10

Product identification	Not applicable (for documentation only)
Anticipated impact of change	No change of product (neither of technology/package nor of chip design), only change of datasheet. DeQuMa-ID(s): SEM-DS-01

Attachments	1_cip21080_A	affected product list
	3_cip21080_A	customer information package

Time schedule

Final qualification report	Not applicable (for documentation only)
First samples available	Not applicable (for documentation only)
Intended start of delivery [1]	Not applicable (for documentation only)

[1] Provided date or earlier after customer approval

If you have any questions, please do not hesitate to contact your local sales office.

Datasheet update for products TLE9180x and TLE9183QK

Customer Information Package
PCN 2021-080-A

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Motivation of the change

- Infineon has reviewed all datasheets (DS) for the product family TLE9180x and TLE9183QK.
  - TLE9180-20QK, TLE9180-21QK
  - TLE9180C-20QK, TLE9180C-21QK, TLE9180C-31QK
  - TLE9180D-21QK, TLE9180D-31QK, TLE9180D-32QK
  - TLE9180D-26QK
  - TLE9183QK

- Several changes are required due to different aspects. The changes are listed in the revision history of each data sheet and on the following pages (see next sections) for better readability.

- The datasheets are accessible via the links listed at the end in section 5.

Sales Type	Old DS	New DS
TLE9180-xxQK	Rev. 1.72	Rev. 1.80
TLE9180C-xxQK	Rev. 1.01	Rev. 1.10
TLE9180D-x1QK	Rev. 1.10	Rev. 1.20
TLE9180D-26QK	Rev. 1.00	Rev. 1.10
TLE9180D-32QK	Rev. 1.01	Rev. 1.10
TLE9183QK	Rev. 1.01	Rev. 1.10

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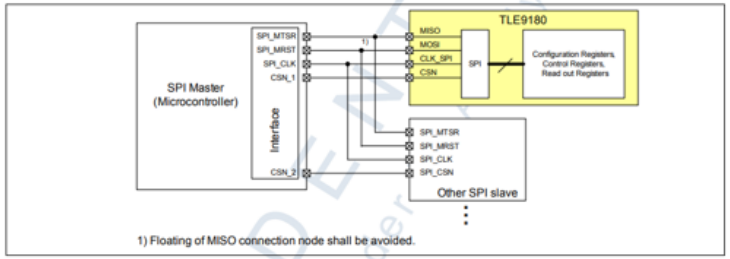
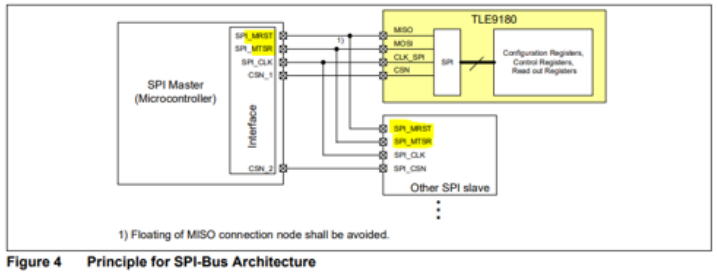
Change Overview TLE9180

Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
4.1 Absolute Maximum Ratings	**Table 1 Absolute Maximum Ratings** Supply Voltage for Power-up[1] V_{Vs3} – – 30 V – P_4.1.7 Supply Voltage V_{Vs3} 5.5 – 60 V Thermally limited P_4.3.1	**Table 1 Absolute Maximum Ratings** Supply Voltage for Power-up[1] V_{Vs6} – – 30 V – P_4.1.7 Supply Voltage V_{Vs3} 5.5 – 60 V Thermally limited P_4.3.1
4.1 Absolute Maximum Ratings	**Table 1 Absolute Maximum Ratings** (cont'd) T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) Voltage Difference SHx-SLx[1] V_{SSx1} -7 – 90 V – P_4.1.29 ~~Voltage Difference SHx-SLx[1] V_{SSx2} -10 – – V [10] P_4.1.30~~ ~~Voltage Difference SHx-SLx[1] V_{SSx3} -15 – – V [6] P_4.1.31~~ Voltage Difference VDHP-SHx $V_{dVDHPSHx2}$ -90 – 85 V en_vdh3=0x1 (cfg.: 3 VDHx pins enabled) P_4.1.32	**Table 1 Absolute Maximum Ratings** T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) Voltage Difference SHx-SLx[1] V_{SSx1} -12 – 90 V – P_4.1.29 Voltage Difference SHx-SLx[1] V_{SSx1} -12 – 90 V – P_4.1.29 Voltage Difference VDHP-SHx $V_{dVDHPSHx2}$ -90 – 85 V en_vdh3=0x1 (cfg.: 3 VDHx pins enabled) P_4.1.32
4.1 Absolute Maximum Ratings Modification valid for: TLE9180-21QK	**Table 1 Absolute Maximum Ratings** (cont'd) Voltage Range APC V_{AOP1} -0.3 – 60 V – P_4.1.39	**Table 1 Absolute Maximum Ratings** (cont'd) Voltage Range APC V_{AOP1} -0.3 – 60 V [10] P_4.1.39 10) A short circuit at APC for > 10 hrs might damage the device
4.1 Absolute Maximum Ratings	**Table 1 Absolute Maximum Ratings** (cont'd) **Temperatures** Storage Temperature T_{stg} -55 – 150 °C – P_4.1.54 Junction Temperature T_{J1} -40 – 150 °C – P_4.1.55 ~~Junction Temperature T_{J2} 40 – 175 °C 200h over lifetime P_4.1.56~~	**Table 1 Absolute Maximum Ratings** (cont'd) **Temperatures** Storage Temperature T_{stg} -55 – 150 °C – P_4.1.54 Junction Temperature T_{J1} -40 – 150 °C [12] P_4.1.55 12) For T_j >150°C please check compliance with the IFX qualification
4.2 Thermal Resistance Modification done in: TLE9180-20QK & TLE9180-21QK	**Table 2 Thermal Resistance** 2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip + Package) was simulated on a 76.2 × 114.3 ×1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 ×35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.	**Table 2 Thermal Resistance** 2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip + Package) was simulated on a 76.2 × 114.3 ×1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 ×35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

Change Overview TLE9180

Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
5.7 Electrical Characteristics IOs	1) Not subject of production test, specified by design	1) Not subject to production test, specified by design.
5.7 Electrical Characteristics IOS Modification valid for the TLE9180-21QK	**Table 5 Electrical Characteristics IOs** High Level Output Voltage | V_{AOPH1} | 4.2 | 5.0 | 6.0 | V | I_{load} = -1 mA | P_5.7.47	**Table 5 Electrical Characteristics IOs** High Level Output Voltage | V_{AOPH1} | 3.9 | 5.0 | 6.0 | V | I_{load}= -1mA | P_5.7.47
6 Serial Peripheral Interface - SPI	 **Figure 4 Principle for SPI-Bus Architecture**	 **Figure 4 Principle for SPI-Bus Architecture**
6.4 Cyclic Redundancy Check - CRC Generation and Detection	**6.4 Cyclic Redundancy Check - CRC Generation and Detection** The CRC is added to any data transmitted. It is calculated for the whole SPI frame, CRC bits excluded. The CRC check for incoming data is performed over the complete SPI frame.	**6.4 Cyclic Redundancy Check - CRC Generation and Detection** The CRC is added to any data transmitted. It is calculated for the whole SPI frame, CRC bits excluded. The CRC check for incoming data is performed over the complete SPI frame. In case of a CRC3 Error Detection on the MISO line by the µC, the message should be discarded and the register access should be repeated.
6.5 Electrical Characteristics SPI	**Table 6 Electrical Characteristics: Timing** (cont'd) Sequential Transfer Delay[3] | t_{SPI_td} | 250 | – | – | ns | [2] Figure 6, N | P_6.5.19	**Table 6 Electrical Characteristics: Timing** (cont'd) Sequential Transfer Delay[3] | t_{SPI_td} | 330 | – | – | ns | [2] Figure 6, N | P_6.5.19
6.5 Electrical Characteristics SPI	**Table 6 Electrical Characteristics: Timing** SPI Data Output (MISO) Lag | t_{SPI_lag1} | 0 | – | – | ns | [2] Figure 6, M | P_6.5.15 Enable (SS) Lag Time | t_{SPI_lag2} | 25 | – | – | ns | [2] Figure 6, M | P_6.5.18	**Table 6 Electrical Characteristics: Timing** (cont'd) Enable (SS) Lag Time | t_{SPI_lag} | 25 | – | – | ns | [2] Figure 6, M | P_6.5.15
6.5 Electrical Characteristics SPI	**Table 6 Electrical Characteristics: Timing** T_j = -40 °C to +150 °C, V_S = 5.5 V to 60 V and with respect to ground, positive current flowing into pin (unless otherwise specified). Parameter | Symbol | Values (Min. | Typ. | Max.) | Unit | Note / Test Condition | Number SPI Operating Frequency | f_{SPI_clk} | –[1] | – | 10 | MHz | [2] | P_6.5.1	**Table 6 Electrical Characteristics: Timing** T_j = -40 °C to +150 °C, V_S = 5.5 V to 60 V and with respect to ground, positive current flowing into pin (unless otherwise specified). Timings valid for 10 MHz operation. Parameter | Symbol | Values (Min. | Typ. | Max.) | Unit | Note / Test Condition | Number SPI Operating Frequency | f_{SPI_clk} | –[1] | – | 10 | MHz | [2] | P_6.5.1

Change Overview TLE9180

Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
6.5 Electrical Characteristics SPI	**Table 6 Electrical Characteristics: Timing** CLK_SPI Operating Period — t_{SPI_clk} — 100 — – — – — ns — 2) Figure 6, C — P_6.5.2 CLK_SPI High Time — t_{SPI_wsckh} — 37 — – — – — ns — 2) Figure 6, A — P_6.5.3 CLK_SPI Low Time — t_{SPI_wsckl} — 37 — – — – — ns — 2) Figure 6, B — P_6.5.4 CLK_SPI Fall Time — t_{SPI_clkf} — – — – — 13 — ns — 2) Figure 6, D — P_6.5.5 2) Not subject to production test; verified by design or characterization; measured between 10% and 90%; output load capacitance on MISO pin is ≤ 60pF.	**Table 6 Electrical Characteristics: Timing** CLK_SPI Operating Period — t_{SPI_clk} — 100 — – — – — ns — 2) Figure 6, C — P_6.5.2 CLK_SPI High Time — t_{SPI_wsckh} — 37 — – — – — ns — 2) Figure 6, A — P_6.5.3 CLK_SPI Low Time — t_{SPI_wsckl} — 37 — – — – — ns — 2) Figure 6, B — P_6.5.4 CLK_SPI Fall Time — t_{SPI_clkf} — – — – — 13 — ns — 2) Figure 6, D — P_6.5.5 2) Not subject to production test; verified by design or characterization; measured between 20% and 80%; output load capacitance on MISO pin is ≤ 60pF.
8.1 Output Stage Supply Concept	**8.1 Output Stage Supply Concept** requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20kHz PWM frequency. The charge pumps will be deactivated if the gate driver IC is set to sleep mode via $\overline{INH}$.	**8.1 Output Stage Supply Concept** requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20kHz PWM frequency. The charge pumps will be deactivated if the $\overline{INH}$ pin is set to low or a charge pump related error is detected. For details please check the supervision descriptions.
8.3 Electrical Characteristics Power Supply Modification done in: TLE9180-20QK & TLE9180-21QK	**Table 9 Electrical Characteristics: Power Supply** (cont'd) Quiescent Current VDHx — I_{QVDHx2} — – — 50 — 200 — nA — V_{VDHP}≤14V; T_a≤25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.31 Quiescent Current VDHx — I_{QVDHx1} — – — 50 — 200 — nA — V_{VDHP}≤60V; T_a≤25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.32	**Table 9 Electrical Characteristics: Power Supply** (cont'd) Quiescent Current VDHx — I_{QVDHx2} — – — 50 — 200 — nA — V_{VDHP}≤14V; V_{VDHx}≤14V; T_a≤25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.31 Quiescent Current VDHx — I_{QVDHx1} — – — 50 — 200 — nA — V_{VDHP}≤60V; V_{VDHx}≤60V; T_a≤25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.32
8.3 Electrical Characteristics Power Supply	**Table 9 Electrical Characteristics: Power Supply** (cont'd) Quiescent Current VDHP — I_{QVDH1} — – — – — 60 — µA — V_{VDHP}≤60V; T_j≤25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.48 Quiescent Current VDHP — I_{QVDH1} — – — – — 60 — µA — V_{VDHP}≤60V; T_j≤150°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.30 Total Quiescent Current Vs and VDHP, VDHx[16] — I_{Q2} — – — – — 12 — µA — V_{VS}=V_{VDHP}≤14V; T_j=25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.49 Total Quiescent Current Vs and VDHP, VDHx[16] — I_{Q2} — – — – — 55 — µA — V_{VS}=V_{VDHP}≤14V; T_j=150°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.33	**Table 9 Electrical Characteristics: Power Supply** (cont'd) Quiescent Current VDHP — I_{QVDH1} — – — – — 60 — µA — V_{VDHP}≤60V; T_j≤25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.48 Quiescent Current VDHP — I_{QVDH3} — – — – — 60 — µA — V_{VDHP}≤60V; T_j≤150°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.30 Total Quiescent Current Vs and VDHP, VDHx[16] — I_{Q1} — – — – — 12 — µA — V_{VS}=V_{VDHP}≤14V; T_j=25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.49 Total Quiescent Current Vs and VDHP, VDHx[16] — I_{Q2} — – — – — 55 — µA — V_{VS}=V_{VDHP}≤14V; T_j=150°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND — P_8.3.33

Change Overview TLE9180

Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
8.3 Electrical Characteristics Power Supply	**Table 9 Electrical Characteristics: Power Supply** (cont'd) Quiescent Current VDHP; I_{QVDH1}; –; –; 60; µA; V_{VDHP}≤60V; T_j≤25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND; P_8.3.48 Quiescent Current VDHP; I_{QVDH1}; –; –; 60; µA; V_{VDHP}≤60V; T_j≤150°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND; P_8.3.30 Total Quiescent Current Vs and VDHP, VDHx[16]; I_{Q2}; –; –; 12; µA; V_{VS}=V_{VDHP}≤14V; T_j=25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND; P_8.3.49 Total Quiescent Current Vs and VDHP, VDHx[16]; I_{Q2}; –; –; 55; µA; V_{VS}=V_{VDHP}≤14V; T_j=150°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND; P_8.3.33	**Table 9 Electrical Characteristics: Power Supply** (cont'd) Quiescent Current VDHP; I_{QVDH1}; –; –; 60; µA; V_{VDHP}≤60V; T_j≤25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND; P_8.3.48 Quiescent Current VDHP; I_{QVDH3}; –; –; 60; µA; V_{VDHP}≤60V; T_j≤150°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND; P_8.3.30 Total Quiescent Current Vs and VDHP, VDHx[16]; I_{Q1}; –; –; 12; µA; V_{VS}=V_{VDHP}≤14V; T_j=25°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND; P_8.3.49 Total Quiescent Current Vs and VDHP, VDHx[16]; I_{Q2}; –; –; 55; µA; V_{VS}=V_{VDHP}≤14V; T_j=150°C; V_{INH}=V_{SOFF}=GND[15]; V_{SHx}=GND; P_8.3.33
8.3 Electrical Characteristics Power Supply	**Table 9 Electrical Characteristics: Power Supply** 4) Accuracy derived from digital clock, for details please see Table 8	**Table 9 Electrical Characteristics: Power Supply** 4) Internal clock frequency accuracy has to be added to the specified values, please see Table 8
9.4 Electrical Characteristics Floating MOSFET Driver	**Table 11 Electrical Characteristics MOSFET drivers** Low Level Output Voltage Gxx-Sxx; V_{GS_LL}; –; –; 0.2; V; $I_{DCLoadOS}$≤-2mA; V_{ENA}=Low or Pins IHx and ILx=off; P_9.4.1 Low Level Output Voltage Gxx-Sxx; V_{GS_LLS}; –; –; 0.2; V; V_{SOFF}=Low; $I_{DCLoadOS}$=≤-2mA; P_9.4.2 High Level Output Voltage Difference between Low-side Output Stages GLx-SLx; dV_{G_HLS}; –; –; 0.5; V; $I_{DCLoadOS}$≤-2mA; V_{SLx}=0V; P_9.4.5 High Level Output Voltage Difference between High-side Output Stages GHx-SHx; dV_{G_HHS}; –; –; 0.5; V; $I_{DCLoadOS}$≤-2mA; V_{SHx}=0V; P_9.4.6	**Table 11 Electrical Characteristics MOSFET drivers** Low Level Output Voltage Gxx-Sxx; V_{GS_LL}; –; –; 0.2; V; 0 mA ≤ $I_{DCLoadOS}$ ≤ 2 mA; V_{ENA}=Low or Pins IHx and ILx=off; P_9.4.1 Low Level Output Voltage Gxx-Sxx; V_{GS_LLS}; –; –; 0.2; V; V_{SOFF}=Low; 0 mA ≤ $I_{DCLoadOS}$ ≤ 2mA; P_9.4.2 High Level Output Voltage Difference between Low-side Output Stages GLx-SLx; dV_{G_HLS}; –; –; 0.5; V; -2mA ≤ $I_{DCLoadOS}$ ≤ 0 mA; V_{SLx}=0V; P_9.4.5 High Level Output Voltage Difference between High-side Output Stages GHx-SHx; dV_{G_HHS}; –; –; 0.5; V; -2mA ≤ $I_{DCLoadOS}$ ≤ 0 mA; V_{SHx}=0V; P_9.4.6
9.4 Electrical Characteristics Floating MOSFET Driver	**Table 11 Electrical Characteristics MOSFET drivers** (cont'd) **Dynamic Characteristics** Turn On Gate Current; $I_{G(on)1}$; -0.75; -2.0; –; A; V_{BS}≥V_{BSUV}; V_{Gxx} - V_{Sxx}=0V; P_9.4.14	**Table 11 Electrical Characteristics MOSFET drivers** (cont'd) **Dynamic Characteristics** Turn On Gate Current; $I_{G(on)1}$; –; -2.0; -0.75; A; V_{BS}≥V_{BSUV}; V_{Gxx} - V_{Sxx}=0V; P_9.4.14

Change Overview TLE9180

Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
9.4 Electrical Characteristics Floating MOSFET Driver	**Table 11 Electrical Characteristics MOSFET drivers** (cont'd) Propagation Delay Time Matching (all FETs on) – – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.22 Propagation Delay Time Matching (all FETs turn off) – – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.23 Propagation Delay Time Matching Single Phase (high-side off to low-side on) 0 – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.24 Propagation Delay Time Matching Single Phase (low-side off to high-side on) 0 – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.25 Propagation Delay Time Matching all Phases (all high-sides off to all low-sides on) 0 – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.26 Propagation Delay Time Matching all Phases (all low-sides off to high-side on) 0 – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.27	**Table 11 Electrical Characteristics MOSFET drivers** (cont'd) Propagation Delay Time **Mismatch** (all FETs on) – – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.22 Propagation Delay Time **Mismatch** (all FETs turn off) – – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.23 Propagation Delay Time **Mismatch** Single Phase (high-side off to low-side on) 0 – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.24 Propagation Delay Time **Mismatch** Single Phase (low-side off to high-side on) 0 – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.25 Propagation Delay Time **Mismatch** all Phases (all high-sides off to all low-sides on) 0 – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.26 Propagation Delay Time **Mismatch** all Phases (all low-sides off to high-side on) 0 – 20 ns R_{Load}=2kΩ[3]; V_{Sxx}=0V P_9.4.27
10.5 Electrical Parameter Shunt Signal Conditioning	**Table 19 Electrical Characteristics - Shunt Signal Conditioning** (cont'd) Slew Rate SR – 15 – V/µs – P_10.5.22	**Table 19 Electrical Characteristics - Shunt Signal Conditioning** (cont'd) Slew Rate[2] SR – 15 – V/µs – P_10.5.22 2) Not subject to production test, specified by design
11.2.2 Failure Behavior Configuration	**Table 23 Shutdown Error Overview[1]** 3 sd_clk_fail Internal Clock Supervision Shutdown[3] ARE Active 3) In the case of monitoring clock stops operation fault reaction of output stages is latched error	**Table 23 Shutdown Error Overview[1]** 3 sd_clk_fail Internal Clock Supervision Shutdown[3] ARE **or LE** Active 3) Failure reaction can be ARE or LE dependent on type of internal fault
11.4.11 Overload Digital Output Pins	**11.4.11 Overload Digital Output Pins** The digital outputs are protected against short to GND and battery. If one output is shorted the output pin will be disconnected, a dedicated error register bit will be set. The pin $\overline{ERR}$ will be set to low. To unlock the output pin reset with ENA has to be performed. The failure behavior of the gate driver IC is adjustable at configuration mode, either the output stages will turn all external FETs off or not. Register **Err_outp** bit 4 to bit 0 indicate a short of a digital output pin.	**11.4.11 Overload Digital Output Pins** The digital outputs are protected against short to GND and battery. If one output is shorted the output pin will be disconnected, a dedicated error register bit will be set. The pin $\overline{ERR}$ will be set to low in case $\overline{ERR}$ is not the affected pin. To unlock the output pin, reset with ENA has to be performed. The failure behavior of the gate driver IC is adjustable at configuration mode, either the output stages will turn all external FETs off or not. Functionality of the overload detection of the digital output pins is limited, for details please refer to **Chapter 18.11.4**.

Change Overview TLE9180

Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
11.4.4 High-side Buffer Capacitor Voltage Monitoring	**11.4.4 High-side Buffer Capacitor Voltage Monitoring** An integrated undervoltage monitoring for the external high-side buffer capacitor guarantees a sufficient supply for the high-side output stages. Additionally the external high-side FETs are protected not to turn on into linear mode if failure behavior is configured either as latched or auto restart error. The high-side buffer capacitor voltage will be monitored at pin BHx referred to pin SHx. If the voltage of the high-side buffer capacitor is below a certain threshold undervoltage will be detected at the affected output stage. The high-side buffer undervoltage threshold is not programmable. The detection is operational unless reduced operation mode has been entered. An overvoltage monitoring for the external high-side buffer capacitor guarantees gate source voltage for the external FET not higher as the destructive gate source voltage. Failure behavior and filter time is not configurable. High-side buffer overvoltage monitoring can be deactivated at configuration if diagnosis is not required. In case of overvoltage detection all output stages remain active but charge pump 2 will be deactivated. A reset via ENA is necessary for reactivation of charge pump 2. If overvoltage high-side buffer has been detected and charge pump 2 has been turned off duty cycle operation higher than 95% is not recommended and might end up in undervoltage high-side buffer detection. Register Err_i_2 bit 7, bit 6 and bit 5 indicate an overvoltage condition detected, bit 2, bit 1 and bit 0 indicate an undervoltage detection.	**11.4.4 High-side Buffer Capacitor Voltage Monitoring** An integrated undervoltage monitoring for the external high-side buffer capacitor guarantees a sufficient supply for the high-side output stages. Additionally the external high-side FETs are protected not to turn on into linear mode if failure behavior is configured either as latched or auto restart error. The high-side buffer capacitor voltage will be monitored at pin BHx referred to pin SHx. If the voltage of the high-side buffer capacitor is below a certain threshold undervoltage will be detected at the affected output stage. The high-side buffer undervoltage threshold is not programmable. The detection is operational unless reduced operation mode has been entered. An overvoltage monitoring for the external high-side buffer capacitor detects too high gate source voltages for the external FET. The failure behavior and filter time are not configurable. In case of an overvoltage detection, the ERR pin is set low and the dedicated error bit in the register will be set. The second charge pump will be deactivated all output stages remain active. A reset via ENA is necessary for the reactivation of the second charge pump. If the second charge pump is deactivated, an undervoltage high-side buffer detection might occur mainly at operation with high duty cycles. The overvoltage monitoring for the external high-side buffer capacitor can be deactivated at configuration. Register Err_i_2 bit 7, bit 6 and bit 5 indicate an overvoltage condition detected, bit 2, bit 1 and bit 0 indicate an undervoltage detection.
11.5 Electrical Characteristics Protection and Diagnostic Functions	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** Accuracy Undervoltage Threshold Vs | $V_{VSUVacc2}$ | -13.5 | PROG | +13.5 | % | 4.4V≥V_{VSUV}<7.5V | P_11.6.12	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** Accuracy Undervoltage Threshold Vs | $V_{VSUVacc2}$ | -13.5 | PROG | +13.5 | % | 4.2Vs≤V_{VSUV}<7.5V | P_11.6.12
11.5 Electrical Characteristics Protection and Diagnostic Functions	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** Entry Filter and Reaction Time of Reduced Operation Mode Detection at Vs[4] | $V_{VsROPf1}$ | 0.6 | – | – | µs | – | P_11.6.8 Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs[4] | $V_{VsROPf2}$ | 20 | – | – | µs | – | P_11.6.9	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** Entry Filter and Reaction Time of Reduced Operation Mode Detection at Vs[4] | $t_{VsROPf1}$ | 0.6 | – | – | µs | – | P_11.6.8 Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs[4] | $t_{VsROPf2}$ | 20 | – | – | µs | – | P_11.6.9
	Table 47 Electrical Characteristics - Protection and Diagnostic Functions Entry Filter and Reaction Time of Reduced Operation Mode Detection at VCC[4] | $V_{VCCROPf1}$ | 0.6 | – | – | µs | – | P_11.6.78 Exit Filter and Reaction Time of Reduced Operation Mode Detection at VCC[4] | $V_{VCCROPf2}$ | 20 | – | – | µs | – | P_11.6.79 Temperature Read Out Accuracy | T_{Tread_t} | -25 | – | +25 | K | – | P_11.6.115	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** Entry Filter and Reaction Time of Reduced Operation Mode Detection at VCC[4] | $t_{VCCROPf1}$ | 0.6 | – | – | µs | – | P_11.6.78 Exit Filter and Reaction Time of Reduced Operation Mode Detection at VCC[4] | $t_{VCCROPf2}$ | 20 | – | – | µs | – | P_11.6.79 Temperature Read Out Accuracy | T_{Tread_a} | -25 | – | +25 | K | – | P_11.6.115

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Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
11.5 Electrical Characteristics Protection and Diagnostic Functions	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Filter Time of SCD[2)3)] | t_{SCDf} | 1 | PROG | 6 | µs | 4 steps programmable | P_11.6.69	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Filter Time of SCD[2)3)] | t_{SCDf} | 0.5 1.7 3.4 5.7 | – | 2.3 3.5 5.2 7.5 | µs | f_fi_scd = '0x0' f_fi_scd = '0x1' f_fi_scd = '0x2' f_fi_scd = '0x3' | P_11.6.69
11.5 Electrical Characteristics Protection and Diagnostic Functions	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) **Timing Error Handling** Fault Reaction Time[4)] | t_{FRT} | 20 | – | 500 | ns | – | P_11.6.103 ENA Low Time Clearing Latched Errors | t_{clear} | 2.2 | 3.0[3)] | 3.8 | µs | ENA falling edge | P_11.6.104 ~~ENA Low Time Without Clearing Latched Errors~~ | ~~t_{Res}~~ | ~~–~~ | ~~1.0[2)]~~ | ~~1.3~~ | ~~µs~~ | ~~–~~ | ~~P_11.6.105~~	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Fault Reaction Time[4)] | t_{FRT} | 20 | – | 500 | ns | – | P_11.6.103 ENA Low Time Threshold for Clearing Latched Errors | t_{clear} | 2.2 | 3.0 | 3.8 | µs | ENA falling edge | P_11.6.104 Return Time to Normal Operation for ARE Fault Behavior Configuration[2)] | t_{RT} | – | – | 1.0 | µs | – | P_11.6.106
11.5 Electrical Characteristics Protection and Diagnostic Functions	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** Overvoltage Detection and Shutdown Filter Time Range Vs[2)3)] | t_{OVVS} | 10 | – | 100 | µs | 4 steps programmable | P_11.6.5 Undervoltage Filter Time Range Vs[2)3)] | t_{UVVSr} | 10 | – | 100 | µs | 4 steps programmable | P_11.6.14 Overvoltage Detection and Shutdown Filter Time Range VDHP[2)3)] | t_{OVVDHr} | 10 | – | 100 | µs | 4 steps programmable | P_11.6.19 Undervoltage Filter Time Range VDHP[2)3)] | t_{UVVDHr} | 10 | – | 100 | µs | 4 steps programmable | P_11.6.29 Undervoltage Detection and Shutdown Filter Time Range CB[2)3)] | t_{UVCBr} | 10 | – | 100 | µs | 4 steps programmable | P_11.6.43 Undervoltage Detection Filter Time BHx-SHx[2)3)] | t_{UVBS} | 1 | – | 10 | µs | 4 steps programmable | P_11.6.52 Filter Time of SCD[2)3)] | t_{SCDf} | 1 | PROG | 6 | µs | 4 steps programmable | P_11.6.69 VCC Filter Time[2)3)] | t_{VCCf} | 10 | – | 100 | µs | 4 steps programmable | P_11.6.85	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** Overvoltage Detection and Shutdown Filter Time Range Vs[2)3)] | t_{OVVS} | 8 24 48 96 | – | 17 33 57 105 | µs | f_ov_vs = '0x0' f_ov_vs = '0x1' f_ov_vs = '0x2' f_ov_vs = '0x3' | P_11.6.5 Undervoltage Filter Time Range Vs[2)3)] | t_{UVVSr} | 8 24 48 96 | – | 17 33 57 105 | µs | f_uv_vs = '0x0' f_uv_vs = '0x1' f_uv_vs = '0x2' f_uv_vs = '0x3' | P_11.6.14 Overvoltage Detection and Shutdown Filter Time Range VDHP[2)3)] | t_{OVVDHr} | 8 24 48 96 | – | 17 33 57 105 | µs | f_ov_vdh = '0x0' f_ov_vdh = '0x1' f_ov_vdh = '0x2' f_ov_vdh = '0x3' | P_11.6.19 Undervoltage Filter Time Range VDHP[2)3)] | t_{UVVDHr} | 8 24 48 96 | – | 17 33 57 105 | µs | f_uv_vdh = '0x0' f_uv_vdh = '0x1' f_uv_vdh = '0x2' f_uv_vdh = '0x3' | P_11.6.29 Undervoltage Detection and Shutdown Filter Time Range CB[2)3)] | t_{UVCBr} | 8 20 48 96 | – | 13 25 53 101 | µs | f_uv_cb = '0x0' f_uv_cb = '0x1' f_uv_cb = '0x2' f_uv_cb = '0x3' | P_11.6.43 Undervoltage Detection Filter Time BHx-SHx[2)3)] | t_{UVBS} | 0.8 2.8 4.8 9.8 | – | 1.8 3.8 5.8 10.8 | µs | f_uv_bs = '0x0' f_uv_bs = '0x1' f_uv_bs = '0x2' f_uv_bs = '0x3' | P_11.6.52 Filter Time of SCD[2)3)] | t_{SCDf} | 0.5 1.7 3.4 5.7 | – | 2.3 3.5 5.2 7.5 | µs | f_fi_scd = '0x0' f_fi_scd = '0x1' f_fi_scd = '0x2' f_fi_scd = '0x3' | P_11.6.69 VCC Filter Time[2)3)] | t_{VCCf} | 8 | – | 17 | µs | f_uv_vcc = f_ov_vcc = '0x0' | P_11.6.85 24 | – | 33 | µs | f_uv_vcc = f_ov_vcc = '0x1' 48 | – | 57 | µs | f_uv_vcc = f_ov_vcc = '0x2' 96 | – | 105 | µs | f_uv_vcc = f_ov_vcc = '0x3'

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Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
9.4 Electrical Characteristics Floating MOSFET Driver	**Table 11 Electrical Characteristics MOSFET drivers** (cont'd) **Dead Time**[8)9)] Programmable Dead Time Range | t_{DTr} | 107 | – | 5998 | ns | 166 steps programmable | P_9.4.30	**Table 11 Electrical Characteristics MOSFET drivers** (cont'd) **Dead Time**[8)9)] Programmable Dead Time Range[10)] | t_{DTr} | 107 | – | 5998 | ns | 166 steps programmable | P_9.4.30 10) Dead time can additionally take up to one internal clock cycle for synchronization
11.6 Electrical Characteristics Protection and Diagnostic Functions Modification done in: TLE9180-21QK	**Table 51 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) **VCC Read Out** Voltage Detection Range | V_{ADCr} | 0 | – | 5.554 | V | 0 to FFh | P_11.6.86	**Table 51 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) **VCC Read Out** Voltage Detection Range | V_{ADCr} | 0 | – | 5.55 | V | 0 to FFh | P_11.6.86
11.6 Electrical Characteristics Protection and Diagnostic Functions Modification done in: TLE9180-21QK	**Table 51 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) **Digital Driving Path Monitoring** Digital Driving Path Monitoring Filter Time[2)3)] | t_{STDTf} | – | 500 | – | ns | – | P_11.6.92 **Input Pattern Violation Monitoring** Input Pattern Violation Filter and Reaction Time[2)] | t_{STDTf} | – | 750 | – | ns | – | P_11.6.93	**Table 51 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) **Digital Driving Path Monitoring** Digital Driving Path Monitoring Filter Time[2)3)] | t_{STDTf1} | – | 500 | – | ns | – | P_11.6.92 **Input Pattern Violation Monitoring** Input Pattern Violation Filter and Reaction Time[2)] | t_{STDTf3} | – | 750 | – | ns | – | P_11.6.93
11.6 Electrical Characteristics Protection and Diagnostic Functions Modification done in: TLE9180-20QK	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) **Digital Driving Path Monitoring** Digital Driving Path Monitoring Filter Time[2)3)] | t_{STDTf} | – | 500 | – | ns | – | P_11.6.92	**Table 47 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) **Digital Driving Path Monitoring** Digital Driving Path Monitoring Filter Time[2)3)] | t_{STDTf1} | – | 500 | – | ns | – | P_11.6.92
11.4.8.2 Temperature Read Out	**11.4.8.2 Temperature Read Out** The absolute temperature can be read in the related SPI register in steps of 5.8 Kelvin per LSB. A temperature sensor is integrated at the output stage low-side 1. The signal is filtered with a moving average filter. After transition from configuration mode to normal operation mode it is recommended to wait 1ms before first temperature readout will be performed. The temperature read out result is stored in the register **temp_ls1**. The temperature sensor is independent to the sensor used for temperature detection and shutdown.	**11.4.8.2 Temperature Read Out** The absolute temperature can be read in the related SPI register in steps of T_{Tread_step} per LSB. A temperature sensor is integrated at the output stage low-side 1. The signal is filtered with a moving average filter. After transition from configuration mode to normal operation mode it is recommended to wait 1ms before first temperature readout will be performed. The temperature read out result is stored in the register **temp_ls1**. The temperature sensor is independent to the sensor used for temperature detection and shutdown.

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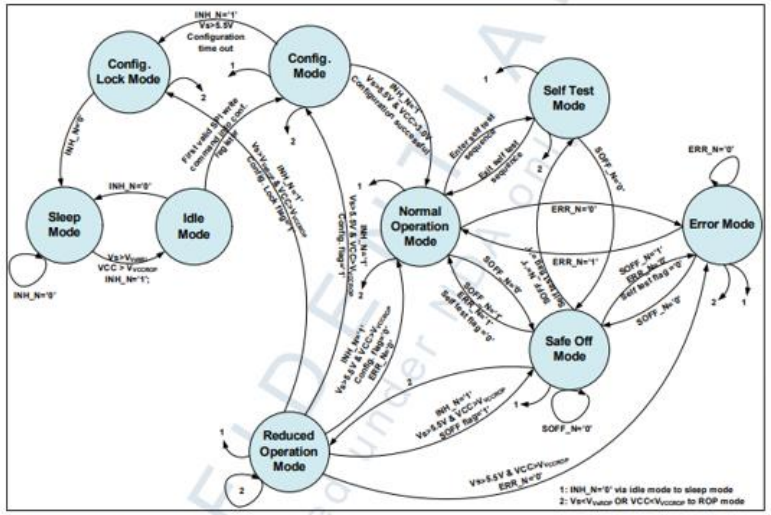
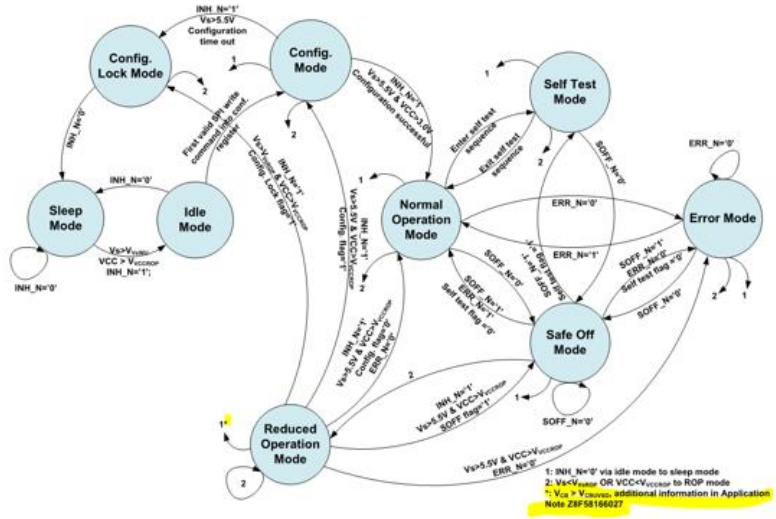
Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
13 Operation Modes	 Figure 29 Overview of Digital Operation Modes	 Figure 29 Overview of Digital Operation Modes
13.3 Sleep Mode	**13.3 Sleep Mode** If the $\overline{INH}$ pin is set to low the driver will be set into sleep mode. First the $\overline{INH}$ pin switches off the external FETs actively with the output stages and afterwards the complete power supply structure of the device. If the charge pump and high-side buffer capacitors are discharged the gate of the external FET will be clamped to its source with an internal passive clamping circuit. Once set to sleep mode the TLE9180-20QK has to be reconfigured.	**13.3 Sleep Mode** If the $\overline{INH}$ pin is set to low, the internal power down sequence will be initiated. After detection of the low transition changes at the $\overline{INH}$ pin will be ignored until the sleep mode has been reached. The gate driver IC will enter sleep mode after undervoltage shutdown at pin CB has been detected. First the $\overline{INH}$ pin switches off the external FETs actively with the output stages. The undervoltage shutdown at pin CB will be checked after the internal blocks – output stages, OPAMPs, internal 5 V voltage regulator, charge pumps, PFB blocks, output stages logic blocks and SCD blocks – are switched off. Afterwards the remaining clocks, the VCC supervision, all digital pads, the temperature sensors and the HV ADC will be deactivated. Then the digital core will be reset and the internal 3.3 V and 1.5 V regulators will be deactivated. If the charge pump and high-side buffer capacitors are discharged the gate of the external FET will be clamped to its source with an internal passive clamping circuit. Once set to sleep mode the TLE9180-20QK has to be reconfigured.
15.1.1 Configuration registers Modification done in: TLE9180-20QK	**fm_osfb** | 3:2 | rmw | **Output Stage Feedback Failure Behavior** 11_B , LE - Latched Error 10_B , ARE - Auto Restart Error 01_B , ERR - Error 00_B , W - Warning (default)	fm_osfb | 3:2 | none | **fixed bit field for TLE9180 basic** 00_B , fixed value for TLE9180 basic

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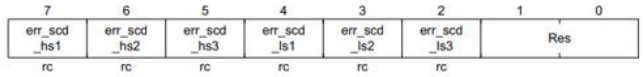
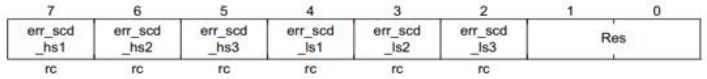
<table>
<tr><th>Datasheet Chapter</th><th>TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72</th><th>TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80</th></tr>
<tr><td>15.1.4 Read registers</td><td>
Short Circuit Errors

Err_scd Offset Reset Value
Short Circuit Errors 47_H 00_H



<table>
<tr><th>Field</th><th>Bits</th><th>Type</th><th>Description</th></tr>
<tr><td>err_scd_hs1</td><td>7</td><td>rc</td><td>Short Circuit at High-side 1
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_hs2</td><td>6</td><td>rc</td><td>Short Circuit at High-side 2
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_hs3</td><td>5</td><td>rc</td><td>Short Circuit at High-side 3
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls1</td><td>4</td><td>rc</td><td>Short Circuit at Low-side 1
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls2</td><td>3</td><td>rc</td><td>Short Circuit at Low-side 2
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls3</td><td>2</td><td>rc</td><td>Short Circuit at Low-side 3
1_B , Error set
0_B , No error</td></tr>
<tr><td>Res</td><td>1:0</td><td>none</td><td>Reserved
00_B , default value. do not change.</td></tr>
</table>
</td><td>
Err_scd Offset Reset Value
Short Circuit Errors 47_H 00_H



<table>
<tr><th>Field</th><th>Bits</th><th>Type</th><th>Description</th></tr>
<tr><td>err_scd_hs1</td><td>7</td><td>rc</td><td>Short Circuit Detection at High-side 1
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_hs2</td><td>6</td><td>rc</td><td>Short Circuit Detection at High-side 2
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_hs3</td><td>5</td><td>rc</td><td>Short Circuit Detection at High-side 3
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls1</td><td>4</td><td>rc</td><td>Short Circuit Detection at Low-side 1
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls2</td><td>3</td><td>rc</td><td>Short Circuit Detection at Low-side 2
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls3</td><td>2</td><td>rc</td><td>Short Circuit Detection at Low-side 3
1_B , Error set
0_B , No error</td></tr>
<tr><td>Res</td><td>1:0</td><td>none</td><td>Reserved
00_B , default value. do not change.</td></tr>
</table>
</td></tr>
<tr><td>16.1 Layout Guide Lines</td><td>
Application Information

• Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors)
• The exposed pad on the backside of the package is recommended to connect to GND
• VDHP has to be connected and referenced to a common point of the drains of the high-side MOSFETs
• For further information you may contact http://www.infineon.com/
</td><td>
• Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors)
• The exposed pad on the backside of the package is recommended to connect to GND
• The ground pins GND, CP_GND, A_GND have to be connected together to the PCB GND closely to the chip
• VDHP has to be connected and referenced to a common point of the drains of the high-side MOSFETs
• For further information you may contact http://www.infineon.com/
</td></tr>
</table>

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Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
18.8.2 Cross Talk of Automatic Recharging Circuits	**18.8.1 Quiescent Current Consumption at Pin Vs** Item 8.1. integrated into datasheet please refer to **Chapter 8.3**, maximum limits of quiescent current specification updated ~~**18.8.2 Cross Talk of Automatic Recharging Circuits**~~ ~~Item 8.2. integrated into datasheet please refer to **Chapter 9.4** and **Chapter 8.3**.~~ ~~Cross talk of the high-side buffer recharging circuit of phase 2 and phase 3 to phase 1 has been identified. This might lead to a higher high-side buffer supply capacitor voltage between pins BH1 to SH1. Higher gate voltages for high-side FET 1 has been observed. Gate source voltage of 15V will not be exceeded.~~ **18.9 Floating MOSFET Driver**	**18.8.1 Quiescent Current Consumption at Pin Vs** Item 8.1. integrated into datasheet please refer to **Chapter 8.3**, maximum limits of quiescent current specification updated **18.9 Floating MOSFET Driver** Erratas identified.
9.4 Electrical Characteristics Floating MOSFET Driver **8.3** Electrical Characteristics Power Supply	**Table 11 Electrical Characteristics MOSFET drivers** High Level Output Voltage Gxx-Sxx 1) — V_{G_HL1} — 8.5 — – — 13.5 — V — 7V≤V_{VS}<60V; C_{CPx}=1.0µF; C_{CB}=4.7µF; $I_{DCLoadOS}$=-2mA; V_{SLx}=V_{SHx}=0V — P_9.4.3 High Level Output Voltage Gxx-Sxx 1) — V_{G_HL2} — 8 — – — 12.5 — V — 5.5V≤V_{VS}<7V; C_{CPx}=1.0µF; C_{CB}=4.7µF; $I_{DCLoadOS}$=-2mA; V_{SLx}=V_{SHx}=0V — P_9.4.4 1) Max. limit may differ for output stage HS1. Output voltage of GH1-SH1 might be higher. Please refer to B13 errata, item 8.2., **Chapter 18.8.2**. **Table 9 Electrical Characteristics: Power Supply** (cont'd) High-side Buffer Supply Limitation Voltage BHx to SHx at CP2 Charging 10) — $V_{BHSHxlim}$ — 10 — 11 — 12 — V — – — P_8.3.15 10) Automatic charging of the high-side buffer supply capacitor (BHx-SHx) with charge pump 2 will be stopped if voltage level $V_{BHSHxlim}$ has been reached.	**Table 11 Electrical Characteristics MOSFET drivers** High Level Output Voltage Gxx-Sxx 1) — V_{G_HL1} — 8.5 — – — 13.5 — V — 7V≤V_{VS}<60V; C_{CPx}=1.0µF; C_{CB}=4.7µF; $I_{DCLoadOS}$=-2mA; V_{SLx}=V_{SHx}=0V — P_9.4.3 High Level Output Voltage Gxx-Sxx 1) — V_{G_HL2} — 8 — – — 12.5 — V — 5.5V≤V_{VS}<7V; C_{CPx}=1.0µF; C_{CB}=4.7µF; $I_{DCLoadOS}$=-2mA; V_{SLx}=V_{SHx}=0V — P_9.4.4 1) The bootstrap voltages might exceed the max. value due to capacitive coupling of the SHx voltages **Table 9 Electrical Characteristics: Power Supply** (cont'd) High-side Buffer Supply Limitation Voltage BHx to SHx at CP2 Charging 10) — $V_{BHSHxlim}$ — 10 — 11 — 12 — V — – — P_8.3.15 10) The bootstrap voltages might exceed the max value due to capacitive coupling of the SHx voltages

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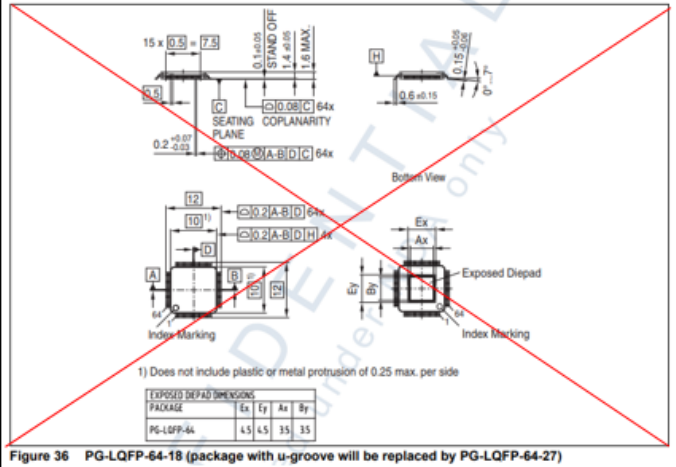
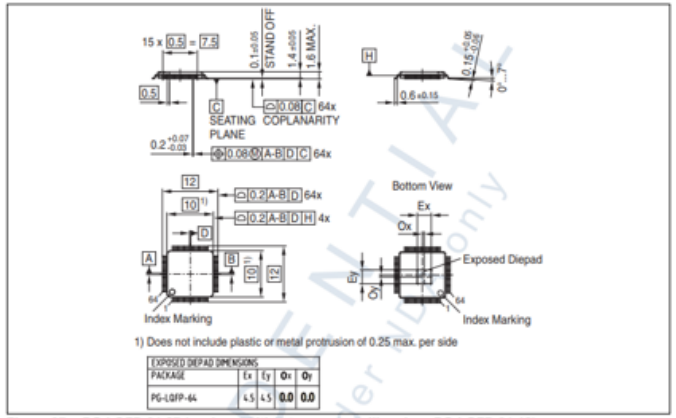
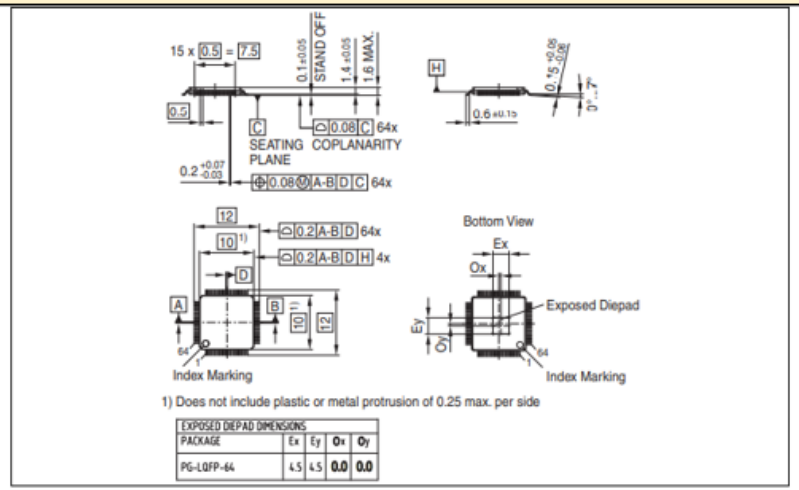
Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
17 Package Outlines Modification valid for the TLE9180-20QK & TLE9180-21QK	 1) Does not include plastic or metal protrusion of 0.25 max. per side EXPOSED DIEPAD DIMENSIONS PACKAGE | Ex | Ey | Ax | By PG-LQFP-64 | 4.5 | 4.5 | 3.5 | 3.5 **Figure 36 PG-LQFP-64-18 (package with u-groove will be replaced by PG-LQFP-64-27)**  1) Does not include plastic or metal protrusion of 0.25 max. per side EXPOSED DIEPAD DIMENSIONS PACKAGE | Ex | Ey | Ox | Oy PG-LQFP-64 | 4.5 | 4.5 | 0.0 | 0.0 **Figure 37 PG-LQFP-64-27 (package without u-groove will replace PG-LQFP-64-18)**	 1) Does not include plastic or metal protrusion of 0.25 max. per side EXPOSED DIEPAD DIMENSIONS PACKAGE | Ex | Ey | Ox | Oy PG-LQFP-64 | 4.5 | 4.5 | 0.0 | 0.0 **Figure 36 PG-LQFP-64**

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Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
3.1 Absolute Maximum Ratings	**Table 2 Absolute Maximum Ratings** Maximum Peak Pulse Current CB to CH2 | I_{CBCH2} | – | – | 1 | A | t = 5 µs | P_4.1.61	**Table 2 Absolute Maximum Ratings** Maximum Peak Pulse Current CB to CH2 | I_{CBCH2} | – | – | 1 | A | t = 5 µs 1) | P_4.1.61 1 Not subject to production test, specified by design
3.1 Absolute Maximum Ratings	**Table 2 Absolute Maximum Ratings** Supply Voltage for Power-up 1) | V_{Vs3} | – | – | 30 | V | – | P_4.1.7	**Table 2 Absolute Maximum Ratings** Supply Voltage for Power-up 1) | V_{Vs6} | – | – | 40 | V | – | P_4.1.7 Supply Voltage for Power-up 1) | V_{Vs6} | – | – | 40 | V | – | P_4.1.7
3.1 Absolute Maximum Ratings	**Table 2 Absolute Maximum Ratings** (cont'd) Voltage Difference SHx-SLx 1) | V_{SSx1} | -7 | – | 90 | V | – | P_4.1.29 ~~Voltage Difference SHx-SLx 1) | V_{SSx2} | -10 | – | – | V | 9) | P_4.1.30~~ ~~Voltage Difference SHx-SLx 1) | V_{SSx3} | -15 | – | – | V | 5) | P_4.1.31~~	**Table 2 Absolute Maximum Ratings** (cont'd) Voltage Difference SHx-SLx 1) | V_{SSx1} | -12 | – | 90 | V | IHx = High | P_4.1.29 Voltage Difference VDHP-SHx | V_{dVDHP} | -90 | – | 85 | V | en_vdh3 = 0x1 (cfg.: 3 VDHx pins enabled) | P_4.1.32
3.1 Absolute Maximum Ratings Modification valid for : TLE9180C-21QK & TLE9180C-31QK	**Table 2 Absolute Maximum Ratings** (cont'd) Voltage Range APC | V_{AOP1} | -0.3 | – | 60 | V | – | P_4.1.39	**Table 2 Absolute Maximum Ratings** (cont'd) Voltage Range APC | V_{AOP1} | -0.3 | – | 60 | V | 9) | P_4.1.39 9 A short circuit at APC for >10hrs might damage the device
3.1 Absolute Maximum Ratings	**Table 2 Absolute Maximum Ratings** (cont'd) **Temperatures** Storage Temperature | T_{stg} | -55 | – | 150 | °C | – | P_4.1.54 Junction Temperature | T_{J1} | -40 | – | 150 | °C | – | P_4.1.55 ~~Junction Temperature | T_{J2} | -40 | – | 175 | °C | 200h over lifetime | P_4.1.56~~	**Table 2 Absolute Maximum Ratings** (cont'd) **Temperatures** Storage Temperature | T_{stg} | -55 | – | 150 | °C | – | P_4.1.54 Junction Temperature | T_{J1} | -40 | – | 150 | °C | 11) | P_4.1.55 11 For T_J>150°C please check compliance with the IFX qualification
3.1 Absolute Maximum Ratings	**Table 2 Absolute Maximum Ratings** (cont'd) Max. Voltage Transients at SHx | V_{fSH_tr1} | – | – | 20 | V | Slew rate ≤ 1 V/ns 7)1) | P_4.3.31 1) Not subject to production test, specified by design. 7) Exceeding specified slew rate in combination with the maximum specified voltage transient may set the affected output stage in an undefined state for typically 1 µs.	**Table 2 Absolute Maximum Ratings** (cont'd) Max. Voltage Transients at SHx | V_{fSH_tr1} | – | – | 55 | V | Slew rate ≤ 1 V/ns 7)1) | P_4.3.31 1 Not subject to production test, specified by design. 7 At amplitudes higher than 20V the HS output stage can show unexpected switch off of the external MOSFET for typically 1 µs if the output stage is not switching. If the output stage is switching on or switching off, the output stage is switching normally even with amplitudes up 55V and slew rates up to 1V/ns

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<table>
<tr><th>Datasheet Chapter</th><th>TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01
TLE9180C-31QK DS V1.01</th><th>TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10
TLE9180C-31QK DS V1.10</th></tr>
<tr><td>3.2 Thermal Resistance</td><td>
Table 3 Thermal Resistance
2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip + Package) was simulated on a 76.2 × 114.3 ×1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 ×35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
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Table 3 Thermal Resistance
12 Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip + Package) was simulated on a 76.2 × 114.3 ×1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
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</td></tr>
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<table>
<tr><td>~~High Level Output Voltage~~</td><td>V_{ERRH5b}</td><td>3.8</td><td>–</td><td>V_{VCC}</td><td>V</td><td>~~V_{VS} > 7.2 V;~~ V_{VCC} = 5.0 V; I_{load} = -0.2 mA; ~~All Digital I/Os~~ = static</td><td>~~P_5.7.24~~</td></tr>
<tr><td>Low Level Output Voltage</td><td>V_{ERRL}</td><td>-0.1</td><td>–</td><td>0.4</td><td>V</td><td>I_{Load} = 0.2 mA</td><td>P_5.7.39</td></tr>
<tr><td>~~High Level Output Voltage~~</td><td>V_{SPIH5b}</td><td>3.8</td><td>–</td><td>V_{VCC}</td><td>V</td><td>~~V_{VS} > 7.2 V;~~ V_{VCC} = 5.0 V; I_{load} = -0.2 mA; ~~All Digital~~ I/Os = static</td><td>~~P_5.7.57~~</td></tr>
<tr><td>Low Level Output Voltage</td><td>V_{SPIL}</td><td>-0.1</td><td>–</td><td>0.4</td><td>V</td><td>I_{Load} = 0.2 mA</td><td>P_5.7.45</td></tr>
<tr><td>High Level Output Voltage[30)]</td><td>V_{ERRH5a}</td><td>3.3</td><td>–</td><td>V_{VCC}</td><td>V</td><td>~~5.5 V ≤ V_{VS} ≤ 7.2 V;~~ V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static</td><td>P_5.7.38</td></tr>
<tr><td>High Level Output Voltage[31)]</td><td>V_{SPIH5a}</td><td>3.3</td><td>–</td><td>V_{VCC}</td><td>V</td><td>~~5.5 V ≤ V_{VS} ≤ 7.2 V;~~ V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static</td><td>P_5.7.44</td></tr>
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<tr><td>High Level Output Voltage[31)]</td><td>V_{ERRH5a}</td><td>3.3</td><td>–</td><td>V_{VCC}</td><td>V</td><td>V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static</td><td>P_5.7.38</td></tr>
<tr><td>Low Level Output Voltage</td><td>V_{ERRL}</td><td>-0.1</td><td>–</td><td>0.4</td><td>V</td><td>I_{Load} = 0.2 mA</td><td>P_5.7.39</td></tr>
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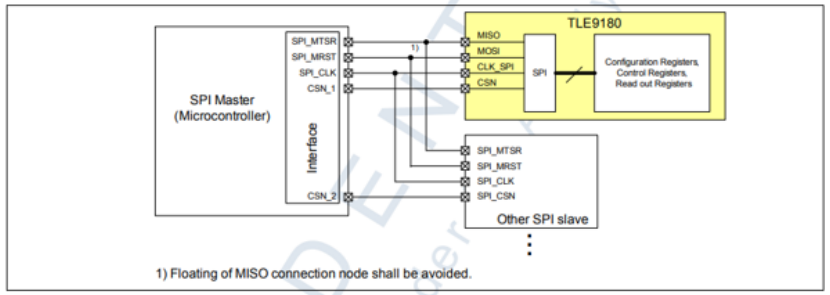
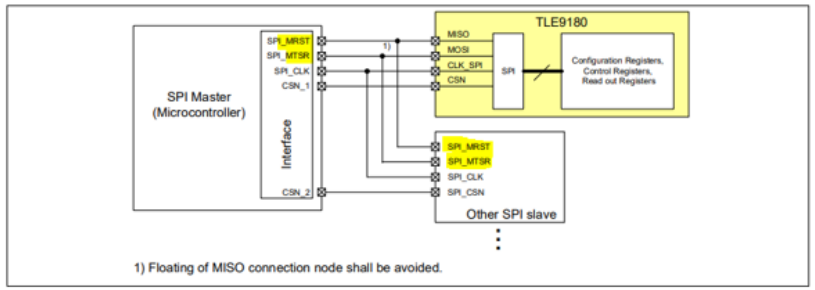
Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
4.7 Electrical Characteristics IOs	**Table 6 Electrical Characteristics IOs (continued)** High Level Output Voltage[7] | V_{ERRH5a} | 3.4 | – | V_{VCC} | V | 5.5 V ≤ V_{VS} ≤ 7.2 V; V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.38	**Table 6 Electrical Characteristics IOs (continued)** High Level Output Voltage[31] | V_{ERRH5a} | 3.3 | – | V_{VCC} | V | V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.38
	Table 6 Electrical Characteristics IOs (cont'd) High Level Output Voltage[7] | V_{SPIH5a} | 3.4 | – | V_{VCC} | V | 5.5 V ≤ V_{VS} ≤ 7.2 V; V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.44	**Table 6 Electrical Characteristics IOs** (cont'd) High Level Output Voltage[31] | V_{SPIH5a} | 3.3 | – | V_{VCC} | V | V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.44
4.7 Electrical Characteristics IOs	**Table 6 Electrical Characteristics IOs** (cont'd) **Pin ENA** ENA Propagation Time (for enable or disable the output stages) | t_{PENA} | – | 100 | – | ns | – | P_5.7.17	**Table 6 Electrical Characteristics IOs** (cont'd) **Pin ENA** ENA Propagation Time (for enable or disable the output stages) | t_{PENA} | – | 100 | 500 | ns | – | P_5.7.17
4.7 Electrical Characteristics Ios Change done in the TLE9180C-21QK & TLE9180C-31QK	**Table 6 Electrical Characteristics IOs** (cont'd) High Level Output Voltage | V_{AOPH1} | 4.2 | 5.0 | 6.0 | V | I_{load} = -1 mA | P_5.7.47	**Table 6 Electrical Characteristics IOs** (cont'd) High Level Output Voltage | V_{AOPH1} | 3.9 | 5.0 | 6.0 | V | I_{load} = -1 mA | P_5.7.47
5 Serial Peripheral Interface - SPI	 **Figure 4 Principle for SPI-Bus Architecture**	 **Figure 4 Principle for SPI-Bus Architecture**

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Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
5.4 Cyclic Redundancy Check - CRC Generation and Detection	**5.4 Cyclic Redundancy Check - CRC Generation and Detection** The CRC is added to any data transmitted. It is calculated for the whole SPI frame, CRC bits excluded. The CRC check for incoming data is performed over the complete SPI frame.	**5.4 Cyclic Redundancy Check - CRC Generation and Detection** The CRC is added to any data transmitted. It is calculated for the whole SPI frame, CRC bits excluded. The CRC check for incoming data is performed over the complete SPI frame. In case of an CRC3 Error Detection on the MISO line by the µC, the message should be discarded and the register access should be repeated.
5.5 Electrical Characteristics SPI	**Table 7 Electrical Characteristics: Timing** (cont'd) Sequential Transfer Delay[3] | t_{SPI_td} | 250 | – | – | ns | [2] Figure 6, N | P_6.5.19	**Table 7 Electrical Characteristics: Timing** (cont'd) Sequential Transfer Delay[34] | t_{SPI_td} | 330 | – | – | ns | [33] Figure 6, N | P_6.5.19
5.5 Electrical Characteristics SPI	**Table 7 Electrical Characteristics: Timing** T_j = -40°C to +150°C, V_S = 5.5 V to 60 V and with respect to GND, positive current flowing into pin (unless s otherwise specified). SPI Operating Frequency | f_{SPI_clk} | –[1] | – | 10 MHz | [2] | P_6.5.1	**Table 7 Electrical Characteristics: Timing** T_j = -40°C to +150°C, V_S = 5.5 V to 60 V, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified). Timings valid for 10 MHz operation. SPI Operating Frequency | f_{SPI_clk} | –[1] | – | 10 MHz | [2] | P_6.5.1
5.5 Electrical Characteristics SPI	**Table 7 Electrical Characteristics: Timing** SPI Data Output ~~(MISO)~~ Lag | t_{SPI_lag} | 25 | – | – | ns | [2] Figure 6, M | P_6.5.15	**Table 7 Electrical Characteristics: Timing** Enable (SS) Lag Time | t_{SPI_lag} | 25 | – | – | ns | [33] Figure 6, M | P_6.5.15
5.5 Electrical Characteristics SPI	**Table 7 Electrical Characteristics: Timing** CLK_SPI Operating Period | t_{SPI_clk} | 100 | – | – | ns | [2] Figure 6, C | P_6.5.2 CLK_SPI High Time | t_{SPI_wsclkh} | 37 | – | – | ns | [2] Figure 6, A | P_6.5.3 CLK_SPI Low Time | t_{SPI_wsclkl} | 37 | – | – | ns | [2] Figure 6, B | P_6.5.4 CLK_SPI Fall Time | t_{SPI_clkf} | – | – | 13 | ns | [2] Figure 6, D | P_6.5.5 2) Not subject to production test; verified by design or characterization; measured between 10% and 90%; output load capacitance on MISO pin is ≤ 60pF.	**Table 7 Electrical Characteristics: Timing** CLK_SPI Operating Period | t_{SPI_clk} | 100 | – | – | ns | [33] Figure 6, C | P_6.5.2 CLK_SPI High Time | t_{SPI_wsclkh} | 37 | – | – | ns | [33] Figure 6, A | P_6.5.3 CLK_SPI Low Time | t_{SPI_wsclkl} | 37 | – | – | ns | [33] Figure 6, B | P_6.5.4 33 Not subject to production test; verified by design or characterization; measured between 20% and 80%; output load capacitance on MISO pin is ≤ 60 pF
7.1 Output Stage Supply Concept	**7.1 Output Stage Supply Concept** requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20kHz PWM frequency. The charge pumps will be deactivated if the gate driver IC is set to sleep mode via $\overline{INH}$.	**7.1 Output Stage Supply Concept** fulfills the requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20 kHz PWM frequency. The charge pumps will be deactivated if the gate driver IC is set to sleep mode via pin $\overline{INH}$ or a charge pump related error is detected. For details please check the supervision descriptions.

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Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
7.3 Electrical Characteristics Power Supply (tbd)	**Table 10 Electrical Characteristics: Power Supply** (cont'd) **Supply current in Reduced Operation Mode at Vs** Supply Current Vs | $I_{Vs(ROMVS)}$ | – | 12 | 20 | mA | $V_{Vs}=V_{VDHP}=3V$ | P_8.3.36	**Table 10 Electrical Characteristics: Power Supply** (cont'd) 'd) Supply Current Vs | $I_{Vs(ROMVS)}$ | – | 12 | 24 | mA | $V_{Vs} = V_{VDHP} = 3$ V | P_8.3.36
7.3 Electrical Characteristics Power Supply	**Table 10 Electrical Characteristics: Power Supply** (cont'd) Voltage Vs for Guaranteed Power-up of Charge Pumps | V_{VsWU} | 6.0 | – | – | V | – | P_8.3.38	**Table 10 Electrical Characteristics: Power Supply** (cont'd) Voltage Vs for ensured Power-up of Charge Pumps | V_{VsWU} | 6.0 | – | – | V | – | P_8.3.38
7.3 Electrical Characteristics Power Supply	**Table 10 Electrical Characteristics: Power Supply** (cont'd) Quiescent Current VDHx | I_{QVDHx2} | – | 50 | 200 | nA | $V_{VDHP} \le 14$ V; $T_a \le 25°C$; $V_{INH} = V_{SOFF} = GND$[14]; $V_{SHx} = GND$ | P_8.3.31 Quiescent Current VDHx | I_{QVDHx1} | – | 50 | 200 | nA | $V_{VDHP} \le 60$ V; $T_a \le 25°C$; $V_{INH} = V_{SOFF} = GND$[14]; $V_{SHx} = GND$ | P_8.3.32	**Table 10 Electrical Characteristics: Power Supply** (cont'd) Quiescent Current VDHx | I_{QVDHx2} | – | 50 | 200 | nA | $V_{VDHP} \le 14$ V; $V_{VDHx} \le 14$ V; $T_a \le 25°C$; $V_{INH} = V_{SOFF} = GND$[49]; $V_{SHx} = GND$ | P_8.3.31 Quiescent Current VDHx | I_{QVDHx1} | – | 50 | 200 | nA | $V_{VDHP} \le 60$ V; $V_{VDHx} \le 60$ V; $T_a \le 25°C$; $V_{INH} = V_{SOFF} = GND$[49]; $V_{SHx} = GND$ | P_8.3.32
7.3 Electrical Characteristics Power Supply	**Table 10 Electrical Characteristics: Power Supply** (cont'd) Quiescent Current VDHP | I_{QVDH1} | – | – | 61 | µA | $V_{VDHP} \le 60$ V; $T_j \le 25°C$; $V_{INH} = V_{SOFF} = GND$[14]; $V_{SHx} = GND$ | P_8.3.48 Quiescent Current VDHP | I_{QVDH1} | – | – | 61 | µA | $V_{VDHP} \le 60$ V; $T_j \le 150°C$; $V_{INH} = V_{SOFF} = GND$[14]; $V_{SHx} = GND$ | P_8.3.30 Total Quiescent Current Vs and VDHP | I_{Q2} | – | – | 17 | µA | $V_{VS} = V_{VDHP} \le 14$ V; $T_j = 25°C$; $V_{INH} = V_{SOFF} = GND$[14]; $V_{SHx} = GND$ | P_8.3.49 Total Quiescent Current Vs and VDHP | I_{Q2} | – | – | 70 | µA | $V_{VS} = V_{VDHP} \le 14$ V; $T_j = 150°C$; $V_{INH} = V_{SOFF} = GND$[14]; $V_{SHx} = GND$ | P_8.3.33	**Table 10 Electrical Characteristics: Power Supply** (cont'd) Quiescent Current VDHP | I_{QVDH1} | – | – | 61 | µA | $V_{VDHP} \le 60$ V; $T_j \le 25°C$; $V_{INH} = V_{SOFF} = GND$[49]; $V_{SHx} = GND$ | P_8.3.48 Quiescent Current VDHP | I_{QVDH3} | – | – | 61 | µA | $V_{VDHP} \le 60$ V; $T_j \le 150°C$; $V_{INH} = V_{SOFF} = GND$[49]; $V_{SHx} = GND$ | P_8.3.30 Total Quiescent Current Vs and VDHP | I_{Q1} | – | – | 17 | µA | $V_{VS} = V_{VDHP} \le 14$ V; $T_j = 25°C$; $V_{INH} = V_{SOFF} = GND$[49]; $V_{SHx} = GND$ | P_8.3.49 Total Quiescent Current Vs and VDHP | I_{Q2} | – | – | 70 | µA | $V_{VS} = V_{VDHP} \le 14$ V; $T_j = 150°C$; $V_{INH} = V_{SOFF} = GND$[49]; $V_{SHx} = GND$ | P_8.3.33

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Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
7.3 Electrical Characteristics Power Supply	2) Filter Time Accuracy referenced from internal clock accuracy, please see **Chapter 6.2**	87 Internal clock frequency accuracy has to be added to the specified values, please see ***Chapter 6.2***
8.4 Electrical Characteristics Floating MOSFET Driver	**Table 12 Electrical Characteristics MOSFET drivers**	**Table 12 Electrical Characteristics MOSFET drivers**
8.4 Electrical Characteristics Floating MOSFET Driver	**Table 12 Electrical Characteristics MOSFET drivers** (cont'd)	**Table 12 Electrical Characteristics MOSFET drivers** (cont'd)
8.4 Electrical Characteristics Floating MOSFET Driver	**Table 12 Electrical Characteristics MOSFET drivers** (cont'd)	**Table 12 Electrical Characteristics MOSFET drivers** (cont'd)

Table 12 Electrical Characteristics MOSFET drivers

Low Level Output Voltage Gxx-Sxx	V_{GS_LL}	–	–	0.2	V	$I_{DCLoadOS} \le$ -2 mA; V_{ENA} = Low or Pins IHx and ILx = off	P_9.4.1
Low Level Output Voltage Gxx-Sxx	V_{GS_LLS}	–	–	0.2	V	V_{SOFF} = Low; $I_{DCLoadOS} \le$ -2 mA	P_9.4.2
High Level Output Voltage Gxx-Sxx[1)]	V_{G_HL2}	8	–	12.5	V	5.5 V ≤ V_{VS} < 7 V; C_{CPx} = 1.0 µF; C_{CB} = 4.7 µF; $I_{DCLoadOS}$ = -2 mA; $V_{SLx} = V_{SHx}$ = 0 V	P_9.4.4
High Level Output Voltage Difference between Low-side Output Stages GLx-SLx	dV_{G_HLS}	–	–	0.5	V	$I_{DCLoadOS} \le$ -2 mA; V_{SLx} = 0 V	P_9.4.5

Table 12 Electrical Characteristics MOSFET drivers

Low Level Output Voltage Gxx-Sxx	V_{GS_LL}	–	–	0.2	V	0 mA ≤ $I_{DCLoadOS} \le$ 2 mA; V_{ENA}=Low or Pins IHx and ILx=off	P_9.4.1
Low Level Output Voltage Gxx-Sxx	V_{GS_LLS}	–	–	0.2	V	V_{SOFF}=Low; 0 mA ≤ $I_{DCLoadOS} \le$ 2mA	P_9.4.2
High Level Output Voltage Difference between Low-side Output Stages GLx-SLx	dV_{G_HLS}	–	–	0.5	V	-2mA ≤ $I_{DCLoadOS} \le$ 0 mA; V_{SLx}=0V	P_9.4.5
High Level Output Voltage Difference between High-side Output Stages GHx-SHx	dV_{G_HHS}	–	–	0.5	V	-2mA ≤ $I_{DCLoadOS} \le$ 0 mA; V_{SHx}=0V	P_9.4.6

Table 12 Electrical Characteristics MOSFET drivers (cont'd)

Turn On Gate Current	$I_{G(on)1}$	-0.75	-2.0	–	A	$V_{BS} \ge V_{BSUV}$; $V_{Gxx} - V_{Sxx}$ = 0 V	P_9.4.14

Table 12 Electrical Characteristics MOSFET drivers (cont'd)

Turn On Gate Current	$I_{G(on)1}$	–	-2.0	-0.75	A	$V_{BS} \ge V_{BSUV}$; $V_{Gxx} - V_{Sxx}$ = 0 V	P_9.4.14

Table 12 Electrical Characteristics MOSFET drivers (cont'd)

Propagation Delay Time (all low-side FETs off)	$t_{P(ILF)}$	30	35	70	ns	R_{Load} = 2 kΩ[3)]; V_{Sxx} = 0 V	P_9.4.19
Propagation Delay Time (all high-side FETs off)	$t_{P(IHF)}$	30	35	70	ns	R_{Load} = 2 kΩ[3)]; V_{Sxx} = 0 V	P_9.4.21

Table 12 Electrical Characteristics MOSFET drivers (cont'd)

Propagation Delay Time (all low-side FETs off)	$t_{P(ILF)}$	25	35	70	ns	R_{Load} = 2 kΩ[52)]; V_{Sxx} = 0 V	P_9.4.19
Propagation Delay Time (all high-side FETs off)	$t_{P(IHF)}$	25	35	70	ns	R_{Load} = 2 kΩ[52)]; V_{Sxx} = 0 V	P_9.4.21

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Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
8.4 Electrical Characteristics Floating MOSFET Driver	**Table 12 Electrical Characteristics MOSFET drivers** (cont'd) Propagation Delay Time Matching (all FETs on) | $t_{P(an)}$ | – | – | 20 | ns | R_{Load} = 2 kΩ[3]; V_{Sxx} = 0 V | P_9.4.22 Propagation Delay Time Matching (all FETs turn off) | $t_{P(af)}$ | – | – | 20 | ns | R_{Load} = 2 kΩ[3]; V_{Sxx} = 0 V | P 9.4.23 Propagation Delay Time Matching Single Phase (high-side off to low-side on) | $t_{P(1hfln)}$ | 0 | – | 20 | ns | R_{Load} = 2 kΩ[3]; V_{Sxx} = 0 V | P_9.4.24 Propagation Delay Time Matching Single Phase (low-side off to high-side on) | $t_{P(1lfhn)}$ | 0 | – | 20 | ns | R_{Load} = 2 kΩ[3]; V_{Sxx} = 0 V | P_9.4.25 Propagation Delay Time Matching all Phases (all high-sides off to all low-sides on) | $t_{P(ahfln)}$ | 0 | – | 20 | ns | R_{Load} = 2 kΩ[3]; V_{Sxx} = 0 V | P_9.4.26 Propagation Delay Time Matching all Phases (all low-sides off to high-side on) | $t_{P(alfhn)}$ | 0 | – | 20 | ns | R_{Load} = 2 kΩ[3]; V_{Sxx} = 0 V | P_9.4.27	**Table 12 Electrical Characteristics MOSFET drivers** (cont'd) Propagation Delay Time Mismatch (all FETs on) | $t_{P(an)}$ | – | – | 20 | ns | R_{Load} = 2 kΩ[52]; V_{Sxx} = 0 V | P_9.4.22 Propagation Delay Time Mismatch (all FETs turn off) | $t_{P(af)}$ | – | – | 20 | ns | R_{Load} = 2 kΩ[52]; V_{Sxx} = 0 V | P_9.4.23 Propagation Delay Time Mismatch Single Phase (high-side off to low-side on) | $t_{P(1hfln)}$ | 0 | – | 20 | ns | R_{Load} = 2 kΩ[52]; V_{Sxx} = 0 V | P_9.4.24 Propagation Delay Time Mismatch Single Phase (low-side off to high-side on) | $t_{P(1lfhn)}$ | 0 | – | 20 | ns | R_{Load} = 2 kΩ[52]; V_{Sxx} = 0 V | P_9.4.25 Propagation Delay Time Mismatch all Phases (all high-sides off to all low-sides on) | $t_{P(ahfln)}$ | 0 | – | 20 | ns | R_{Load} = 2 kΩ[52]; V_{Sxx} = 0 V | P_9.4.26 Propagation Delay Time Mismatch all Phases (all low-sides off to high-side on) | $t_{P(alfhn)}$ | 0 | – | 20 | ns | R_{Load} = 2 kΩ[52]; V_{Sxx} = 0 V | P_9.4.27
9.5 Electrical Parameter Shunt Signal Conditioning	**Table 18 Electrical Characteristics - Shunt Signal Conditioning** (cont'd) Slew Rate | *SR* | – | 15 | – | V/µs | – | P_10.5.22	**Table 18 Electrical Characteristics - Shunt Signal Conditioning** (cont'd) Slew Rate[60] | *SR* | – | 15 | – | V/µs | – | P_10.5.22 60 Not subject to production test, specified by design
10.2.2 Failure Behavior Configuration	**Table 24 Shutdown Error Overview**[1] Bit Position | Bit Name | Description | Output Stages | Charge Pumps | ERR Pin 3 | sd_clk_fail | Internal Clock Supervision Shutdown[3] | ARE | Active | Low (LE) 3) In the case of monitoring clock stops operation fault reaction of output stages is latched error	**Table 24 Shutdown Error Overview**[1] Bit Position | Bit Name | Description | Output Stages | Charge Pumps | ERR Pin 3 | sd_clk_fail | Internal Clock Supervision Shutdown[82] | ARE or LE | Active | Low (ARE or LE) 82 Failure reaction can be ARE or LE dependent on type of internal fault
10.2.2 Failure Behavior Configuration	**Table 24 Shutdown Error Overview**[78] Bit Position | Bit Name | Description | Output Stages | Charge Pumps | ERR Pin 4 | sd_uv_cb | Undervoltage CB Shutdown | ARE | Active | Low (LE)	**Table 24 Shutdown Error Overview**[78] Bit Position | Bit Name | Description | Output Stages | Charge Pumps | ERR Pin 4 | sd_uv_cb | Undervoltage CB Shutdown | ARE | Active | Low (ARE)

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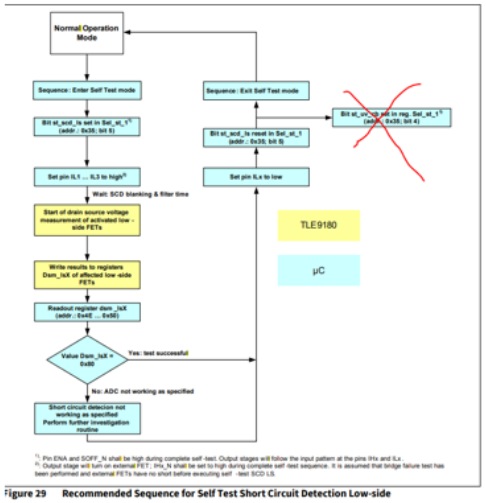
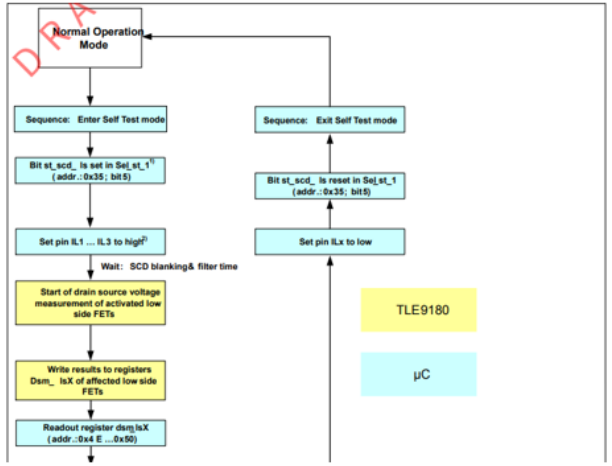
Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
10.5.16 Overload Digital Output Pins	**10.5.16 Overload Digital Output Pins** The digital outputs are protected against short to GND and battery. If one output is shorted the output pad will be disconnected, a dedicated error register bit will be set. The pin $\overline{ERR}$ will be set to low. To unlock the output pin reset with ENA has to be performed. The failure behavior of the gate driver IC is adjustable at configuration mode, either the output stages will turn all external FETs off or not. Functionality of the overload detection of the digital output pins is limited, for details please refer to **Chapter 16.3.8**. Register **Err_outp** bit 4 to bit 0 indicate a short of a digital output pin.	**10.5.16 Overload Digital Output Pins** The digital outputs are protected against short to GND and battery. If one output is shorted the output pad will be disconnected, a dedicated error register bit will be set. The pin $\overline{ERR}$ will be set to low in case pin $\overline{ERR}$ is not the affected pin. To unlock the output pin reset with ENA has to be performed. The failure behavior of the gate driver IC is adjustable at configuration mode, either the output stages will turn all external FETs off or not. Functionality of the overload detection of the digital output pins is limited, for details please refer to ***Chapter 16.3.7***. Register ***Err_outp*** bit 4 to bit 0 indicate a short of a digital output pin.
10.5.4 High-side Buffer Capacitor Voltage Monitoring	**10.5.4 High-side Buffer Capacitor Voltage Monitoring** An overvoltage monitoring for the external high-side buffer capacitor guarantees gate source voltage for the external FET not higher as the destructive gate source voltage. Failure behavior and filter time is not configurable. High-side buffer overvoltage monitoring can be deactivated at configuration if diagnosis is not required. In case of overvoltage detection all output stages remain active but charge pump 2 will be deactivated. A reset via ENA is necessary for reactivation of charge pump 2. If overvoltage high-side buffer has been detected and charge pump 2 has been turned off duty cycle operation higher than 95% is not recommended and might end up in undervoltage high-side buffer detection.	**10.5.4 High-side Buffer Capacitor Voltage Monitoring** An overvoltage monitoring for the external high-side buffer capacitor detects too high gate source voltages for the external FET. The failure behavior and filter time are not configurable. In case of an overvoltage detection, the ERR pin is set low and the dedicated error bit in the register is set. The 2nd charge pump is deactivated and all output stages remain active. A reset via ENA is necessary for the reactivation of the 2nd charge pump. If the 2nd charge pump is deactivated, an undervoltage high-side buffer detection might occur mainly at operation with high duty cycles. The overvoltage monitoring for the external high-side buffer capacitor can be deactivated at configuration.
10.5.11.2 S Self-test Function for SCD Modification valid for TLE9180C-21QK & TLE9180C-31QK	 Figure 29 Recommended Sequence for Self Test Short Circuit Detection Low-side	

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Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
10.6 Electrical Characteristics Protection and Diagnostic Functions	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Accuracy Undervoltage Threshold Vs | $V_{VSUVacc2}$ | -13.5 | PROG | +13.5 | % | 4.4 V ≥ V_{VSUV} < 7.5 V | P_11.6.12	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Accuracy Undervoltage Threshold Vs | $V_{VSUVacc2}$ | -13.5 | PROG | +13.5 | % | 4.2 V ≤ V_{VSUV} < 7.5 V | P_11.6.12
10.6 Electrical Characteristics Protection and Diagnostic Functions	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** Entry Filter and Reaction Time of Reduced Operation Mode Detection at Vs | $V_{VsROPf1}$ | 0.6 | – | – | µs | 4) | P_11.6.8 Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs | $V_{VsROPf2}$ | 20 | – | – | µs | 4) | P_11.6.9	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** Entry Filter and Reaction Time of Reduced Operation Mode Detection at Vs | $t_{VsROPf1}$ | 0.6 | – | – | µs | 89) | P_11.6.8 Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs | $t_{VsROPf2}$ | 20 | – | – | µs | 89) | P_11.6.9
10.6 Electrical Characteristics Protection and Diagnostic Functions	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** Entry Filter and Reaction Time of Reduced Operation Mode Detection at VCC | $V_{VCCROPf1}$ | 0.6 | – | – | µs | 4) | P_11.6.78 Exit Filter and Reaction Time of Reduced Operation Mode Detection at VCC | $V_{VCCROPf2}$ | 20 | – | – | µs | 4) | P_11.6.79 Temperature Read Out Accuracy | t_{Tread_f} | -25 | – | +25 | K | – | P_11.6.115	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** Entry Filter and Reaction Time of Reduced Operation Mode Detection at VCC | $t_{VCCROPf1}$ | 0.6 | – | – | µs | 89) | P_11.6.78 Exit Filter and Reaction Time of Reduced Operation Mode Detection at VCC | $t_{VCCROPf2}$ | 20 | – | – | µs | 89) | P_11.6.79 Temperature Read Out Accuracy | T_{Tread_a} | -25 | – | +25 | K | – | P_11.6.115
10.6 Electrical Characteristics Protection and Diagnostic Functions	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Filter Time of SCD[2)3)] | t_{SCDf} | 1 | PROG | 6 | µs | 4 steps programmable | P_11.6.69	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Filter Time of SCD[87)88)] | t_{SCDf} | 0.5 1.7 3.4 5.7 | PROG | 2.3 3.5 5.2 7.5 | µs | f_fi_scd = '0x0' f_fi_scd = '0x1' f_fi_scd = '0x2' f_fi_scd = '0x3' | P_11.6.69
10.6 Electrical Characteristics Protection and Diagnostic Functions	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) ENA Low Time Clearing Latched Errors | t_{clear} | 2.2 | 3.0 | 3.8 | µs | ENA falling edge | P_11.6.104 ENA Low Time Without Clearing Latched Errors | t_{Res} | – | 1.0[2)] | 1.3 | µs | – | ~~P_11.6.105~~ Return Time to Normal Operation for ARE Fault Behavior Configuration[2)] | t_{RT} | – | – | 1.0 | µs | – | P_11.6.106	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) ENA Low Time Threshold for Clearing Latched Errors | t_{clear} | 2.2 | 3.0 | 3.8 | µs | ENA falling edge | P_11.6.104 Return Time to Normal Operation for ARE Fault Behavior Configuration[87)] | t_{RT} | – | – | 1.0 | µs | – | P_11.6.106

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Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
10.6 Electrical Characteristics Protection and Diagnostic Functions	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions**	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions**

Table 53 Electrical Characteristics - Protection and Diagnostic Functions

Overvoltage Detection and Shutdown Filter Time Range Vs[2)3)]	t_{OVVS}	10	–	100	µs	4 steps programmable	P_11.6.5
Undervoltage Filter Time Range Vs[2)3)]	t_{UVVSr}	10	–	100	µs	4 steps programmable	P_11.6.14
Overvoltage Detection and Shutdown Filter Time Range VDHP[2)3)]	t_{OVVDHr}	10	–	100	µs	4 steps programmable	P_11.6.19
Undervoltage Filter Time Range VDHP[2)3)]	t_{UVVDHr}	10	–	100	µs	4 steps programmable	P_11.6.29
Undervoltage Detection and Shutdown Filter Time Range CB[2)3)]	t_{UVCBr}	10	–	100	µs	4 steps programmable	P_11.6.43
Undervoltage Detection Filter Time BHx-SHx[2)3)]	t_{UVBS}	1	–	10	µs	4 steps programmable	P_11.6.52
Filter Time of SCD[2)3)]	t_{SCDf}	1	PROG	6	µs	4 steps programmable	P_11.6.69
VCC Filter Time[2)3)]	t_{VCCf}	10	–	100	µs	4 steps programmable	P_11.6.85

Table 53 Electrical Characteristics - Protection and Diagnostic Functions

Overvoltage Detection and Shutdown Filter Time Range Vs[87)88)]	t_{OVVS}	8 24 48 96	–	17 33 57 105	µs	f_ov_vs = '0x0' f_ov_vs = '0x1' f_ov_vs = '0x2' f_ov_vs = '0x3'	P_11.6.5
Undervoltage Filter Time Range Vs[87)88)]	t_{UVVSr}	8 24 48 96	–	17 33 57 105	µs	f_uv_vs = '0x0' f_uv_vs = '0x1' f_uv_vs = '0x2' f_uv_vs = '0x3'	P_11.6.14
Overvoltage Detection and Shutdown Filter Time Range VDHP[87)88)]	t_{OVVDHr}	8 24 48 96	–	17 33 57 105	µs	f_ov_vdh = '0x0' f_ov_vdh = '0x1' f_ov_vdh = '0x2' f_ov_vdh = '0x3'	P_11.6.19
Undervoltage Filter Time Range VDHP[87)88)]	t_{UVVDHr}	8 24 48 96	–	17 33 57 105	µs	f_uv_vdh = '0x0' f_uv_vdh = '0x1' f_uv_vdh = '0x2' f_uv_vdh = '0x3'	P_11.6.29
Undervoltage Detection and Shutdown Filter Time Range CB[87)88)]	t_{UVCBr}	8 20 48 96	–	13 25 53 101	µs	f_uv_cb = '0x0' f_uv_cb = '0x1' f_uv_cb = '0x2' f_uv_cb = '0x3'	P_11.6.43
Undervoltage Detection Filter Time BHx-SHx[87)88)]	t_{UVBS}	0.8 2.8 4.8 9.8	–	1.8 3.8 5.8 10.8	µs	f_uv_bs = '0x0' f_uv_bs = '0x1' f_uv_bs = '0x2' f_uv_bs = '0x3'	P_11.6.52
Filter Time of SCD[87)88)]	t_{SCDf}	0.5 1.7 3.4 5.7	PROG	2.3 3.5 5.2 7.5	µs	f_fi_scd = '0x0' f_fi_scd = '0x1' f_fi_scd = '0x2' f_fi_scd = '0x3'	P_11.6.69
VCC Filter Time[87)88)]	t_{VCCf}	8 24 48 96	–	17 33 57 105	µs	f_uv_vcc = f_ov_vcc = '0x0' f_uv_vcc = f_ov_vcc = '0x1' f_uv_vcc = f_ov_vcc = '0x2' f_uv_vcc = f_ov_vcc = '0x3'	P_11.6.85

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Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
8.4 Electrical Characteristics Floating MOSFET Driver	**Table 12 Electrical Characteristics MOSFET drivers** (cont'd) Programmable Dead Time Range | t_{DTr} | 107 | – | 5998 | ns | 166 steps programmable | P_9.4.30	**Table 12 Electrical Characteristics MOSFET drivers** (cont'd) Programmable Dead Time Range[57] | t_{DTr} | 107 | – | 5998 | ns | 166 steps programmable | P_9.4.30 57 Dead time can additionally take up to one internal clock cycle for synchronization
10.5 Electrical Characteristics Protection and Diagnostic Functions Modification valid for: TLE9180C-21QK & TLE9180C-31QK	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) **VCC Read Out** Voltage Detection Range | V_{ADCr} | 0 | – | 5.554 | V | 0 to FFh | P_11.6.86	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) **VCC Read Out** Voltage Detection Range | V_{ADCr} | 0 | – | 5.55 | V | 0 to FFh | P_11.6.86
10.6 Electrical Characteristics Protection and Diagnostic Functions	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) **Digital Driving Path Monitoring** Digital Driving Path Monitoring Filter Time[2)3)] | t_{STDTf} | – | 500 | – | ns | – | P_11.6.92 Input Pattern Violation Filter and Reaction Time[2)] | t_{STDTf} | – | 750 | – | ns | – | P_11.6.93	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Digital Driving Path Monitoring Filter Time[87)88)] | t_{STDTf1} | – | 500 | – | ns | – | P_11.6.92 Input Pattern Violation Filter and Reaction Time[87)] | t_{STDTf3} | – | 750 | – | ns | – | P_11.6.93
10.5.8.2 Temperature Read Out	**10.5.8.2 Temperature Read Out** The absolute temperature can be read in the related SPI register in steps of 5.8 Kelvin per LSB. Six sensors are integrated monitoring all output stages. So the temperature of every output stage can be read out. The signal is filtered with a moving average filter. After transition from configuration mode to normal operation mode it is required to wait 1 ms before first temperature readout will be performed. A significant higher temperature at one output stage with a regular PWM pattern applied will indicate some irregularities at the affected output stage, either internally or caused by external circuit. The six temperature sensors are independent to the sensor used for temperature detection and shutdown. Measurement results are stored in the registers called **temp_ls1**, **temp_ls2**, **temp_ls3**, **temp_hs1**, **temp_hs2** and **temp_hs3**.	**10.5.8.2 Temperature Read Out** The absolute temperature can be read in the related SPI register in steps of T_{Tread_step} per LSB. Six sensors are integrated monitoring all output stages. So the temperature of every output stage can be read out. The signal is filtered with a moving average filter. After transition from configuration mode to normal operation mode it is required to wait 1 ms before first temperature readout will be performed. A significant higher temperature at one output stage with a regular PWM pattern applied will indicate some irregularities at the affected output stage, either internally or caused by external circuit. The six temperature sensors are independent to the sensor used for temperature detection and shutdown. Measurement results are stored in the registers called ***temp_ls1***, ***temp_ls2***, ***temp_ls3***, ***temp_hs1***, ***temp_hs2*** and ***temp_hs3***.
11.2 Electrical Parameter Phase Feedback	**Table 55 Electrical Characteristics - Phase Feedback** Propagation Delay Time | t_{PDfb} | – | 60 70 | 100 100 | ns | 50%/50% selected 80%/25% selected | P_12.2.6	**Table 55 Electrical Characteristics - Phase Feedback** Propagation Delay Time | t_{PDfb} | – | 60 70 | 110 110 | ns | 50%/50% selected 80%/25% selected | P_12.2.6

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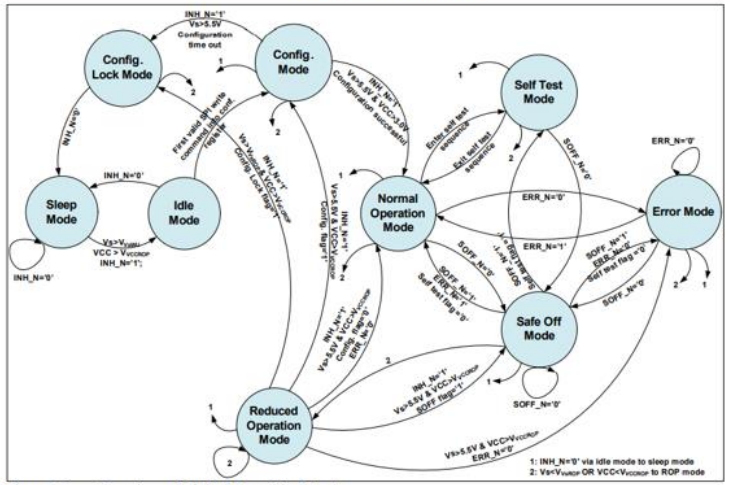
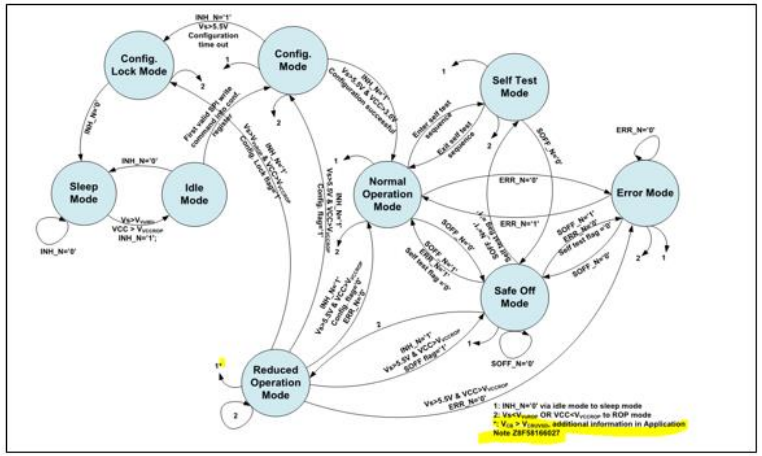
Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
13 Operation Modes	 **Figure 33 Overview of Digital Operation Modes**	 **Figure 33 Overview of Digital Operation Modes**
13.2.1 SPI Status Flags: Modification valid only for: TLE9180C-20QK	**SPI Status Flag Error, Warning and Special Event** The SPI status flags Error, Warning or Special Event in a transmitted frame (MISO) indicate the status of the device according to the current register value. If the fault is not present anymore and the indicated fault is cleared by a read command (MOSI) of a register 0x41 to 0x4D (except register 0x4A) the fault is not visible in the SPI status flags. In this case the error information can only be seen once in the detailed error bit of the transmitted error register (transmitted data of error-register 0x41 to 0x4D (except register 0x4A)). It can only be detected by the SPI status flags of the previous transmitted SPI frame (MISO), if the fault was already present at that time. The bits 2, 5 and 6 of the register 0x4A, for details see **Table 53** set the SPI status flags only once and it is cleared after the next valid SPI frame automatically. For details please contact Infineon.	**SPI Status Flag Error, Warning and Special Event** The SPI status flags Error, Warning or Special Event in a transmitted frame (MISO) indicate the status of the device according to the current register value. If the fault is not present anymore and the indicated fault is cleared by a read command (MOSI) of a register 0x41 to 0x4D (except register 0x4A) the fault is not visible in the SPI status flags. In this case the error information can only be seen once in the detailed error bit of the transmitted error register (transmitted data of error-register 0x41 to 0x4D (except register 0x4A)). It can only be detected by the SPI status flags of the previous transmitted SPI frame (MISO), if the fault was already present at that time. The bits 5 and 6 of the register 0x4A, for details see ***Table 53*** set the SPI status flags only once and it is cleared after the next valid SPI frame automatically. For details please contact Infineon.
13.3 Sleep Mode	**13.3 Sleep Mode** If the $\overline{INH}$ pin is set to low the driver will be set into sleep mode. First the $\overline{INH}$ pin switches off the external FETs actively with the output stages and afterwards the complete power supply structure of the device. If the charge pump and high-side buffer capacitors are discharged the gate of the external FET will be clamped to its source with an internal passive clamping circuit. Once set to sleep mode the TLE9180C-21QK has to be reconfigured.	**13.3 Sleep Mode** If the $\overline{INH}$ pin is set to low, the internal power down sequence will be initiated. After detection of the low transition changes at the $\overline{INH}$ pin will be ignored until the sleep mode has been reached. The gate driver IC will enter sleep mode after undervoltage shutdown at pin CB has been detected. First the $\overline{INH}$ pin switches off the external FETs actively with the output stages. The undervoltage shutdown at pin CB will be checked after the internal blocks – output stages, OPAMPs, internal 5 V voltage regulator, charge pumps, PFB blocks, output stages logic blocks and SCD blocks – are switched off. Afterwards the remaining clocks, the VCC supervision, all digital pads, the temperature sensors and the HV ADC will be deactivated. Then the digital core will be reset and the internal 3.3 V and 1.5 V regulators will be deactivated. If the charge pump and high-side buffer capacitors are discharged the gate of the external FET will be clamped to its source with an internal passive clamping circuit. Once set to sleep mode, the TLE9180C-21QK has to be reconfigured.

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<table>
<tr><th>Datasheet Chapter</th><th>TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01
TLE9180C-31QK DS V1.01</th><th>TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10
TLE9180C-31QK DS V1.10</th></tr>
<tr><td>14.1.1.13 Short Circuit Detection & Signal Path Supervision Failure Modes

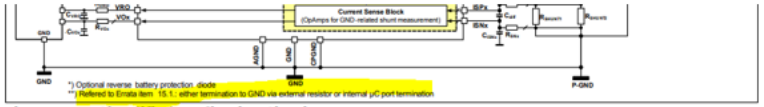
Modification done in:
TLE9180C-20QK</td><td>
<table>
<tr><td>fm_osfb</td><td>3:2</td><td>rmw</td><td>Output Stage Feedback Failure Behavior
11_B , LE - Latched Error
10_B , ARE - Auto Restart Error
01_B , ERR - Error
00_B , W - Warning (default)</td></tr>
</table>
</td><td>
<table>
<tr><td>fm_osfb</td><td>3:2</td><td>none</td><td>fixed bit field for TLE9180 basic
00_B , fixed value for TLE9180 basic</td></tr>
</table>
</td></tr>
<tr><td>15.1.4.8 Short Circuit Errors</td><td>
Err_scd — Short Circuit Errors — Offset 47_H — Reset Value 00_H
<table>
<tr><th>Field</th><th>Bits</th><th>Type</th><th>Description</th></tr>
<tr><td>err_scd_hs1</td><td>7</td><td>rc</td><td>Short Circuit at High-side 1
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_hs2</td><td>6</td><td>rc</td><td>Short Circuit at High-side 2
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_hs3</td><td>5</td><td>rc</td><td>Short Circuit at High-side 3
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls1</td><td>4</td><td>rc</td><td>Short Circuit at Low-side 1
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls2</td><td>3</td><td>rc</td><td>Short Circuit at Low-side 2
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls3</td><td>2</td><td>rc</td><td>Short Circuit at Low-side 3
1_B , Error set
0_B , No error</td></tr>
<tr><td>Res</td><td>1:0</td><td>none</td><td>Reserved
00_B , default value. do not change.</td></tr>
</table>
</td><td>
Err_scd — Short Circuit Errors — Offset 47_H — Reset Value 00_H
<table>
<tr><th>Field</th><th>Bits</th><th>Type</th><th>Description</th></tr>
<tr><td>err_scd_hs1</td><td>7</td><td>rc</td><td>Short Circuit Detection at High-side 1
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_hs2</td><td>6</td><td>rc</td><td>Short Circuit Detection at High-side 2
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_hs3</td><td>5</td><td>rc</td><td>Short Circuit Detection at High-side 3
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls1</td><td>4</td><td>rc</td><td>Short Circuit Detection at Low-side 1
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls2</td><td>3</td><td>rc</td><td>Short Circuit Detection at Low-side 2
1_B , Error set
0_B , No error</td></tr>
<tr><td>err_scd_ls3</td><td>2</td><td>rc</td><td>Short Circuit Detection at Low-side 3
1_R , Error set
0_B , No error</td></tr>
<tr><td>Res</td><td>1:0</td><td>none</td><td>Reserved
00_B , default value. do not change.</td></tr>
</table>
</td></tr>
<tr><td>16 Application Information</td><td>


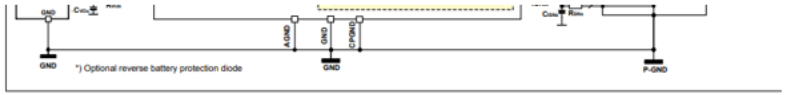
Figure 38 Simplified Application Circuit
</td><td>


Figure 38 Simplified Application Circuit
</td></tr>
</table>

Change Overview TLE9180C

Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
16.1 Layout Guide Lines	**Application Information** • Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors) • The exposed pad on the backside of the package is recommended to connect to GND • VDHP has to be connected and referenced to a common point of the drains of the high-side MOSFETs • For further information you may contact **http://www.infineon.com/**	• Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors) • The exposed pad on the backside of the package is recommended to connect to GND • The ground pins GND, CP_GND, A_GND have to be connected together to the PCB GND closely to the chip • VDHP has to be connected and referenced to a common point of the drains of the high-side MOSFETs • For further information you may contact ***http://www.infineon.com/***
16.2.1 Additional Components	[3] D2 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin V_s. Voltage drops at pin Vs in the range from 13V down to 6V shall not be shorter than 100µs. In the case of faster slew reates an input filter is required. For details please contact Infineon. [4] D4 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after CB capacitor has been shorted to GND.	[3] D2 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs with a slew rate ≥ 6V/100µs. D2 is not required with sufficient input filtering at the Vs pin. [4] D4 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data.
16.2.1 Additional Components	[6] D3 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs. The effect can be avoided with sufficient input filtering with C_{Vs} and (R_{Vs} or D1).	[8] D3 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs with a slew rate ≥ 6V/100µs. D3 is not required with sufficient filtering at the Vs pin. In case D3 is not used a 100 kΩ pull down to GND at CL1 shall be placed.
16.3.2 Cross Talk of Automatic Recharging Circuits	**16.3.2 Quiescent Current Consumption at Pin Vs** Please refer to **Table 10**. After pulling $\overline{INH}$ to low the quiescent current can be up to 20 µA at pin Vs for a short period of time. The effect is strongly temperature dependent. Under hot conditions the decay time is in the range of seconds, at ambient conditions in the range of minutes and at cold up to 1h. **16.3.3 Cross Talk of Automatic Recharging Circuits** Please refer to **Chapter 7.3** and **Chapter 8.4**. Cross talk of the high-side buffer recharging circuit of phase 2 and phase 3 to phase 1 has been identified. This might lead to a higher high-side buffer supply capacitor voltage between pins BH1 to SH1. Higher gate voltages for high-side FET 1 has been observed. Gate source voltage of 15 V will not be exceeded. **16.3.4 Minimum Input Pulses at Pins $\overline{IHx}$ and ILx**	**16.3.2 Quiescent Current Consumption at Pin Vs** Please refer to ***Table 10***. After pulling $\overline{INH}$ to low the quiescent current can be up to 20 µA at pin Vs for a short period of time. The effect is strongly temperature dependent. Under hot conditions the decay time is in the range of seconds, at ambient conditions in the range of minutes and at cold up to 1h. **16.3.3 Minimum Input Pulses at Pins $\overline{IHx}$ and ILx** Please refer to ***Chapter 8.4***.

Change Overview TLE9180C

Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
8.4 Electrical Characteristics Floating MOSFET Driver	**Table 12 Electrical Characteristics MOSFET drivers** High Level Output Voltage Gxx-Sxx[1] | V_{G_HL1} | 8.5 | – | 13.5 | V | 7 V ≤ V_{VS} < 60 V; C_{CPx} = 1.0 µF; C_{CB} = 4.7 µF; $I_{DCLoadOS}$ = -2 mA; V_{SLx} = V_{SHx} = 0 V | P_9.4.3 High Level Output Voltage Gxx-Sxx[1] | V_{G_HL2} | 8 | – | 12.5 | V | 5.5 V ≤ V_{VS} < 7 V; C_{CPx} = 1.0 µF; C_{CB} = 4.7 µF; $I_{DCLoadOS}$ = -2 mA; V_{SLx} = V_{SHx} = 0 V | P_9.4.4 1) Max. limit may differ for output stage HS1. Output voltage of GH1-SH1 might be higher. For details please refer to **Chapter 16.3.3**	**Table 12 Electrical Characteristics MOSFET drivers** High Level Output Voltage Gxx-Sxx | V_{G_HL1} | 8.5 | – | 13.5 | V | 7 V ≤ V_{VS} < 60 V; C_{CPx} = 1.0 µF; C_{CB} = 4.7 µF; $I_{DCLoadOS}$ = -2 mA; V_{SLx} = V_{SHx} = 0 V | P_9.4.3 High Level Output Voltage Gxx-Sxx | V_{G_HL2} | 8 | – | 12.5 | V | 5.5 V ≤ V_{VS} < 7 V; C_{CPx} = 1.0 µF; C_{CB} = 4.7 µF; $I_{DCLoadOS}$ = -2 mA; V_{SLx} = V_{SHx} = 0 V | P_9.4.4
16.3.3 Minimum Input Pulses at Pins IHx and ILx	**16.3.4 Minimum Input Pulses at Pins $\overline{IHx}$ and ILx** Please refer to **Chapter 8.4**. Input turn on pulses at the pins $\overline{IHx}$ and ILx shorter than 50 ns may cause an increase of the turn on time of the external FET to maximum 1000 ns. Short voltage glitches at the pin CB have been observed. If 6 µC output ports are used to drive 6 FETs and dead time is generated by the µC avoid input pulses at $\overline{IHx}$ and ILx shorter than 50 ns. If 3 µC output ports are used to drive 6 FETs using the internal dead time of the TLE9180C-21QK avoid input pulses at $\overline{IHx}$ and ILx shorter than the internal dead + 50 ns. In case of glitches at pin CB has been identified please contact Infineon.	**16.3.3 Minimum Input Pulses at Pins $\overline{IHx}$ and ILx** Please refer to ***Chapter 8.4***. Input turn on pulses at the pins $\overline{IHx}$ and ILx shorter than 50 ns may cause an increase of the turn on time of the external FET to maximum 1000 ns. Short voltage glitches at the pin CB have been observed. If 6 µC output ports are used to drive 6 FETs and dead time is generated by the µC avoid input pulses at $\overline{IHx}$ and ILx shorter than t_{Pulse_in}. If 3 µC output ports are used to drive 6 FETs using the internal dead time of the TLE9180C-21QK avoid input pulses at $\overline{IHx}$ and ILx shorter than the internal dead + t_{Pulse_in}. In case of glitches at pin CB has been identified please contact Infineon.

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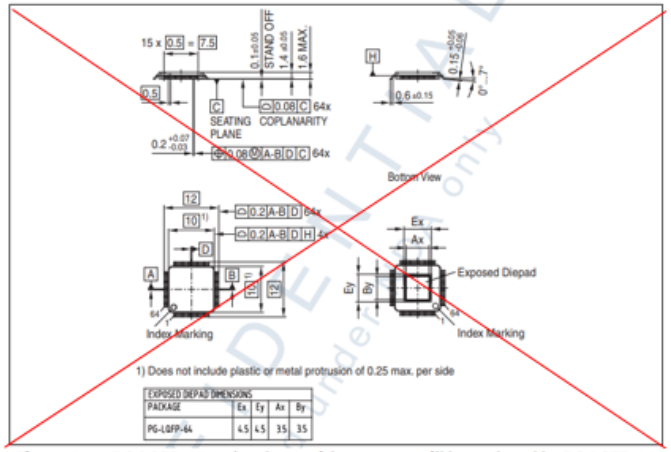
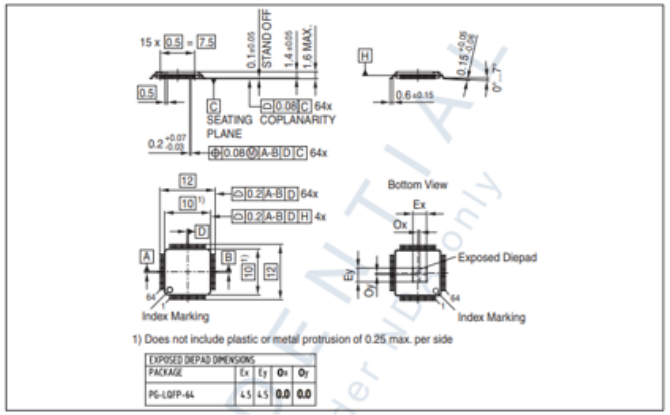
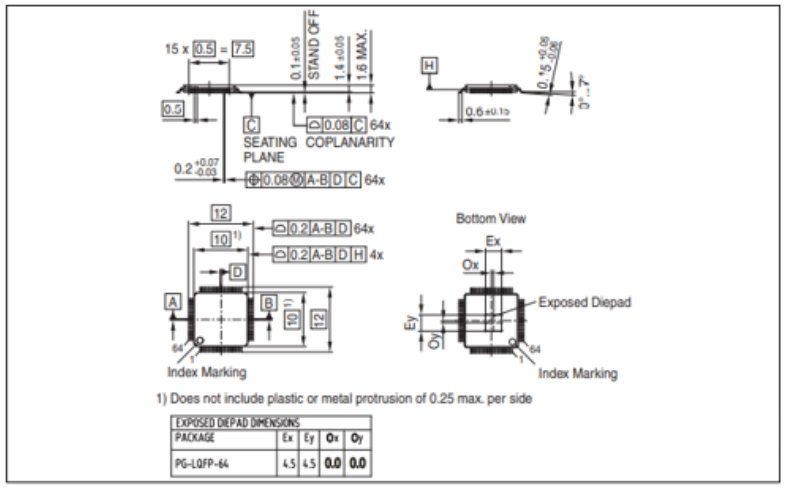
Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
17 Package Outlines	 1) Does not include plastic or metal protrusion of 0.25 max. per side EXPOSED DIEPAD DIMENSIONS PACKAGE | Ex | Ey | Ax | By PG-LQFP-64 | 4.5 | 4.5 | 3.5 | 3.5 **Figure 40 PG-LQFP-64-18 (package with u-groove will be replaced by PG-LQFP-64-27)**  1) Does not include plastic or metal protrusion of 0.25 max. per side EXPOSED DIEPAD DIMENSIONS PACKAGE | Ex | Ey | Ox | Oy PG-LQFP-64 | 4.5 | 4.5 | 0.0 | 0.0 **Figure 41 PG-LQFP-64-27 (package without u-groove will replace PG-LQFP-64-18)**	 1) Does not include plastic or metal protrusion of 0.25 max. per side EXPOSED DIEPAD DIMENSIONS PACKAGE | Ex | Ey | Ox | Oy PG-LQFP-64 | 4.5 | 4.5 | 0.0 | 0.0 **Figure 40 PG-LQFP-64**

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Change Overview TLE9180D

Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
3.1 Absolute Maximum Ratings Modification valid for TLE9180D-26QK only.	**Table 2 Absolute Maximum Ratings** Supply Voltage | V_{Vs1} | -0.3 | – | 60 | V | – | P_4.1.1 Voltage Range VDHP | V_{VDHP1} | -5 | – | 85 | V | 3) | P_4.1.3 ~~Voltage Difference Vs-VDHP | $V_{dVsVDHP}$ | -85 | – | 60 | V | – | P_4.1.5~~ Voltage Range VDH1, VDH2, VDH3 | V_{VDHx1} | -5 | – | 90 | V | – | P_4.1.6 ~~Voltage Difference Vs-VDH1, VDH2, VDH3 | $V_{dVsVDHx}$ | -90 | – | 60 | V | – | P_4.1.8~~ Voltage Range CL1 | V_{CL1} | -0.3 | – | 60 | V | – | P_4.1.9 Voltage Range CL2, CH2 | V_{CHL2} | -0.3 | – | 90 | V | – | P_4.1.12 Voltage Range SHx | V_{SHx1} | -7 | – | 90 | V | – | P_4.1.19 Voltage Range GHx | V_{GHx1} | -7 | – | 90 | V | – | P_4.1.22 Voltage Range BHx | V_{BH} | -0.3 | – | 90 | V | – | P_4.1.25 Voltage Difference SHx-SLx1) | V_{SSx1} | -12 | – | 90 | V | $\overline{IHx}$ = High | P_4.1.29 ~~Voltage Difference VDHP-SHx | $V_{dVDHPSHx2}$ | -90 | – | 90 | V | – | P_4.1.32~~ ~~Voltage Difference VDHx-SHx | $V_{dVDHxSHx}$ | -90 | – | 90 | V | – | P_4.1.33~~ Voltage Range $\overline{IHx}$, ILx, ENA | V_{DIP1} | -0.3 | – | 60 | V | – | P_4.1.34 Voltage Range VCC | V_{VCC1} | -0.3 | – | 60 | V | – | P_4.1.35 Voltage Range $\overline{INH}$ | V_{INH} | -0.3 | – | 90 | V | – | P_4.1.36 Voltage Range $\overline{SOFF}$ | V_{SOFF} | -0.3 | – | 90 | V | – | P_4.1.37 Voltage Range PFBx, $\overline{ERR}$ | V_{DOP1} | -0.3 | – | 60 | V | – | P_4.1.38 Voltage Range APC | V_{AOP1} | -0.3 | – | 60 | V | 9) | P_4.1.39 Voltage Range CLK_SPI, CSN, MOSI | V_{SPI1} | -0.3 | – | 60 | V | – | P_4.1.40 Voltage Range MISO | V_{SPI2} | -0.3 | – | 60 | V | – | P_4.1.41	**Table 2 Absolute Maximum Ratings** Supply Voltage | V_{Vs1} | -0.3 | – | 40 | V | – | P_4.1.1 Voltage Range VDHP | V_{VDHP1} | -5 | – | 50 | V | 3) | P_4.1.3 Voltage Range VDH1, VDH2, VDH3 | V_{VDHx1} | -5 | – | 50 | V | – | P_4.1.6 Voltage Range CL1 | V_{CL1} | -0.3 | – | 40 | V | – | P_4.1.9 Voltage Range CL2, CH2 | V_{CHL2} | -0.3 | – | 60 | V | – | P_4.1.12 Voltage Range SHx | V_{SHx1} | -7 | – | 50 | V | – | P_4.1.19 Voltage Range GHx | V_{GHx1} | -7 | – | 60 | V | – | P_4.1.22 Voltage Range BHx | V_{BH} | -0.3 | – | 60 | V | – | P_4.1.25 Voltage Difference SHx-SLx1) | V_{SSx1} | -12 | – | 50 | V | $\overline{IHx}$ = High | P_4.1.29 Voltage Range $\overline{IHx}$, ILx, ENA | V_{DIP1} | -0.3 | – | 40 | V | – | P_4.1.34 Voltage Range VCC | V_{VCC1} | -0.3 | – | 40 | V | – | P_4.1.35 Voltage Range $\overline{INH}$ | V_{INH} | -0.3 | – | 40 | V | – | P_4.1.36 Voltage Range $\overline{SOFF}$ | V_{SOFF} | -0.3 | – | 40 | V | – | P_4.1.37 Voltage Range PFBx, $\overline{ERR}$ | V_{DOP1} | -0.3 | – | 40 | V | – | P_4.1.38 Voltage Range APC | V_{AOP1} | -0.3 | – | 40 | V | 9) | P_4.1.39 Voltage Range CLK_SPI, CSN, MOSI | V_{SPI1} | -0.3 | – | 40 | V | – | P_4.1.40 Voltage Range MISO | V_{SPI2} | -0.3 | – | 40 | V | – | P_4.1.41
3.1 Absolute Maximum Ratings Modification valid for: TLE9180D-21QK, TLE9180D-31QK, TLE9180D-32QK	**Table 2 Absolute Maximum Ratings** (cont'd) Voltage Range APC | V_{AOP1} | -0.3 | – | 60 | V | – | P_4.1.39	**Table 2 Absolute Maximum Ratings** (cont'd) Voltage Range APC | V_{AOP1} | -0.3 | – | 60 | V | 9) | P_4.1.39 9 A short circuit at APC for >10hrs might damage the device
3.1 Absolute Maximum Ratings Modification valid for all, except TLE9180D-26QK and TLE9183QK.	**Table 2 Absolute Maximum Ratings** (cont'd) **Temperatures** Storage Temperature | T_{stg} | -55 | – | 150 | °C | – | P_4.1.54 Junction Temperature | T_{J1} | -40 | – | 150 | °C | – | P_4.1.55 Junction Temperature | T_{J2} | -40 | – | 175 | °C | 200h over lifetime | P_4.1.56	**Table 2 Absolute Maximum Ratings** (cont'd) **Temperatures** Storage Temperature | T_{stg} | -55 | – | 150 | °C | – | P_4.1.54 Junction Temperature | T_{J1} | -40 | – | 150 | °C | 11) | P_4.1.55 11 For T_J>150°C please check compliance with the IFX qualification

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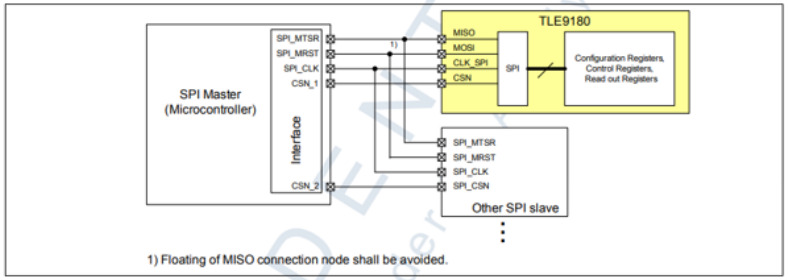
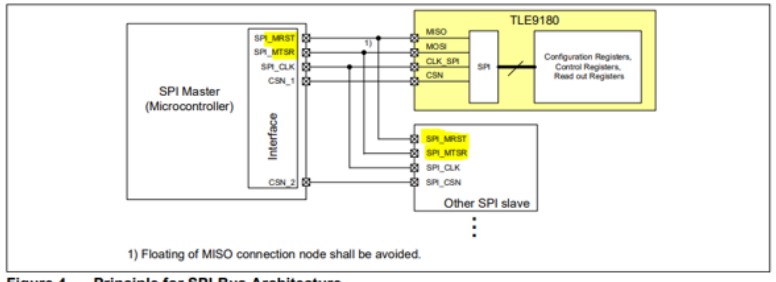
Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
3.1 Absolute Maximum Ratings Modification valid for all data sheets, except TLE9180D-26QK & TLE9183QK.	**Table 2 Absolute Maximum Ratings** (cont'd) Max. Voltage Transients at SHx | V_{ISH_tr1} | – | – | 20 | V | Slew rate ≤ 1 V/ns[7)1)] | P_4.3.31 1 Not subject to production test, specified by design 7 Exceeding specified slew rate in combination with the maximum specified voltage transient may set the affected output stage in an undefined state for typically 1 µs	**Table 2 Absolute Maximum Ratings** (cont'd) Max. Voltage Transients at SHx | V_{ISH_tr1} | – | – | 55 | V | Slew rate ≤ 1 V/ns[7)1)] | P_4.3.31 1 Not subject to production test, specified by design 7 At amplitudes higher than 20 V the HS output stage can show unexpected switch off of the external MOSFET for typically 1 µs if the output stage is not switching. If the output stage is switching on or switching off, the output stage is switching normally even with amplitudes up 55 V and slew rates up to 1 V/ns
4.7 Electrical Characteristics IOs	1) Not subject of production test, specified by design	1) Not subject to production test, specified by design.
4.7 Electrical Characteristics IOs Modification valid for all, except TLE9180D-26QK and TLE9183QK.	**Table 6 Electrical Characteristics IOs (continued)** **Pin ENA** ENA Propagation Time (for enable or disable the output stages) | t_{PENA} | – | 100 | – | ns | – | P_5.7.17	**Table 6 Electrical Characteristics IOs (continued)** **Pin ENA** ENA Propagation Time (for enable or disable the output stages) | t_{PENA} | – | 100 | 500 | ns | – | P_5.7.17
4.7 Electrical Characteristics IOs	**Table 6 Electrical Characteristics IOs (continued)** ~~High Level Output Voltage | V_{ERRH5b} | 3.8 | – | V_{VCC} | V | V_{VS} > 7.2 V; V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.24~~ Low Level Output Voltage | V_{ERRL} | -0.1 | – | 0.4 | V | I_{Load} = 0.2 mA | P_5.7.39 ~~High Level Output Voltage | V_{SPIH5b} | 3.8 | – | V_{VCC} | V | V_{VS} > 7.2 V; V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.57~~ Low Level Output Voltage | V_{SPIL} | -0.1 | – | 0.4 | V | I_{Load} = 0.2 mA | P_5.7.45	**Table 6 Electrical Characteristics IOs (continued)** Low Level Output Voltage | V_{ERRL} | -0.1 | – | 0.4 | V | I_{Load} = 0.2 mA | P_5.7.39 Low Level Output Voltage | V_{SPIL} | -0.1 | – | 0.4 | V | I_{Load} = 0.2 mA | P_5.7.45
4.7 Electrical Characteristics IOs Modification valid for TLE9180D-26QK only.	**Table 6 Electrical Characteristics IOs (continued)** High Level Output Voltage[30)] | V_{ERRH5a} | 3.3 | – | V_{VCC} | V | ~~5.5 V < V_{VS} < 7.2 V;~~ V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.38 High Level Output Voltage[30)] | V_{SPIH5a} | 3.3 | – | V_{VCC} | V | ~~5.5 V < V_{VS} < 7.2 V;~~ V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.44	**Table 6 Electrical Characteristics IOs (continued)** High Level Output Voltage[30)] | V_{ERRH5a} | 3.3 | – | V_{VCC} | V | V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.38 High Level Output Voltage[30)] | V_{SPIH5a} | 3.3 | – | V_{VCC} | V | V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.44

Change Overview TLE9180D

Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
4.7 Electrical Characteristics IOs Modification valid for all, except TLE9180D-26QK.	**Table 6 Electrical Characteristics IOs (continued)** High Level Output Voltage[7] | V_{ERRH5a} | 3.35 | – | V_{VCC} | V | ~~5.5 V ≤ V_S ≤ 7.2 V;~~ V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.38 High Level Output Voltage[7] | V_{SPIH5a} | 3.35 | – | V_{VCC} | V | 5.5 V ≤ V_S ≤ 7.2 V; V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.44	**Table 6 Electrical Characteristics IOs (continued)** High Level Output Voltage[31] | V_{ERRH5a} | 3.35 | – | V_{VCC} | V | V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.38 High Level Output Voltage[31] | V_{SPIH5a} | 3.35 | – | V_{VCC} | V | V_{VCC} = 5.0 V; I_{load} = -0.2 mA; All Digital I/Os = static | P_5.7.44
4.7 Electrical Characteristics IOs Change valid for all, except TLE9180D-26QK.	**Table 6 Electrical Characteristics IOs** (cont'd) High Level Output Voltage | V_{AOPH1} | 4.2 | 5.0 | 6.0 | V | I_{load} = -1 mA | P_5.7.47	**Table 6 Electrical Characteristics IOs** (cont'd) High Level Output Voltage | V_{AOPH1} | 3.9 | 5.0 | 6.0 | V | I_{load} = -1 mA | P_5.7.47
4.7 Electrical Characteristics IOs Change valid for TLE9180D-26QK only.	**Table 6 Electrical Characteristics IOs** (cont'd) High Level Output Voltage | V_{AOPH1} | 4.2 | 5.0 | 6.0 | V | I_{load} = -1 mA | P_5.7.47	**Table 6 Electrical Characteristics IOs** (cont'd) High Level Output Voltage | V_{AOPH1} | 3.7 | 5.0 | 6.0 | V | I_{load} = -1 mA | P_5.7.47
5 Serial Peripheral Interface - SPI	 **Figure 4 Principle for SPI-Bus Architecture**	 **Figure 4 Principle for SPI-Bus Architecture**
5.5 Electrical Characteristics SPI	**Table 7 Electrical Characteristics: Timing** T_j = -40°C to +165°C, V_S = 5.5 V to 60 V, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)	**Table 7 Electrical Characteristics: Timing** T_j = -40°C to +165°C, V_S = 5.5 V to 60 V, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified). Timings valid for 10 MHz operation.

Change Overview TLE9180D

Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
5.5 Electrical Characteristics SPI	**Table 7 Electrical Characteristics: Timing** CLK_SPI Operating Period | t_{SPI_clk} | 100 | – | – | ns | 2) Figure 6, C | P_6.5.2 CLK_SPI High Time | t_{SPI_wsclh} | 37 | – | – | ns | 2) Figure 6, A | P_6.5.3 CLK_SPI Low Time | t_{SPI_wsckl} | 37 | – | – | ns | 2) Figure 6, B | P_6.5.4 CLK_SPI Fall Time | t_{SPI_clkf} | – | – | 13 | ns | 2) Figure 6, D | P_6.5.5 2) Not subject to production test; verified by design or characterization; measured between 10% and 90%; output load capacitance on MISO pin is ≤ 25 pF	**Table 7 Electrical Characteristics: Timing** CLK_SPI Operating Period | t_{SPI_clk} | 100 | – | – | ns | 33) Figure 6, C | P_6.5.2 CLK_SPI High Time | t_{SPI_wsclh} | 37 | – | – | ns | 33) Figure 6, A | P_6.5.3 CLK_SPI Low Time | t_{SPI_wsckl} | 37 | – | – | ns | 33) Figure 6, B | P_6.5.4 33 Not subject to production test; verified by design or characterization; measured between 20% and 80%; output load capacitance on MISO pin is ≤ 25 pF
7.1 Output Stage Supply Concept	**7.1 Output Stage Supply Concept** fulfills the requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20 kHz PWM frequency. The charge pumps will be deactivated if the pin $\overline{INH}$ is set to low.	**7.1 Output Stage Supply Concept** fulfills the requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20 kHz PWM frequency. The charge pumps will be deactivated if the pin $\overline{INH}$ is set to low or a charge pump related error is detected. For details please check the supervision descriptions.
7.3 Electrical Characteristics Power Supply Modification not valid for TLE9183QK.	**Table 10 Electrical Characteristics: Power Supply** (cont'd) **Supply current in Reduced Operation Mode at Vs** Supply Current Vs | $I_{Vs(ROMVS)}$ | – | 12 | 20 | mA | $V_{Vs}=V_{VDHP}$=3V | P_8.3.36	**Table 10 Electrical Characteristics: Power Supply** (cont'd) Supply Current Vs | $I_{Vs(ROMVS)}$ | – | 12 | 24 | mA | $V_{Vs} = V_{VDHP}$ = 3 V | P_8.3.36
7.3 Electrical Characteristics Power Supply	**Table 10 Electrical Characteristics: Power Supply** (cont'd) Voltage Vs for Guaranteed Power-up of Charge Pumps | V_{VsWU} | 6.0 | – | – | V | – | P_8.3.38	**Table 10 Electrical Characteristics: Power Supply** (cont'd) Voltage Vs for ensured Power-up of Charge Pumps | V_{VsWU} | 6.0 | – | – | V | – | P_8.3.38
7.3 Electrical Characteristics Power Supply	2) Filter Time Accuracy referenced from internal clock accuracy, please see **Chapter 6.2**	87 Internal clock frequency accuracy has to be added to the specified values, please see ***Chapter 6.2***
8.4 Electrical Characteristics Floating MOSFET Driver	**Table 12 Electrical Characteristics MOSFET drivers (continued)** Propagation Delay Time (all low-side FETs off) | $t_{P(ILF)}$ | 30 | 35 | 70 | ns | R_{Load} = 2 kΩ 52); V_{Sxx} = 0 V | P_9.4.19 Propagation Delay Time (all high-side FETs off) | $t_{P(IHF)}$ | 30 | 35 | 70 | ns | R_{Load} = 2 kΩ 52); V_{Sxx} = 0 V | P_9.4.21	**Table 12 Electrical Characteristics MOSFET drivers (continued)** Propagation Delay Time (all low-side FETs off) | $t_{P(ILF)}$ | 25 | 35 | 70 | ns | R_{Load} = 2 kΩ 52); V_{Sxx} = 0 V | P_9.4.19 Propagation Delay Time (all high-side FETs off) | $t_{P(IHF)}$ | 25 | 35 | 70 | ns | R_{Load} = 2 kΩ 52); V_{Sxx} = 0 V | P_9.4.21

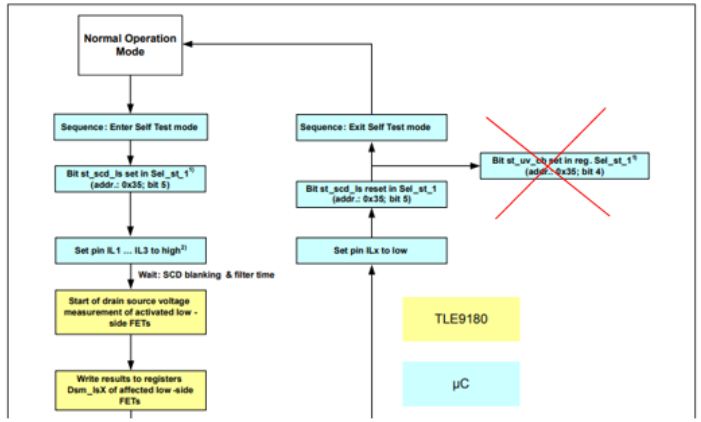
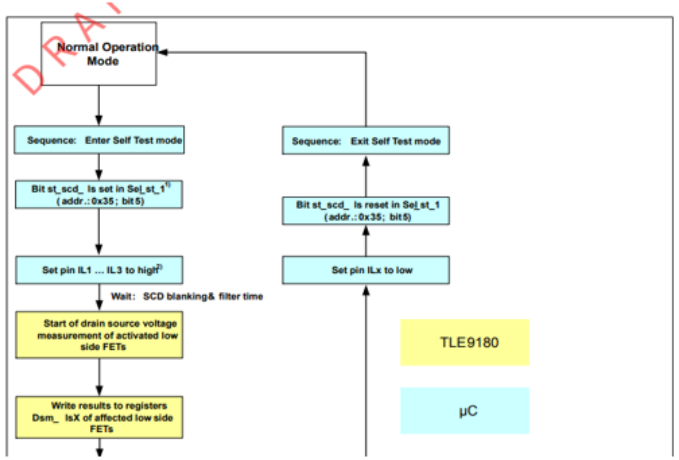
Change Overview TLE9180D

Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
9.5.1 Gain Test	**9.5.1 Gain Test** Gain test can only be activated in self-test mode, for details see ***Table 30***. Two different internal generated self-test voltages V_{SSC_GTILV} and V_{SSC_GTIHV} for gain test can be selected at the inputs of the CSAs. The input voltage V_{SSC_GTILV} is always applied to gain register 1 of the CSAs. The input voltage V_{SSC_GTIHV} is always applied to gain register 2 of the CSAs. It is recommended to use the gain register 2 only in the self-test mode for the gain test of the CSAs. By changing a dedicated bit sh_op_gain the gain of the CSA toggles between both gain register settings. Reading the bit will indicate which gain is selected. Toggling sh_op_gain will affect always all CSAs. The resulting output voltage shall be measured by the ADC of the µC and compared to the configured gain. The µC can rate if the CSA output voltage matches the programmed gain. Thereby, the accuracy of the gain, see A_{SSC_diff} AND G_{SSC_Gdacc}, the input offset voltage, see $V_{SSC\_Oofscal}$ or V_{SSC_Oofs} the accuracy of the self-test, see V_{SSC_GTILV} and V_{SSC_GTIHV} and the accuracy of the VRO output voltage, see V_{SSC_OVRO} have to be taken into account. Amplification of differential input voltage ISP - ISN is not possible for the CSA which is selected for gain test.	**9.5.1 Gain Test** DRAFT Gain test can only be activated in self-test mode, for details see ***Table 30***. Two different internal generated self-test voltages ***VSSC_GTILV*** and ***VSSC_GTIHV*** for gain test can be selected at the inputs of the CSAs. The input voltage ***VSSC_GTILV*** is always applied to gain register 1 of the CSAs. The input voltage ***VSSC_GTIHV*** is always applied to gain register 2 of the CSAs. By changing a dedicated bit sh_op_gain the gain of the CSA toggles between both gain register settings. Reading the bit will indicate which gain is selected. Toggling sh_op_gain will affect always all CSAs. The resulting output voltage shall be measured by the ADC of the µC and compared to the configured gain. The µC can rate if the CSA output voltage matches the programmed gain. Thereby, the accuracy of the gain, see ***ASSC_diff*** AND ***GSSC_Gdacc***, the input offset voltage, see ***VSSC_Oofscal*** or ***VSSC_Oofs*** the accuracy of the self-test, see ***VSSC_GTILV*** and ***VSSC_GTIHV*** and the accuracy of the VRO output voltage, see ***VSSC_OVRO*** have to be taken into account. Amplification of differential input voltage ISP - ISN is not possible for the CSA which is selected for gain test.
9.6 Electrical Parameter Shunt Signal Conditioning (SSC) Modification valid for TLE9180D-26QK only.	**Table 20 Electrical Characteristics - Reference Buffer** Negative Trim Range VRO | $V_{SSC\_OVRO\_TRN}$ | -7.0 / -2.8 / -3.6 | – | -5.7 / -2.3 / -3.0 | % of $V_{OVRO@ofs='0x20'}$ | zcl = '0b00'; zcl = '0b01'; zcl = '0b10'; @ ofs = '0x00' | P_9.6.52	**Table 20 Electrical Characteristics - Reference Buffer** Negative Trim Range VRO | $V_{SSC\_OVRO\_TRN}$ | -7.0 / -2.8 / -3.7 | – | -5.7 / -2.3 / -3.1 | % of $V_{OVRO@ofs='0x20'}$ | zcl = '0b00'; zcl = '0b01'; zcl = '0b10'; @ ofs = '0x00' | P_9.6.52
10.1 Supervision Overview Modification valid for TLE9183QK only.	**Table 21 Diagnostic overview** Overvoltage VS (Programmable Threshold) | yes (default value) | no[2] | yes | no | ***Table 25*** | ***Chapter 10.5.1*** Overvoltage VS shutdown | yes | no[2] | yes | no | ~~***Table 24***~~ | ***Chapter 10.5.1*** Undervoltage VS (Programmable Threshold) | yes (default value) | no[2] | yes | no | ***Table 25*** | ***Chapter 10.5.1***	**Table 21 Diagnostic overview** Overvoltage VS (Programmable Threshold) | yes (default value) | no[56] | yes | no | ***Table 25*** | ***Chapter 10.5.1*** Undervoltage VS (Programmable Threshold) | yes (default value) | no[56] | yes | no | ***Table 25*** | ***Chapter 10.5.1***
	10.5.1 Vs Voltage Monitoring The Vs supply voltage is monitored (under- and overvoltage detection). The threshold, the error reaction and the filter time can be adjusted via SPI. ~~Additionally to the overvoltage detection a maximum overvoltage threshold, the so called overvoltage shutdown, is set to signalize the µC that a maximum rating violation might has been occurred at the pin Vs. The failure behavior and the threshold of the shutdown is not adjustable. The shutdown failure behavior is fix as a latched error.~~ Register Err_sd bit 6 indicates overvoltage Vs shutdown and register Err_e bit 3 and bit 2 for undervoltage and overvoltage detection at pin Vs. Additionally the VS voltage is stored in register res_vs and can be read out via SPI.	**10.5.1 Vs Voltage Monitoring** The Vs supply voltage is monitored (under- and overvoltage detection). The threshold, the error reaction and the filter time can be adjusted via SPI. Register Err_sd bit 6 indicates overvoltage Vs shutdown and register Err_e bit 3 and bit 2 for undervoltage and overvoltage detection at pin Vs. Additionally the VS voltage is stored in register res_vs and can be read out via SPI.

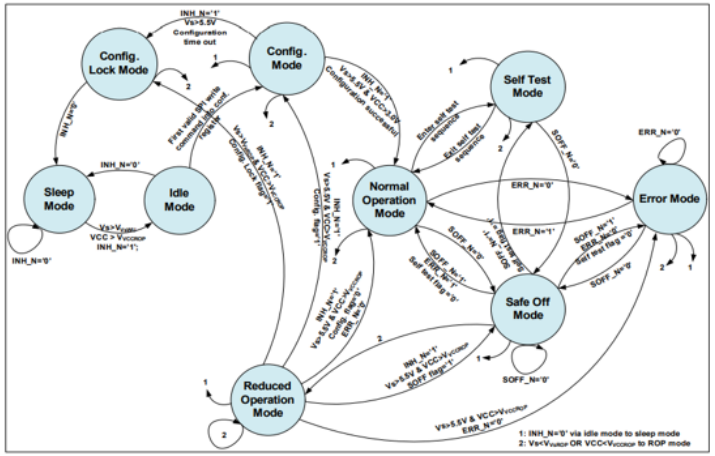
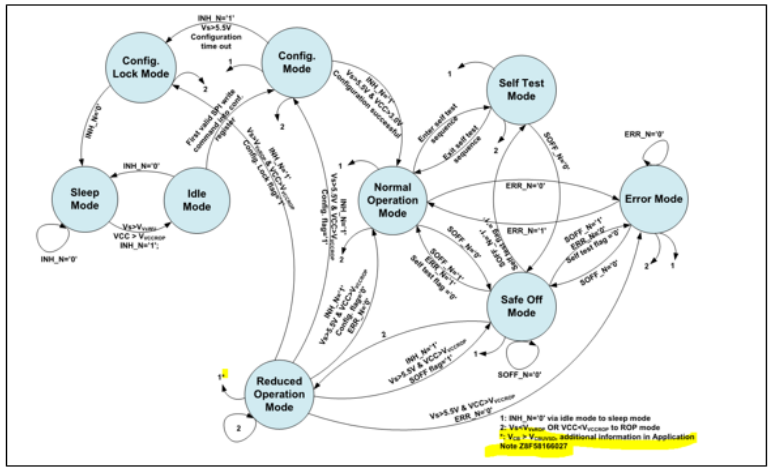
Change Overview TLE9180D

Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
10.2.2 Failure Behavior Configuration	**Table 24 Shutdown Error Overview[1)]** 22 **Bit Position** | **Bit Name** | **Description** | **Output Stages** | **Charge Pumps** | **$\overline{\text{ERR}}$ Pin** 3 | sd_clk_fail | Internal Clock Supervision Shutdown[80)] | ARE | Active | Low (LE) 80 In the case of monitoring clock stops operation fault reaction of output stages is latched error	**Table 24 Shutdown Error Overview[1)]** **Bit Position** | **Bit Name** | **Description** | **Output Stages** | **Charge Pumps** | **$\overline{\text{ERR}}$ Pin** 3 | sd_clk_fail | Internal Clock Supervision Shutdown[80)] | ARE or LE | Active | Low (ARE or LE) 80 Failure reaction can be ARE or LE dependent on type of internal fault
10.2.2 Failure Behavior Configuration	**Table 24 Shutdown Error Overview[78)]** **Bit Position** | **Bit Name** | **Description** | **Output Stages** | **Charge Pumps** | **$\overline{\text{ERR}}$ Pin** 4 | sd_uv_cb | Undervoltage CB Shutdown | ARE | Active | Low (LE)	**Table 24 Shutdown Error Overview[78)]** **Bit Position** | **Bit Name** | **Description** | **Output Stages** | **Charge Pumps** | **$\overline{\text{ERR}}$ Pin** 4 | sd_uv_cb | Undervoltage CB Shutdown | ARE | Active | Low (ARE)
10.5.16 Overload Digital Output Pins	**10.5.16 Overload Digital Output Pins** The digital outputs are protected against short to GND and battery. If one output is shorted the output pad will be disconnected, a dedicated error register bit will be set. The pin $\overline{\text{ERR}}$ will be set to low. To unlock the output pin reset with ENA has to be performed. The failure behavior of the gate driver IC is adjustable at configuration mode, either the output stages will turn all external FETs off or not. Functionality of the overload detection of the digital output pins is limited, for details please refer to **Chapter 16.3.8**. Register **Err_outp** bit 4 to bit 0 indicate a short of a digital output pin.	**10.5.16 Overload Digital Output Pins** The digital outputs are protected against short to GND and battery. If one output is shorted the output pad will be disconnected, a dedicated error register bit will be set. The pin $\overline{\text{ERR}}$ will be set to low in case pin $\overline{\text{ERR}}$ is not the affected pin. To unlock the output pin reset with ENA has to be performed. The failure behavior of the gate driver IC is adjustable at configuration mode, either the output stages will turn all external FETs off or not. Functionality of the overload detection of the digital output pins is limited, for details please refer to ***Chapter 16.3.7***. Register ***Err_outp*** bit 4 to bit 0 indicate a short of a digital output pin.
10.5.4 High-side Buffer Capacitor Voltage Monitoring	**10.5.4 High-side Buffer Capacitor Voltage Monitoring** An overvoltage monitoring for the external high-side buffer capacitor guarantees gate source voltage for the external FET not higher as the destructive gate source voltage. Failure behavior and filter time is not configurable. High-side buffer overvoltage monitoring can be deactivated at configuration if diagnosis is not required. In case of overvoltage detection all output stages remain active but charge pump 2 will be deactivated. A reset via ENA is necessary for reactivation of charge pump 2. If overvoltage high-side buffer has been detected and charge pump 2 has been turned off duty cycle operation higher than 95% is not recommended and might end up in undervoltage high-side buffer detection.	**10.5.4 High-side Buffer Capacitor Voltage Monitoring** An overvoltage monitoring for the external high-side buffer capacitor detects too high gate source voltages for the external FET. The failure behavior and filter time are not configurable. In case of an overvoltage detection, the ERR pin is set low and the dedicated error bit in the register is set. The 2nd charge pump is deactivated and all output stages remain active. A reset via ENA is necessary for the reactivation of the 2nd charge pump. If the 2nd charge pump is deactivated, an undervoltage high-side buffer detection might occur mainly at operation with high duty cycles. The overvoltage monitoring for the external high-side buffer capacitor can be deactivated at configuration.

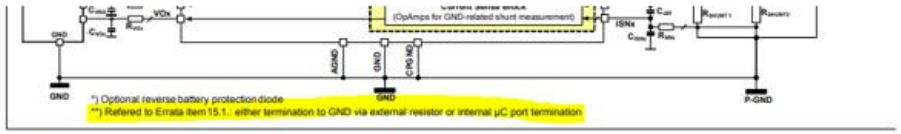
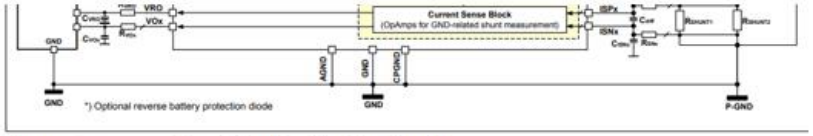
Change Overview TLE9180D

Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
10.5.11.2 Self-test Function for SCD Change valid for all, except TLE9183QK.	 **Figure 27** Recommended Sequence for Self Test Short Circuit Detection Low-side	 **Figure 27** Recommended Sequence for Self Test Short Circuit Detection Low-side
10.6 Electrical Characteristics Protection and Diagnostic Functions Modification valid for all data sheets, except TLE9180D-26QK.	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Accuracy Undervoltage Threshold Vs | $V_{VSUVacc2}$ | -13.5 | PROG | +13.5 | % | 4.4 V ≥ V_{VSUV} < 7.5 V | P_11.6.12	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Accuracy Undervoltage Threshold Vs | $V_{VSUVacc2}$ | -13.5 | PROG | +13.5 | % | 4.2 V ≤ V_{VSUV} < 7.5 V | P_11.6.12
10.6 Electrical Characteristics Protection and Diagnostic Functions Modification valid for TLE9180D-26QK only.	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Accuracy Undervoltage Threshold Vs | $V_{VSUVacc2}$ | -17.5 | PROG | +17.5 | % | 4.4 V ≥ V_{VSUV} < 7.5 V | P_11.6.12	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions** (cont'd) Accuracy Undervoltage Threshold Vs | $V_{VSUVacc2}$ | -17.5 | PROG | +17.5 | % | 4.0 V ≤ V_{VSUV} < 7.5 V | P_11.6.12
10.5 Electrical Characteristics Protection and Diagnostic Functions Modification valid for TLE9183QK only, other data sheets already updated.	**VCC Read Out** Voltage Detection Range | V_{ADCr} | 0 | – | 5.554 | V | 0 to FFh | P_11.6.86	**VCC Read Out** Voltage Detection Range | V_{ADCr} | 0 | – | 5.55 | V | 0 to FFh | P_11.6.86

Change Overview TLE9180D

Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
10.6 Electrical Characteristics Protection and Diagnostic Function	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions (continued)** Entry Filter and Reaction Time of Reduced Operation Mode Detection at VCC — $V_{VCCROPf1}$ — 0.6 – – µs — 87) — P_11.6.78 Exit Filter and Reaction Time of Reduced Operation Mode Detection at VCC — $V_{VCCROPf2}$ — 20 – – µs — 87) — P_11.6.79 Temperature Read Out Accuracy — t_{Tread_f} — -28 – +28 K – P_11.6.115	**Table 53 Electrical Characteristics - Protection and Diagnostic Functions (continued)** Entry Filter and Reaction Time of Reduced Operation Mode Detection at VCC — $t_{VCCROPf1}$ — 0.6 – – µs — 87) — P_11.6.78 Exit Filter and Reaction Time of Reduced Operation Mode Detection at VCC — $t_{VCCROPf2}$ — 20 – – µs — 87) — P_11.6.79 Temperature Read Out Accuracy — T_{Tread_a} — -28 – +28 K – P_11.6.115
11.2 Electrical Parameter Phase Feedback Modification valid for all data sheets, except TLE9183QK.	**Table 55 Electrical Characteristics - Phase Feedback** Propagation Delay Time — t_{PDfb} — – — 60 100 — 70 100 — ns — 50%/50% selected 80%/25% selected — P_12.2.6	**Table 55 Electrical Characteristics - Phase Feedback** Propagation Delay Time — t_{PDfb} — – — 60 110 — 70 110 — ns — 50%/50% selected 80%/25% selected — P_12.2.6
11.2 Electrical Parameter Phase Feedback Modification valid for TLE9183QK only.	**Table 55 Electrical Characteristics - Phase Feedback** Propagation Delay Time — t_{PDfb} — – — 60 — 100 — ns — P_12.2.6	**Table 55 Electrical Characteristics - Phase Feedback** Propagation Delay Time — t_{PDfb} — – — 60 — 110 — ns — P_12.2.6
13 Operation Modes	 **Figure 31 Overview of Digital Operation Modes**	 **Figure 31 Overview of Digital Operation Modes**

Change Overview TLE9180D

Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
16.3.10 Reduced Operation Mode INH set to low Modification valid for all data sheets, except TLE9180D-26QK & TLE9183QK.		**16.3.10 Reduced Operation Mode INH set to low** In Reduced Operation Mode if INH is set to „low" if $V_{CB} < V_{CBUVSD}$, Sleep Mode might not be entered. For additional information please refer to TLE9180 Application Note „Reduced Operation Mode INH set to low".
16 Application Information Modification valid for all data sheets, except TLE9180D-26QK.	 **Figure 36 Simplified Application Circuit**	 **Figure 36 Simplified Application Circuit**
16.2.1 Additional Components Modification valid for all data sheets, except TLE9180D-26QK and TLE9183QK.	[6] D3 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs. The effect can be avoided with sufficient input filtering with C_{Vs} and (R_{Vs} or D1).	[8] D3 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs with a slew rate ≥ 6V/100µs. D3 is not required with sufficient filtering at the Vs pin. In case D3 is not used a 100 kΩ pull down to GND at CL1 shall be placed.
16.2.1 Additional Components Modification valid for all data sheets, except TLE9180D-26QK and TLE9183QK.	[4] D4 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after CB capacitor has been shorted to GND.	[4] D4 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data.
16.2.1 Additional Components Modification valid for all data sheets, except TLE9180D-26QK and TLE9183QK.	[3] D2 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin V_s. Voltage drops at pin Vs in the range from 13V down to 6V shall not be shorter than 100µs. In the case of faster slew reates an input filter is required. For details please contact Infineon.	[3] D2 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs with a slew rate ≥ 6V/100µs. D2 is not required with sufficient input filtering at the Vs pin.

Change Overview TLE9180D

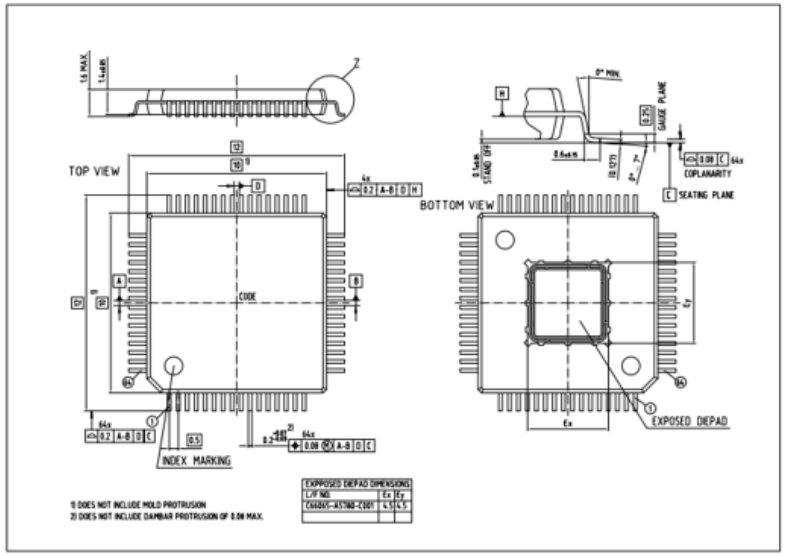
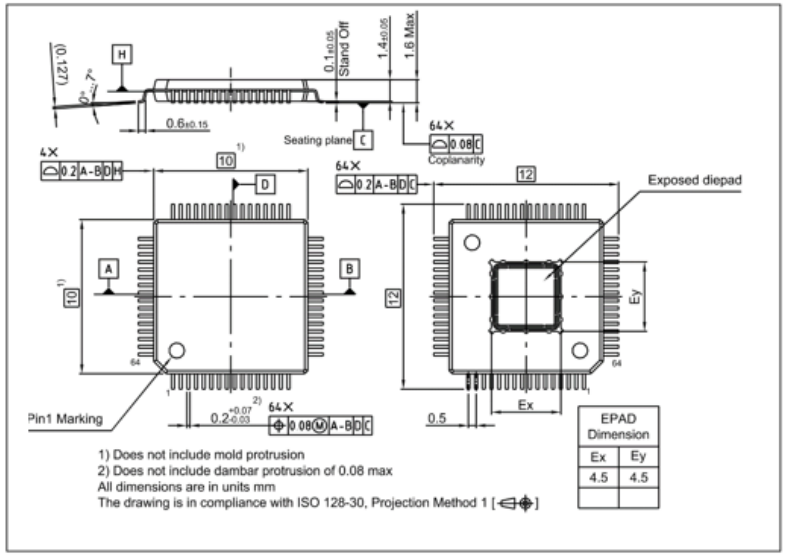
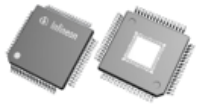
Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
17 Package Outlines Modification valid for TLE9180D-26QK only.	**17 Package Outlines**  **Figure 38 PG-LQFP-64**	**17 Package Outlines**  **Figure 38 PG-LQFP-64**
Front page Modification valid for TLE9180D-26QK only.		

Table of contents

Data sheets and Safety documentation

› MyICP links to the Infineon data base

Sales Code	Datasheet folder	Safety documentation folder
TLE9180-20QK	Infineon-TLE9180-20QK-DS-v01_80-EN	for TLE9180-20QK
TLE9180-21QK	Infineon-TLE9180-21QK-DS-v01_80-EN	for TLE9180-21QK
TLE9180C-21QK	Infineon-TLE9180C-21QK-DS-v01_10-EN	for TLE9180C-21QK and TLE9180C-31QK
TLE9180C-31QK	Infineon-TLE9180C-31QK-DS-v01_10-EN	
TLE9180C-20QK	Infineon-TLE9180C-20QK-DS-v01_10-EN	for TLE9180C-20QK
TLE9180D-21QK	Infineon-TLE9180D-21QK-DS-v01_20-EN	for TLE9180D-21QK and TLE9180D-31QK
TLE9180D-31QK	Infineon-TLE9180D-31QK-DS-v01_20-EN	
TLE9180D-26QK	Infineon-TLE9180D-26QK-DS-v01_10-EN	for TLE9180D-26QK
TLE9180D-32QK	Infineon-TLE9180D-32QK-DS-v01_10-EN	for TLE9180D-32QK
TLE9183QK	Infineon-TLE9183QK-DS-v01_10-EN	for TLE9183QK

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