

Product/Process Change Notification

N° 2021-080-A

Dear customer,

please find attached our Infineon Technologies AG PCN:

Datasheet update for products TLE9180x and TLE9183QK

Important information for your attention:

- Please respond to this PCN by indicating your decision on the approval form, sign it and return to your sales partner before 2021-08-02.
- Infineon aligns with the widely-recognized JEDEC STANDARD "JESD46", which stipulates: "Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change." Notwithstanding the aforesaid individual agreements shall prevail.

Your prompt reply will help Infineon to assure a smooth and well-executed transition. If Infineon does not hear from your side by the due date, we will assume your full acceptance to this proposed change and its implementation.

Your attention and response to this matter is greatly appreciated.



On 16 April 2020, Infineon acquired Cypress. We are now in the process of merging and consolidating our tools and processes for PCN, Information Notes, Errata and Product Discontinuance. We ask for your patience in the meantime. For further details, please visit our website: https://www.infineon.com/cms/en/about-infineon/company/cypress-acquisition/

Infineon Technologies AG

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Product/Process Change Notification

N° 2021-080-A

Products affected	Please refer to attached affected product	t list 1_cip21080_A
Detailed change information		
Subiect:	Datasheet update for products TLE9180x	and TLE9183QK
Reason/Motivation:	Datasheet update.	
Description	Old	New
Description		
	TLE9180-xxQK: datasheet rev. 1.72	TLE9180-xxQK: datasheet rev. 1.80
DATA SHEET: Change of datasheet	TLE9180C-xxQK: datasheet rev. 1.01	TLE9180C-xxQK: datasheet rev. 1.10
parameters/electrical specification	TLE9180D-x1QK: datasheet rev. 1.10	TLE9180D-x1QK: datasheet rev. 1.20
(min./max./typ. values) and/or AC/DC	TLE9180D-26QK: datasheet rev. 1.01	TLE9180D-26QK: datasheet rev. 1.10
specification	TLE9180D-32QK: datasheet rev. 1.01	TLE9180D-32QK: datasheet rev. 1.10
	TLE9183QK: datasheet rev. 1.01	TLE9183QK: datasheet rev. 1.10
Product identification	Not applicable (for documentation only)	
	Not applicable (for documentation only)	
Anticipated impact of change	No change of product (neither of technol	logy/package nor of chip design), only
	change of datasheet.	
	DeQuMa-ID(s): SEM-DS-01	
Attachments	1_cip21080_A	affected product list
Attachiments		
	3_cip21080_A	customer information package
Time schedule		
	Not applicable (for documentation only)	
rinal qualification report		

First samples available	Not applicable (for documentation only)
Intended start of delivery [1]	Not applicable (for documentation only)

[1] Provided date or earlier after customer approval

If you have any questions, please do not hesitate to contact your local sales office.

Datasheet update for products TLE9180x and TLE9183QK

Customer Information Package PCN 2021-080-A





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Motivation of the change

- > Infineon has reviewed all datasheets (DS) for the product family TLE9180x and TLE9183QK.
 - TLE9180-20QK, TLE9180-21QK
 - TLE9180C-20QK, TLE9180C-21QK, TLE9180C-31QK
 - TLE9180D-21QK, TLE9180D-31QK, TLE9180D-32QK
 - TLE9180D-26QK
 - TLE9183QK
- Several changes are required due to different aspects. The changes are listed in the revision history of each data sheet and on the following pages (see next sections) for better readability.
- > The datasheets are accessible via the links listed at the end in section <u>5</u>.

Sales Type	Old DS	New DS
TLE9180-xxQK	Rev. 1.72	Rev. 1.80
TLE9180C-xxQK	Rev. 1.01	Rev. 1.10
TLE9180D-x1QK	Rev. 1.10	Rev. 1.20
TLE9180D-26QK	Rev. 1.00	Rev. 1.10
TLE9180D-32QK	Rev. 1.01	Rev. 1.10
TLE9183QK	Rev. 1.01	Rev. 1.10





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Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
4.1 Absolute Maximum Ratings	Table 1 Absolute Maximum RatingsSupply Voltage for Power-up ¹⁾ V_{Vs3} 30V-P_4.1.7Supply Voltage V_{Vs3} 5.5-60VThermally limitedP_4.3.1	Table 1 Absolute Maximum RatingsSupply Voltage for Power-up ¹⁰ V_{Vs6} $ 30$ V $-$ P_4.1.7Supply Voltage V_{Vs3} 5.5 $ 60$ VThermally limitedP_4.3.1
	Table 1 Absolute Maximum Ratings (cont'd) $T_j = -40$ °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) Voltage Difference SHx-SLx ¹⁾ V_{SSx1}	Table 1 Absolute Maximum Ratings T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) Voltage Difference SHx-SLx ¹⁾ V_{SSx1} -12 - 90 V - P_4.1.29
4.1 Absolute Maximum Ratings	Voltage Difference SHx-SLx ¹) V_{SSx1} -7 90 V - P_4.1.29 Voltage Difference SHx-SLx ¹) V_{SSx2} -10 - V 10) P_4.1.30 Voltage Difference SHx-SLx ¹) V_{SSx2} -10 - V 10) P_4.1.30 Voltage Difference SHx-SLx ¹) V_{SSx3} -15 - V 6) P_4.1.31 Voltage Difference VDHP-SHx $V_{dVDHPSHx2}$ -90 - 85 V en_vdh3=0x1 (cfg.:3 P_4.1.32 VDHx pins enabled) VDHx pins enabled) - - 85 V NDHx pins enabled)	Voltage Difference SHx-SLx ¹⁾ V -12 - 90 V - P_4.1.29 Voltage Difference VDHP-SHx V V - 85 V en_vdh3=0x1 (cfg.: 3) P_4.1.32
4.1 Absolute Maximum Ratings Modification valid for: TLE9180-21QK	Table 1 Absolute Maximum Ratings (cont'd) Voltage Range APC V _{AOP1} -0.3 - 60 V - P_4.1.39	Table 1 Absolute Maximum Ratings (cont'd) Voltage Range APC V _{AOP1} -0.3 - 60 V 10) 10) A short circuit at APC for > 10 hrs might damage the device
4.1 Absolute Maximum Ratings	Table 1 Absolute Maximum Ratings (cont'd) Temperatures Storage Temperature T _{stg} -55 - 150 °C - P_4.1.54 Junction Temperature T _{J1} -40 - 150 °C - P_4.1.55 Junction Temperature T _{J2} 40 176 °C 200h over lifetime P_4.1.56	Table 1 Absolute Maximum Ratings (cont'd) Temperatures Temperature T_{slg} -55 - 150 °C - P_4.1.54 Junction Temperature T_{J1} -40 - 150 °C 120 P_4.1.55 12) For T_j >150°C please check compliance with the IFX qualification - 150 °C 120 P_4.1.55
4.2 Thermal Resistance Modification done in: TLE9180-20QK & TLE9180-21QK	Table 2 Thermal Resistance 2) Specified R _{thUA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.	Table 2 Thermal Resistance 2) Specified R _{thuk} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.



Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
5.7 Electrical Characteristics IOs	1) Not subject of production test, specified by design	1) Not subject to production test, specified by design.
5.7 Electrical Characteristics IOS Modification valid for the TLE9180-21QK	Table 5 Electrical Characteristics IOs High Level Output Voltage V _{AOPH1} 4.2 5.0 6.0 V I _{load} = -1 mA P_5.7.47	Table 5 Electrical Characteristics IOs High Level Output Voltage V _{AOPH1} 3.9 5.0 6.0 V I _{load} = -1mA P_5.7.47
6 Serial Peripheral Interface - SPI	SPI Master (Microcontroller) (Microcontroller) (Microcontroller)) Floating of MISO connection node shall be avoided.	SPI Master (Microcontroller))) Fibating of MISO connection node shall be avoided. Figure 4 Principle for SPI-Bus Architecture
6.4 Cyclic Redundancy Check - CRC Generation and Detection	6.4 Cyclic Redundancy Check - CRC Generation and Detection The CRC is added to any data transmitted. It is calculated for the whole SPI frame, CRC bits excluded. The CRC check for incoming data is performed over the complete SPI frame.	6.4 Cyclic Redundancy Check - CRC Generation and Detection The CRC is added to any data transmitted. It is calculated for the whole SPI frame. CRC bits excluded. The CRC check for incoming data is performed over the complete SPI frame. In case of a CRC3 Error Detection on the MISO line by the µC, the message should be discarded and the register access should be repeated.
6.5 Electrical Characteristics SPI	Table 6 Electrical Characteristics: Timing (cont'd) Sequential Transfer Delay ³) Image: Sequential Transfer Delay ³ Image: Sequentia	Table 6 Electrical Characteristics: Timing (cont'd) Sequential Transfer Delay ³⁾ I _{SPLM} 330 - - ns ²⁾ Figure 6, N P_6.5.19
6.5 Electrical Characteristics SPI	Table 6 Electrical Characteristics: Timing SPI Data Output (MISO) Lag $l_{SPL,lag1}$ 0 - ns 21 Figure 6, M P_6.5.15 Enable (SS) Lag Time $l_{SPL,lag2}$ 25 - - ns 21 Figure 6, M P_6.5.18	Table 6 Electrical Characteristics: Timing (cont'd) Enable (SS) Lag Time If april lag 25 - Ins 2) Figure 6, M P_6.5.15
6.5 Electrical Characteristics SPI	Table 6 Electrical Characteristics: Timing $T_j = -40$ °C to +150 °C, $V_S = 5.5$ V to 60 V and with respect to ground, positive current flowing into pin (unless otherwise specified). Parameter Symbol Values Unit Note / Number SPI Operating Frequency $f_{SPL_{CR}}$ $-^{11}$ $-$ 10 MH 2^2 P_6.5.1	Table 6 Electrical Characteristics: Timing $T_j = -40$ °C to +150 °C, $P_g = 5.5$ V to 60 V and with respect to ground, positive current flowing into pin (unless otherwise specified). Timings valid for 10 MHz operation. Values Unit Note / Number Parameter Symbol Values Unit Note / Test Condition Number SPI Operating Frequency $f_{SPL ck}$ $-^{10}$ $-$ 10 MHz 2^{2} P_6.5.1



Datasheet Chapter	TLE91	80-20QK D	S V1.72	TLE918)-21Q	K DS V1.72		TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
5.5 Electrical Characteristics SPI	CLK_SPI High Time CLK_SPI Low Time	l _{SPI_dk} 10 l _{SPI_weckth} 37 l _{SPI_wecktl} 37 l _{SPI_dkf} -	-	- - 13	ns ² ns ² ns ²	⁹ Figure 6, A F ⁹ Figure 6, B F ⁹ Figure 6, D F	P_6.5.2 P_6.5.3 P_6.5.4 P_6.5.5	Table 6 Electrical Characteristics: Timing CLK_SPI Operating Period $I_{SPI, dk}$ 100 - - ns 21 Figure 6, C P_6.5.2 CLK_SPI High Time $I_{SPI, dk}$ 37 - - ns 21 Figure 6, A P_6.5.3 CLK_SPI Low Time $I_{SPI, dkd}$ 37 - - ns 21 Figure 6, B P_6.5.4 CLK_SPI Low Time $I_{SPI, dkd}$ - - ns 21 Figure 6, D P_6.5.5 CLK_SPI Fall Time $I_{SPI, dkd}$ - - 13 ns 21 Figure 6, D P_6.5.5 2) Not subject to production test; verified by design or characterization; measured between 20% and 80%; output loa capacitance on MISO pin is ≤ 60pF.
8.1 Output Stage Supply Concept	8.1 Output Stage Su requirement to drive the external FE frequency. The charge pumps will be deactivate	Ts within a F	WM spec				at 20kHz PWM	8.1 Output Stage Supply Concept requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20kHz PWM frequency. The charge pumps will be deactivated if the INH pin is set to low or a charge pump related error is detected. For details please check the supervision descriptions.
8.3 Electrical Characteristics Power Supply <u>Modification done in:</u> <u>TLE9180-20QK & TLE9180-21QK</u>		IavDHx2	- 50 - 50	rd) 200 200	nA	$\begin{split} & V_{\text{VDHP}} \leq 14\text{V}; \\ & T_{\text{s}} \leq 25^{\circ}\text{C}; \\ & V_{\text{INH}} = V_{\text{SOFF}} = \text{GND}^{15}; \\ & V_{\text{SHx}} = \text{GND} \\ & V_{\text{VDHF}} \leq 660\text{V}; \\ & T_{\text{s}} \leq 25^{\circ}\text{C}; \\ & V_{\text{NH}} = V_{\text{SOFF}} = \text{GND}^{15}; \\ & V_{\text{SHx}} = \text{GND} \end{split}$	P_8.3.31 P_8.3.32	Table 9 Electrical Characteristics: Power Supply (cont'd)Quiescent Current VDHx I_{OVDHo2} -50200nA $V_{VDHP}=514V$; $V_{DHH}=1 \text{ sport}=6ND^{19}$; $V_{DHP}=2 \text{ sport}=6ND^{19}$; $V_{DHH}=1 \text{ sport}=6ND^{19}$; $V_{DHH}=6ND$ P_8.3.31Quiescent Current VDHx I_{OVDHo1} -50200nA $V_{VDHP}=600$; $V_{SHH}=6ND$ P_8.3.32Quiescent Current VDHx I_{OVDHo1} -50200nA $V_{VDHP}=600$; $V_{SHH}=6ND$ P_8.3.32
	Table 9 Electrical Characteria Quiescent Current VDHP	I _{QVDH1}	Supply (co	ont'd) 60	μΑ	V_{VDHP} \$60V; T_{j} \$25°C; V_{NH} V_{SOFF} = GND ¹⁵ ; V_{SH4} = GND	P_8.3.48	$\label{eq:constraint} \hline \begin{array}{ c c c c } \hline Table 9 & Electrical Characteristics: Power Supply (cont'd) \\ \hline \hline Quiescent Current VDHP & I_{QVDH1} & - & - & 60 & \mu A & V_{VDHP} \leq 60V; \\ \hline T_{\leq 2} \leq 5C; \\ T_{\leq 2} \leq C; \\ T_{State} = GND^{10}; \\ T_{State} = GND^{10}; \\ \end{array} $
8.3 Electrical Characteristics	Quiescent Current VDHP	I _{QVDH1}		60	Αц	V _{VDHP} ≤60V; Tj≤150°C; V _{INH} =V _{SOFF} =GND ¹⁵); V _{SH4} =GND	P_8.3.30	Quiescent Current VDHP Iovore - - 60 μA V _{VDHP} ≤60V; T[≤150°C; V _{DHP} =V _{SOFF} =GND ¹⁵); P_8.3.30
Power Supply	Total Quiescent Current Vs and VDHP, VDHx ¹⁶⁾	I _{Q2}	42	12	μA	$\begin{split} & V_{\text{VS}} = V_{\text{VDHP}} \leq 14\text{V}; \\ & T_{j} = 25^{\circ}\text{C}; \\ & V_{\text{INH}} = V_{\text{SOFF}} = \text{GND}^{15}; \\ & V_{\text{SHx}} = \text{GND} \end{split}$	P_8.3.49	Total Quiescent Current Vs and VDHP, VDHx ¹⁶⁾ I μA V _{VS} =V _{VOHP} S14V; V _{INH} =V _{SOFP} S14V;
	Total Quiescent Current Vs and VDHP, VDHx ¹⁶⁾		>	55	μA	$\begin{split} & V_{\rm VS} = V_{\rm VDHP} \le 14 {\rm V}; \\ & T_{\rm } = 150^{\circ}{\rm C}; \\ & V_{\rm INH} = V_{\rm SOFF} = {\rm GND}^{15}; \\ & V_{\rm SHz} = {\rm GND} \end{split}$	P_8.3.33	Total Quiescent Current Vs and I_{Q2} 55 μA $V_{V_3} = V_{V_0 HP} > 14V;$ P_8.3.33 $T_j = 150^{\circ}C;$ $V_{U_0 HP} = GND^{15};$ $V_{Stat} = GND$



Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80						
	Table 9 Electrical Characteristics: Power Supply (cont'd)	Table 9 Electrical Characteristics: Power Supply (cont'd)						
	Quiescent Current VDHP I_{QVDH1} 60 μA $V_{VDHP} \le 60V;$ $T \le 25^{\circ}C;$ $V_{NNI} = V_{SOFF} = GND^{10};$ P_8.3.48	Quiescent Current VDHP $I_{QVDH1} = -$ 60 $\mu A = V_{VDHP} = 560V;$ $T_{j} \le 25^{\circ}C;$ $V_{NH} = F_{SOFF} = GND^{10};$ $I_{SHH} = GND$						
8.3 Electrical Characteristics	Quiescent Current VDHP I_{QVDH1} - - 60 μA $V_{VDHP} \le 60V;$ P_8.3.30 $T_{j} \le 150^{\circ}C;$ $V_{RH} = V_{SOFF} = GND^{15};$ $V_{SHI} = GND$ - -	Quiescent Current VDHP I - - 60 μA I V _{VDIP} =660V; T[5150*C; V ₁₉₆₄ =V _{50PF} =GND ¹⁵⁰ ; P_8.3.30						
Power Supply	Total Quiescent Current Vs and I_{Q2} 12 $\mu A = V_{VOHP} \leq 14V;$ VDHP, VDHx ¹⁰) $P_{aa} = 0$ $V_{VOHP} \leq 14V;$ $V_{T_{i}} = 25^{\circ}C;$ $V_{BH} = V_{SOFF} = GND^{15};$ $V_{SHX} = GND$	Total Quiescent Current Vs and I_{Q1} 12 μA $V_{VS} = V_{VDHP} \le 14V;$ VDHP, VDHx ¹⁶) P_8.3.49 $T_{j}^{-25'C};$ $V_{NPA} = GND^{16};$ P_8.3.49						
	Total Quiescent Current Vs and I_{Q2} 55 $\mu A = V_{VOH2} + V_{VOH2} + 14V;$ VDHP, VDHx ¹⁶) $V_{DH2} + V_{VOH2} + $	Total Quiescent Current Vs and I_{C2} 55 μ A $V_{VS} = V_{VDHP} \le 14V;$ P_8.3.33 $V_{DHP} = V_{DHP} = 10^{16};$ $V_{SDHP} = GND^{16};$ $V_{SDHP} = GND^{16};$ $V_{SDHP} = GND^{16};$						
	Table 9 Electrical Characteristics: Power Supply 4) Accuracy derived from digital clock, for details please see Table 8	Table 9 Electrical Characteristics: Power Supply 4) Internal clock frequency accuracy has to be added to the specified values, please see Table 8						
	 4) Accuracy derived from digital clock, for details please see Table 8 Table 11 Electrical Characteristics MOSFET drivers Low Level Output Voltage Gxx-Sxx P_{GS II} - - - - - - - - - 	4) Internal clock frequency accuracy has to be added to the specified values, please see Table 8 Table 11 Electrical Characteristics MOSFET drivers Low Level Output Voltage I/ _{05 LL} - 0.2 V 0 mA ≤ J _{DCL metops} ≤ 2 mA; P_9.4.1						
Power Supply	4) Accuracy derived from digital clock, for details please see Table 8 Table 11 Electrical Characteristics MOSFET drivers Low Level Output Voltage Gxx-Sxx Vos_LL Low Level Output Voltage Gxx-Sxx Vos_LL Low Level Output Voltage Gxx-Sxx Vos_LLS Low Level Output Vostage Gxx-Sxx Vos_LLS Low Level Output Vostage Gxx-Sxx Vostage Gxx-Sxx Low Level Output Vostage Gxx-Sxx Vostage Gxx-Sxx Low Level Output Vostage Gxx-S	4) Internal clock frequency accuracy has to be added to the specified values, please see Table 8 Table 11 Electrical Characteristics MOSFET drivers Low Level Output Voltage V _{GS_LL} - 0.2 V 0 mA ≤ f _{DCLoseOS} ≤ 2 mA; V _{FNN} ⁻¹ Electrical Characteristics P_9.4.1 Gox-Sxx - - 0.2 V 0 mA ≤ f _{DCLoseOS} ≤ 2 mA; V _{FNN} ⁻¹ Electrical Characteristics P_9.4.2 Low Level Output Voltage V _{GS_LLS} - - 0.2 V V _{SOFF} =Low; P_9.4.2						
Power Supply 9.4 Electrical Characteristics	4) Accuracy derived from digital clock, for details please see Table 8 Table 11 Electrical Characteristics MOSFET drivers Low Level Output Voltage Gxx-Sxx $V_{OS_{LLS}}$ 0.2 V $\frac{I_{OCLOBOD}S-2mA;}{V_{ELW}-Low or}$ P_9.4.1 Low Level Output Voltage GxX-Sxx $V_{OS_{LLS}}$ 0.2 V $\frac{I_{OCLOBOD}S-2mA;}{V_{COLOBOD}-Low or}$ P_9.4.2 High Level Output Voltage $\frac{dV_{O,PLS}}{dV_{O,PLS}}$ 0.5 V $\frac{I_{OCLOBOD}S-2mA;}{V_{SL}}$ P_9.4.5 Difference between Low-side Output Stages GLx-SLx	4) Internal clock frequency accuracy has to be added to the specified values, please see Table 8 Table 11 Electrical Characteristics MOSFET drivers $ \frac{L_{ow} \text{ Level Output Voltage } V_{GS_LL} 0.2 V 0 \text{ mA } \leq I_{DCLeedOS} \leq 2 \text{ mA:} P_{=}9.4.1 P_{=}9.4.1 P_{=}9.4.1 P_{=}9.4.2 P$						
 8.3 Electrical Characteristics Power Supply 9.4 Electrical Characteristics Floating MOSFET Driver 	4) Accuracy derived from digital clock, for details please see Table 8 Table 11 Electrical Characteristics MOSFET drivers Low Level Output Voltage Gxx-Sxx Vos_LL - - 0.2 V I_OCL68005 P_9.4.1 P_9.4.1 Low Level Output Voltage Gxx-Sxx Vos_LLS - - 0.2 V I_OCL68005 P_9.4.2 Low Level Output Voltage Gxx-Sxx Vos_LLS - - 0.2 V I_Sort=Lowr P_9.4.2 High Level Output Voltage dV'o_HLS - - 0.5 V I_OCL68005 2-mA; P_9.4.2 Dight Level Output Voltage dV'o_HLS - - 0.5 V I_OCL68005 2-mA; P_9.4.5 Dutput Stages GLx-SLx - - 0.5 V I_OCL68005 2-mA; P_9.4.5	4) Internal clock frequency accuracy has to be added to the specified values, please see Table 8 Table 11 Electrical Characteristics MOSFET drivers $ \frac{1}{V_{GS_{LL}}} = \frac{1}{1 - 1} = \frac{1}{1 - 1}$						
Power Supply	4) Accuracy derived from digital clock, for details please see Table 8 Table 11 Electrical Characteristics MOSFET drivers Low Level Output Voltage Gxx-Sxx $V_{OS,LL}$ Low Level Output Voltage Gxx-Sxx $V_{OS,LL}$ Low Level Output Voltage Gxx-Sxx $V_{OS,LLS}$ Difference between Low-side $dV_{O,HLS}$ Output Stages GLx-SLx $dV_{O,HLS}$ High Level Output Voltage $dV_{O,HLS}$ Difference between High-side $dV_{O,HLS}$ P.9.4.6 V_{Stage}	4) Internal clock frequency accuracy has to be added to the specified values, please see Table 8 Table 11 Electrical Characteristics MOSFET drivers $ \frac{Low Level Output Voltage}{Gxx-Sxx} \frac{V_{GS_LL}}{V_{GS_LL}} - \frac{-}{-} 0.2 V 0 \text{ mA} \leq I_{DCLeetOS} \leq 2 \text{ mA}; P_{=}9.4.1 \text{ P}_{S}, P_{=}9.4.1 \text{ P}_{S}, P_{=}9.4.2 \text{ Or } P_{S}, P_{=}0.4 \text{ Or } P_{S}, P_{=}0.4$						



Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80					
	Table 11 Electrical Characteristics MOSFET drivers (cont'd)	Table 11 Electrical Characteristics MOSFET drivers (cont'd)					
	Propagation Delay Time Matching $I_{P(an)}$ 20 ns $R_{Load}=2k\Omega^{3}$; $V_{Sxx}=0V$ P_9.4.22 (all FETs on)	Propagation Delay Time Mismatch $t_{P(m)}$ – – 20 ns $R_{Load}=2k\Omega^{31}$; $V_{Six}=0V$ P_9.4.22 (all FETs on)					
	Propagation Delay Time Matching $I_{P(af)}$ 20 ns $R_{Load}=2k\Omega^{3}$; $V_{Sxx}=0V$ P_9.4.23 (all FETs turn off)	Propagation Delay Time Mismatch $t_{P(af)}$ – – 20 ns $R_{Load}=2k\Omega^{3}$; $V_{Sxx}=0V$ P_9.4.23 (all FETs turn off)					
	Propagation Delay Time Matching $I_{P(1Min)}$ 0 – 20 ns $R_{Load}=2k\Omega^{3+}$; $V_{Six}=0V$ P_9.4.24 Single Phase (high-side off to low-side on)	Propagation Delay Time Mismatch $I_{P(1hfm)}$ 0 – 20 ns $R_{Load}=2k\Omega^{3}$; $V_{Sxx}=0V$ P_9.4.24 Single Phase (high-side off to low- side on)					
4 Electrical Characteristics loating MOSFET Driver	Propagation Delay Time Matching Single Phase (low-side off to high- side on) $I_{P(1IIhv)}$ 0 – 20 ns $R_{Load}=2k\Omega^{3}$; $V_{Sox}=0V$ P_9.4.25	Propagation Delay Time Mismatch $I_{P(1ibn)}$ 0 – 20 ns $R_{Load}=2k\Omega^{3}$; $V_{Sox}=0V$ P_9.4.25 Single Phase (low-side off to high-side on)					
	Propagation Delay Time Matching all Phases (all high-sides off to all low-sides on) $I_{P(ahlfn)} = 0$ and $R_{Load} = 2k\Omega^{3}; V_{Soc} = 0$ P_9.4.26	Propagation Delay Time Mismatch $I_{P(ahfin)}$ 0 – 20 ns $R_{Load}=2k\Omega^{3}$; $V_{Sxx}=0V$ P_9.4.26 all Phases (all high-sides off to all low-sides on)					
	Propagation Delay Time Matching all Phases (all low-sides off to high- side on) $t_{P(althn)} = 0$ and $R_{Load} = 2k\Omega^{3}; V_{Six} = 0$ P_9.4.27	Propagation Delay Time Mismatch all Phases (all low-sides off to high- side on) $t_{P(allbox)}$ 0 - 20 ns $R_{t nant}=2k\Omega^{3}; V_{Sax}=0V$ P_9.4.27					
10.5 Electrical Parameter Shunt Signal Conditioning	Table 19 Electrical Characteristics - Shunt Signal Conditioning (cont'd) Slew Rate SR - 15 - V/µs - P_10.5.22	Slew Rate ²¹ SR - 15 - V/µs - P_10.5.22 2) Not subject to production test, specified by design					
1.2.2 Failure Behavior Configuration	Table 23 Shutdown Error Overview ¹⁾ 3 sd_clk_fail Internal Clock Supervision Shutdown ³⁾ ARE Active 3) In the case of monitoring clock stops operation fault reaction of output stages is latched error State	Table 23 Shutdown Error Overview ¹⁾ 3 sd_clk_fail Internal Clock Supervision Shutdown ³⁾ ARE or LE Active 3) Failure reaction can be ARE or LE dependent on type of internal fault					
1 1.4.11 Overload Digital Output ⁹ ins	11.4.11 Overload Digital Output Pins The digital outputs are protected against short to GND and battery. If one output is shorted the output pin will be disconnected, a dedicated error register bit will be set. The pin ERR will be set to low. To unlock the output pin reset with ENA has to be performed. The failure behavior of the gate driver IC is adjustable at configuration mode, either the output stages will turn all external FETs off or not. Register Err_outp bit 4 to bit 0 indicate a short of a digital output pin.	11.4.11 Overload Digital Output Pins The digital outputs are protected against short to GND and battery. If one output is shorted the output pin will be disconnected, a dedicated error register bit will be set. The pin ERR will be set to low in case ERR is not the affected pin. To unlock the output pin, reset with ENA has to be performed. The failure behavior of the gate driver IC is adjustable at configuration mode, either the output stages will turn all external FETs off or not. Functionality of the overload detection of the digital output pins is limited, for details please refer to Chapter 18.11.4.					



Datasheet Chapter	TLE9180-	72	TLE	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80									
11.4.4 High-side Buffer Capacitor Voltage Monitoring	11.4.4 High-side Buffer Capacity An integrated undervoltage monitoring for thi for the high-side output stages. Additionally 1 mode if failure behavior is configured either as will be monitored at pin BHx referred to pin SI threshold undervoltage will be detected at the is not programmable. The detection is operat An overvoltage monitoring for the external An overvoltage detection all output stages remain necessary for reactivation of charge pump 2. 2 has been turned off duty cycle operation high high-side buffer detection. Register Err. 1.2 bit 7, bit 6 and bit 5 indicate undervoltage detection.	11.4.4 High-side Buffer Capacitor Voltage Monitoring An integrated undervoltage monitoring for the external high-side buffer capacitor guarantees a sufficient supp the high-side output stages. Additionally the external high-side buffer capacitor guarantees a sufficient supp the high-side output stages. Additionally the external high-side buffer capacitor guarantees a sufficient supp the high-side buffer capacitor guarantees a sufficient supp the high-side buffer capacitor is below a certain three undervoltage will be detected at the affected output stage. The high-side buffer capacitor is below a certain three undervoltage monitoring for the external high-side buffer capacitor detects too high gate source voltages for external FET. The failure behavior and filter time are not configurable. In case of an overvoltage detection, the ERR prin is set low and the dedicated error bit in the register will be set second charge pump will be deactivated all output stages remain active. A reset via ENA is necessary for the reactivation of the second charge pump. If the second charge pump is deactivated, an undervoltage high-side buffer detection might occur mainly at oper with high duty cycles. The overvoltage monitoring for the external high-side buffer capacitor can be deactivated at configuration. Register Err_j_2 bit 7, bit 6 and bit 5 indicate an overvoltage condition detected, bit 2, bit 1 and bit 0 indicat undervoltage detection.					inear mode if oltage will be ain threshold eshold is not tages for the ill be set. The y at operation ion.						
11.5 Electrical Characteristics Protection and Diagnostic Functions	Table 47 Electrical Characteria Accuracy Undervoltage Threshold Vrst			ind Diag		ions _{'SUV} <7.5V	Table 47 Electrical Chara Accuracy Undervoltage Threshold Vs	all annes	0.000278	PROG		and the standards	V P_11.6.12
	Table 47 Electrical Characterist	cs - Protecti	ion and D	iagnostic	Functions		Table 47 Electrical Character	stics - Prot	ection a	nd Diagn	ostic Fu	nctions	
	Entry Filter and Reaction Time of Vue	ROPH 0.6	ď	-	µs –	P_11.6.8	Entry Filter and Reaction Time of Reduced Operation Mode	I _{VsROP11}	0.6	-	-	μs –	P_11.6.8
	Reduced Operation Mode Detection at Vs ⁴	-		_			Detection at Vs ⁴⁾	_					
	Reduced Operation Mode Detection at Vs ⁴	ROPI2 20	-	-	µs –	P_11.6.9	Detection at Vs ⁴) Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs ⁴)	7 _{VSROPI2}	20	-	-	μs –	P_11.6.9
Protection and Diagnostic	Reduced Operation Mode Detection at Vs ⁴ ¹ Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs ⁴ ¹	6	-	-		P_11.6.9	Exit Filter and Reaction Time of Reduced Operation Mode			nd Diagn	- ostic Fu		P_11.6.9
Protection and Diagnostic	Reduced Operation Mode Detection at Vs ⁴¹ Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs ⁴¹ Fvs Table 47 Electrical Characteristics - Entry Filter and Reaction Time of Fvcc Reduced Operation Mode Fvcc	6	nd Diagn	1 1		P_11.6.9	Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs ⁴⁾			nd Diagn	- ostic Fu		P_11.6.9
11.5 Electrical Characteristics Protection and Diagnostic Functions	Reduced Operation Mode Detection at Vs ⁴¹ Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs ⁴¹ Filter Table 47 Electrical Characteristics - Entry Filter and Reaction Time of Reduced Operation Mode Detection at VCC ⁴¹ Filter	Protection an	nd Diagn	-	octions		Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs ⁴) Table 47 Electrical Charactern Entry Filter and Reaction Time of Reduced Operation Mode	stics - Prot	ection an	nd Diagn		nctions	



Datasheet Chapter	TLE	9180-200	21Q	CDS V1.72	TLE9	180-20QI	K DS V1	.80 / TI	E9180-	21QK	DS V1.80					
11.5 Electrical Characteristics	Table 47 Electrical Characterist	ics - Protec	ction and	Diagnosti	c Functio	ns (co	nťď)		Table 47 Electrical Characteris	itics - Prot	ection a	nd Diag	nostic I	Functio	ns (cont'd)	
Protection and Diagnostic Functions	Filter Time of SCD ^{2]3)}	t _{SCDf}	1	PROG	6	μs	4 steps programmable	P_11.6.69	Filter Time of SCD ²⁽³⁾	I _{SCDI}	0.5 1.7 3.4 5.7	-	2.3 3.5 5.2 7.5	1	_fi_scd = '0x0' _fi_scd = '0x1' _fi_scd = '0x2' _fi_scd = '0x3'	P_11.6.69
	Table 47 Electrical Characterist	cs - Prote	ction and	Diagnos	tic Funct	tions (cont'd)		Table 47 Electrical Characte	eristics - F	rotectio	n and [Diagnos	stic Fur	ctions (cont'd)	
	Timing Error Handling								Fault Reaction Time ⁴⁾	1 _{FRT}	20	-	500	ns	-	P_11.6.1
1.5 Electrical Characteristics	Fault Reaction Time ⁴⁾	I _{FRT}	20	-	500	ns	-	P_11.6.103	ENA Low Time Threshold for	t _{clear}	2.2	3.0	3.8	μs	ENA falling edg	e P_11.6.1
rotection and Diagnostic	ENA Low Time Clearing Latched Errors	l _{clear}	2.2	3.0**	3.8	μs	ENA falling edge	P_11.6.104	Clearing Latched Errors				_			
Functions	ENA Low Time Without Clearing Latched Errors	f _{Res}	-3	1.02)	1.3	μs	-	P_11.6.105	Return Time to Normal Operation for ARE Fault Behavior Configuration ²⁾	I _{RT}	-	-	1.0	μs	-	P_11.6.1
	Table 47 Electrical Characteris Overvoltage Detection and Shutdown Silter Time Reason Vo200	tics - Pro	tection a	and Diagr	100	unctio µs	4 steps	P_11.6.5	Table 47 Electrical Characteris	tics - Prot	8	d Diagn	17	µs	_ov_vs = '0x0'	P_11.6.5
	Shutdown Filter Time Range Vs ²⁽³⁾ Undervoltage Filter Time Range Vs ²⁽³⁾	l _{uvvar}	10	-	100	μs	programmable 4 steps	P_11.6.14	Shutdown Filter Time Range Vs ²⁽³⁾		24 48 96		33 57 105		_ov_vs = '0x1' _ov_vs = '0x2' _ov_vs = '0x3'	
	Overvoltage Detection and		10	-	100	μs	programmable 4 steps	P 11.6.19	Undervoltage Filter Time Range	t _{uvvsr}	8	-	17			2_11.6.14
	Shutdown Filter Time Range VDHP ²⁽³⁾	LOVVDHr		Γ,		μο	programmable	P_11.0.19	Vs ²⁾³⁾		24 48 96		33 57 105	1	_uv_vs = '0x1' _uv_vs = '0x2' _uv_vs = '0x3'	
	Undervoltage Filter Time Range VDHP ²⁽³⁾	1UVVDHr	10	-	100	μs	4 steps programmable	P_11.6.29	Overvoltage Detection and Shutdown Filter Time Range VDHP ²⁾³⁾	I _{OVVDHr}	8 24 48	-	17 33 57		_ov_vdh = '0x0' _ov_vdh = '0x1' _ov_vdh = '0x2'	P_11.6.19
	Undervoltage Detection and Shutdown Filter Time Range CB ²⁽³⁾	I _{UVCBr}	10	-	100	μs	4 steps programmable	P_11.6.43	VDH- ···		96		105		_ov_vdh = '0x3'	
	Undervoltage Detection Filter Time BHx-SHx ²⁽³⁾	I _{UVBS}	1	-0	10	μs	4 steps programmable	P_11.6.52	Undervoltage Filter Time Range VDHP ²⁽³⁾	t _{uvvo+r}	8 24 48	-	17 33 57	· •	_uv_vdh = '0x0' _uv_vdh = '0x1' _uv_vdh = '0x2'	2_11.6.29
	Filter Time of SCD ²⁾³⁾	t _{SCDf}	1	PROG	6	μs	4 steps	P_11.6.69			96		105		_uv_vdh = '0x3'	
1.5 Electrical Characteristics Protection and Diagnostic	VCC Filter Time ²⁾³⁾	tvccr	10	-	100	μs	programmable 4 steps	P 11.6.85	Undervoltage Detection and Shutdown Filter Time Range CB ²⁽³⁾	f _{UVCBr}	8 20	-	13 25		_uv_cb = '0x0'	2_11.6.43
unctions		*VCCI		-		po	programmable	1_11.0.00	Shutdown Filter Time Kange CB		48		53	1 1	uv_cb = '0x2'	
									Undervoltage Detection Filter Time		96 0.8	_	101		_uv_cb = '0x3' uv_bs = '0x0'	9 11.6.52
									BHx-SHx ²⁽³⁾	"UVBS	2.8	-	3.8		_uv_bs = '0x1'	_11.0.02
											4.8 9.8		5.8 10.8		_uv_bs = '0x2' uv_bs = '0x3'	
									Filter Time of SCD ²⁽³⁾	ISCOF	0.5	-	2.3			9 11.6.69
										- 3001	1.7		3.5	1	fi_scd = '0x1'	_
											3.4 5.7		5.2 7.5		_fi_scd = '0x2' _fi_scd = '0x3'	
									VCC Filter Time ²⁽³⁾	I _{VCCI}	8	-	17		_uv_vcc =	2_11.6.85
											24	-	33		_uv_vcc =	
											48	-	57	µs 1	_ov_vcc = '0x1' _uv_vcc = _ov_vcc = '0x2'	
															$_{0v}vcc = 0xz$	



Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
9.4 Electrical Characteristics Floating MOSFET Driver	Table 11 Electrical Characteristics MOSFET drivers (cont'd) Dead Time ⁸⁽⁹⁾ Programmable Dead Time Range Image I	Dead Time ⁸⁾⁽⁹⁾ Programmable Dead Time Range ¹⁽⁹⁾ Image Topologic Content of the transformation of transformatio of transformation of transformation of tra
11.6 Electrical Characteristics Protection and Diagnostic Functions <u>Modification done in:</u> <u>TLE9180-21QK</u>	Table 51 Electrical Characteristics - Protection and Diagnostic Functions (cont'd) VCC Read Out Voltage Detection Range V_ADCr 0 – 5.554 V 0 to FFh P_11.6.86	Table 51 Electrical Characteristics - Protection and Diagnostic Functions (cont'd) VCC Read Out V Voltage Detection Range V_ADCr 0 – 5.55 V 0 to FFh P_11.6.86
11.6 Electrical Characteristics Protection and Diagnostic Functions <u>Modification done in:</u> <u>TLE9180-21QK</u>	Table 51 Electrical Characteristics - Protection and Diagnostic Functions (cont'd) Digital Driving Path Monitoring Digital Driving Path Monitoring Filter IsTDIT - 500 - ns - P_11.6.92 Input Pattern Violation Monitoring Input Pattern Violation Filter and IsTDIT - 750 - ns - P_11.6.93 Reaction Time ² Istor - 750 - ns - P_11.6.93	Table 51 Electrical Characteristics - Protection and Diagnostic Functions (cont'd) Digital Driving Path Monitoring Digital Driving Path Monitoring Digital Driving Path Monitoring Filter Image: State of the state
11.6 Electrical Characteristics Protection and Diagnostic Functions <u>Modification done in:</u> <u>TLE9180-20QK</u>	Table 47 Electrical Characteristics - Protection and Diagnostic Functions (cont'd) Digital Driving Path Monitoring Digital Driving Path Monitoring Filter Image: Transform of the state of the s	Table 47 Electrical Characteristics - Protection and Diagnostic Functions (cont'd) Digital Driving Path Monitoring Filter Image: Control of the second s
11.4.8.2 Temperature Read Out	11.4.8.2 Temperature Read Out The absolute temperature can be read in the related SPI register in steps of 5.8 Kelvin per LSB. A temperature sensor is integrated at the output stage low-side 1. The signal is filtered with a moving average filter. After transition from configuration mode to normal operation mode it is recommended to wait 1ms before first temperature readout will be performed. The temperature read out result is stored in the register temp_ls1. The temperature sensor is independent to the sensor used for temperature detection and shutdown.	11.4.8.2 Temperature Read Out The absolute temperature can be read in the related SPI register in steps of 7 _{Tread, usp} per LSB. A temperature sensor is integrated at the output stage low-side 1. The signal is filtered with a moving average filter. After transition from configuration mode to normal operation mode it is recommended to wait 1ms before first temperature readout will be performed. The temperature read out result is stored in the register temp_is1. The temperature sensor is independent to the sensor used for temperature detection and shutdown.



Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80
13 Operation Modes	<figure></figure>	Fyre 2 Overview of Digital Operation
13.3 Sleep Mode	13.3 Sleep Mode If the INH pin is set to low the driver will be set into sleep mode. First the INH pin switches off the external FETs actively with the output stages and afterwards the complete power supply structure of the device. If the charge pump and high-side buffer capacitors are discharged the gate of the external FET will be clamped to its source with an internal passive clamping circuit. Once set to sleep mode the TLE9180-20QK has to be reconfigured.	13.3 Sleep Mode If the INH pin is set to low, the internal power down sequence will be initiated. After detection of the low transition changes at the INH pin will be ignored until the sleep mode has been reached. The gate driver IC will enter sleep mode after undervoltage shutdown at pin CB has been detected. First the INH pin switches off the external FETs actively with the output stages. The undervoltage shutdown at pin CB will be checked after the internal blocks – output stages, OPAMPs, internal 5 V voltage regulator, charge pumps, PFB blocks, output stages logic blocks and SCD blocks – are switched off. Afterwards the remaining clocks, the VCC supervision, all digital pads, the temperature sensors and the HV ADC will be deactivated. Then the digital core will be reset and the internal 3.3 V and 1.5 V regulators will be deactivated. If the charge pump and high-side buffer capacitors are discharged the gate of the external FET will be clamped to its source with an internal passive clamping circuit. Once set to sleep mode the TLE9180-20QK has to be reconfigured.
15.1.1 Configuration registers Modification done in: TLE9180-20QK	fm_osfb 3:2 rmw Output Stage Feedback Failure Behavior 11 _B , LE - Latched Error 10 _B , ARE - Auto Restart Error 01 _B , ERR - Error 00 _B , W - Warning (default)	fm_osfb 3:2 none fixed bit field for TLE9180 basic 00 _B , fixed value for TLE9180 basic



Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS	1.72		TLE9180	9-20QK DS V1.80 / TLE9180-2	21QK DS V1.80		
	Short Circuit Errors Err_scd Of Short Circuit Errors 4 7 6 5 4 3 2 err_scd err_scd err_scd err_scd err_scd err_scd _hs1 _hs2 _hs3 _is1 _is2 _is3 rc rc rc rc rc rc rc	et Reset value	freuit Errors 6 acd err_s 1 _hs	cd err_s 2 _hs	scd err_scd err_scd s3 _ls1 _ls2	Offs 47, 2 1 err_scd _ls3 rc		
		Field	Bits	Туре	Description			
	Field Bits Type Description	err_scd		rc	Short Circuit Detection at His	igh-side 1		
	err_scd_hs1 7 rc Short Circuit at High-side 1 1 ₈ . Error set			12.5	1 _B , Error set 0 _B , No error			
15.1.4 Read registers	Og , No error err_scd_hs2 6 rc Short Circuit at High-side 2 1 _B , Error set	err_scd_	err_scd_hs2 6 rc Short Circuit Detection at High-side 2 1 _B , Error set 0 _B , No error err_scd_hs3 5 rc Short Circuit Detection at High-side 3 1 _B , Error set 0 _R , Fror set 0 _R , Error set 0 _R , Error set 0 _R , No error					
	OB , No error err_scd_hs3 5 rc Short Circuit at High-side 3 1 _B , Error set	err_scd_						
	err_scd_is1 4 rc Short Circuit at Low-side 1 1 ₈ , Error set 0 ₈ , No error	err_scd_	ls1 4	rc	Short Circuit Detection at Lo 1 _B , Error set 0 _B , No error	ow-side 1		
	err_scd_ls2 3 rc Short Circuit at Low-side 2 1 _B , Error set 0 ₀ , No error	err_scd_	ls2 3	rc	Short Circuit Detection at Lo 1 _B , Error set 0 _B , No error			
	err_scd_ls3 2 rc Short Circuit at Low-side 3 1 _B , Error set 0 ₀ , No error	err_scd_	Is3 2	rc	Short Circuit Detection at Lo 1 _B , Error set 0 _B , No error	ow-side 3		
	Res 1:0 none Reserved 00 ₈ , default value, do not change.	Res	Res 1:0 none Reserved 00 _B , default value. do not change.					
I 6.1 Layout Guide Lines	 Application Information Additional R-C snubber circuits (R and C in series) can be placed to attenuate/supp switching of the MOSFETs, there may be one or two snubber circuits per half brid C (several nF) must be low inductive in terms of routing and packaging (ceramic c The exposed pad on the backside of the package is recommended to connect to 0 VDHP has to be connected and referenced to a common point of the drains of the For further information you may contact http://www.infineon.com/ 	e, R (several Ohm) and switchin (several Ohm) and (several Ohm) an	g of the MOSF nF) must be lo osed pad on the osed pins GND, os to be conne	ETs, there ma ow inductive in the backside of CP_GND, A_C cted and refer	and C in series) can be placed to a ay be one or two snubber circuits in terms of routing and packaging of the package is recommended to GND have to be connected togeth renced to a common point of the ontact http://www.infineon.com/	s per half bridge, R (se g (ceramic capacitors) o connect to GND her to the PCB GND cli e drains of the high-sid	everal Ohm) and C) osely to the chip	



Datasheet Chapter	TLE9180-20QK DS V1.72 / TLE9180-21QK DS V1.72	TLE9180-20QK DS V1.80 / TLE9180-21QK DS V1.80				
18.8.2 Cross Talk of Automatic Recharging Circuits	 18.8.1 Quiescent Current Consumption at Pin Vs Item 8.1. integrated into datasheet please refer to Chapter 8.3, maximum limits of quiescent current specification updated 18.8.2 Cross Talk of Automatic Recharging Circuits Item 8.2. integrated into datastneet please refer to Chapter 9.4 and Chapter 8.3, Cross talk of the high-side buffer recharging circuit Of these 2 and phase 3 to phase 1 has been identified. This might lead to a higher high-side buffer supply capacitor voltage between pins BH1 to SH1. Higher gate voltages for high-side FET 1 has been observed. Gate source voltage of 15V will not be exceeded. 18.9 Floating MOSFET Driver 	 18.8.1 Quiescent Current Consumption at Pin Vs Item 8.1. integrated into datasheet please refer to Chapter 8.3, maximum limits of quiescent current specification updated 18.9 Floating MOSFET Driver Erratas identified. 				
9.4 Electrical Characteristics Floating MOSFET Driver 8.3 Electrical Characteristics Power Supply	Table 11 Electrical Characteristics MOSFET drivers High Level Output Voltage Gxx-Sxx $V_{G_1H_1}$ 8.5 - 13.5 V $7V \le V_{VS} < 60V$; $C_{CPk} = 1.0 \mu$ F; $C_{CB} = 4.7 \mu$ F; $I_{DCLoad CS} = 2mA$; $V_{G_1, H_2} = 000$ P_9.4.3	Table 11 Electrical Characteristics MOSFET driversHigh Level Output Voltage Gxx-Sxx $V_{G_{a}HL1}$ 8.5-13.5V $7V \le V_{VS} < 60V;$ $C_{CPX} = 1.0 \mu F;$ $I_{OCL0000S} = -2mA;$ $V_{SLA} = V_{SHA} = 0V$ P_9.4.3				
	High Level Output Voltage Gxx-Sxx $V_{G_{L}H_{2}}$ 8 - 12.5 V $5.5V \le V_{V_{S}} \le 7V$; P_9.4.4 $C_{CP_{R}} = 1.0 \mu$ F; $C_{CB} = 4.7 \mu$ F; $I_{DCLoadOS} = -2mA$; $V_{S_{L}x} = V_{Shx} = 0V$	High Level Output Voltage Gxx-Sxx $V_{G_{_{_{_{_{_{_{_{_{_{_{_{_{_{_{_{_{_{$				
	1) Max. limit may differ for output stage HS1. Output voltage of GH1-SH1 might be higher. Please refer to B13 errata, item 8.2., Chapter 18.8.2. Table 9 Electrical Characteristics: Power Supply (cont'd)	 The bootstrap voltages might exceed the max. value due to capacitive coupling of the SHx voltages Table 9 Electrical Characteristics: Power Supply (cont'd) 				
	High-side Buffer Supply Limitation VietStatim 10 11 12 V - P_8.3.15 Voltage BHx to SHx at CP2 Charging 10	High-side Buffer Supply Limitation V _{BHSHullm} 10 11 12 V – P_8.3.15 Voltage BHx to SHx at CP2 Charging ¹⁰⁾				
	10) Automatic charging of the high-side buffer supply capacitor (BHx-SHx) with charge pump 2 will be stopped if voltage level V _{BHDBas} has been reached.	10) The bootstrap voltages might exceed the max value due to capacitive coupling of the SHx voltages				



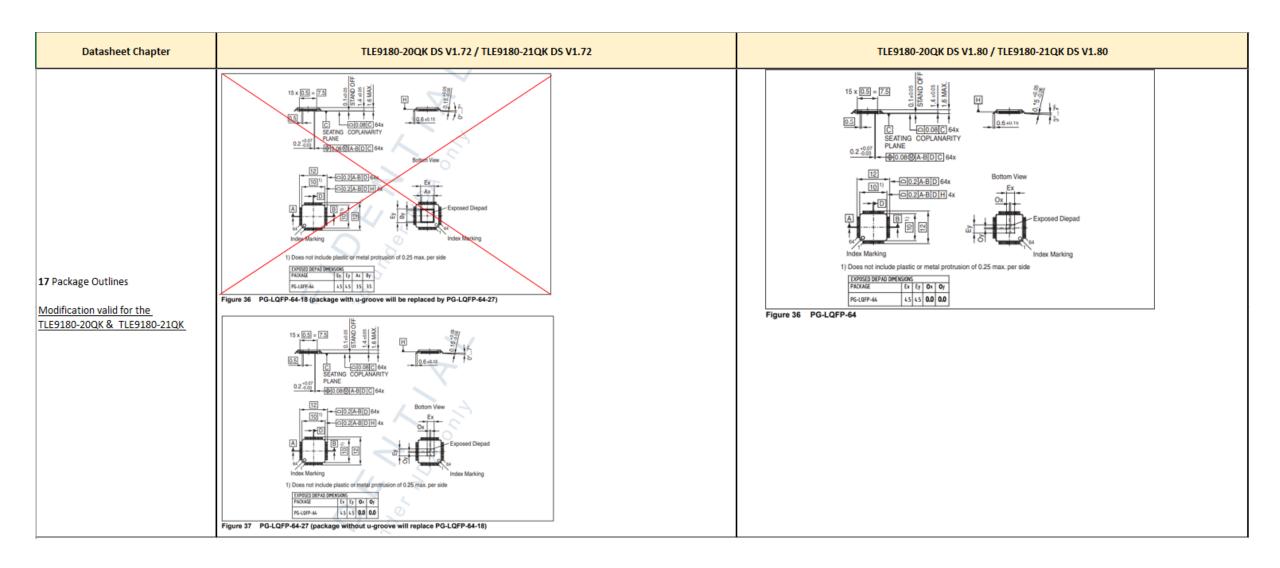




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Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
3.1 Absolute Maximum Ratings	Table 2 Absolute Maximum Ratings Maximum Peak Pulse Current CB Image: Comparison of the comparison of t	Table 2 Absolute Maximum Ratings Maximum Peak Pulse Current CB l_{CBCH2} - 1 A $t = 5 \mu s^{3/2}$ P_4.1.61 To CH2 Not subject to production test, specified by design - 1 A $t = 5 \mu s^{3/2}$ P_4.1.61
3.1 Absolute Maximum Ratings	Supply Voltage for Power-up ¹) Vvs3 - - 30 V - P_4.1.7	Table 2 Absolute Maximum Ratings Supply Voltage for Power-up ¹ /V _{V56} - 40 V - P_4.1.7 Supply Voltage for Power-up ¹ /V _{V56} - - 40 V - P_4.1.7
3.1 Absolute Maximum Ratings	Voltage Difference SHx-SLx ¹¹ V _{SSx1} -7 - 90 V - P_4.1.29 Voltage Difference SHx-SLx ¹¹ V _{SSx2} 10 V 9 P_4.1.30 Voltage Difference SHx-SLx ¹¹ V _{SSx2} 10 V 9 P_4.1.30 Voltage Difference SHx-SLx ¹¹ V _{SSx3} -15 - V 5 P_4.1.31	Table 2 Absolute Maximum Ratings (cont'd) Voltage Difference SHx-SLx ^{1J} V _{SSx1} -12 - 90 V IHx = High P_4.1.29 Voltage Difference VDHP-SHx V _{dVDHP} -90 - 85 V en_vdh3 = 0x1 (cfg.: 3 VDHx pins enabled) P_4.1.32
3.1 Absolute Maximum Ratings Modification valid for : TLE9180C-21QK & TLE9180C-31QK	Table 2 Absolute Maximum Ratings (cont'd) Voltage Range APC V _{AOP1} -0.3 - 60 V - P_4.1.39	Table 2 Absolute Maximum Ratings (cont'd) Voltage Range APC V _{AOP1} -0.3 - 60 V 9 P_4.1.39 ⁹ A short circuit at APC for >10hrs might damage the device P_4.1.39
3.1 Absolute Maximum Ratings	Table 2 Absolute Maximum Ratings (cont'd) Temperatures Storage Temperature T_{stg} -55 - 150 °C - P_4.1.54 Junction Temperature T_{stg} -40 - 150 °C - P_4.1.55 Junction Temperature T_{J1} -40 - 150 °C - P_4.1.55 Junction Temperature T_{J2} 40 - 175 °C 200h over lifetime P_4.1.56	Table 2 Absolute Maximum Ratings (cont'd) Temperatures Storage Temperature T_{stg} -55 - 150 °C - P_4.1.54 Junction Temperature T_{J1} -40 - 150 °C 10 °C 110 °C 1
3.1 Absolute Maximum Ratings	Table 2 Absolute Maximum Ratings (cont'd) Max. Voltage Transients at SHx V _{ISH_VI} - 20 V Slew rate ≤ 1 V/ns ⁷ 11 P_4.3.31 1) Not subject to production test, specified by design. 7) Exceeding specified slew rate in combination with the maximum specified voltage transient may set the affected output stage in an undefined state for typically 1 μs.	Table 2 Absolute Maximum Ratings (cont'd) Max. Voltage Transients at SHx V _{ISH_tr1} - - 55. V Slew rate ≤ 1 V/ns ^{7/22} P_4.3.31 1 Not subject to production test, specified by design. - - 55. V Slew rate ≤ 1 V/ns ^{7/22} P_4.3.31 2 At amplitudes higher than 20V the HS output stage can show unexpected switch off of the external MOSFET for typically 1 µs if the output stage is not switching. If the output stage is switching on or switching off, the output stage is switching normally even with amplitudes up 55V and slew rates up to 1V/ns



Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10				
3.2 Thermal Resistance	Table 3 Thermal Resistance 2) Specified R _{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip + Package) was simulated on a 76.2 × 114.3 ×1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 ×35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.	Table 3 Thermal Resistance 12 Specified R _{th,J,A} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.				
4.7 Electrical Characteristics IOs	1) Not subject of production test, specified by design	1) Not subject to production test, specified by design.				
	Table 6 Electrical Characteristics IOS (continued) High Level Output Voltage V _{ERRHSb} 3.8 - V _{VCC} V V _{VS} > 7.2 V; P_5.7.24 Vicc V V _{VCC} = 5.0 V; Inoad = -0.2 mA; All Digital I/Os All Digital I/Os	Table 6 Electrical Characteristics IOs (continued)				
	Low Level Output Voltage V_{ERRL} -0.1-0.4V $I_{Load} = 0.2 \text{ mA}$ P_5.7.39High Level Output Voltage V_{SPHHSD} 3.8- V_{VCC} V $V_{VS} > 7.2 \text{ V};$ P_5.7.57	High Level Output Voltage V_{ERRHSa} 3.3- V_{VCC} V $V_{VCC} = 5.0 \text{ V};$ P_5.7.38Image: Image of the second				
4.7 Electrical Characteristics IOs	Vice V V _{VCC} = 5:0 V; / _{load} = -0.2 mA; All Digital I/Os = static	Low Level Output Voltage V -0.1 - 0.4 V I _{Load} = 0.2 mA P_5.7.39				
4.7 Electrical characteristics los	Low Level Output Voltage V_{SPIL} -0.1-0.4V $I_{Load} = 0.2 \text{ mA}$ P_5.7.45High Level Output Voltage ³⁰⁾ V_{ERRHSa} 3.3- V_{VCC} V $\frac{5.5 V \le V_{VS} \le 7.2 V}{V_{VCC} = 5.0 V};$ P_5.7.38 $V_{Load} = -0.2 \text{ mA};$ - $V_{Load} = -0.2 \text{ mA};$ $V_{Load} = -0.2 \text{ mA};$ -	High Level Output Voltage V_{SPIH5a} 3.3- V_{VCC} V $V_{VCC} = 5.0 \text{ V};$ P_5.7.44Ilogial I/Os = staticstatic <t< td=""></t<>				
	All Digital I/Os = static	Low Level Output Voltage V V I_Load = 0.2 mA P_5.7.45				
	High Level Output Voltage ³¹⁾ V_{SPIH5a} 3.3- V_{VCC} V $\frac{5.5 V \le V_{VS} \le 7.2 V}{V_{VCC} = 5.0 V};$ $V_{load} = -0.2 mA;$ All Digital I/Os = staticP_5.7.44					



Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10				
4.7 Electrical Characteristics IOs	Table 6Electrical Characteristics IOs (continued)High Level Output Voltage ⁷¹ V_{ERRHSa} 3.4 - V_{VCC} V $5.5 V \le V_{VS} \le 7.2 V;$ $V_{Icad} = .0.2 mA;$ All Digital $I/Os = staticP_5.7.38$	Table 6 Electrical Characteristics IOs (continued) High Level Output Voltage ³¹⁾ V _{ERRH5a} 3.3 - V _{VCC} V V _{VCC} = 5.0 V; I _{load} = -0.2 mA; All Digital I/Os = static P_5.7.38				
	Table 6Electrical Characteristics IOS (cont'd)High Level Output Voltage ⁷ V_{SPHSa} 3.4- V_{VCC} V $5.5 V \le V_{VS} \le 7.2 V;$ $V_{VCC} = 5.0 V;$ $I_{load} = -0.2 mA;$ All Digital $I/Os = staticP_5.7.44$	Table 6Electrical Characteristics IOs (cont'd)High Level Output Voltage V_{SPIHSa} 3.3- V_{VCC} V $V_{VCC} = 5.0 V;$ $P_{-5.7.44}$ $I_{load} = -0.2 mA;$ All Digital I/Os $=$ static				
4.7 Electrical Characteristics IOs	Table 6 Electrical Characteristics IOs (cont'd) Pin ENA ENA Propagation Time (for enable or disable the output stages) t_{PENA} - 100 - ns - P_5.7.17	Table 6 Electrical Characteristics IOs (cont'd) Pin ENA ENA Propagation Time (for enable or disable the output stages) t_{PENA} - 100 500 ns - P_5.7.17				
4.7 Electrical Characteristics los	Table 6 Electrical Characteristics IOs (cont'd)	Table 6 Electrical Characteristics IOs (cont'd)				
Change done in the <u>TLE9180C-21QK & TLE9180C-31QK</u>	High Level Output Voltage V 4.2 5.0 6.0 V I _{load} = -1 mA P_5.7.47	High Level Output Voltage V V I				
5 Serial Peripheral Interface - SPI	SPI Master SPLMTSR Image: SPLMTSR SPLMTSR SPLMTSR Control Registers SPI Master SPLMTSR SPLMTSR SPLMTSR Control Registers SPI Master SPLMTSR SPLMTSR Control Registers SPL SPI Master SPLMTSR SPLMTSR Control Registers SPL SPI Master SPLMTSR SPLMTSR Control Registers Uter SPI slave SPLCSN Other SPI slave Image: SPLCSN I) Floating of MISO connection node shall be avoided. Figure 4 Principle for SPI-Bus Architecture	SPI Master (Microcontroller) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				

Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10						
5.4 Cyclic Redundancy Check - CRC Generation and Detection	5.4 Cyclic Redundancy Check - CRC Generation and Detection The CRC is added to any data transmitted. It is calculated for the whole SPI frame, CRC bits excluded. The CRC check for incoming data is performed over the complete SPI frame.	5.4 Cyclic Redundancy Check - CRC Generation and Detection The CRC is added to any data transmitted. It is calculated for the whole SPI frame, CRC bits excluded. The CRC check for incoming data is performed over the complete SPI frame. In case of an CRC3 Error Detection on the MISO line by the μC, the message should be discarded and the register access should be repeated.						
5.5 Electrical Characteristics SPI	Table 7 Electrical Characteristics: Timing (cont'd) Sequential Transfer Delay ³) Ispl_td 250 - ns 1 Figure 6, N P_6.5.19	Table 7 Electrical Characteristics: Timing (cont'd) Sequential Transfer Delay ³⁴⁾ $t_{SPL_{1d}}$ 330. - ns 33)Figure 6, N P_6.5.19						
5.5 Electrical Characteristics SPI	Table 7 Electrical Characteristics: Timing T_j = -40°C to +150°C, V _S = 5.5 V to 60 V and with respect to GND, positive current flowing into pin (unless 3 otherwise specified). Parameter Symbol Values Unit Note / Test Condition Number SPI Operating Frequency \int_{SPI_cck} $-^{10}$ $ 10$ MH 2^{10} P_6.5.1	Table 7 Electrical Characteristics: Timing $T_j = -40^{\circ}$ C to +150°C, $V_S = 5.5$ V to 60 V, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified). Timings valid for 10 MHz operation. Parameter Symbol Values Unit Note / Number SPI Operating Frequency f_{SPl_ctk} $-^{11}$ $-$ 10 MH 21 P_6.5.1						
5.5 Electrical Characteristics SPI	Table 7 Electrical Characteristics: Timing SPI Data Output (MISO) Lag 25 - ns 2) Figure 6, M P_6.5.15	Table 7 Electrical Characteristics: Timing Enable (SS) Lag Time tspt_lag 25 - ns 33)Figure 6, M P_6.5.15						
5.5 Electrical Characteristics SPI	Table 7Electrical Characteristics: Timing CLK_SPI Operating Period l_{SPI_dk} 100 ns $^{2)}$ Figure 6, CP_6.5.2 CLK_SPI High Time l_{SPI_wsckh} 37 ns $^{2)}$ Figure 6, AP_6.5.3 CLK_SPI Low Time l_{SPI_wsckh} 37 ns $^{2)}$ Figure 6, BP_6.5.4 CLK_SPI Fall Time l_{SPI_wsckl} 37 ns $^{2)}$ Figure 6, DP_6.5.52) Not subject to production test; verified by design or characterization; measured between 10% and 90%; output load capacitance on MISO pin is ≤ 60pF.	Table 7 Electrical Characteristics: TimingCLK_SPI Operating Period t_{SPL_clk} 100ns $33J_Figure 6, C$ P_6.5.2CLK_SPI High Time t_{SPL_wscklh} 37ns $33J_Figure 6, A$ P_6.5.3CLK_SPI Low Time t_{SPL_wsckll} 37ns $33J_Figure 6, B$ P_6.5.4Not subject to production test; verified by design or characterization; measured between 20% and 80%; output load capacitance on MISO pin is $\leq 60 \text{ pF}$						
7.1 Output Stage Supply Concept	7.1 Output Stage Supply Concept requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20kHz PWM frequency. The charge pumps will be deactivated if the gate driver IC is set to sleep mode via INH.	7.1 Output Stage Supply Concept fulfills the requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20 kHz PWM frequency. The charge pumps will be deactivated if the gate driver IC is set to sleep mode via pin INH or a charge pump related error is detected. For details please check the supervision descriptions.						



Datasheet Chapter	TLE91				E91800 DS V1.		K DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10	
7.3 Electrical Characteristics Power Supply (tbd)	Table 10 Electrical Characteristic Supply current in Reduced Operation	on Mode at							Table 10 Electrical Characteristics: Power Supply (cont'd) 'd) Supply Current Vs Image:
		Vs(ROMVS)	-				V _{Vs} =V _{VDHP} =3V	_8.3.36	
7.3 Electrical Characteristics Power Supply	Table 10 Electrical Character Voltage Vs for Guaranteed Power- up of Charge Pumps		6.0		-	V	-	P_8.3.38	Table 10 Electrical Characteristics: Power Supply (cont'd) Voltage Vs for ensured Power-up of Charge Pumps V _{VSWU} 6.0 - - V - P_8.3.38
	Table 10 Electrical Characte	eristics: Po	ower S	upply (cont'd)				Table 10 Electrical Characteristics: Power Supply (cont'd)
7.3 Electrical Characteristics Power Supply	Quiescent Current VDHx /	QVDHx2	-	50	200	nA	$\begin{split} & V_{\text{VDHP}} \leq 14 \text{ V}; \\ & T_a \leq 25^{\circ}\text{C}; \\ & V_{\text{INH}} = V_{\text{SOFF}} = \text{GND}^{14}; \\ & V_{\text{SHx}} = \text{GND} \end{split}$	P_8.3.31	Quiescent Current VDHx I_{QVDHx2} -50200nA $V_{VDHx} \le 14 V;$ $V_{VDHx} \le 14 V;$ $T_a \le 25^4 C;$ $V_{INH} = V_{SOFF} = GND^{49};$ $V_{SHx} = GND$ P_8.3.31
	Quiescent Current VDHx //	QVDH×1	-	50	200	nA	$\begin{split} & V_{\text{VDHP}} \leq 60 \text{ V}; \\ & T_a \leq 25^{\circ}\text{C}; \\ & V_{\text{INH}} = V_{\text{SOFF}} = \text{GND}^{14}; \\ & V_{\text{SHx}} = \text{GND} \end{split}$	P_8.3.32	Quiescent Current VDHx I_{QVDHx1} -50200nA $V_{VDHP} \leq 60 V;$ $V_{SOHP} \leq 60 V;$ $T_{a} \leq 25^{\circ} C;$ $V_{INH} = V_{SOFF} = GND^{49};$ $V_{STHz} = GND$ P_8.3.32
	Table 10 Electrical Charact	torictics: P	ower	upply (cont'd)				Table 10 Electrical Characteristics: Power Supply (cont'd)
	Quiescent Current VDHP	I _{QVDH1}	-	-	61	μA	$V_{VDHP} \le 60 \text{ V};$ $T_j \le 25^\circ\text{C};$ $V_{INH} = V_{SOFF} = \text{GND}^{14};$ $V_{SHv} = \text{GND}$	P_8.3.48	Quiescent Current VDHP I_{QVDH1} - - 61 μA $V_{VDHP} \le 60 V;$ P_8.3.48 $T_1 \le 25^\circ C;$ $V_{INH} = V_{SOFF} = GND^{49};$ $V_{SHx} = GND$ - -
.3 Electrical Characteristics Power	Quiescent Current VDHP	I _{QVDH1}	-	-	61	μA	$V_{\text{VDHP}} \le 60 \text{ V};$ $T_j \le 150^{\circ}\text{C};$ $V_{\text{INH}} = V_{\text{SOFF}} = \text{GND}^{14};$ $V_{\text{SHx}} = \text{GND}$	P_8.3.30	Quiescent Current VDHP I_{QVDH3} - 61 μA $V_{VDHP} \le 60 V;$ P_8.3.30 $T_j \le 150^{\circ}C;$ $V_{NH} = V_{SOFF} = GND^{49};$ $V_{SHx} = GND$ $V_{SHx} = GND^{49};$ $V_{SHx} = GND^{$
Supply	Total Quiescent Current Vs and VDHP	1 _{Q2}	-	-	17	μA	$V_{VS} = V_{VDHP} \le 14 \text{ V};$ $T_j = 25^{\circ}\text{C};$ $V_{INH} = V_{SOFF} = \text{GND}^{14)};$ $V_{SHx} = \text{GND}$	P_8.3.49	Total Quiescent Current Vs and V_{Q1} - 17 μA $V_{VS} = V_{VDHP} \le 14 V;$ P_8.3.49 VDHP VDHP $T_j = 25^{\circ}C;$ $V_{NH} = V_{SOFF} = GND^{49};$ $V_{SHx} = GND$
	Total Quiescent Current Vs and VDHP	I _{Q2}	-	-	70	μA	$\begin{split} V_{\rm VS} &= V_{\rm VDHP} \leq 14 \text{ V}; \\ T_{\rm j} &= 150^{\circ}\text{C}; \\ V_{\rm INH} &= V_{\rm SOFF} = \text{GND}^{14}; \\ V_{\rm SHx} &= \text{GND} \end{split}$	P_8.3.33	Total Quiescent Current Vs and VDHP I_{Q2} -70 μA $V_{VS} = V_{VDHP} \le 14 V;$ $T_j = 150°C;$ $V_{INH} = V_{SOFF} = GND^{49};$ $V_{SHx} = GNDP_8.3.33$



Datasheet Chapter	TLE918	0C-20QK D TLE		1 / TLE9 31QK D			95 V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10				
7.3 Electrical Characteristics Power Supply	2) Filter Time Accuracy referenced from	internal clock	k accurad	cy, please	see Chaj	oter 6.2			⁸⁷ Internal clock frequency accuracy has to be added to the specified values, please see <i>Chapter 6.2</i>			
	Table 12 Electrical Characte		SFET d	lrivers	0.0		4	0.041	Table 12 Electrical Characteristics MOSFET drivers			
	Low Level Output Voltage Gxx-Sxx	V _{GS_LL}	-	-	0.2	V	$I_{\text{DCLoadOS}} \le -2 \text{ mA};$ $V_{\text{ENA}} = \text{Low or}$ Pins IHx and ILx = off	P_9.4.1	Low Level Output Voltage V_{GS_LL} 0.2 V $0 \text{ mA} \le I_{DCLoadOS} \le 2 \text{ mA};$ P_9.4.1 Gxx-Sxx Pins IHx and ILx=off			
8.4 Electrical Characteristics Floating	Low Level Output Voltage Gxx-Sxx	V _{GS_LLS}	-	-	0.2	v	$V_{\text{SOFF}} = \text{Low};$ $I_{\text{DCLoadOS}} = \le -2 \text{ mA}$	P_9.4.2	Low Level Output Voltage V_{GS_LLS} 0.2V V_{SOFF} =Low; 0 mA $\leq I_{DCLoadOS} \leq 2mA$ P_9.4.2			
MOSFET Driver	High Level Output Voltage Gxx- Sxx ¹⁾	V _{G_HL2}	8	-	12.5	V	5.5 V $\leq V_{VS} < 7$ V; $C_{CPx} = 1.0 \mu$ F; $C_{CB} = 4.7 \mu$ F;	P_9.4.4	High Level Output Voltage Difference between Low-side Output Stages GLx-SLx $dV_{G_{HLS}}$ 0.5V $-2mA \le I_{DCLoadOS} \le 0 \text{ mA}$; $V_{SLx}=0V$ P_9.4.5			
							$I_{\text{DCLoadOS}} = -2 \text{ mA};$ $V_{\text{SLx}} = V_{\text{SHx}} = 0 \text{ V}$	D 0.15	High Level Output Voltage $dV_{G_{HHS}}$ 0.5V $-2mA \le I_{DCLoadOS} \le 0$ mA; $V_{SHx}=0V$ P_9.4.6			
	High Level Output Voltage Difference between Low-side Output Stages GLx-SLx	dV _{G_HLS}	-	-	0.5	V	$I_{\rm DCLoadOS} \le -2 \text{ mA};$ $V_{\rm SLx} = 0 \text{ V}$	P_9.4.5	Output Stages GHx-SHx			
	Table 12 Electrical Characte	ristics MO	SFET d	rivers (cont'd)				Table 12 Electrical Characteristics MOSFET drivers (cont'd)			
8.4 Electrical Characteristics Floating MOSFET Driver	Turn On Gate Current	I _{G(on)1}	-0.75	5 -2.0	-	A	$V_{BS} \ge V_{BSUV};$ $V_{Gxx} - V_{Sxx} = 0 V$	P_ <u>9.4.14</u>	Turn On Gate Current $I_{G(on)1}$ 2.0-0.75.A $V_{BS} \ge V_{BSUV}$; $V_{Gxx} - V_{Sxx} = 0 V$ P_9.4.14			
	Table 12 Electrical Characteristic	s MOSFET dr	ivers (co	ont'd)					Table 12 Electrical Characteristics MOSFET drivers (cont'd)			
8.4 Electrical Characteristics Floating MOSFET Driver	Propagation Delay Time (all low-side FETs off) $t_{P(IL)}$	´	35		V	_{Load} = 2 _{Sxx} = 0 V			Propagation Delay Time (all low- side FETs off) $t_{P(LF)}$ 253570ns $R_{Load} = 2 k\Omega^{52}$; $V_{Sxx} = 0 V$ P_9.4.19			
	Propagation Delay Time (all high-side FETs off) $t_{\rm P(H)}$	_{F)} 30	35	70	ns R V	_{Load} = 2 _{Sxx} = 0 V	kΩ ³⁾ ; P_9.4.21		Propagation Delay Time (all high- side FETs off) $t_{P(IHF)}$ 25.35.70.ns. $R_{Load} = 2 k\Omega^{52}$; $V_{Sxx} = 0 V$ P_9.4.21			



Datasheet Chapter		TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01											TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10								
	Table 12 Electrical Cha	racteristics M	OSFET d	drivers (c	cont'd)	i)					Table 12			MOSFET	drivers (c	ont'd)					
	Propagation Delay Time Matc (all FETs on)	ning t _{P(an)}	-	-	20	ns	$R_{\text{Load}} = 2$ $V_{\text{Sxx}} = 0$		P_9.4.22		Propagati (all FETs o	on Delay Time <mark>Misr</mark> n)	natch t _{P(an)}	-	-	20		R _{Load} = 2 kΩ ⁵²⁾ ; V _{Sxx} = 0 V	P_9.4.22		
8.4 Electrical Characteristics Floating MOSFET Driver	Propagation Delay Time Matc (all FETs turn off)	ning t _{P(af)}	-	-	20	ns	$R_{\text{Load}} = 2$ $V_{\text{Sxx}} = 0$	2 kΩ ³⁾ ;	P_9.4.23		Propagati (all FETs t	on Delay Time <mark>Misr</mark> urn off)	natch t _{P(af)}	-	-	20		$R_{Load} = 2 k\Omega^{52};$ $V_{Sxx} = 0 V$	P_9.4.23		
	Propagation Delay Time Matc Single Phase (high-side off to side on)		0	-	20	ns	$R_{\text{Load}} = 2$ $V_{\text{Sxx}} = 0$		P_9.4.24		Propagati Single Pha side on)	on Delay Time <mark>Misr</mark> ase (high-side off to	low-	_{n)} 0	-	20		$R_{\text{Load}} = 2 \text{ k}\Omega^{52};$ $V_{\text{Sxx}} = 0 \text{ V}$	P_9.4.24		
	Propagation Delay Time Matc Single Phase (low-side off to l side on)	igh-	0	-	20	ns	$R_{\text{Load}} = 2$ $V_{\text{Sxx}} = 0$	2 kΩ ³⁾ ; V	P_9.4.25		Propagati Single Pha side on)	on Delay Time <mark>Misr</mark> ase (low-side off to	natch t _{P(1lfh} high-	_{n)} 0	-	20		$R_{\text{Load}} = 2 \text{ k}\Omega^{52};$ $V_{\text{Sxx}} = 0 \text{ V}$	P_9.4.25		
	Propagation Delay Time Matc all Phases (all high-sides off to low-sides on)	hing t _{P(ahfin)} all	0	-	20	ns	$R_{\text{Load}} = 2$ $V_{\text{Sxx}} = 0$	2 kΩ ³⁾ ; V	P_9.4.26		Propagati all Phases low-sides	on Delay Time <mark>Misr</mark> ; (all high-sides off t on)	natch t _{P(ahf} o all	n) 0	-	20		$R_{\text{Load}} = 2 \text{ k}\Omega^{52};$ $V_{\text{Sxx}} = 0 \text{ V}$	P_9.4.26		
	Propagation Delay Time Matc all Phases (all low-sides off to high-side on)	hing t _{P(alfhn)}	0	-	20	ns	$R_{\text{Load}} = 2$ $V_{\text{Sxx}} = 0$		P_9.4.27			on Delay Time <mark>Misr</mark> ; (all low-sides off to on)		n) 0	-	20		R _{Load} = 2 kΩ ⁵²⁾ ; V _{Sxx} = 0 V	P_9.4.27		
	Table 18 Electrical Cha	racteristics - S	Shunt Sig	gnal Con	ndition	ning (co	ont'd)				Table 18	Electrical Chara	cteristics - S	Shunt Sig	nal Cond	itioning	(cont'd)				
.5 Electrical Parameter Shunt Signal onditioning	Slew Rate	SR	-	- 1	15	-	V/µs	-	P_1	0.5.22	Slew Rate		SR .	-	15	-	V/µs	-	P_10.5.22		
											60 Not	subject to production	on test, speci	fied by de	<mark>sign</mark>						
	Table 24 Shutdown E	ror Overview	1)								Table 24	Shutdown Erro	r Overview ¹								
	Bit Bit Name Position	Descriptio				S	Output Stages	Charge Pumps	ERR Pin		Bit Position	Bit Name	Description				Output Stages	Charge Pumps	ERR Pin		
0.2.2 Failure Behavior Configuration	3 sd_clk_fail	Internal Clo						Active	Low (LE)	_	3	sd_clk_fail	Internal Cloc Shutdown ⁸²		sion		ARE <mark>or LE</mark>	Active	Low (ARE or LE)		
	3) In the case of monitoring c	3) In the case of monitoring clock stops operation fault reaction of output stages is latched error												82 Failuré reaction can be ARE or LE dependent on type of internal fault							
	Table 24 Shutdow	n Error Overv	view ⁷⁸⁾								Table 24	Shutdow	n Error Over	view ⁷⁸⁾							
0.2.2 Failure Behavior Configuration	Bit Bit Name Position	Description					Output Stages	Charge Pumps	ERR P	n	Bit Position	Bit Name	Descriptio	n			Outpu Stage		ERR Pin		
	Position								1												



Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
10.5.16 Overload Digital Output Pins	 10.5.16 Overload Digital Output Pins The digital outputs are protected against short to GND and battery. If one output is shorted the output pad will be disconnected, a dedicated error register bit will be set. The pin ERR will be set to low. To unlock the output pin reset with ENA has to be performed. The failure behavior of the gate driver IC is adjustable at configuration mode, either the output stages will turn all external FETs off or not. Functionality of the overload detection of the digital output pins is limited, for details please refer to Chapter 16.3.8. Register Err_outp bit 4 to bit 0 indicate a short of a digital output pin. 	10.5.16 Overload Digital Output Pins The digital outputs are protected against short to GND and battery. If one output is shorted the output pad will be disconnected, a dedicated error register bit will be set. The pin ERR will be set to low in case pin ERR is not the affected pin. To unlock the output pin reset with ENA has to be performed. The failure behavior of the gate driver IC is adjustable at configuration mode, either the output pins is limited, for details please refer to Chapter 16.3.7. Register Err_outp bit 4 to bit 0 indicate a short of a digital output pin.
10.5.4 High-side Buffer Capacitor Voltage Monitoring	10.5.4 High-side Buffer Capacitor Voltage Monitoring An overvoltage monitoring for the external high-side buffer capacitor guarantees gate source voltage for the external FET not higher as the destructive gate source voltage. Failure behavior and filter time is not configurable. High-side buffer overvoltage monitoring can be deactivated at configuration if diagnosis is not required. In case of overvoltage detection all output stages remain active but charge pump 2 will be deactivated. A reset via ENA is necessary for reactivation of charge pump 2. If overvoltage high-side buffer has been detected and charge pump 2 has been turned off duty cycle operation higher than 95% is not recommended and might end up in undervoltage high-side buffer detection.	10.5.4 High-side Buffer Capacitor Voltage Monitoring An overvoltage monitoring for the external high-side buffer capacitor detects too high gate source voltages for the external FET. The failure behavior and filter time are not configurable. In case of an overvoltage detection, the ERR pin is set low and the dedicated error bit in the register is set. The 2 nd charge pump is deactivated and all output stages remain active. A reset via ENA is necessary for the reactivation of the 2 nd charge pump. If the 2 nd charge pump is deactivated, an undervoltage high-side buffer detection might occur mainly at operation with high duty cycles. The overvoltage monitoring for the external high-side buffer capacitor can be deactivated at configuration.
10.5.11.2 S Self-test Function for SCD <u>Modification valid for</u> <u>TLE9180C-21QK & TLE9180C-31QK</u>	immed (new for the formation of the format	Sequence: Enter Self Test mode Sequence: Enter Self Test mode Bit et_scd_, is set in Self et_1 ¹ (add:::0.025; Dt5) Bit et_scd_, is reset in Self et_1 ² Bit et_scd_, is reset in Self et_1 ² (add:::0.025; Dt5) Unit: SCD blanking& filter time Unit: SCD blanking& filter time Unit: SCD blanking& filter time Due_tit of atticked low side FETs Readout register dung hX (add:::0.025) Provide the side filter dung hX (add:::0.025) Bit et_scd_, is reset in Self et_1 ² Bit et_scd_, is reset in Self et_1 ³ Bit



Datasheet Chapter	TLE9	180C-20QH TI		01 / TLE -31QK [S V1.01		TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10									
	Table 53 Electrical Charact	teristics - F	rotecti	on and I	Diagnos	tic Fun	ctions (cont'd)		Table 53 Electrical Characteristics - Protection and Diagnostic Functions (cont'd)								
10.6 Electrical Characteristics Protection and Diagnostic Functions	Accuracy Undervoltage Threshold Vs	V _{VSUVacc2}	-13.5	PROG	+13.5	%	4.4 V ≥ V _{VSUV} < 7.5 V	P_11.6.12	Accuracy Undervoltage Threshold Vs	V _{VSUVacc2}	-13.5	PROG	+13.5	%	4.2 V ≤ V _{VSUV} < 7.	5V P_11.6.12	
	Table 53 Electrical Charac	teristics -	Protect	ion and	Diagno	stic Fu	inctions		Table 53 Electrical Charact	eristics - F	rotecti	on and	Diagno	stic Fu	nctions		
	Entry Filter and Reaction Time of Reduced Operation Mode Detection at Vs	V _{VsROPf1}	0.6	-	20	μs	4)	P_11.6.8	Entry Filter and Reaction Time of Reduced Operation Mode Detection at Vs	t _{vsROPf1}	0.6	-	-	μs	89)	P_11.6.8	
	Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs	V _{vsROPf2}	20	-	-	μs	4)	P_11.6.9	Exit Filter and Reaction Time of Reduced Operation Mode Detection at Vs	t _{vsROPf2}	20	ē.	-	μs	89)	P_11.6.9	
10.6 Electrical Characteristics	Table 53 Electrical Charac	teristics - I	Protect	ion and	Diagno	stic Fu	nctions		Table 53 Electrical Charac	teristics -	Protec	tion and	d Diagn	ostic F	unctions		
Protection and Diagnostic Functions	Entry Filter and Reaction Time of Reduced Operation Mode Detection at VCC	V _{VCCROPf1}	0.6	-	-	μs	4)	P_11.6.78	Entry Filter and Reaction Time of Reduced Operation Mode Detection at VCC	tvccrop	0.6	-	-	μ	5 89)	P_11.6	
	Exit Filter and Reaction Time of Reduced Operation Mode Detection at VCC	V _{VCCROPf2}	20	_	-	μs	4)	P_11.6.79	Exit Filter and Reaction Time of Reduced Operation Mode Detection at VCC	t _{vccrop}	2 20	-	-	μ	89)	P_11.6	
	Temperature Read Out Accuracy	t _{Tread_f}	-25	-	+25	к	-	P_11.6.115	Temperature Read Out Accuracy	T _{Tread_a}	-25	-	+25	к	-	P_11.6.115	
									Table 53 Electrical Character	istics - Prot	ection a	nd Diagn	ostic Fu	nctions	(cont'd)		
10.6 Electrical Characteristics Protection and Diagnostic Functions	Table 53 Electrical Characteris Filter Time of SCD ^{2 3)}			PROG 6		IS 4		1.6.69	Filter Time of SCD ^{87]88)}	t _{SCDf}	0.5 1.7 3.4 5.7	PROG	2.3 3.5 5.2 7.5	μs	f_fi_scd = '0x0' f_fi_scd = '0x1' f_fi_scd = '0x2' f_fi_scd = '0x3'	P_11.6.69	
	Table 53 Electrical Characteristics	- Protection	and Diag	nostic Fu	nctions (cont'd)			Table 53 Electrical Characteristic	s - Protectio	n and Dia	gnostic F	unctions	(cont'd)			
10.6 Electrical Characteristics	ENA Low Tim <mark>e Clearing L</mark> atched Errors	clear 2.	2 3.0	3.8	μs	ENA fa	lling edge P_11.6.104	4	ENA Low Time Threshold for Clearing Latched Errors	t _{clear}	2.2	3.0	3.8	μs E	NA falling edge	P_11.6.104	
Protection and Diagnostic Functions	Latched Errors	Res -	1.0	107-3	μs	-	P_11.6.105	22 22	Return Time to Normal Operation for ARE Fault Behavior	t _{RT}	- 2	-	1.0	μs –	S	P_11.6.106	
	Return Time to Normal Operation for ARE Fault Behavior Configuration ²⁾	RT	-	1.0	μs	-	P_11.6.106	D	Configuration ⁸⁷⁾								



P_11.6.5

P_11.6.14

P_11.6.19

P_11.6.29

P_11.6.43

P_11.6.52

P_11.6.69

P_11.6.85

f_ov_vs = '0x0' f_ov_vs = '0x1' f_ov_vs = '0x2' f_ov_vs = '0x3' f_uv_vs = '0x0'

f_uv_vs = '0x1' f_uv_vs = '0x2' f_uv_vs = '0x3'

 $f_ov_vdh = '0x0'$

f_ov_vdh = '0x1' f_ov_vdh = '0x2' f_ov_vdh = '0x3'

f_uv_vdh = '0x0' f_uv_vdh = '0x1' f_uv_vdh = '0x2' f_uv_vdh = '0x3' f_uv_cb = '0x0'

f_uv_cb = '0x1' f_uv_cb = '0x2' f_uv_cb = '0x3' f_uv_bs = '0x0'

f_uv_bs = '0x1' f_uv_bs = '0x2' f_uv_bs = '0x3'

f_fi_scd = '0x0'

f_fi_scd = '0x1' f_fi_scd = '0x2' f_fi_scd = '0x3' f_uv_vcc =

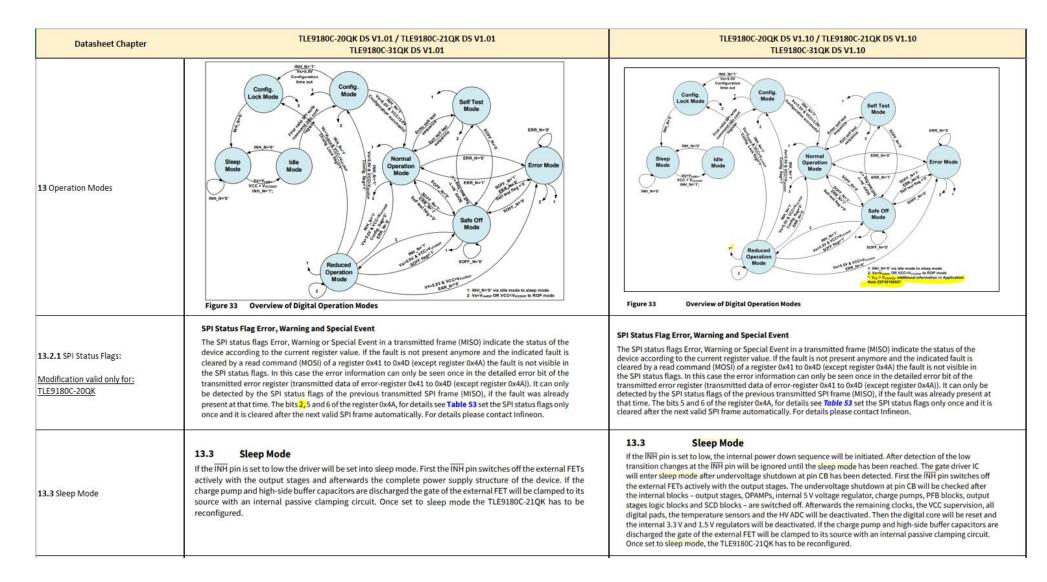
f_ov_vcc = '0x0' f_uv_vcc = f_ov_vcc = '0x1' f_uv_vcc = f_ov_vcc = '0x2' f_uv_vcc = f_ov_vcc = '0x3'

Datasheet Chapter	TLE	9180C-20C		1.01 / TL DC-31QK		TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10									
									Table 53 Electrical Character	istics - Prote	ction an	d Diagnos	stic Funct	tions	
	Table 53 Electrical Characteria Overvoltage Detection and	teristics	- Prote	ction an	d Diag	µs	4 steps	P_11.6.5	Overvoltage Detection and Shutdown Filter Time Range	tovvs	8 24	-	17 33	μs	f_ov_vs
	Shutdown Filter Time Range Vs ²⁾³⁾	*OVVS				μο	programmable		Vs ⁸⁷⁾⁸⁸⁾		48		57		f_ov_v
	Undervoltage Filter Time Range Vs ²⁾³⁾	t _{uvv3r}	10	-	100	μs	4 steps programmable	P_11.6.14	Undervoltage Filter Time Range		96 8	ļ	105 17		f_ov_vs
	Overvoltage Detection and Shutdown Filter Time Range VDHP ²⁾³⁾	t _{ovvDHr}	10	-	100	μs	4 steps programmable	P_11.6.19	Vs ⁸⁷⁾⁸⁸⁾	t _{UVVSr}	8 24 48	-	33 57	μs	f_uv_v f_uv_v f_uv_v
	Undervoltage Filter Time Range VDHP ²⁾³⁾	<i>t</i> _{UVVDHr}	10	-	100	μs	4 steps programmable	P_11.6.29	Overvoltage Detection and	t _{OVVDHr}	96 8	-	105 17	μs	f_uv_v
	Undervoltage Detection and Shutdown Filter Time Range CB ^{2 3)}	t _{UVCBr}	10	-	100	μs	4 steps programmable	P_11.6.43	Shutdown Filter Time Range VDHP ⁸⁷⁾⁸⁸⁾		24 48		33 57		f_ov_v
	Undervoltage Detection Filter Time BHx-SHx ²⁾³⁾	<i>t</i> _{UVBS}	1	-0	10	μs	4 steps programmable	P_11.6.52			96		105		f_ov_v
	Filter Time of SCD ²⁾³⁾	t _{SCDf}	1	PROG	6	μs	4 steps programmable	P_11.6.69	Undervoltage Filter Time Range VDHP ⁸⁷⁾⁸⁸⁾	t _{UVVDHr}	8 24	-	17 33	μs	f_uv_vo
	VCC Filter Time ²⁾³⁾	t _{VCCf}	10	-	100	μs	4 steps programmable	P_11.6.85			48 96		57 105		f_uv_v
10.6 Electrical Characteristics									Undervoltage Detection and Shutdown Filter Time Range	t _{UVCBr}	8 20	-	13 25	μs	f_uv_cl
rotection and Diagnostic Functions									CB ⁸⁷⁾⁸⁸⁾		48		53		f_uv_cl
									Undervoltage Detection Filter	t _{UVBS}	96 0.8	-	101 1.8	μs	f_uv_cl
									Time BHx-SHx ⁸⁷⁾⁸⁸⁾	LOVBS	2.8	-	3.8	μs	f_uv_b
											4.8		5.8		f_uv_b
											9.8		10.8		f_uv_b
									Filter Time of SCD ⁸⁷⁾⁸⁸⁾	t _{SCDf}	0.5	PROG	2.3	μs	f_fi_sc
											1.7		3.5		f_fi_sc
											3.4 5.7		5.2 7.5		f_fi_so
									VCC Filter Time ⁸⁷⁾⁸⁸⁾	t _{vccf}	8	-	17	μs	f_uv_v f_ov_v
											24	1	33	1	f_uv_v f_ov_v
											48		57]	f_uv_v f_ov_v
										1	96	1	<u> </u>	1	f_uv_v



Datasheet Chapter	TLE	9180C-20C	IK DS V1 TLE9180				DS V1.01		TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10									
	Table 12 Electrical Chara	cteristics	MOSFET	T driver	s (cont	'd)			Table 12 Electrical Charact	eristics M	OSFET d	rivers	(cont'd)					
8.4 Electrical Characteristics Floating MOSFET Driver	Programmable Dead Time Range	t _{DTr}	107	-	5998	ns	166 steps programmable	P_9.4.30	Programmable Dead Time Range ^{\$7)}	t _{DTr}	107	-	5998	ns	166 steps programmable	P_9.4.30		
									57 Dead time can additional	ly take up	to one in	ternal	clock cy	cle for	synchronization			
10.5 Electrical Characteristics Protection and Diagnostic Functions	Table 53 Electrical Charac	teristics -	Protect	tion and	Diagn	ostic F	unctions (cont'd)		Table 53 Electrical Chara	cteristics	- Protec	tion ar	nd Diagr	nostic	Functions (cont'd)	9		
	VCC Read Out	-	-	3		-			VCC Read Out									
Modification valid for: TLE9180C-21QK & TLE9180C-31QK	Voltage Detection Pange / I/ I I I I I I I I I I I I I I I I I							Voltage Detection Range	V _{ADCr}	0	-	5.55	V	0 to FFh	P_11.6.86			
	Table 53 Electrical Charact		Protectio	on and D	iagnos	tic Fun	ctions (cont'd)		Table 53 Electrical Characte	ristics - Pr	otection	and D	iagnosti	c Func	tions (cont'd)			
10.6 Electrical Characteristics Protection and Diagnostic Functions	Digital Driving Path Monitoring			1		Digital Driving Path Monitoring			500		ns		P_11.6.92					
	Digital Driving Path Monitoring Filter Time ²⁽³⁾	tSTDTf	-	500	-	ns	-	P_11.6.92	Filter Time ⁸⁷⁾⁸⁸⁾	TSTDTf1		500	-	11.5	-	r_11.0.52		
	Input Pattern Violation Filter and Reaction Time ²⁾	t _{stdtf}	-	750	-	ns	-	P_11.6.93	Input Pattern Violation Filter and Reaction Time ⁸⁷⁾	t _{stdtf3}	-	750	-	ns	-	P_11.6.93		
10.5.8.2 Temperature Read Out	10.5.8.2 Temperature The absolute temperature car Six sensors are integrated more out. The signal is filtered with operation mode it is required higher temperature at one ou at the affected output stage, independent to the sensor use Measurement results are store and temp_hs3 .	be read in nitoring all n a moving to wait 1 to wait 1 to ut stage wither inte ed for temp	empera ansition ture rea ttern ap ernal cir shutdov	ture of every output from configuration adout will be perfor oplied will indicate rcuit. The six tempory wn.	10.5.8.2 Temperat The absolute temperature can b Six sensors are integrated monit out. The signal is filtered with a r operation mode it is required to higher temperature at one outpu at the affected output stage, eith independent to the sensor used Measurement results are stored temp_hs3.	e read in the oring all out noving aver wait 1 ms be ut stage with er internally for tempera	e related S put stage age filter. efore first a regula y or cause ture dete	s. So th After tra temper PWM p ed by exit	e temper ansition f ature rea attern ap ternal cirr ad shutdo	ature o from co dout w oplied w cuit. Th	f every output stage of nfiguration mode to ill be performed. A sig vill indicate some irre e six temperature ser	normal gnificant gularities nsors are						
	Table 55 Electrical Char	acteristic	s - Phas	se Feed	back	_			Table 55 Electrical Char	acteristic	s - Phas	e Feed	back					
11.2 Electrical Parameter Phase	Propagation Delay Time	t _{PDfb}	-	60 70	100 100		50%/50% selected 80%/25% selected	P_12.2.6	Propagation Delay Time	t _{PDfb}	-	60	110	ns	50%/50% selected	0 1226		







Datasheet Chapter		τι		: DS V1.01 / TLE9180C-21QK DS V1.01 LE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10								
14.1.1.13 Short Circuit Detection & Signal Path Supervision Failure Modes Modification done in: ILE9180C-20QK	fm_osfb 3:	:2	11 _B 10 _B 01 _B		fm_osfb	3:2	none	fixed bit field for TLE9180 basic 00 _B , fixed value for TLE9180 basic					
	Err_scd Short Circuit Erro	ors		Offset Reset Value 47 _H 00 _H	Err_scd Short Circuit Errors			Offset Reset Value 47 _H 00 _H					
	Field	Bits	Туре	Description	Field	Bits	Туре	Description					
L5.1.4.8 Short Circuit Errors	err_scd_hs1	7	rc	Short Circuit at High-side 1 1	err_scd_hs1	7	rc	Short Circuit Detection at High-side 1 1 _B , Error set 0 _B , No error					
	err_scd_hs2	6	rc	Short Circuit at High-side 2 1 _B , Error set 0 _B , No error	err_scd_hs2	6	rc	Short Circuit Detection at High-side 2 1 _B , Error set 0 _B , No error					
	err_scd_hs3	5	rc	Short Circuit at High-side 3 1 _B , Error set 0 _B , No error	err_scd_hs3	5	rc	Short Circuit Detection at High-side 3 1 _B , Error set 0 _B , No error					
	err_scd_ls1	4	rc	Short Circuit at Low-side 1 1 _B , Error set 0 _B , No error	err_scd_ls1	4	rc	Short Circuit Detection at Low-side 1 1 _B , Error set 0 _B , No error					
	err_scd_ls2	3	rc	Short Circuit at Low-side 2 1 _B , Error set 0 _B , No error	err_scd_ls2	3	rc	Short Circuit Detection at Low-side 2 1 _B , Error set 0 _B , No error					
	err_scd_ls3	2	rc	Short Circuit at Low-side 3 1 _B , Error set 0 _B , No error	err_scd_ls3	2	rc	Short Circuit Detection at Low-side 3 1 _R , Error set 0 _B , No error					
	Res	1:0	none	Reserved 00 _B , default value. do not change.	Res	1:0	none	Reserved 00 _B , default value. do not change.					
16 Application Information	Generation Simple	bilified Applic	ention Circuit	Convert Series Bands to D20 matter that measurements to D20 matter that measurements Convert Series Bands Convert		sattery protection diod		tion Circuit					



Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10
16.1 Layout Guide Lines	 Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors) The exposed pad on the backside of the package is recommended to connect to GND VDHP has to be connected and referenced to a common point of the drains of the high-side MOSFETs For further information you may contact http://www.infineon.com/ 	 Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors) The exposed pad on the backside of the package is recommended to connect to GND The ground pins GND, CP_GND, A_GND have to be connected together to the PCB GND closely to the chip VDHP has to be connected and referenced to a common point of the drains of the high-side MOSFETs For further information you may contact http://www.infineon.com/
16.2.1 Additional Components	 ³⁾ D2 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin V_s. Voltage drops at pin Vs in the range from 13V down to 6V shall not be shorter than 100μs. In the case of faster slew reates an input filter is required. For details please contact Infineon. ⁴⁾ D4 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after CB capacitor has been shorted to GND. 	 ³⁾ D2 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs with a slew rate ≥ 6V/100µs. D2 is not required with sufficient input filtering at the Vs pin. ⁴⁾ D4 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data.
16.2.1 Additional Components	^{a)} D3 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs. The effect can be avoided with sufficient input filtering with C _{vs} and (R _{vs} or D1).	⁸⁾ D3 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs with a slew rate ≥ 6U/100µs. D3 is not required with sufficient filtering at the Vs pin. In case D3 is not used a 100 kΩ pull down to GND at CL1 shall be placed.
16.3.2 Cross Talk of Automatic Recharging Circuits	 16.3.2 Quiescent Current Consumption at Pin Vs Please refer to Table 10. After pulling INH to low the quiescent current can be up to 20 μA at pin Vs for a short period of time. The effect is strongly temperature dependent. Under hot conditions the decay time is in the range of seconds, at ambient conditions in the range of minutes and at cold up to 1h. 16.3.3 Cross Talk of Automatic Recharging Circuits Please refer to Chapter 7.3 and Chapter 8.4. Cross talk of the high-side buffer recharging circuit of phase 2 and phase 3 to phase 1 has been identified. This might lead to a higher high-side buffer supply capacitor voltage between pins BH1 to SH1. Higher gate voltages for high-side FET 1 has been observed. Gate source voltage of 15 V will not be exceeded. 16.3.4 Minimum Input Pulses at Pins IHx and ILx	 16.3.2 Quiescent Current Consumption at Pin Vs Please refer to Table 10. After pulling INH to low the quiescent current can be up to 20 μA at pin Vs for a short period of time. The effect is strongly temperature dependent. Under hot conditions the decay time is in the range of seconds, at ambient conditions in the range of minutes and at cold up to 1h. 16.3.3 Minimum Input Pulses at Pins IHx and ILx Please refer to Chapter 8.4.

Datasheet Chapter	TLE9180C-20QK DS V1.01 / TLE9180C-21QK DS V1.01 TLE9180C-31QK DS V1.01	TLE9180C-20QK DS V1.10 / TLE9180C-21QK DS V1.10 TLE9180C-31QK DS V1.10								
	Table 12 Electrical Characteristics MOSFET drivers	Table 12 Electrical Characteristics MOSFET drivers								
8.4 Electrical Characteristics Floating MOSFET Driver	High Level Output Voltage Gxx- Sxx ¹⁾ $V_{G_{HL1}}$ 8.5-13.5V $7 V \le V_{VS} < 60 V;$ $C_{CPx} = 1.0 \mu F;$ $C_{CB} = 4.7 \mu F;$ $I_{DCLoadOS} = -2 mA;$ $V_{SLx} = V_{SHx} = 0 V$ P_9.4.3	High Level Output Voltage Gxx-Sxx $V_{G_{HL1}}$ 8.5-13.5V $7 V \le V_{VS} < 60 V;$ $C_{CPX} = 1.0 \ \mu F;$ $C_{CB} = 4.7 \ \mu F;$ $I_{DCLoadOS} = -2 \ mA;$ $V_{SLX} = V_{SHX} = 0 \ V$ P_9.4.3								
	High Level Output Voltage Gxx- Sxx ¹⁾ $V_{G_{HL2}}$ 8-12.5V5.5 V $\leq V_{VS} < 7 V;$ $C_{CPx} = 1.0 \mu F;$ $I_{DCLoadOS} = -2 mA;$ $V_{SLx} = V_{SHx} = 0 V$ P_9.4.41)Max. limit may differ for output stage HS1. Output voltage of GH1-SH1 might be higher. For details please refer to Chapter 16.3.30	High Level Output Voltage Gxx-Sxx $V_{G_{HL2}}$ 8-12.5V5.5 V $\leq V_{VS} < 7 V;$ $C_{CPx} = 1.0 \ \mu F;$ $C_{CB} = 4.7 \ \mu F;$ $I_{DCLoadOS} = -2 \ mA;$ $V_{SLx} = V_{SHx} = 0 \ V$ P_9.4.4								
16.3.3 Minimum Input Pulses at Pins IHx and ILx	 16.3.4 Minimum Input Pulses at Pins Hx and ILx Please refer to Chapter 8.4. Input turn on pulses at the pins Hx and ILx shorter than 50 ns may cause an increase of the turn on time of the external FET to maximum 1000 ns. Short voltage glitches at the pin CB have been observed. If 6 μC output ports are used to drive 6 FETs and dead time is generated by the μC avoid input pulses at Hx and ILx shorter than 50 ns. If 3 μC output ports are used to drive 6 FETs using the internal dead time of the TLE9180C-21QK avoid input pulses at Hx and ILx shorter than the internal dead + 50 ns. In case of glitches at pin CB has been identified please contact Infineon. 	 16.3.3 Minimum Input Pulses at Pins IHx and ILx Please refer to Chapter 8.4. Input turn on pulses at the pins IHx and ILx shorter than 50 ns may cause an increase of the turn on time of the external FET to maximum 1000 ns. Short voltage glitches at the pin CB have been observed. If 6 μC output ports are used to drive 6 FETs and dead time is generated by the μC avoid input pulses at IHx and ILx shorter than 1 pulse. in. If 3 μC output ports are used to drive 6 FETs using the internal dead time of the TLE9180C-21QK avoid input pulses at IHx and ILx shorter than the internal dead the internal dead time of the TLE9180C-21QK avoid input pulses at IHx and ILx shorter than the internal dead to pulses in. In case of glitches at pin CB has been identified please contact Infineon. 								



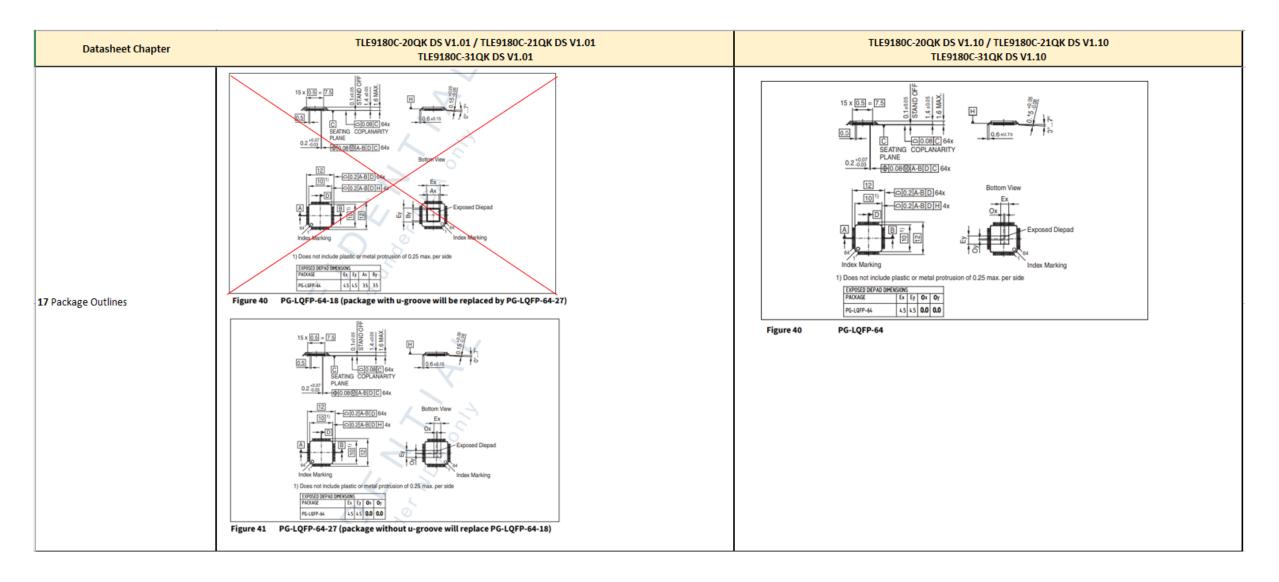




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Datasheet Chapter							QK DS V1.10/ / TLE9180D-26QI	K V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10							
	Table 2 Absolute		Table 2 Absolute Maximum Ratings													
	Supply Voltage	V _{Vs1}	-0.3	-	60	V	-	P_4.1.1								
	Voltage Range VDHP	V _{VDHP1}	-5	-	85	v	3)	P_4.1.3	Supply Voltage	V _{Vs1}	-0.3	-	40	v	-	P_4.1.1
	Voltage Difference Vs-VDHP	VdVsVDHP	-85		60	v	-	P_4.1.5	Voltage Range VDHP	V _{VDHP1}	-5	-	50	V	3)	P_4.1.3
	Voltage Range VDH1, VDH2, VDH3	V _{VDH×1}	-5	-	90	v	-	P_4.1.6	Voltage Range VDH1, VDH2, VDH3	V _{VDHx1}	-5	-	50	v	-	P_4.1.6
	Voltage Difference Vs-VDH1, VDH2,		-90	-	60	v		P_4.1.8	Voltage Range CL1	V _{CL1}	-0.3	-	40	v	-	P_4.1.9
	VDH3	UVSVDIIA						-	Voltage Range CL2, CH2	V _{CHL2}	-0.3	-	60	v	-	P_4.1.12
	Voltage Range CL1	V _{CL1}	-0.3	-	60	v	-	P_4.1.9	Voltage Range SHx	V _{SHx1}	-7	-	50	v	-	P_4.1.19
	Voltage Range CL2, CH2	V _{CHL2}	-0.3	-	90	v	-	P_4.1.12	Voltage Range GHx	V _{GHx1}	-7	-	60	v	-	P_4.1.22
	Voltage Range SHx	V _{SHx1}	-7	-	90	v	-	P_4.1.19	Voltage Range BHx	V _{BH}	-0.3	-	60	v	-	P_4.1.25
8.1 Absolute Maximum Ratings	Voltage Range GHx	V _{GHx1}	-7	-	90	v	-	P_4.1.22	Voltage Difference SHx-SLx ¹⁾	V _{SSx1}	-12	-	50	v	IHx = High	P_4.1.29
_	Voltage Range BHx	V _{BH}	-0.3	-	90	v	-	P_4.1.25	Voltage Range IHx, ILx, ENA	V _{DIP1}	-0.3	-	40	v	-	P_4.1.34
Nodification valid for TLE9180D-26QK only.	Voltage Difference SHx-SLx ¹⁾	V _{SSx1}	-12	-	90	v	IHx = High	P_4.1.29	Voltage Range VCC	V _{VCC1}	-0.3	-	40	v	-	P_4.1.35
	Voltage Difference VDHP-SHx	V _{dVDHPSHx2}		-	90	v		P_4.1.32	Voltage Range INH	VINH	-0.3	-	40	v	-	P_4.1.36
	Voltage Difference VDHx-SHx	VOVDHXSHX	-90		90	v	_	P_4.1.33	Voltage Range SOFF	VSOFF	-0.3	-	40	v	-	P_4.1.37
	Voltage Range IHx, ILx, ENA	V _{DIP1}	-0.3	-	60	v	-	P_4.1.34	Voltage Range PFBx, ERR	V _{DOP1}	-0.3	-	40	v	-	P_4.1.38
	Voltage Range VCC	V _{VCC1}	-0.3	-	60	v	-	P_4.1.35	Voltage Range APC	V _{AOP1}	-0.3	-	40	v	9)	P_4.1.39
	Voltage Range INH	V _{INH}	-0.3	-	90	v	-	P_4.1.36	Voltage Range CLK_SPI, CSN, MOSI		-0.3	-	40	v	-	P_4.1.40
	Voltage Range SOFF	V _{SOFF}	-0.3	-	90	v	-	P_4.1.37	Voltage Range MISO	V _{SPI2}	-0.3	-	40	v	-	P_4.1.41
	Voltage Range PFBx, ERR	V _{DOP1}	-0.3	-	60	v	-	P_4.1.38			_		_			
	Voltage Range APC	V _{AOP1}	-0.3		60	v	9)	P_4.1.39								
	Voltage Range CLK_SPI, CSN, MOSI	VAOP1	-0.3	-	60	v	-	P_4.1.40								
	Voltage Range MISO	V _{SPI2}	-0.3	-	60	v	_	P_4.1.41								
	Voltage Range MISO	* SPI2	-0.5	-	00		_	1,74,1,41								
3.1 Absolute Maximum Ratings	Table 2 Absolute Maximum	Ratings (co	ont'd)						Table 2 Absolute Maximum R	atings (con	t'd)					
Modification valid for:	Voltage Range APC	V _{AOP1}	-0.3	-	60	V	/ _	P_4.1.39	Voltage Range APC	V _{AOP1}	-0.3	-	60	v	<mark>9)</mark>	P_4.1.39
TLE9180D-21QK, TLE9180D-31QK, TLE9180D-32QK		1 1001							9 A short circuit at APC for >10hrs	might dam	age the d	evice				
3.1 Absolute Maximum Ratings	Table 2 Absolute Maximum R Temperatures	atings (cont	:'d)					<u> </u>	Table 2 Absolute Maximum Ra Temperatures	atings (cont	ťd)					
		T _{stg}	55	-	150	°C -	_	P_4.1.54	Storage Temperature 7	r _{stg}	-55 -	15	0 °C	-		P_4.1.54
Modification valid for all, except	Junction Temperature		40	-	150	°C ·	-	P_4.1.55			-40 -	15		11)		P_4.1.55
FLE9180D-26QK and TLE9183QK.	Junction Temperature		40	-	175	°C	200h over lifetime	P_4.1.56	For T _i >150°C please check compliant	1.000						1



Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10			
3.1 Absolute Maximum Ratings Modification valid for all data sheets, except TLE9180D-26QK & TLE9183QK.	Table 2 Absolute Maximum Ratings (cont'd) Max. Voltage Transients at SHx V _{ISH_III} - 20 V Slew rate ≤ 1 V/ns ^{7 1)} P_4.3.31 1 Not subject to production test, specified by design 7 Exceeding specified slew rate in combination with the maximum specified voltage transient may set the affected output stage in an undefined state for typically 1 µs	Table 2 Absolute Maximum Ratings (cont'd) Max. Voltage Transients at SHx $V_{fSH_{L}V1}$ - - 55 V Slew rate $\leq 1 V/ns^{7/11}$ P_4.3.31 1 Not subject to production test, specified by design 7 At amplitudes higher than 20 V the HS output stage can show unexpected switch off of the external MOSFET for typically 1 µs if the output stage is not switching. If the output stage is switching on or			
4.7 Electrical Characteristics IOs	1) Not subject of production test, specified by design	switching off, the output stage is switching normally even with amplitudes up 55 V and slew rates up to 1 V/ns 1) Not subject to production test, specified by design.			
4.7 Electrical Characteristics IOs Modification valid for all, except TLE9180D-26QK and TLE9183QK.	Table 6 Electrical Characteristics IOs (continued) Pin ENA ENA Propagation Time (for enable or disable the output stages) the propagation of the propa	Table 6 Pin ENA Electrical Characteristics IOS (continued) ENA Propagation Time (for enable or disable the output stages) t_{PENA} - 100 500 ns - P_5.7.17			
4.7 Electrical Characteristics IOs	Table 6Electrical Characteristics IOS (continued)High Level-Output Voltage V_{ERRHSD} 3.8- V_{VCC} V $V_{VSS} > 7.2 V_{:}$ P_5.7.24High Level-Output Voltage V_{ERRHSD} 3.8- V_{VCC} V $V_{VSC} = 5.0 V_{;}$ $h_{load} = -0.2 mA;$ Low Level Output Voltage V_{ERRL} -0.1-0.4V $I_{Load} = 0.2 mA$ P_5.7.39High Level-Output Voltage V_{SPHSD} 3.8- V_{VCC} V $V_{VS} > 7.2 V;$ P_5.7.39High Level-Output Voltage V_{SPHSD} 3.8- V_{VCC} V $V_{VS} > 7.2 V;$ P_5.7.51Low Level Output Voltage V_{SPHSD} 3.8- V_{VCC} V $V_{VS} > 7.2 V;$ P_5.7.51Low Level Output Voltage V_{SPHSD} 0.4V $I_{Load} = 0.2 mA;$ All Digital I/OSLow Level Output Voltage V_{SPIL} -0.1-0.4V $I_{Load} = 0.2 mA$ P_5.7.45	Table 6 Electrical Characteristics IOS (continued) Low Level Output Voltage V _{ERRL} -0.1 - 0.4 V I _{Load} = 0.2 mA P_5.7.39 Low Level Output Voltage V _{SPIL} -0.1 - 0.4 V I _{Load} = 0.2 mA P_5.7.45			
	Table 6 Electrical Characteristics IOs (continued)	Table 6 Electrical Characteristics IOs (continued)			
4.7 Electrical Characteristics IOs	High Level Output Voltage 30 V_{ERRH5a} 3.3- V_{VCC} V $\frac{5.5 V < V_{vcc} < 2.2 V}{V_{vcc} < 5.0 V}$ P_5.7.38 V_{ucc}	High Level Output Voltage 30) V_{ERRH5a} 3.3- V_{VCC} V $V_{VCC} = 5.0 \text{ V};$ P_5.7.38 $I_{load} = -0.2 \text{ mA};$ All Digital I/Os= static			
Modification valid for TLE9180D-26QK only.	High Level Output Voltage 30 V_{SPIH5a} 3.3- V_{VCC} V $\frac{5.5 V \le V_{VS} \le 7.2 V_{1}}{V_{VCC} = 5.0 V_{1}}$ $I_{load} = -0.2 mA;$ All Digital I/Os $= static$ P_5.7.44	High Level Output Voltage 20) V_{SPIH5a} 3.3- V_{VCC} V $V_{VCC} = 5.0 \text{ V};$ P_5.7.44 $I_{load} = -0.2 \text{ mA};$ All Digital I/Os=static			



Datasheet Chapter		9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
	Table 6	Electrical Characteristics IOs (continued)	Table 6 Electrical Characteristics IOs (continued)
4.7 Electrical Characteristics IOs	High Level Output Voltage ⁷⁾	V _{ERRHSa} 3.35 - V _{VCC} V 5.5V ± V_{VS} ± 7.2 V; P_5.7.38 V _{VCC} = 5.0 V; I _{load} = -0.2 mA; All Digital I/Os = static	High Level Output Voltage V_{ERRH5a} 3.35- V_{VCC} V $V_{VCC} = 5.0 \text{ V};$ $I_{load} = -0.2 \text{ mA};$ All Digital I/Os = staticP_5.7.38
Modification valid for all, except TLE9180D-26QK.	High Level Output Voltage ⁷⁾	V _{SPHSa} 3.35 - V _{VCC} V 5.5 V ≤ V _{VS} ≤ 7.2 V; V _{VCC} = 5.0 V; h _{oad} = -0.2 mA; All Digital I/Os = static P_5.7.44	High Level Output Voltage ²¹⁾ $V_{SPIHSa} = 3.35 - V_{VCC} V V_{VCC} = 5.0 V; P_{5.7.44}$ $I_{load} = -0.2 mA; All Digital I/Os = static$
4.7 Electrical Characteristics IOs Change valid for all, except TLE9180D-26QK.	Table 6 Electrical Character High Level Output Voltage	Istics IOS (cont'd) V _{AOPH1} 4.2 5.0 6.0 V I _{load} = -1 mA P_5.7.47	Table 6 Electrical Characteristics IOS (cont'd) High Level Output Voltage VAOPH1 3.9 5.0 6.0 V Inad = -1 mA P_5.7.47
4.7 Electrical Characteristics IOs Change valid for TLE9180D-26QK only.	Table 6 Electrical Characteris High Level Output Voltage	VAOPH1 4.2 5.0 6.0 V Iload P_5.7.4	Table 6 Electrical Characteristics IOs (cont'd) High Level Output Voltage V_{AOPH1} 3.7 5.0 6.0 V $I_{load} = -1 \text{ mA}$ P_5.7.47
5 Serial Peripheral Interface - SPI	SPI Maste (Microcontrol 1) Floating of MI Figure 4 Principle for SPI-Bu	ler)	SPI Master (Microcontroller) (
5.5 Electrical Characteristics SPI		aracteristics: Timing D V, all voltages with respect to GND, positive current flowing into pin (unles	Table 7 Electrical Characteristics: Timing $T_j = -40^{\circ}$ C to $+165^{\circ}$ C, $V_S = 5.5$ V to 60 V, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified). Timings valid for 10 MHz operation.



Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10							
	Table 7 Electrical Characteristics: Timing	Table 7 Electrical Characteristics: Timing							
	CLK_SPI Operating Period IsPLak 100 - - ns 2) Figure 6, C P_6.5.2	CLK_SPI Operating Period t _{SPI_clk} 100 ns 33)Figure 6, C P_6.5.2							
	CLK_SPI High Time <i>I</i> _{SPI_wackh} 37 – – ns ²⁾ Figure 6, A P_6.5.3	CLK_SPI High Time t _{SPL wsckth} 37 ns 33) Figure 6, A P_6.5.3							
5.5 Electrical Characteristics SPI	CLK_SPI Low Time triangle 37 - - ns 2) Figure 6, B P_6.5.4 CLK_SPI Fall Time triangle - - 13 ns 2) Figure 6, D P 6.5.5	CLK_SPI Low Time t _{SPI_wsckll} 37 ns 33)Figure 6, B P_6.5.4							
	CLK_SPI Fall Time Image: Ispl_ciki - - 13 ns 2) Figure 6, D P_6.5.5 2) Not subject to production test; verified by design or characterization; measured between 10% and 90%; output load capacitance on MISO pin is ≤ 25 pF	³³ Not subject to production test; verified by design or characterization; measured between 20% and 80%; output load capacitance on MISO pin is ≤ 25 pF							
7.1 Output Stage Supply Concept	7.1 Output Stage Supply Concept fulfills the requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20 kHz PWM frequency. The charge pumps will be deactivated if the pin INH is set to low.	7.1 Output Stage Supply Concept fulfills the requirement to drive the external FETs within a PWM specific duty cycle range of 95% to 100% at 20 kHz PWM frequency. The charge pumps will be deactivated if the pin INH is set to low or a charge pump related error is detected. For details please check the supervision descriptions.							
.3 Electrical Characteristics Power Supply	Table 10 Electrical Characteristics: Power Supply (cont'd)	Table 10 Electrical Characteristics: Power Supply (cont'd)							
Modification not valid for TLE9183QK.	Supply current in Reduced Operation Mode at Vs Supply Current Vs Iveral (ROMVS) - 12 20 mA Iveral (Volter)=3V P_8.3.36	Supply Current Vs Image:							
	Table 10 Electrical Characteristics: Power Supply (cont'd)	Table 10 Electrical Characteristics: Power Supply (cont'd)							
7.3 Electrical Characteristics Power Supply	Voltage Vs for Guaranteed Power- up of Charge Pumps V/VSWU 6.0 - - V - P_8.3.38	Voltage Vs for ensured Power-up of Charge Pumps V - V - P_8.3.38							
7.3 Electrical Characteristics Power Supply	2) Filter Time Accuracy referenced from internal clock accuracy, please see Chapter 6.2	⁸⁷ Internal clock frequency accuracy has to be added to the specified values, please see Chapter 6.2							
	Table 12 Electrical Characteristics MOSFET drivers (continued)	Table 12 Electrical Characteristics MOSFET drivers (continued)							
8.4 Electrical Characteristics Floating MOSFET Driver	Propagation Delay Time (all low-side FETs off) $t_{P(ILF)}$ 30 35 70 ns $R_{Load} = 2 \text{ k}\Omega^{52/};$ P_9.4.19	Propagation Delay Time (all low- side FETs off) t 25 35 70 ns $R_{Load} = 2 k\Omega^{52}$; $V_{Sox} = 0 V$ P_9.4.19							



Datasheet Chapter		TLE918 TLE9183QK DS			TLE9180D-3 2K DS V1.01		Contraction and the second second	Т	TLE9180 LE9183QK DS V1		V1.20 / TLE9 80D-32QK D			
9.5.1 Gain Test	9.5.1 Gain Test Gain test can only be activated in self-test mode, for details see <i>Table 30</i> . Two different internal generated self-test voltages <i>V</i> _{SSC_GTUV} and <i>V</i> _{SSC_GTUV} for gain test can be selected at the inputs of the CSAs. The input voltage <i>V</i> _{SSC_GTUV} is always applied to gain register 1 of the CSAs. The input voltage <i>V</i> _{SSC_GTUV} is always applied to gain register 2 of the CSAs. It is recommended to use the gain register 2 only in the self-test mode for the gain test of the CSAs. By changing a dedicated bit sh_op_gain the gain of the CSA toggles between both gain register settings. Reading the bit will indicate which gain is selected. Toggling sh_op_gain will affect always all CSAs. The resulting output voltage shall be measured by the ADC of the µC and compared to the configured gain. The µC can rate if the CSA output voltage, see <i>V</i> _{SSC_OTE} or <i>V</i> _{SSC_OTE} the self-test, see <i>V</i> _{SSC_GTUV} and <i>V</i> _{SSC_GTUV} and the accuracy of the VRO output voltage, see <i>V</i> _{SSC_OTE} have to be taken into account. Amplification of differential input voltage ISP - ISN is not possible for the CSA which is selected for gain test.					self-test voltages voltage VSSC_GT/ applied to gain re- between both gai will affect always to the configured accuracy of the ga the accuracy of the VSSC_OVRO have	Gain Test be activated in self- /SSC_GTILV and VSS UV is always applied gister 2 of the CSAs. I, n register settings. R all CSAs. The resulting gain. The µC can rate in, see ASSC_diff AN e self-test, see VSSC to be taken into acce elected for gain test.	C_GTIHV for to gain regist By changing a eading the bin goutput volte if the CSA or D GSSC_Gda _GTILV and V pount. Amplifie	gain test can b er 1 of the CSA a dedicated bit t will indicate w tage shall be m atput voltage n cc, the input of SSC_GTIHV and	e selected at s. The input sh_op_gain which gain is easured by the natches the p fset voltage, d the accurate	the inputs of t voltage VSSC_ the gain of the selected. Togg the ADC of the programmed g see VSSC_OOD cy of the VRO of	the CSAs. The input GTIHV is always e CSA toggles gling sh_op_gain μC and compared gin. Thereby, the fscal or VSSC_Oofs		
9.6 Electrical Parameter Shunt Signal Conditioning (SSC) Modification valid for TLE9180D-26QK only.	Table 20 Negative Trim Ra	Electrical Chara	C_OVRO_TRN	Reference Bu 7.0 - 2.8 - 3.6 -	-5.7 9/ -2.3 V	ovro@ zcl = fs = '0x2 zcl =	'0b00'; P_9.6.52 '0b01'; '0b10'; s = '0x00'	Table 20 Negative Trim Range	Electrical Charact		5.7 -2.3 -3.1	% of V _{OVRO@} ofs = '0x2	zcl = '0b00'; zcl = '0b01'; zcl = '0b10'; @ ofs = '0x00'	P_9.6.52
	Table 21 Diagr	ostic overview						Table 21 Dia	agnostic overview					
	Overvoltage VS (Programmable Threshold)	yes (default value)	no ²⁾	yes	no	Table 25	Chapter 10.5.1	Overvoltage VS (Programmable Threshold)	yes (default value)	no ⁵⁶⁾	yes	no	Table 25	Chapter 10.5.1
	Overvoltage VS shutdown Undervoltage VS (Programmable Threshold)	yes yes (default value)	no ²⁾	yes yes	no	Table 24 Table 25	Chapter 10.5.1 Chapter 10.5.1	Undervoltage VS (Programmable Threshold)	yes (default value)	no ⁵⁶⁾	yes	no	Table 25	Chapter 10.5.1
10.1 Supervision Overview Modification valid for TLE9183QK only. 10.5.1 Vs Voltage Monitoring The Vs supply voltage is monitored (under- and overvoltage detection). The threshold, the error reaction and the filter time can be adjusted via SPI. Additionally to the overvoltage detection a maximum overvoltage. threshold, the so-called overvoltage shutdown, is set to signalize the µC that a maximum rating violation might has been occurred at the pin Vs. The failure behavior and the threshold of the shutdown is not adjustable. The shutdown failure behavior is fix as a latched error. Register Err_sd bit 6 indicates overvoltage Vs shutdown and register Err_e bit 3 and bit 2 for undervoltage and overvoltage detection at pin Vs. Additionally the VS voltage is stored in register res_vs and can be read out via SPI.					the filter time can Register Err_sd bit overvoltage detect	6 indicates overvoltag	er- and overvo ge Vs shutdow	n and register E	rr_e bit 3 and					



Datasheet Chapter		TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0							TLE9180D-21QK DS V1.20 / TLE91 3QK DS V1.10 / TLE9180D-32QK DS			V1.10		
	Table 24	Shutdown E	Error Overview ¹⁾			22	Table 24	24 Shutdown Error Overview ¹⁾						
	Bit Position	Bit Name	Bit Name Description		Charge Pumps	ERR Pin	Bit Position	Bit Name	Description	Output Stages	Charge Pumps	ERR Pin		
0.2.2 Failure Behavior Configuration	3	sd_clk_fail	Internal Clock Supervision Shutdown ^{80J}	ARE	Active	Low (LE)	3	sd_clk_fail	Internal Clock Supervision Shutdown ⁸⁰⁾	ARE or LE	Active	Low (ARE or LE)		
	⁸⁰ In the	case of monitoring	g clock stops operation fault reaction of ou	tput stages is latch	ed error		⁸⁰ Fai	lure reaction ca	an be ARE or LE dependent on type of	internal fault				
	Table 24	Shutdo	wn Error Overview ⁷⁸⁾				Table 24	Shutd	own Error Overview ⁷⁸⁾					
10.2.2 Failure Behavior Configuration	Bit Position	Bit Name	Description	Output Stages		ERR Pin	Bit Position	Bit Name	Description	Output Stages	Charge	ERR Pin		
	4	sd_uv_cb	Undervoltage CB Shutdown	ARE	Active	Low (LE)	4	sd_uv_cb	Undervoltage CB Shutdown	ARE	Active	Low (ARE)		
10.5.16 Overload Digital Output Pins	be disconne pin reset wi mode, eithe Functionali Chapter 16	ected, a dedicat ith ENA has to b er the output st ity of the over 5.3.8.	tected against short to GND and batt ted error register bit will be set. The p e performed. The failure behavior of ages will turn all external FETs off or load detection of the digital outpub bit 0 indicate a short of a digital outpub	bin ERR will be s the gate driver I not. ut pins is limite	et to low. To C is adjustab	unlock the output le at configuration	be disconne the affected driver IC is Functionali 16.3.7 .	ected, a dedicat pin. To unlock adjustable at co ty of the overlo	otected against short to GND and batter ted error register bit will be set. The pin the output pin reset with ENA has to be onfiguration mode, either the output st ad detection of the digital output pins bit 0 indicate a short of a digital output	n ERR will be so be performed. tages will turn is limited, for	et to low <mark>in c</mark> The failure b all external l	ase pin ERR is not ehavior of the gate FETs off or not.		
10.5.4 High-side Buffer Capacitor Voltage Monitoring	Register Err_outp bit 4 to bit 0 indicate a short of a digital output pin. 10.5.4 High-side Buffer Capacitor Voltage Monitoring An overvoltage monitoring for the external high-side buffer capacitor guarantees gate source voltage for the external FET not higher as the destructive gate source voltage. Failure behavior and filter time is not configurable. High-side buffer overvoltage monitoring can be deactivated at configuration if diagnosis is not required. In case of overvoltage detection all output stages remain active but charge pump 2 will be deactivated. A reset via ENA is necessary for reactivation of charge pump 2. If overvoltage high-side buffer has been detected and charge pump 2 has been turned off duty cycle operation higher than 95% is not recommended and might end up in undervoltage high-side buffer detection.						10.5.4 An overvo the extern the ERR p all output 2 nd charg	High-sid bltage monitorin hal FET. The failu in is set low and stages remain a e pump is deacti duty cycles. The	Be Buffer Capacitor Voltage M ag for the external high-side buffer capacitor behavior and filter time are not config I the dedicated error bit in the register is active. A reset via ENA is necessary for the ivated, an undervoltage high-side buffer e overvoltage monitoring for the external	itor detects too gurable. In case set. The 2 nd ch e reactivation o detection migh	of an overvo arge pump is of the 2 nd chain nt occur main	Itage detection, deactivated and rge pump. If the ly at operation		



Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10					
10.5.11.2 Self-test Function for SCD Change valid for all, except TLE9183QK.	for the section of the secting of the secting of the	Image: contrast of detain source voltage messures of detain source voltage 					
10.6 Electrical Characteristics Protection and Diagnostic Functions	Table 53 Electrical Characteristics - Protection and Diagnostic Functions (cont'd)	Table 53 Electrical Characteristics - Protection and Diagnostic Functions (cont'd)					
Modification valid for all data sheets, except TLE9180D-26QK.	Accuracy Undervoltage Threshold $V_{VSUVacc2}$ -13.5PROG+13.5% $4.4 V \ge V_{VSUV} < 7.5 V$ P_11.6.12Vs	Accuracy Undervoltage Threshold $V_{VSUVacc2}$ -13.5PROG+13.5% 4.2 V $\leq V_{VSUV} < 7.5$ V P_11.6.12Vs					
10.6 Electrical Characteristics Protection and Diagnostic Functions	Table 53 Electrical Characteristics - Protection and Diagnostic Functions (cont'd) Accuracy Undervoltage Threshold VysiNarc2 -17.5 PROG +17.5 % 4.4 ¥ ≥ VysiN < 7.5 ¥	Table 53 Electrical Characteristics - Protection and Diagnostic Functions (cont'd) Accuracy Undervoltage Threshold VVSUVACC2 -17.5 PROG +17.5 % 4.0 V ≤ VVSUV < 7.5 V					
Modification valid for TLE9180D-26QK only.	Accuracy Undervoltage Threshold V _{VSUVacc2} -17.5 PROG +17.5 % 4.4 V ≥ V _{VSUV} < 7.5 V P_11.6.12 Vs	Vs					
10.5 Electrical Characteristics Protection and Diagnostic Functions Modification valid for TLE9183QK only, other data sheets already updated.	VCC Read Out Voltage Detection Range V _{ADCr} 0 – 5.554 V 0 to FFh P_11.6.86	VCC Read Out Voltage Detection Range VADCr. 0 - 5.55. V 0 to FFh P_11.6.86					



Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10						
	Table 53 Electrical Characteristics - Protection and Diagnostic Functions (continued)	Table 53 Electrical Characteristics - Protection and Diagnostic Functions (continued)						
10.6 Electrical Characteristics Protection and	Entry Filter and Reaction Time of VyccRoP1 0.6 – – µs 87) P_11.6.78 Reduced Operation Mode Detection at VCC	Entry Filter and Reaction Time freduced Operation Mode Detection at VCC 0.6 \mu S 87 P_11.6.78						
Diagnostic Function	Exit Filter and Reaction Time of V _{VCCROP12} 20 – μs ⁸⁷⁾ P_11.6.79 Reduced Operation Mode Detection at VCC	Exit Filter and Reaction Time tyccropriz 20 µs 877 P_11.6.79 of Reduced Operation Mode Detection at VCC						
	Temperature Read Out Accuracy tread - 28 - +28 K - P_11.6.115	Temperature Read Out Accuracy Trread a - +28 K - P_11.6.115						
11.2 Electrical Parameter Phase Feedback	Table 55 Electrical Characteristics - Phase Feedback	Table 55 Electrical Characteristics - Phase Feedback						
Modification valid for all data sheets, except TLE9183QK.	Propagation Delay Time t _{PD/b} - 60 100 ns 50%/50% selected P_12.2.6	Propagation Delay Time tpDfb - 60 110 ns 50%/50% selected P_12.2.6						
11.2 Electrical Parameter Phase Feedback	Table 55 Electrical Characteristics - Phase Feedback	Table 55 Electrical Characteristics - Phase Feedback						
Modification valid for TLE9183QK only.	Propagation Delay Time t _{PDfb} - 60 100 ns P_12.2.6	Propagation Delay Time t _{PDfb} – 60 110 ns P_12.2.6						
13 Operation Modes	FigraOrderword Digital OperationWorderword Digital Operation	Figure 31 Overview of Digital Operation Mode						



Datasheet Chapter	TLE9180D-21QK DS V1.10 / TLE9180D-31QK DS V1.10/ TLE9183QK DS V1.01 / TLE9180D-32QK DS V1.01 / TLE9180D-26QK V1.0	TLE9180D-21QK DS V1.20 / TLE9180D-31QK DS V1.20/ TLE9183QK DS V1.10 / TLE9180D-32QK DS V1.10 / TLE9180D-26QK V1.10
16.3.10 Reduced Operation Mode INH set to low Modification valid for all data sheets, except TLE9180D-26QK & TLE9183QK.		16.3.10 Reduced Operation Mode INH set to low In Reduced Operation Mode if INH is set to "low" if V _{CB} < V _{CBUVSD} , Sleep Mode might not be entered. For additional information please refer to TLE9180 Application Note "Reduced Operation Mode INH set to low".
16 Application Information Modification valid for all data sheets, except TLE9180D-26QK.	Image: Control from the second of the sec	Figure 36 Simplified Application Circuit
16.2.1 Additional Components Modification valid for all data sheets, except TLE9180D-26QK and TLE9183QK.	⁶⁾ D3 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs. The effect can be avoided with sufficient input filtering with C_{vs} and $(R_{vs} \text{ or D1})$.	⁸⁾ D3 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs with a slew rate \geq 6V/100µs. D3 is not required with sufficient filtering at the Vs pin. In case D3 is not used a 100 kΩ pull down to GND at CL1 shall be placed.
16.2.1 Additional Components Modification valid for all data sheets, except TLE9180D-26QK and TLE9183QK.	⁴⁾ D4 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after CB capacitor has been shorted to GND.	⁴⁾ D4 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data.
16.2.1 Additional Components Modification valid for all data sheets, except TLE9180D-26QK and TLE9183QK.	³⁾ D2 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin V _s . Voltage drops at pin Vs in the range from 13V down to 6V shall not be shorter than 100µs. In the case of faster slew reates an input filter is required. For details please contact Infineon.	³⁾ D2 shall prevent that the device will be set unintentionally to idle mode with loss of configuration data after a voltage drop has occurred at the pin Vs with a slew rate ≥ 6V/100µs. D2 is not required with sufficient input filtering at the Vs pin.



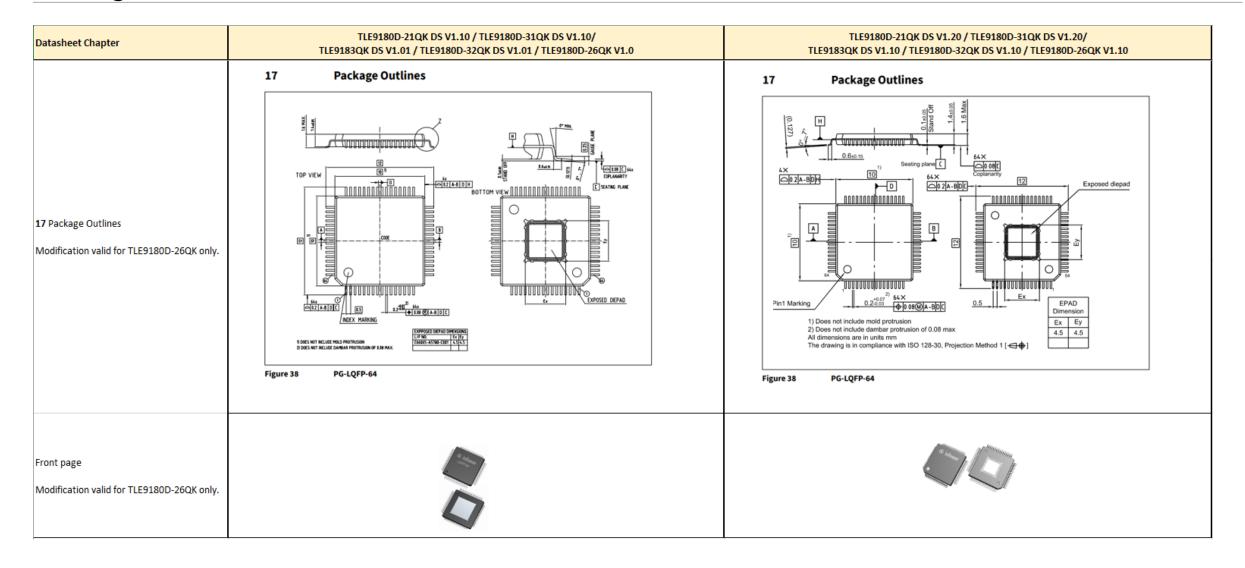




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> MyICP links to the Infineon data base

Sales Code	Datasheet folder	Safety documentation folder
TLE9180-20QK	Infineon-TLE9180-20QK-DS-v01_80-EN	for <u>TLE9180-20QK</u>
TLE9180-21QK	Infineon-TLE9180-21QK-DS-v01_80-EN	for <u>TLE9180-21QK</u>
TLE9180C-21QK	Infineon-TLE9180C-21QK-DS-v01_10-EN	for TI E0190C 210K and TI E0190C 210K
TLE9180C-31QK	Infineon-TLE9180C-31QK-DS-v01_10-EN	for TLE9180C-21QK and TLE9180C-31QK
TLE9180C-20QK	Infineon-TLE9180C-20QK-DS-v01_10-EN	for <u>TLE9180C-20QK</u>
TLE9180D-21QK	Infineon-TLE9180D-21QK-DS-v01_20-EN	for TLE0100D 210K and TLE0100D 210K
TLE9180D-31QK	Infineon-TLE9180D-31QK-DS-v01_20-EN	for TLE9180D-21QK and TLE9180D-31QK
TLE9180D-26QK	Infineon-TLE9180D-26QK-DS-v01_10-EN	for <u>TLE9180D-26QK</u>
TLE9180D-32QK	Infineon-TLE9180D-32QK-DS-v01_10-EN	for <u>TLE9180D-32QK</u>
TLE9183QK	Infineon-TLE9183QK-DS-v01_10-EN	for <u>TLE9183QK</u>



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