ICL88xx

Datasheet for ICL8800, ICL8810 and ICL8820

Feature list

The ICL88xx family of single stage flyback controllers for constant voltage output is tailored for LED lighting applications to meet the required performance. They offer power factor correction (PFC) and low total harmonic distortion (THD) from low to full load conditions.

General features ICL8800, ICL8810, ICL8820

- Constant voltage (CV) output flyback topology with a feature set and operation targeting lighting applications
- Optimized for PFC-flyback topologies with secondary side regulation (SSR) operation, primary side regulation (PSR) possible
- Supports universal input voltage (90 V_{AC} to 300 V_{AC}, 45 Hz to 66 Hz) and DC input voltage operation
- High power factor low THD performance across wide load and input AC line range
- Quasi-resonant operation with continuous conduction mode (CCM)-prevention and valley switching discontinuous conduction mode (DCM) in mid to light load
- Adjustable max on-time – limits input power and current allowing safe-operation under low line condition
- Comprehensive set of protections: Internal overtemperature protection (OTP), output overvoltage protection (OVP), overcurrent protection (OCP), brown-in and brownout protection, open loop protection, input overvoltage protection
- Soft-start to reduce stress during turn-on
- External start-up circuit control signal with V_{CC} support in light load operation
- Reduced gate driver output voltage during start-up sequence and burst mode allowing smaller V_{CC} cap
- Burst mode for very light loads and low system standby power consumption
- Jitter function on DC input to ease electromagnetic interference (EMI) testing for emergency lighting

Additional features ICL8810, ICL8820

- Burst mode for very light loads and low system standby power consumption

Additional features ICL8820

- Jitter function on DC input to ease EMI testing for emergency lighting

Potential applications

PFC-flyback CV

- LED driver and luminaries up to 125 W
- Adapter, charger, flat TV, all-in-one PC, monitor up to 125 W

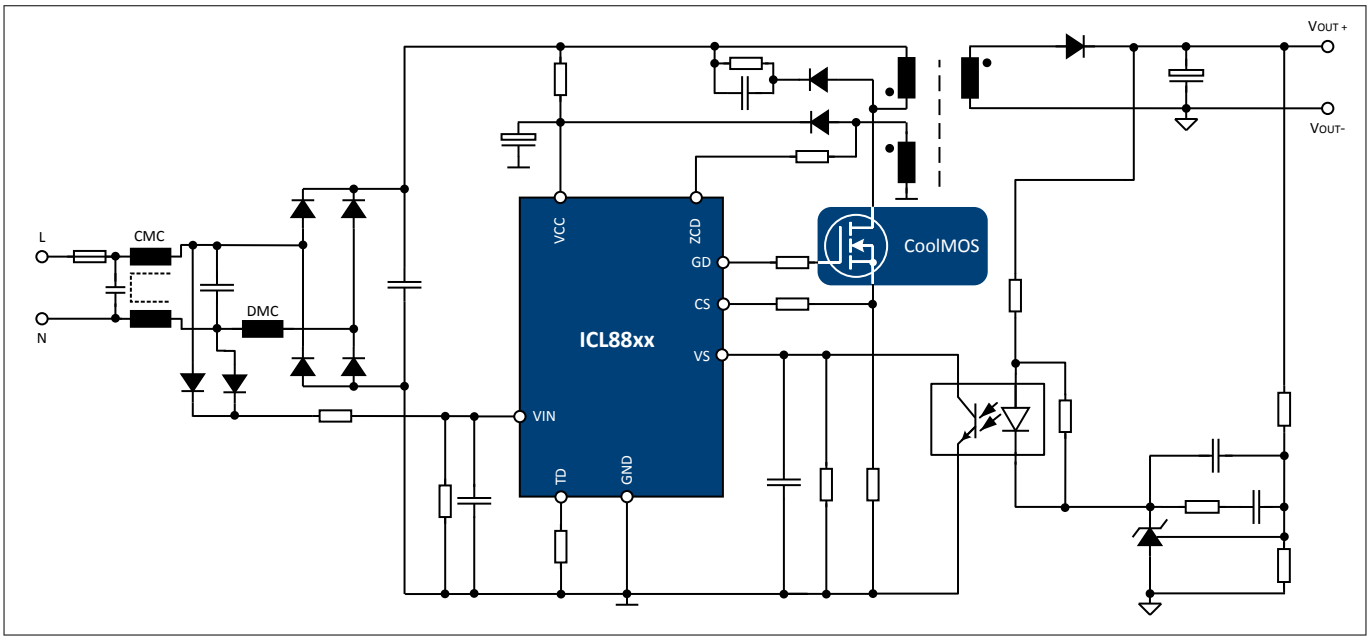

Figure 1 Flyback-SSR-CV

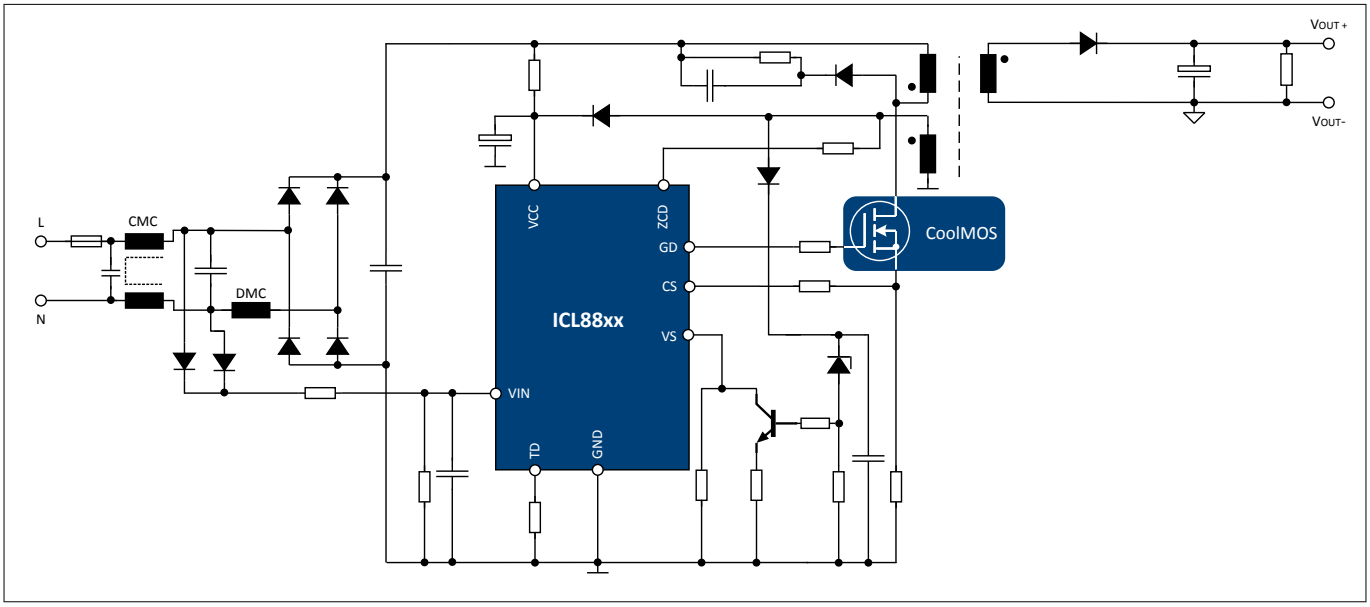

Figure 2 Flyback-PSR-CV

Product type	Package	Ordering code
ICL8800	PG-DSO-8	SP003135776
ICL8810	PG-DSO-8	SP005418406
ICL8820	PG-DSO-8	SP005418407

Product validation

Qualified for applications listed above based on the test conditions in the relevant tests of JEDEC20/22.

Description

The ICL8800, ICL8810 and ICL8820 is a voltage mode controller for flyback topologies operating in quasi-resonant mode and valley switching DCM. It is designed for low and high power lumen LED driver, requiring high power factor and efficiency. The flyback controller is capable of controlling SSR-CV an PSR-CV topologies. Offering a wide usage in low cost applications where a PFC functionality in dual stage topologies is required.

For lighting applications, the IC offers a wide power range as well as a comprehensive set of protections, including a power limitation. The IC is easy to design in and requires a minimum number of external components.

The gate driver current enables reasonable designs up to 125 W with state-of-the-art MOSFETs. The system performance and efficiency, especially in light load conditions, can be optimized using Infineon CoolMOS™ P7 power MOSFETs.

ICL8810 and ICL8820

The integrated burst mode function allows designs with a very low standby power consumption and small output ripple during standby mode and very light loads.

ICL8820

The jitter function eases the design of emergency lighting LED drivers without additional circuitry to improve EMI performance.

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1 Pin configuration

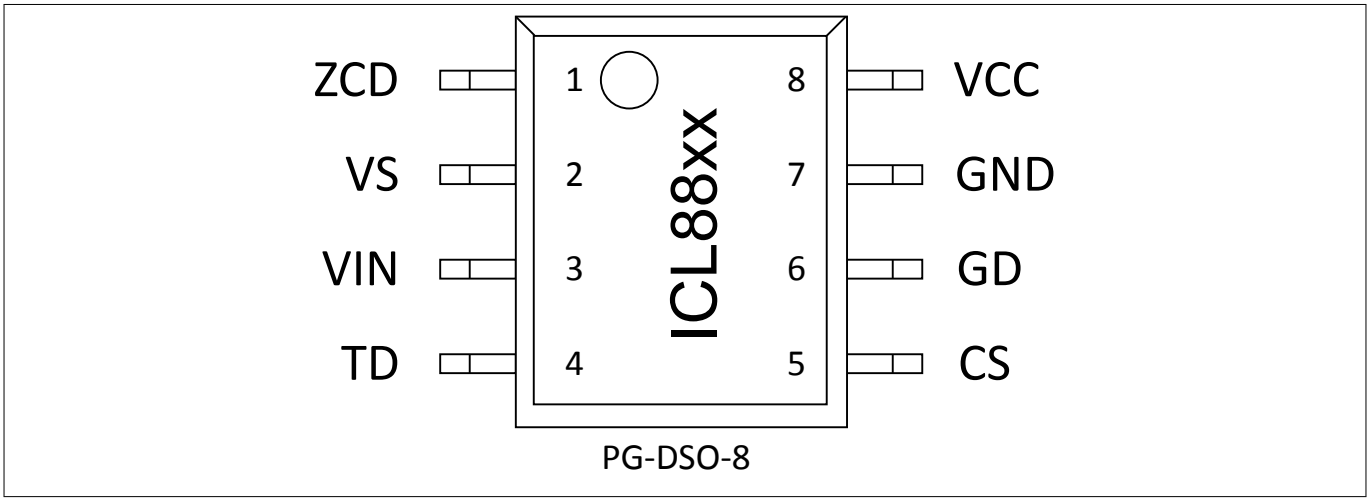


Figure 3 Pin configuration

Table 1 Pin definition and function

Symbol	Pin	Function
ZCD	1	**Zero crossing detection** This pin is connected to an auxiliary winding via a resistor to detect the zero crossing of the switching current. When the zero crossing is detected, the controller initiates a new switching cycle. The resistor from *ZCD* pin to the auxiliary winding is used to set the maximum on-time.
VS	2	**Voltage sense** This pin is connected to the feedback circuit.
VIN	3	**Input voltage detection** This pin is used to measure the AC or DC input voltage for power limitation, input OVP, brown-in and brownout.
TD	4	**THD correction** This pin is used to set the THD correction using a resistor to *GND*. The voltage on this pin can be used to control an external start-up circuit.
CS	5	**MOSFET current sense and secondary side over voltage protection** This pin is used for primary side over current protection. A series resistance between pin and shunt resistor is used to tune the secondary side over voltage protection for the flyback topology.
GD	6	**Gate driver** This pin controls the gate of the MOSFET.
GND	7	**Ground** This pin is connected to ground and represents the ground level of the IC for the supply voltage, gate driver and sense signals.
VCC	8	**Power supply** This pin supplies the IC.

2 Block diagram

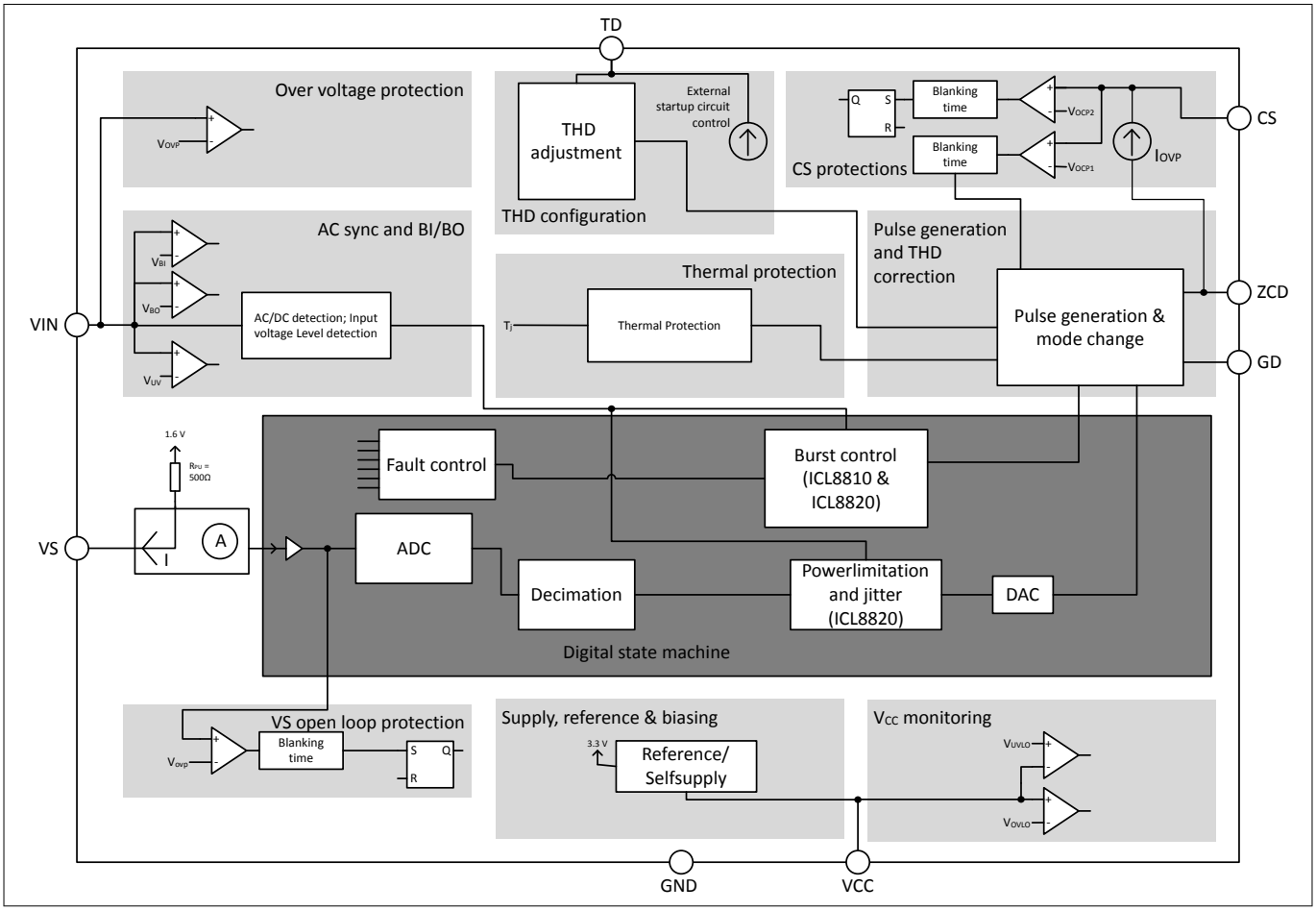


Figure 4 Block diagram

3 Functional description

These sections describe the listed functions in detail.

3.1 Operating modes

The controller operates in voltage mode to optimize the power factor. It also autonomously selects the best mode of operation based on operation conditions like input voltage and input frequency as well as load conditions.

The supported modes are:

- Quasi-resonant mode (QRM)

  This mode controls the on-time and maximizes the efficiency by switching on at the valleys of the *ZCD* signal. This ensures zero-current switching with a minimum of switching losses.

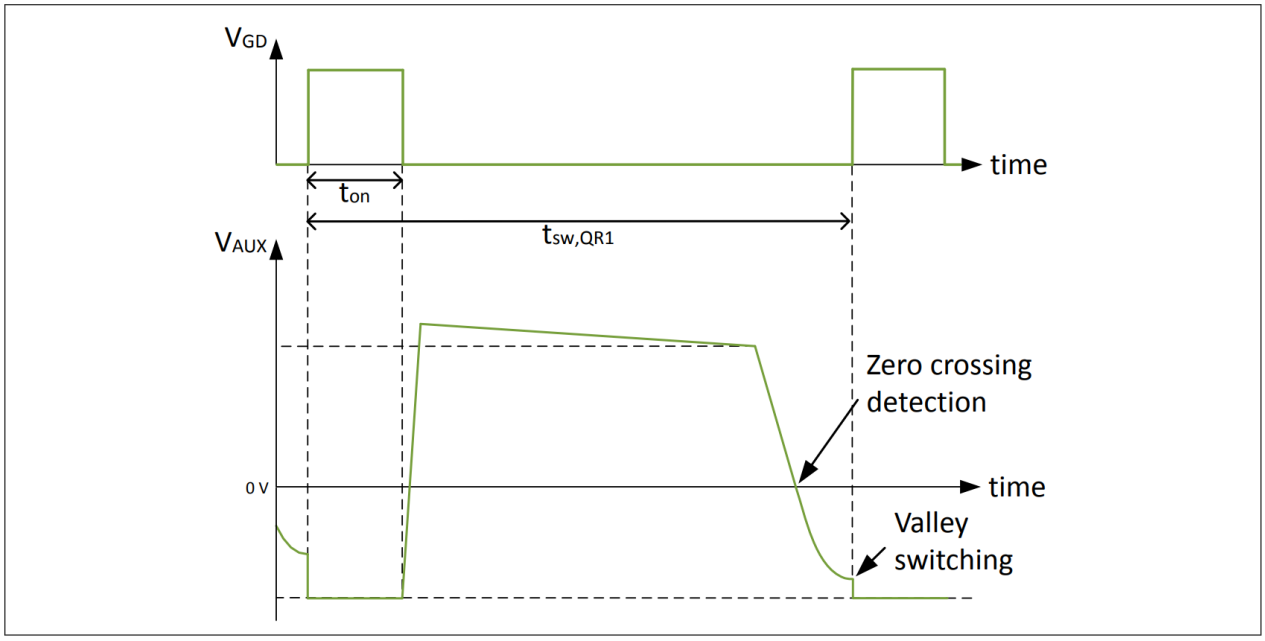


Figure 5 Example of the switching waveform in the first valley

- Burst mode for ICL8810 and ICL8820

  Operation in burst mode to increase the efficiency in light load operation and to extend the power range for wide range input voltage designs. Enables very low standby power.

At highest relative power, the controller operates in voltage mode with constant on-time in QRM, switching at the first valley. The maximum on-time can be tuned using the *ZCD* series resistance to adjust the maximum relative power.

In QRM, the operating frequency depends on the QR resonant frequency of the transformer and the MOSFET. To reduce relative power, the controller reduces the on-time. At certain relative power levels, the controller also starts increasing the valley to avoid high frequencies. The switching frequencies remain within a range of typically 20 kHz to 150 kHz depending on component selection.

The on-time is compensated to ensure a constant relative power for the change of the valley.

The off-time of the controller is limited to T_{Off} = 47 µs to ensure a minimum switching frequency outside the audible range.

To achieve lowest relative output power, the ICL8810 and ICL8820 enter a burst mode with a repetition frequency of approximately four times the AC input frequency.

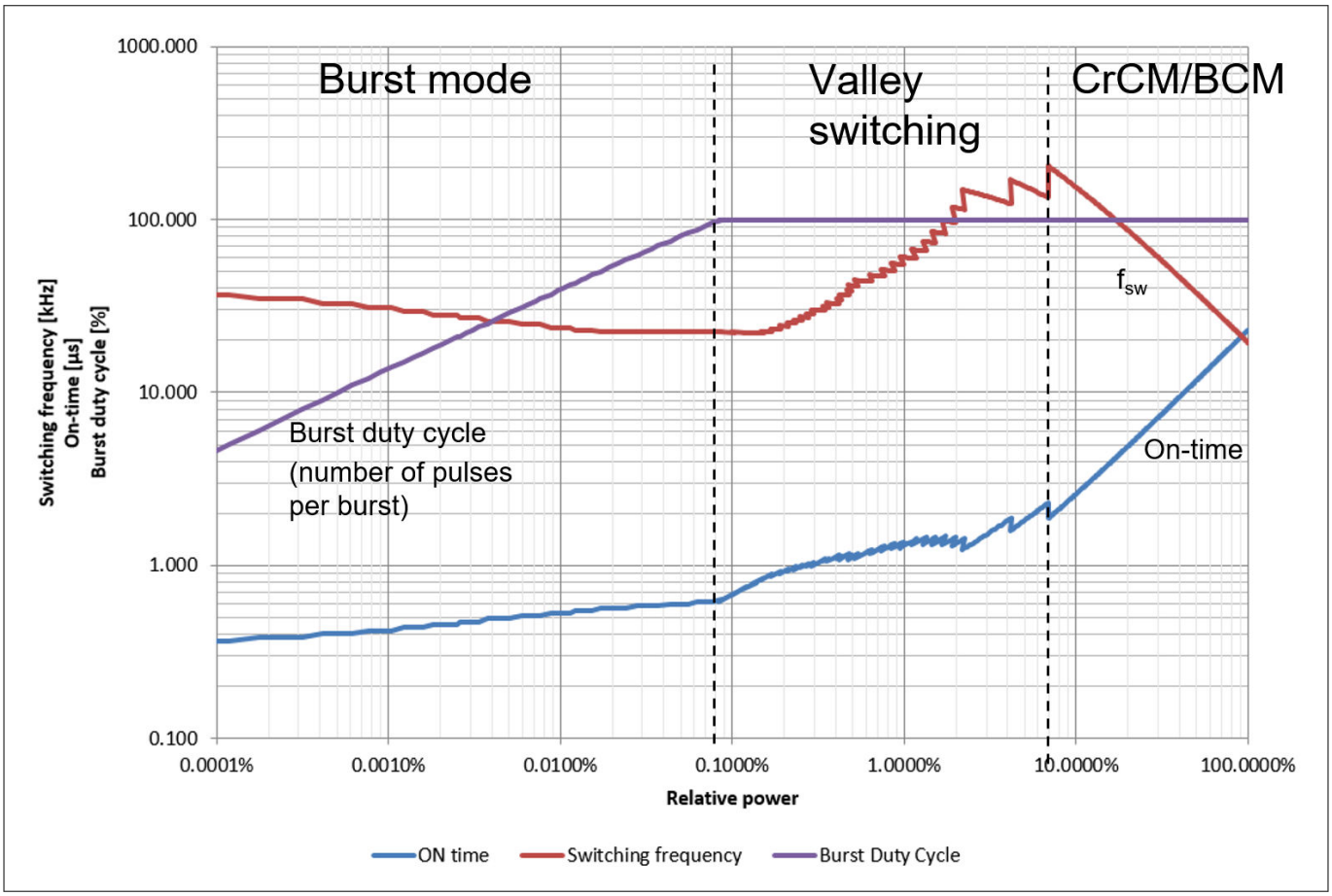


Figure 6 **Exemplary switching characteristics versus relative power for a flyback application with an QR oscillation period of 1.6 µs for a line frequency of 50 Hz for ICL8810 and ICL8820**

To avoid fast changes in the selected valley, for example multiple subsequent changes of the valley during one AC half-wave, the IC uses a valley hysteresis. During each half-wave, the IC measures the required valley to fulfill the power demand for a given AC input voltage and applies the minimum valley for the next half-wave. During this half-wave, the IC adjusts the on-time to stay in the calculated valley. In this way, the number of valley jumps is limited to a minimum.

In addition, if a load jump is detected, the valley number is adjusted immediately and set to the new minimum value in the next AC half cycle. Since in some load and line conditions valley jumps are unavoidable, this IC uses an asymmetric hysteresis to minimize the impact of a changed valley on the input current of the converter. If the valley has to be corrected down, it happens immediately, but changing the valley up either happens on load jumps or at the start of the next AC half-wave.

3 Functional description

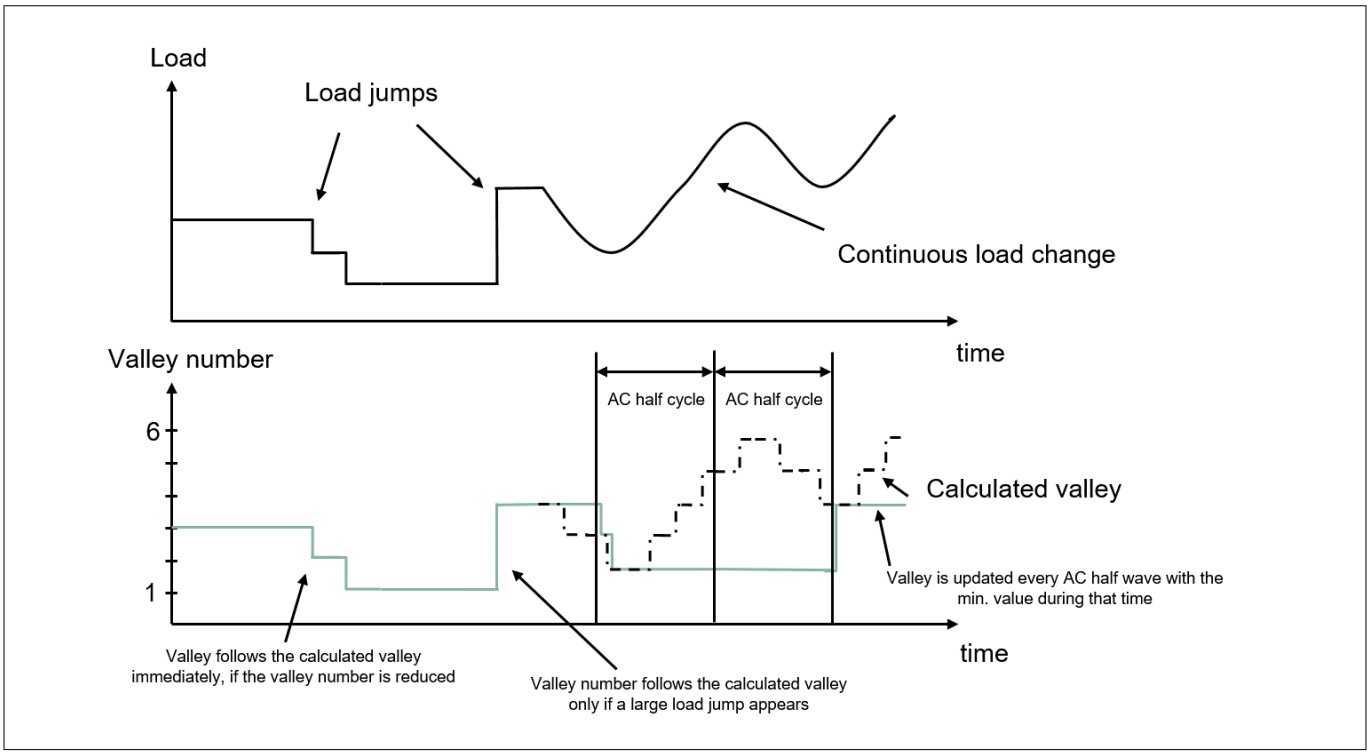


Figure 7 Valley selection hysteresis

Feedback loop

The pulse generation is based upon the current drawn out of the *VS* pin. This method has shown better noise immunity.

The VS-current is exponentially mapped from 200 µA to 600 µA over the entire pulse width range including burst mode. In the range 20 µs to 1 µs, the mapping is relatively well exponential with a halving of the pulse duration per 50 µA opto-current.

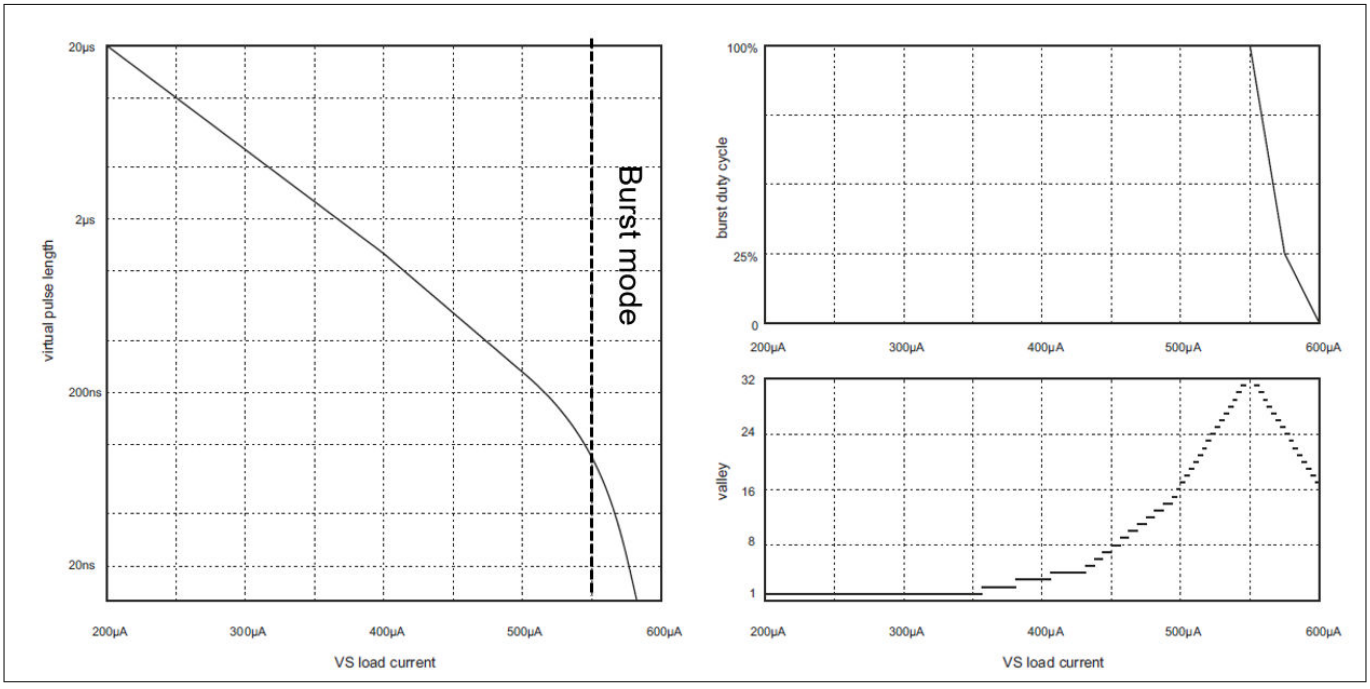


Figure 8 Mapping of the on-time vs the current out of the VS-pin

3 Functional description

To ensure proper operation of the feedback loop, a 12 kΩ resistor must be connected from the *VS* pin to ground. The minimum current drown out of this pin (current through the opto coupler plus the current of the 12 kΩ resistor) results in maximum power transfer, and the maximum current out of the *VS* pin results in loading to the smallest operation point. To achieve the best THD and PF results, a low crossover frequency of a few Hz is recommended.

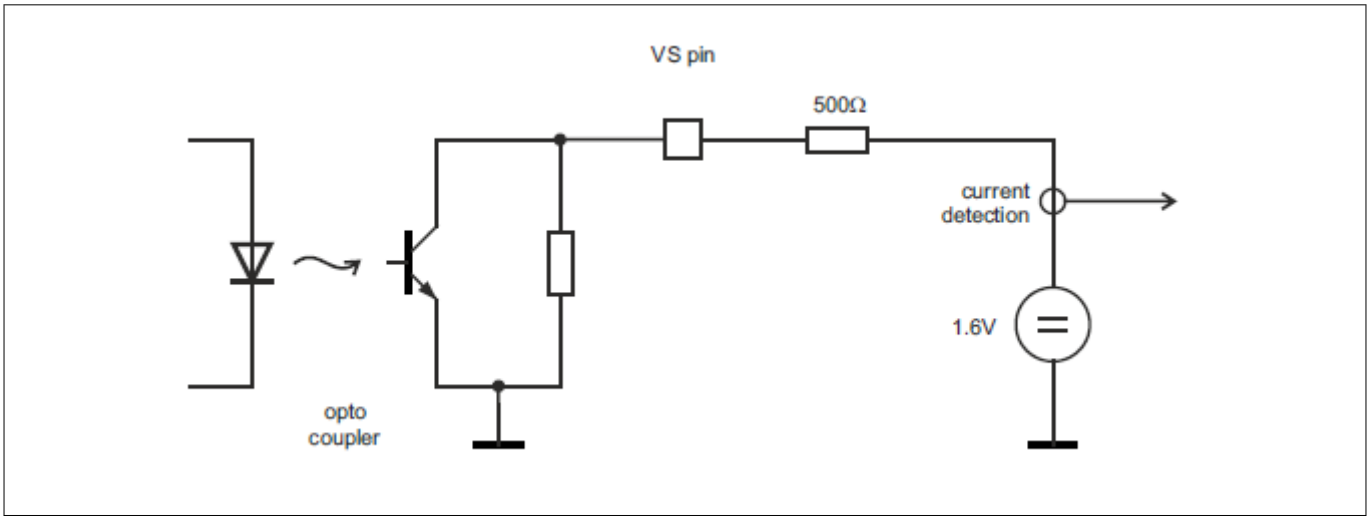


Figure 9 VS pin circuit

3.2 Burst mode

Only valid for ICL8810 and ICL8820.

Burst mode extends the controller's power range for very low loads and enables very low standby power consumption.

The IC wakes up at a fixed repetition frequency of approximately four times the input line frequency and decides based on the *VS* signal, if pulses are necessary to keep the output in regulation range. The duty cycle of each burst is determined by the filtered feedback from the external control loop. The IC uses the current flowing out of the *VS* pin to provide feedback to the IC. This method tends to be less noise sensitive and leads to a very small voltage change on the pin throughout the whole power range.

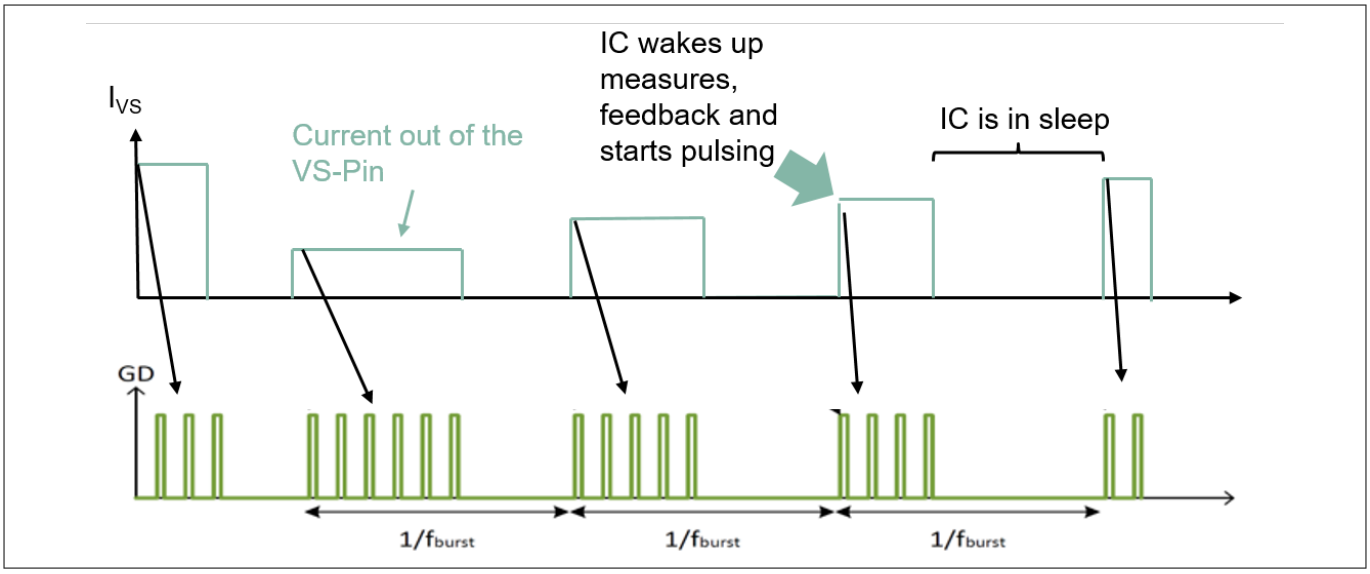


Figure 10 Relation of the feedback current to the duty cycle in the flyback CV topology

Based on the power requested by the *VS* pin, the IC is capable of skipping entire generations of bursts to keep the output in tight regulation range. The missing pulses can lead to a drop of the V_{CC} voltage. To prevent an IC restart due to too low supply voltage, two mechanisms are implemented to overcome this issue:

- In addition to the burst mode wake-up according to the control loop, a higher priority V_{CC} wake-up threshold may trigger a burst start if V_{CC} drops as low as $V_{VCCwake}$. The controller continues with the burst until V_{CC} increases up to $V_{VCCburst}$ again.
- In parallel, the *TD* pin lowers its voltage to allow an external start-up circuit to charge the V_{CC} cap until $V_{VCCburst}$ is reached.

This burst mode control allows tight output regulation and reduces the standby power since no unnecessary pulses are generated. In addition, it allows the use of a small V_{CC} capacitor.

To save energy and lower the standby power consumption, the gate driver operates during burst mode with a lower gate driver level of 7 V.

3.3 Input voltage detection and protection

The controller detects the AC or DC amplitude using an ADC between V_{BI} and V_{VINOV}. The averaged input voltage level is used for power limitation and the brown-in and brownout. In addition, the V_{in} pin voltage is necessary to enable the jitter function (ICL8820 only) for DC input. Theses conditions are checked before start-up and during operation.

In addition, the *VIN* pin has an input OVP threshold of V_{VINOV} and a short protection with a threshold of $V_{VINshort}$ where the IC stops switching and waits until the operating conditions are met again. In case of $V_{VINshort}$, the IC enters a shorter restart cycle of 25 ms. This can be used to achieve lower standby power by actively disabling the IC, but still providing a quick reaction to a turn-on signal.

The brownout and brown-in thresholds of V_{BO} and V_{BI}, respectively, ensure a proper operation at low input voltages.

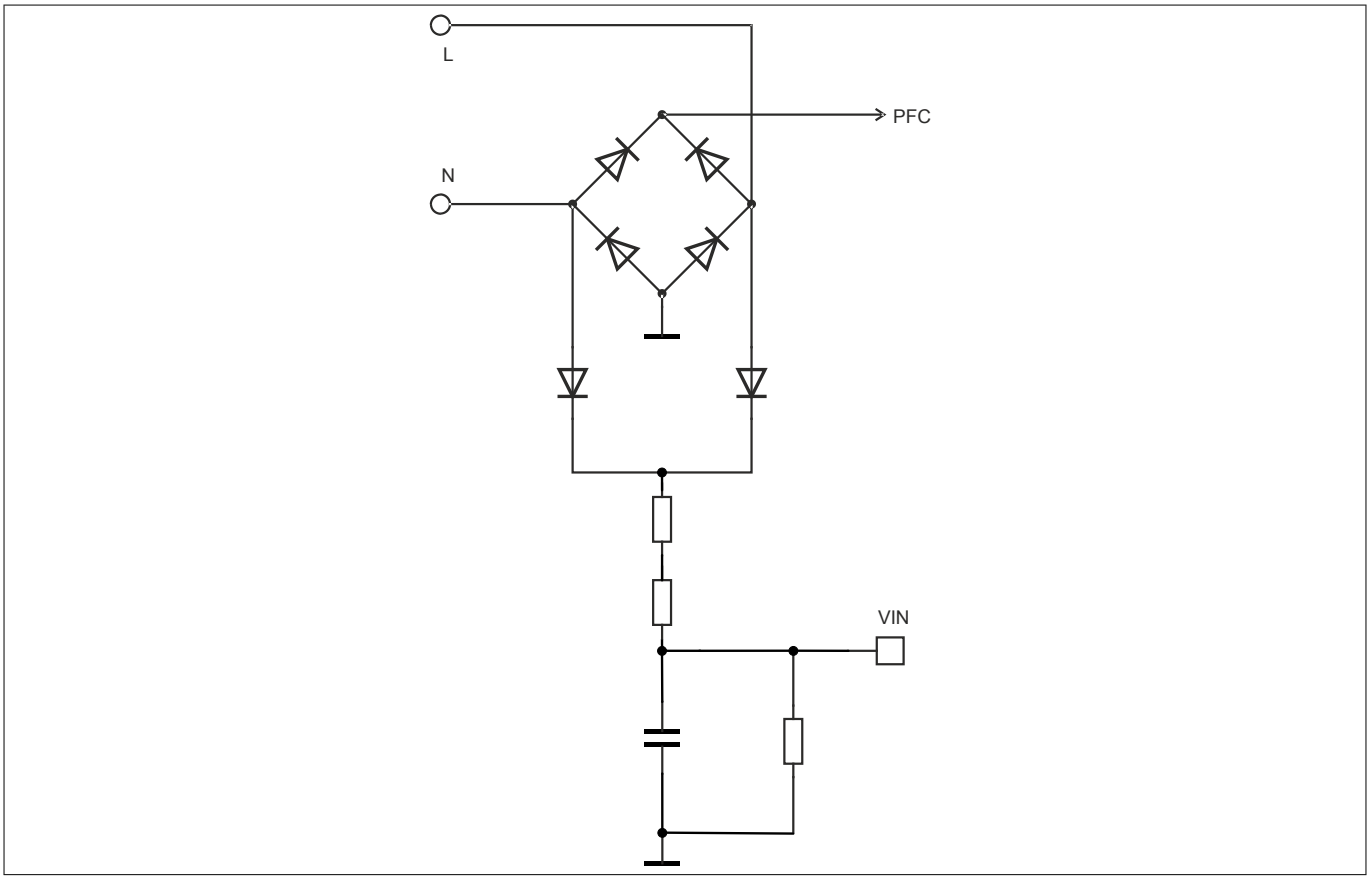


Figure 11 V_{IN} pin circuit

3.4 Zero crossing detection

To minimize switching losses, the controller initiates a new switching cycle when the current through the transformer becomes zero during the off-time of the MOSFET. This time is approximated by detecting the voltage change of the separate *ZCD* winding/auxiliary winding from positive to negative level, which represents a voltage of zero at the inductor windings.

The first occurrence of this condition marks the end of the demagnetization of the flyback transformer and the end of the current flow through the secondary side diode.

For medium to low power levels, the controller switches not at the first occurrence, but counts the number of zero crossings until a desired valley is reached. Even if the valley is not measurable, the IC extrapolates the ringing time to stay in the valley switching.

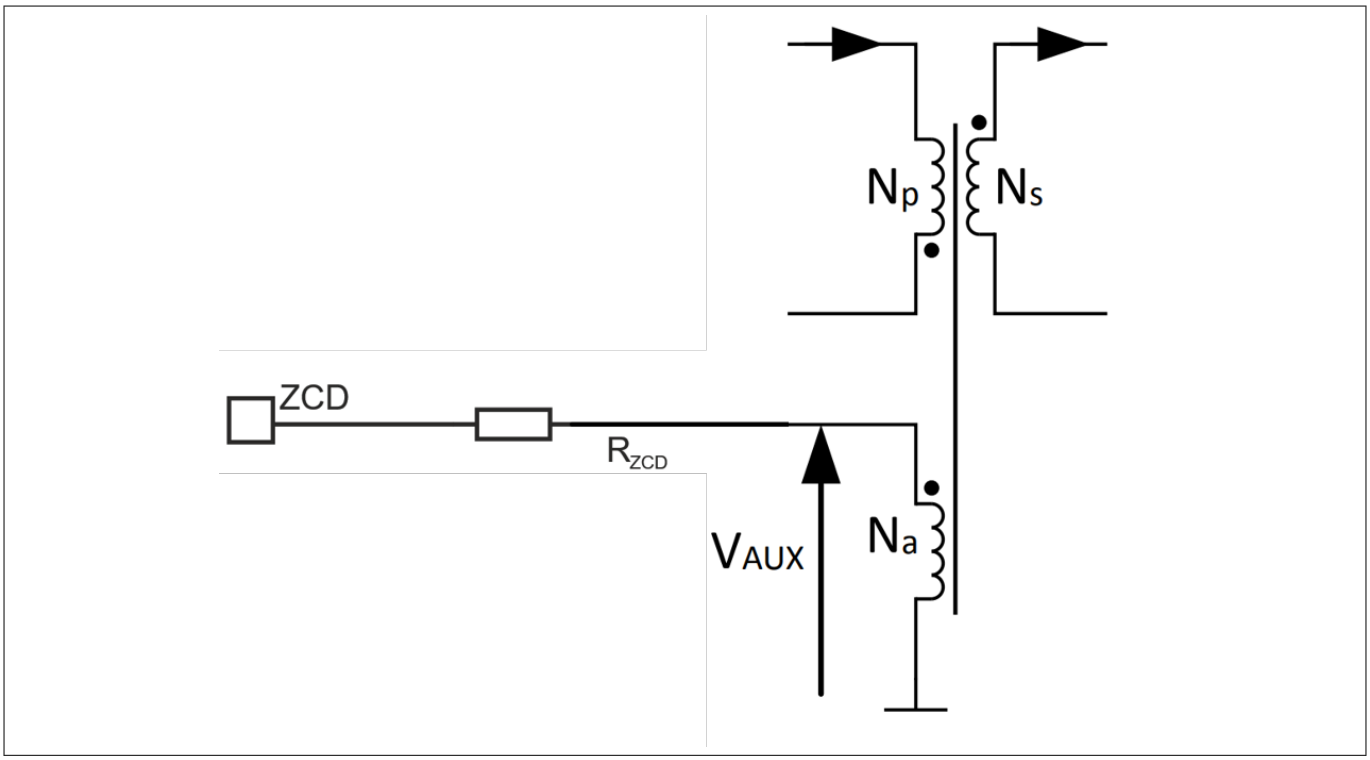


Figure 12 Windings of a flyback transformer

A threshold with hysteresis, V_{ZCDUp} for increasing level and V_{ZCDLow} for decreasing level, is used to detect the change of the transformer voltage. A resistor connected between the auxiliary winding and the *ZCD* pin limits the sink and source currents of the sense pin when the voltage of the auxiliary winding exceeds the internal clamping levels V_{pclp} and V_{nclp} of the IC. When the sensed voltage level of the auxiliary winding is not sufficient (e.g., during start-up), an internal start-up timer will initiate a new cycle every t_{Rep} after turn-off of the gate driver.

The *ZCD* resistor can be used to change the maximum on-time of the controller to limit the power transfer by the system. The maximum on-time for a *ZCD* peak to peak clamp current of 1.2 mA is 20 µs and scales linearly with lower clamp currents as it can be seen in ***Figure 13***.

A very tight limitation of the power by the on-time limits the ability of the system to quickly recover from large load jumps. The adjustment of the *TD* resistor can mitigate the influence on the THD performance caused by changing the maximum on-time.

For wide range designs, an inductor of around 600 µH and for narrow range designs 1000 µH is recommended to utilize the full capabilities of this IC.

3 Functional description

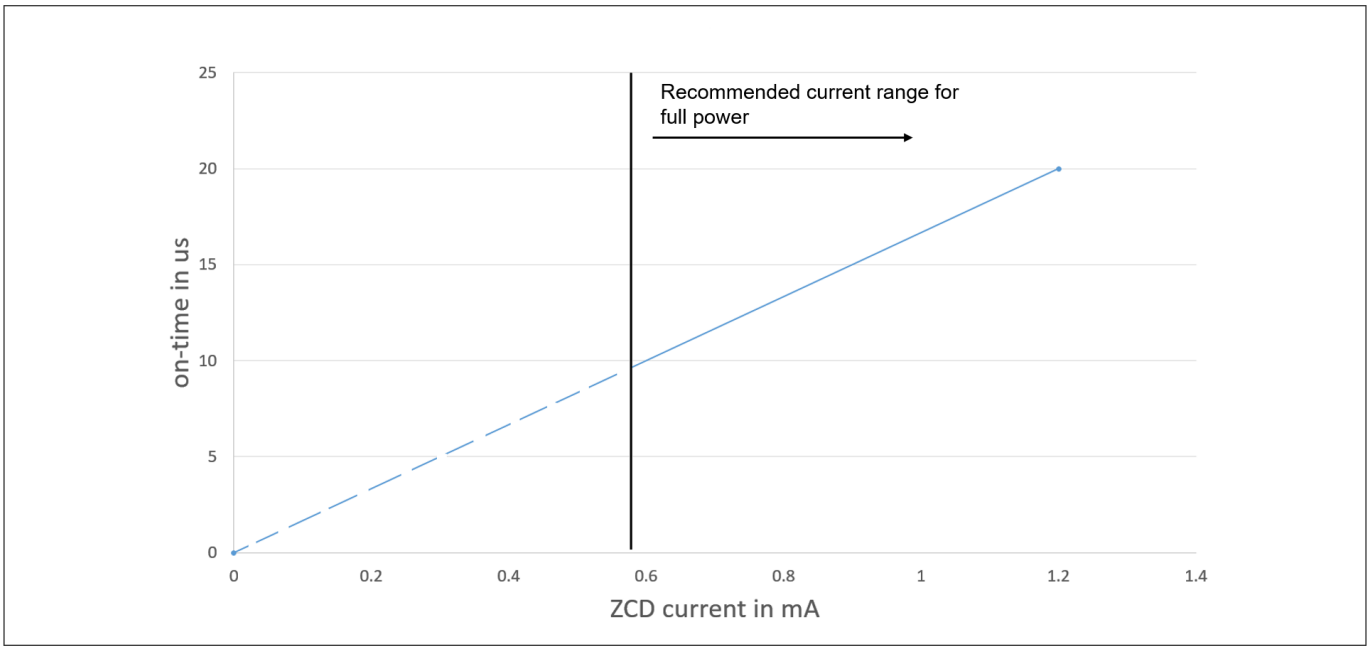


Figure 13 max on-time versus ZCD current

3.5 Power factor correction and THD correction

The gate driver *GD* is used for driving the power MOSFET in voltage mode by on-time control. Suppressing the output ripple with the external feedback loop results in a quasi-constant on-time t_{on} during the AC half-sine wave. This already ensures a basic high power-factor and low THD performance.

In addition, the *ZCD* pin is used for a THD correction function that extends the pulse width of gate signal according to the detected I_{ZCD}. This optimizes the input current waveform, especially in the area near AC voltage zero crossing.

Figure 14 shows the THD correction principle. During low input voltage levels, the on-time of the MOSFET is increased to minimize gaps in the line current during zero crossing of the line voltage and to improve the THD of the input current. This THD correction set with the *TD* resistor. The voltage on the *TD* pin (2.15 V or a 68 kΩ resistor from *TD* to ground) is measured at the start-up and is internally multiplied with the measured I_{ZCD} current. The result is handed over to the pulse generation block inside the IC to create the optimized waveform. In rare cases (small transformer inductance and small capacitor output capacitance which results in a high oscillation frequency), a lower value resistor down to 27 kΩ might result in a better THD performance.

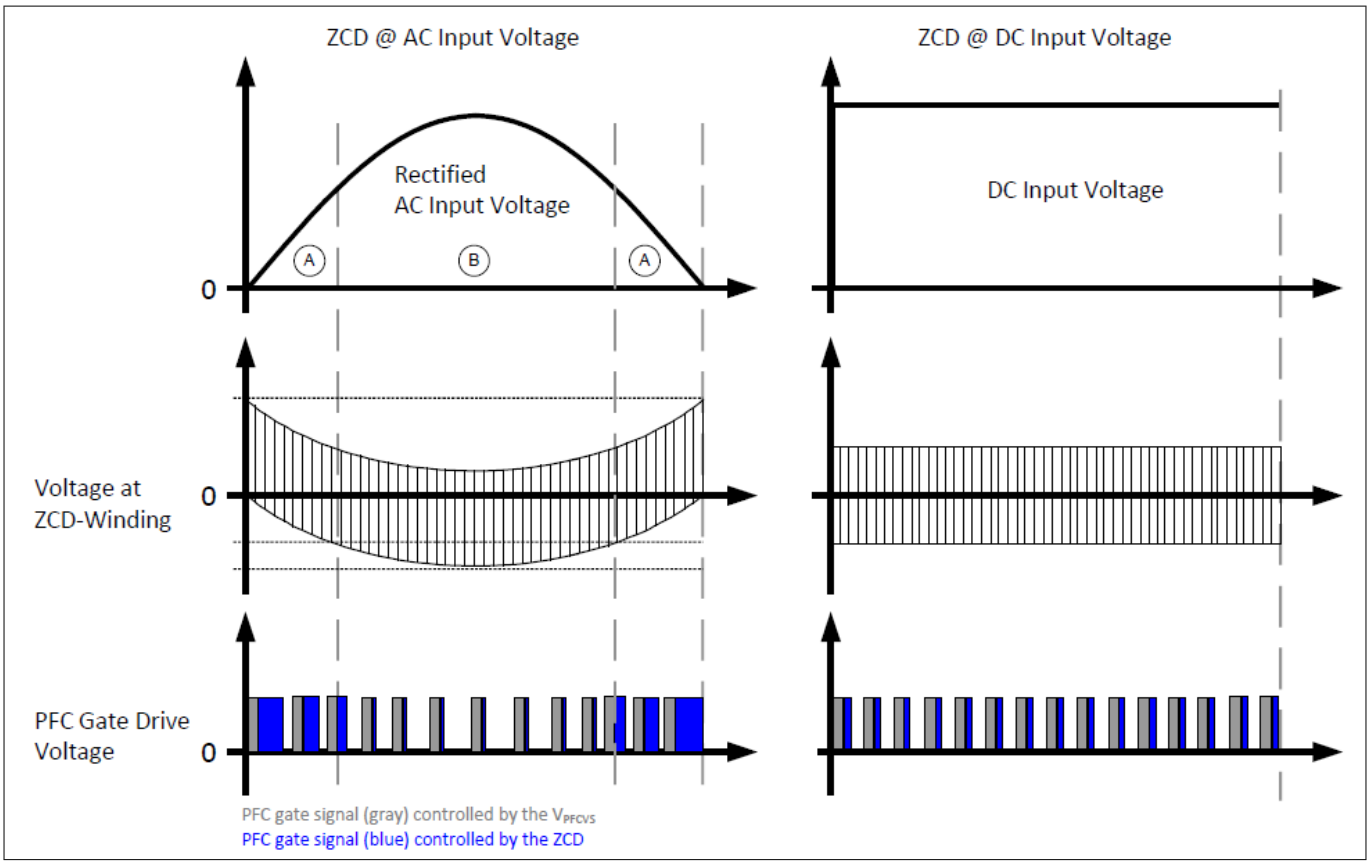


Figure 14 THD improvement – automatic pulse width extension

3.6 Frequency jitter

Only valid for ICL8820.

A jitter function implemented into the IC for DC input voltage eases the design according to EN50172 (Emergency Lighting), which covers the requirements of the radio disturbance according to the EN55015 during mains DC input voltage for emergency lighting.

A DC input voltage usually causes a flyback to operate at a single frequency resulting in the measured EMI spectrum being very high. To avoid this, the IC starts varying the frequency of the gate signal, if a DC voltage is detected at the *VIN* pin. This added jitter spreads the peak and reduces the EMI spectrum. This function is implemented by an additional triangular pattern injected into the internal PWM generator with a frequency of approximately 222 Hz while still adjusting the frequency to maintain the desired output voltage. This manipulation of the internal control loop results in a 5 kHz to 10 kHz jitter of the run frequency dependent on the load and line condition.

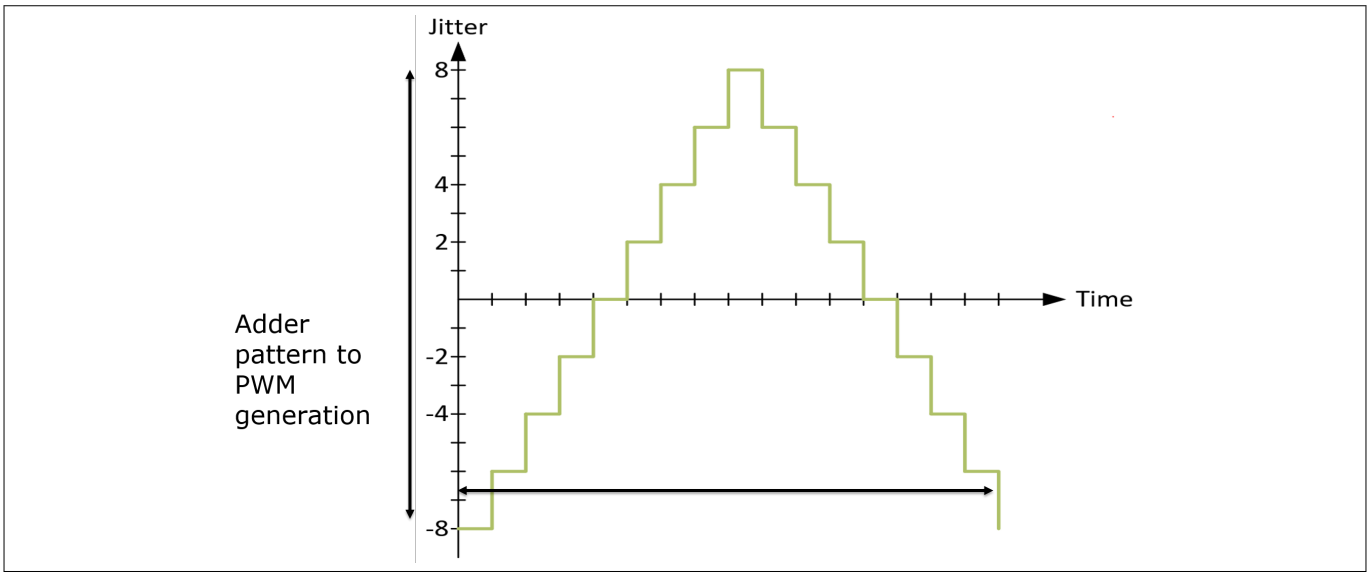


Figure 15 Added jitter function

3.7 Start-up

As long as the voltage on the *VCC* pin is below the V_{CCon} threshold, the controller consumes $I_{VCCstart}$. As soon as the V_{CCon} threshold is reached, the controller senses the resistor at the *TD* pin and the input voltage at the *VIN* pin.

After checking that the start conditions are within the limits (for example input voltage for brown-in, junction temperature), the ICL88xx starts switching. The initial on-time is based on the sensed input voltage. In this phase, the frequency is variable and the IC requires a current of I_{CC} plus the gate driver current. The reduced gate driver voltage V_{GDred} feature enables reducing the V_{CC} capacitor without compromising the time-to-light. In the soft start, the on-time is increased every 280 µs up to a maximum on-time of t_{ON_max}. The control switches to QRM as soon as a sufficient *ZCD* signal becomes available.

The start-up is considered successful as soon as the feedback current requires less power compared to the internal start-up ramp. At the end of the start-up or after 15 ms at the latest, the gate driver level is increased to the voltage level V_{GD} for normal operation to achieve the best possible efficiency for the given power MOSFET.

External start-up cell control:

After the measurement of the *TD* resistance to ground, the pin remains on a high level. The voltage is dependent on the used resistor. It can vary between 0.99 V and 2.33 V. The high level is maintained as long as the IC has a sufficient *VCC* supply. For the ICL8800 the start-up circuit is only active at the initial start-up or during a restart of the IC.

For ICL8810 and ICL8820: While in burst mode, the pin is reset to low when the *VCC* drops below $V_{VCCwake}$ and it is set high again if V_{CC} exceeds $V_{VCCburst}$. The maximum capacitive loading of this pin is 1 nF.

To assure a proper functioning of the IC, a resistor of 12 kΩ has to be placed from *VS* pin to *GND*.

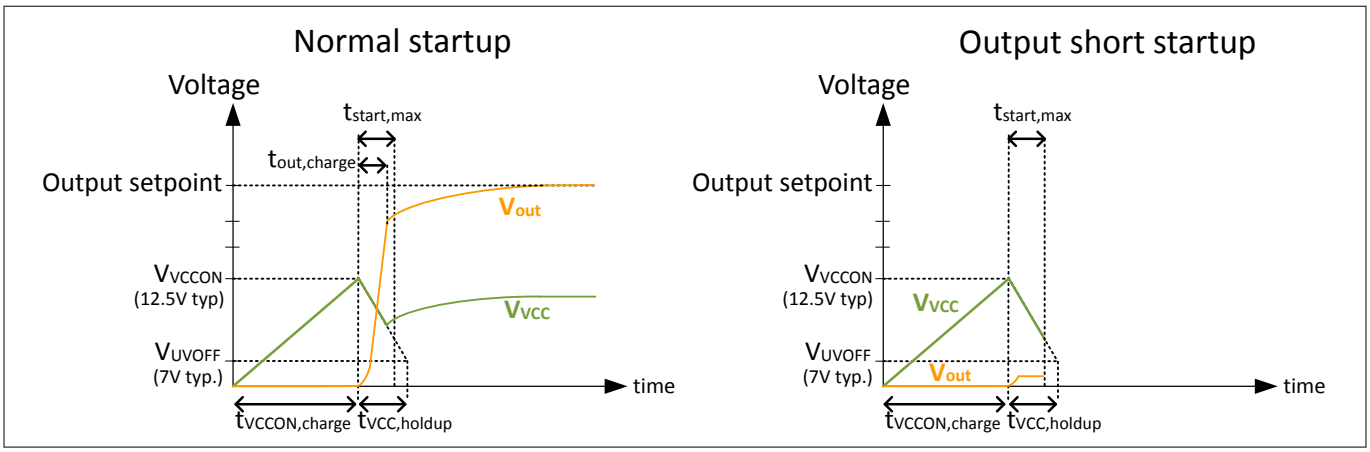


Figure 16 Waveforms of V_{CC} and V_{out} during normal start-up and in output short condition

3.8 Power limitation

Based on the mean voltage detected at the *VIN* pin, the relative power transfer is limited as seen in ***Figure 17***. The power limitation is divided into three sections:

- Voltage range between 0.4 V and 0.6 V: A steep limitation curve to avoid high currents and enable good dynamic behavior above brownout threshold.
- Voltage range between 0.6 V and 2 V: Nearly linear limitation of the output power dependent of V_{ac}.
- Voltage range above 2 V: An input over voltage triggers a restart of the system .

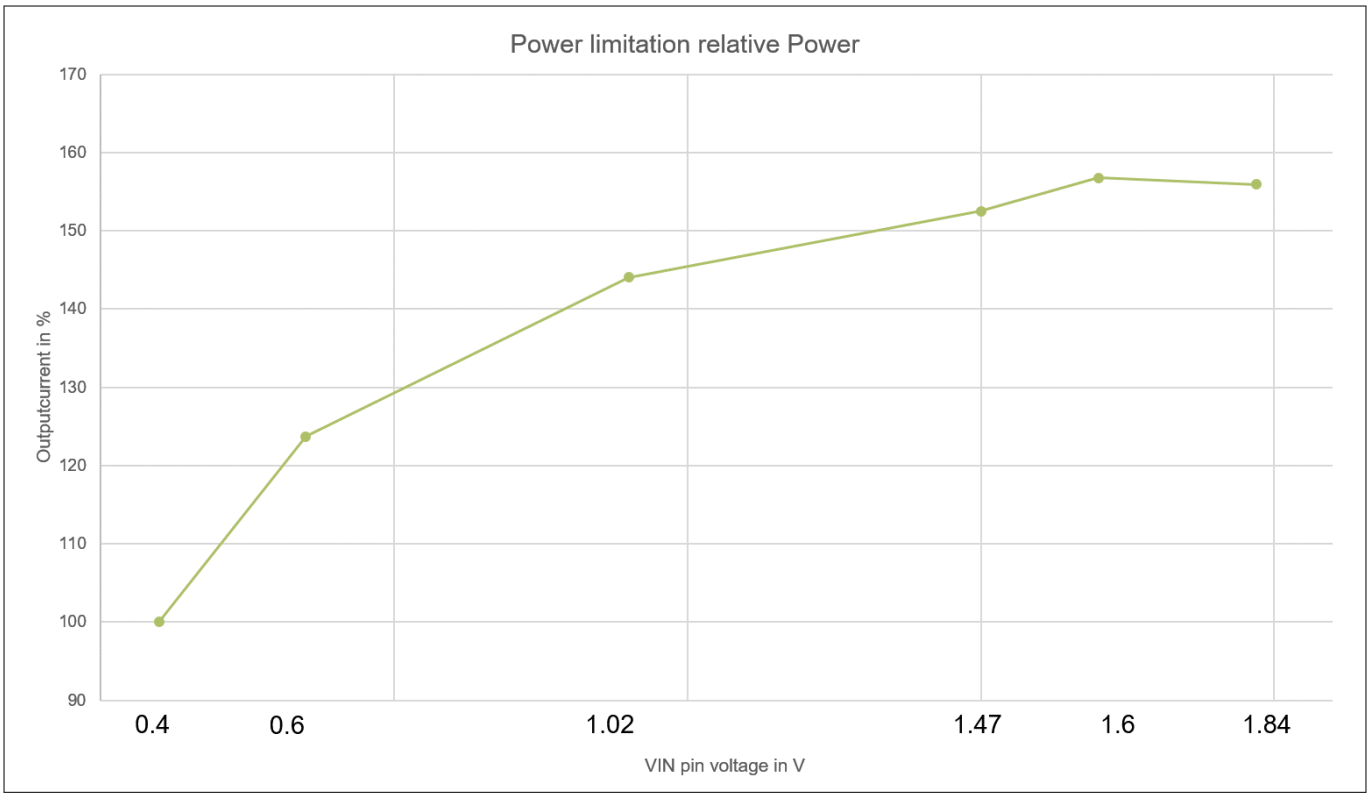


Figure 17 Exemplary representation of the power limitation versus input voltage

This limitation is implemented in the internal pulse generation block by limiting its output to a calculated maximum value.

If an output undervoltage event occurs in the flyback topology, either the power limiting limits the delivered power to the output, allowing large capacitors to be charged, or an insufficient V_{CC} supply triggers a restart.

3.9 Overtemperature protection

ICL8800, ICL8810 and ICL8820 offers a temperature protection using an internal temperature sensor. This feature protects the IC from too high temperatures. The protection starts at an internal temperature of T = 130 °C.

3.10 Overcurrent protection

The input overcurrent protection level 1 is performed by means of the cycle-by-cycle peak current limitation to V_{OCP1}. A leading edge blanking t_{LEB} prevents the IC from falsely switching off the power MOSFET due to a leading edge spike. If the measured current reaches the threshold of 0.6 V at the *CS* pin, the IC turns off the gate.

The input overcurrent protection level 2 is meant for covering fault conditions like a short in the transformer primary winding or transformer core saturation. In this case, overcurrent protection level 1 does not limit properly the peak current due to the very steep slope of the peak current. Once the threshold V_{OCP2} of 1.2 V at the *CS* pin is reached within the time window of t_{OCP2}, the protection is triggered.

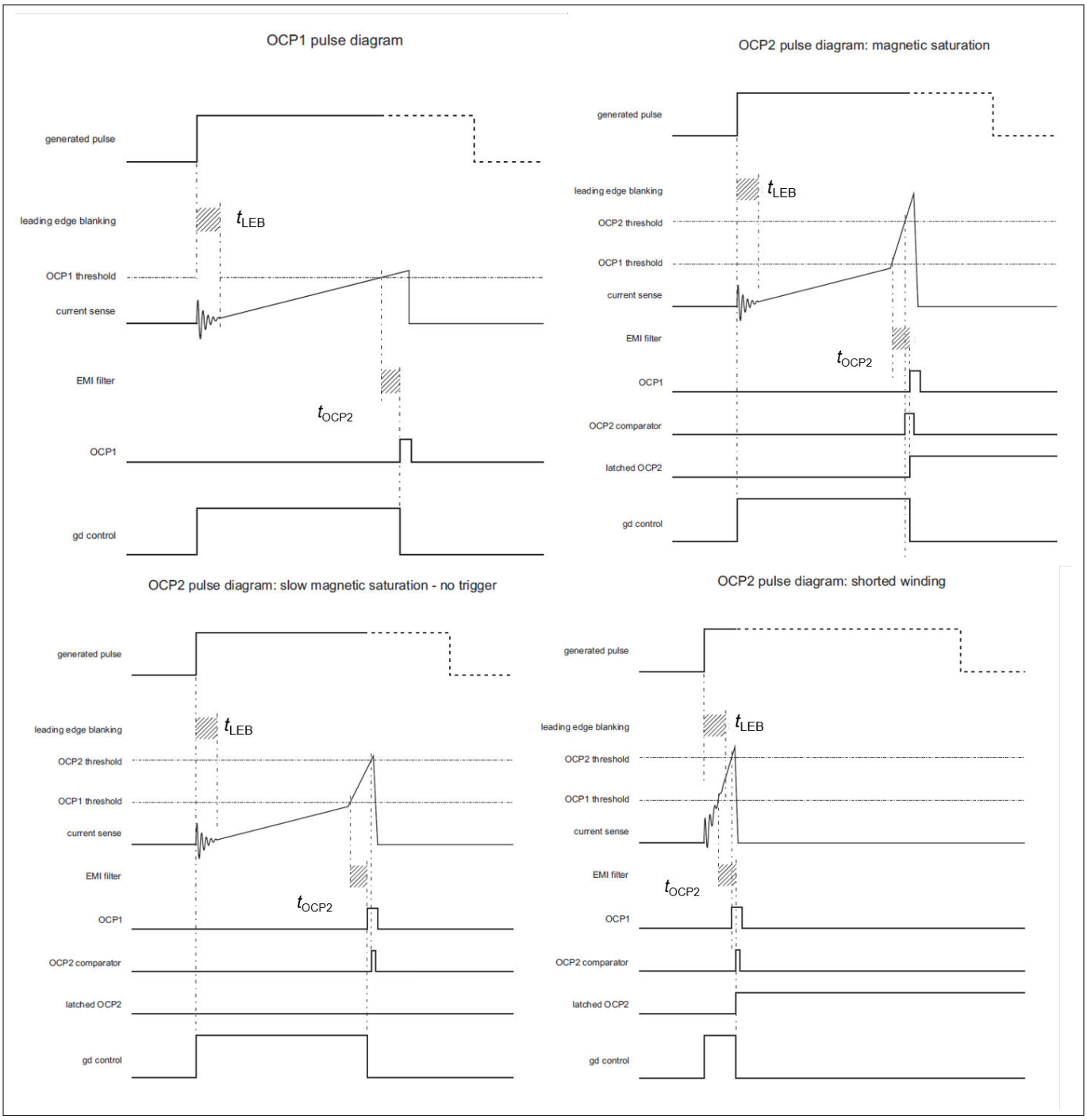


Figure 18 Timing overview of the OCP1 and OCP2

3.11 Output overvoltage protection

The ICL88xx has additionally to the feedback loop a second output overvoltage protection. This protection uses the *ZCD* clamp current during the demagnetization time to protect the output. The *ZCD* clamp current is internally converted to a current out of the *CS* pin with the conversion ratio n_{ZCDOVP}. Depending on the *CS* series resistance, the V_{OCP1} threshold triggers the protection.

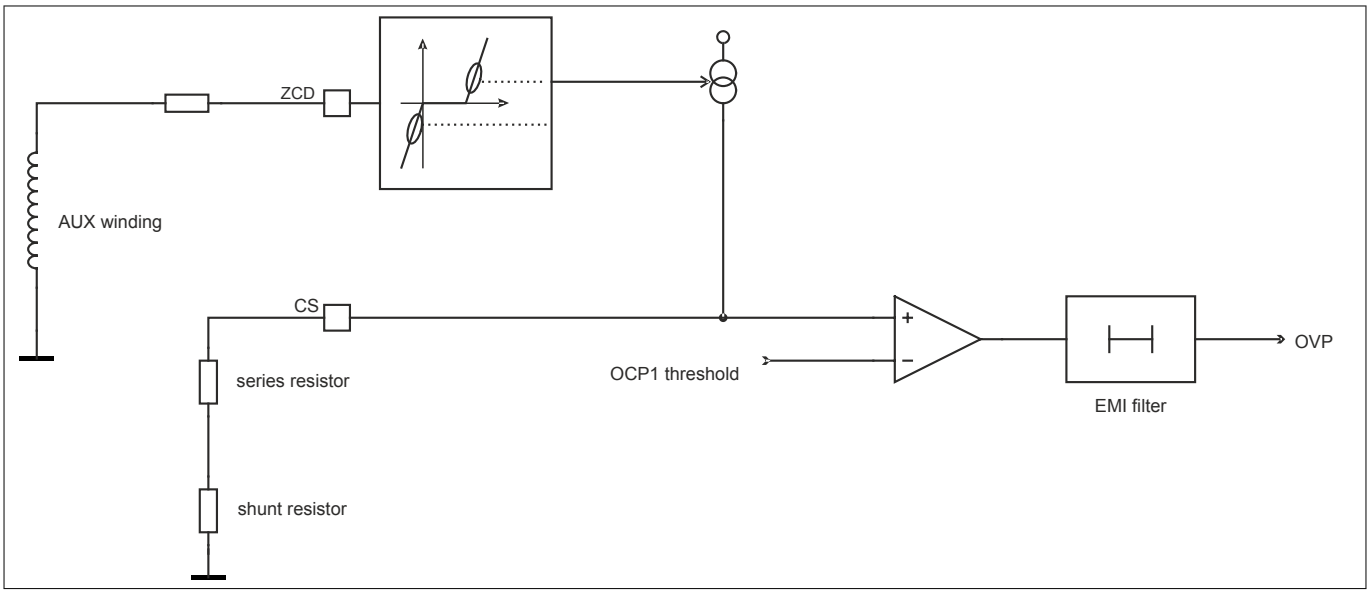


Figure 19 Flyback secondary OVP

Due to this protection, the voltage at the *CS* pin is not zero during the demagnetization, but mirrors the reflected output voltage.

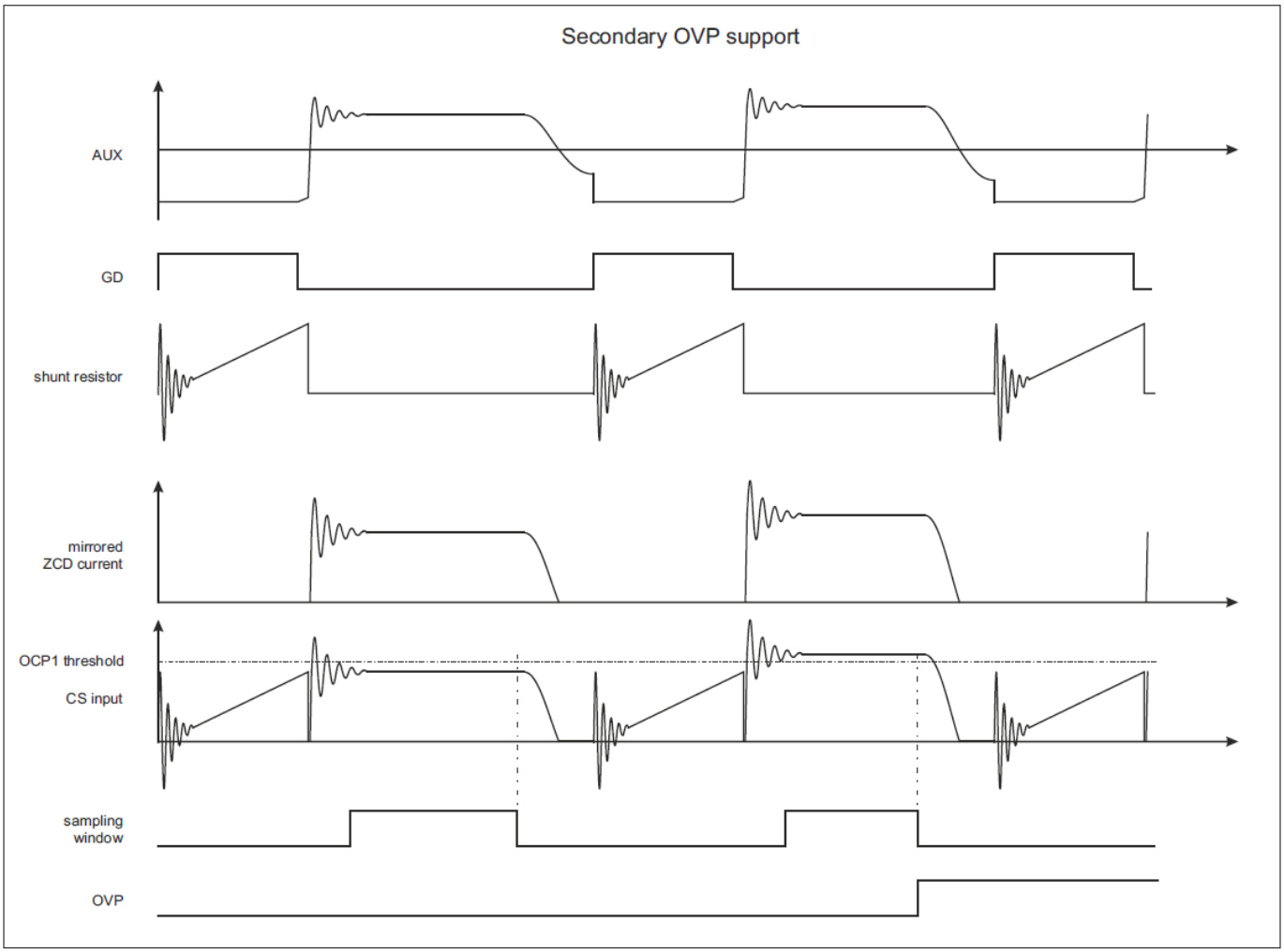


Figure 20 Flyback CS waveform

3.12 Open loop protection

An open feedback loop results in maximum power transfer after the soft-start. The flyback secondary over voltage protection is triggered once the over voltage threshold is exceeded for a longer time than the related blanking time. This causes an auto-restart.

In the case of an open *VS* pin, due to the *VS* pin sourcing, a current of 1 µA out of the IC during normal operation, the voltage at the *VS* pin rises. The *VS* pin voltage is compared to the over voltage comparator threshold $V_{VSOVOFF}$. If the voltage exceeds the threshold for longer than the related blanking time, the overvoltage protection blocks any switching. A restart may occur if the V_{CC} voltage drops below the undervoltage lockout unit (UVLO) threshold.

3.13 VCC protections

An UVLO is implemented that ensures a defined enabling and disabling of the IC operation depending on the supply voltage at the *VCC* pin. The UVLO contains a hysteresis with the voltage thresholds V_{VCCon} for enabling the IC and V_{VCCmin} for disabling the IC. As soon as the mains input voltage is applied, current flows into the *VCC* pin. The IC is enabled when V_{CC} exceeds the threshold V_{VCCon} and enters normal operation when no fault condition is detected. In this phase, V_{CC} drops until the self-supply via the auxiliary winding takes over the supply at the *VCC* pin. For a proper start-up, the self-supply via auxiliary winding must be in place before V_{CC} falls below V_{VCCmin} threshold.

If the voltage at the *VCC* pin reaches $V_{VCCclamp}$ during start-up, restart and in the burst pause, the IC is able to sink up to $I_{VCCclamp}$. Overvoltage detection at the *VCC* pin is implemented via a threshold of V_{VCCmax}. The start-up behaviour can be seen in ***Figure 16***.

ICL8810 and ICL8820 only

To prevent an IC restart due to too low supply voltage, two mechanisms are implemented to overcome this issue:

- In addition to the burst mode wake-up according to the control loop, a higher priority *VCC* wake-up threshold may trigger a burst start if *VCC* drops as low as $V_{VCCwake}$. The controller continues with the burst until V_{CC} increases up to $V_{VCCburst}$ again.
- In parallel, the *TD* pin lowers its voltage to enable an external start-up circuit to charge the *VCC* cap until $V_{VCCburst}$.

3.14 Fault reaction and flow chart

Flow chart

The ***Figure 21*** shows the different states of the IC and the conditions to change the state.

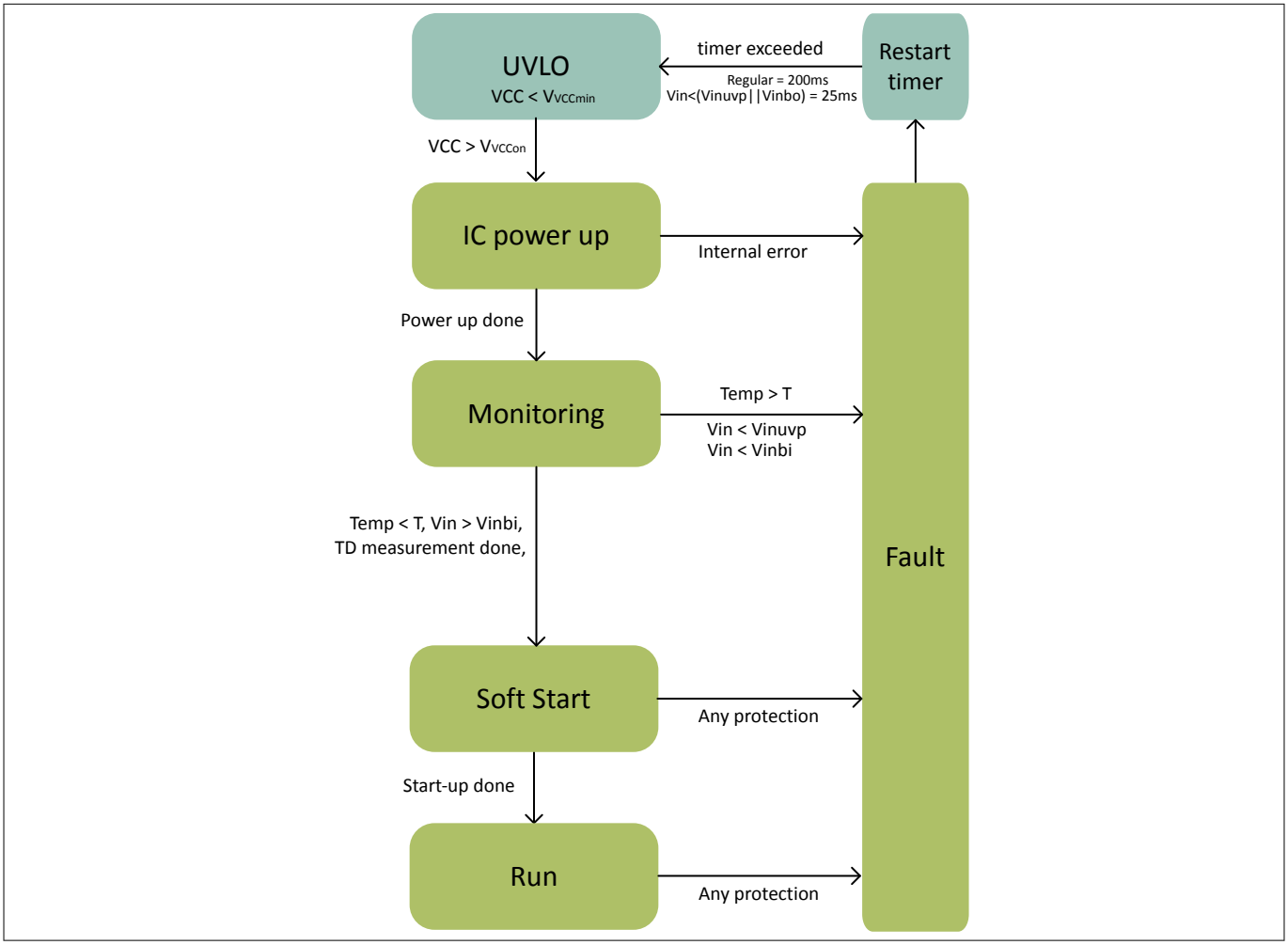


Figure 21 ICL88xx flow chart

Fault reaction

The controller handles protections as listed in ***Table 2***.

Note: Some blanking times vary slightly with the line frequency.

Table 2 Fault matrix

Fault	Detection	Typical blanking time	State			Reaction
			Monitor	Soft-start	Run	
Insufficient supply	$V_{VCC} < V_{VCCon}$	1 µs	X	-	-	Wait in reset
Insufficient supply	$V_{VCC} < V_{VCCmin}$	1 µs	X	X	X	Reset
VCC overvoltage	$V_{CC} > V_{VCCOVP}$	1 µs	-	X	X	Auto-restart after $t_{restart}$
VIN short protection	$V_{VIN} < V_{VINshort}$	1 µs	X	X	X	Auto-restart after $t_{restart}$
VIN undervoltage protection	$V_{VIN} < V_{BI}$	2 ms	X	X	X	Fast auto-restart after $t_{restart,fast}$
VIN overvoltage protection	$V_{VIN} < V_{VINOV}$	2 ms	X	X	X	Auto-restart after $t_{restart}$
Overcurrent protection (OCP1)	$V_{CS} > V_{OCP1}$	250 ns	-	X	X	Turn off gate driver for the on-going switching cycle
Overcurrent protection (OCP2)	$V_{CS} > V_{OCP2}$	150 ns	-	X	X	Auto-restart after $t_{restart}$
Secondary output overvoltage protection	$I_{ZCD}{}^{*}n_{ZCDOVP} > V_{OCP1}$	100 µs	-	X	X	Auto-restart after $t_{restart}$
Overtemperature	$T > T_{critical}$	18 µs	X	X	X	Auto-restart after $t_{restart}$
VS overvoltage	$V_{VS} > V_{VSOVOFF}$	20 µs	-	X	X	Turn off gate driver and restart if $V_{VS} < V_{VSOVON}$

3.15 Adjustable functions

Some features of the controller can be adjusted using external circuitry:

- The maximum power/on-time/operating point can be configured using the *ZCD* to aux winding resistance.
- The flyback output over voltage protection can be configured using the *CS* series resistance to the shunt resistor.
- Brown-in and out Protection and the related input over voltage protection
- Primary side over current protection

Please refer to the Design Guide for details.

4 Electrical characteristics and parameters

All signals are measured with respect to the ground pin, *GND*. The voltage levels are valid provided that other ratings are not violated.

4.1 Absolute maximum ratings

Note: Absolute maximum ratings are defined as ratings, which if exceeded may lead to destruction of the integrated circuit. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.

Table 3 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VCC voltage	V_{CC}	-0.5	–	26	V	
Junction temperature	T_j	-40	–	150	°C	
Storage temperature	T_S	-55	–	150	°C	
Soldering temperature	T_S	–	–	260	°C	Wave soldering according to JESD22-A111 Rev A.
Thermal resistance junction to ambient	R_{ThJA}	–	–	185	K/W	
Power dissipation at 50°C	P_D	–	–	0.5	W	
ESD capability HBM	V_{ESD}	–	–	2	kV	ESD-HBM according to ANSI/ ESDA/JEDEC JS-001.
ESD capability CDM	V_{ESD}	–	–	500	V	ESD-CDM according to ANSI/ ESDA/JEDEC JS-002.
GD voltage	V_{GD}	-0.5	–	V_{CC} + 0.3	V	
CS voltage	V_{CS}	-0.5	–	3.6	V	
CS current	I_{CS}	-2	–	2	mA	
ZCD voltage	V_{ZCD}	-1.2	–	3.6	V	
ZCD current	I_{ZCD}	-4	–	4	mA	
VS voltage	V_{VS}	-0.3	–	3.6	V	
VIN voltage	V_{VIN}	-0.3	–	3.6	V	
TD voltage	V_{TD}	-0.3	–	3.6	V	

4.2 Operating conditions

The recommended operating conditions are shown for which the DC electrical characteristics are valid.

Table 4 Operating characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Junction temperature	T_J	-40	–	125	°C	
Supply voltage	V_{CC}	8	–	24	V	
External capacitance at the *TD* pin	C_{TD}	–	–	1	nF	

4.3 DC electrical characteristics

The electrical characteristics provide the spread of values applicable within the specified supply voltage and junction temperature range. Devices are tested in production at T_A = 25 °C. Values have been verified either with simulation models or by device characterization up to 125 °C. Typical values represent the median values related to T_A = 25 °C.

All voltages refer to *GND*, and the assumed supply voltage is V_{CC} = 15 V, if not otherwise specified.

4.3.1 Power supply

Table 5 Power supply characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VCC turn-on threshold	V_{VCCon}	12.0	12.5	13.1	V	
Start-up current	$I_{VCCstart}$	–	30	–	µA	
Supply current	I_{CC}	–	2.0	–	mA	IC self-supply excluding gate currents.
Supply current during burst pause	$I_{CCburst}$	–	220	–	µA	
Supply current in protection mode	$I_{CCrestart}$	–	40	–	µA	
VCC undervoltage threshold	V_{VCCmin}	6.0	6.6	7.6	V	
VCC wake-up threshold	$V_{VCCwake}$	6.6	7.6	8.8	V	
VCC burst threshold	$V_{VCCburst}$	7.1	8.1	9.1	V	
Difference between $V_{VCCwake}$ and $V_{Vccburst}$	V_{delta}	500	–	–	mV	
VCC overvoltage threshold	V_{VCCmax}	23.8	25	26.4	V	
VCC clamp voltage after *VCC* overvoltage	$V_{VCCclamp}$	–	24.2	–	V	
VCC clamp current	$I_{VCCclamp}$	–	2.5	–	mA	

4.3.2 Zero crossing detection

Table 6 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Zero crossing threshold (falling edge)	$V_{ZCDDown}$	10	45	–	mV	
Zero crossing threshold (rising edge)	V_{ZCDUp}	–	55	90	mV	
Clamping current	I_{ZCDclp}	–	–	1.2	mA	Applies to positive and negative clamping.
Clamping of positive voltages	$V_{ZCDpclp}$	400	550	700	mV	$I_{ZCDSink}$ = 1 mA
Clamping of negative voltages	$V_{ZCDnclp}$	-600	-500	-400	mV	$I_{ZCDSource}$ = - 1 mA
ZCD ringing suppression time	$t_{Ringsup}$	350	700	1100	ns	
ZCD to *CS* current ratio for flyback secondary side OVP	n_{ZCDOVP}	0.455	0.484	0.513		$I_{CSsource}$ / I_{ZCDclp} at 1.2 mA
ZCD to *CS* current ratio for flyback secondary side OVP	n_{ZCDOVP}	0.450	0.484	0.518		$I_{CSsource}$ / I_{ZCDclp} at 0.8 mA

4.3.3 Voltage sense

Table 7 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
VS bias current	- I_{VSBias}	0.5	1.0	1.5	µA	V_{VS} = V_{ref}
Voltage source for optocoupler/feedback supply	V_{VS}	1.56	1.6	1.63	V	Internal series resistance of 500 Ω.
VS current threshold for start up	- I_{VSsink}	102	130	154	µA	12 kΩ from VS to GND recommended.
Open pin turn-off	$V_{VSOVOFFFB}$	2.64	2.7	2.76	V	
ADC lower current limit	- $I_{VSADCmin}$	166	210	260	µA	For maximum ontime during operation
ADC upper current limit	- $I_{VSADCmax}$	500	610	720	µA	For minimum ontime in burst mode

4.3.4 Input voltage detection

Table 8 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Brownout voltage level	V_{BO}	0.4	0.42	0.44	V	DC threshold after internal averaging.
Brown-in voltage level	V_{BI}	0.61	0.63	0.65	V	DC threshold after internal averaging.
VIN pin short to GND threshold	$V_{VINshort}$	150	200	250	mV	
VIN over voltage threshold	V_{VINOV}	1.9	2.0	2.1	V	

4.3.5 THD configuration

Table 9 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Internal pull up resistor for THD tuning	$R_{TD,flyback}$	32	40	48	kΩ	Internal voltage 3.3 V.
Minimum threshold for THD tuning	$V_{TD,low}$	0.94	1.02	1.1	V	
Maximum threshold for THD tuning	$V_{TD,high}$	2.18	2.28	2.4	V	
Resistor range for THD correction function	R_{TD}	27	–	68	kΩ	Only valid for resistor from *TD* pin to *GND.*

4.3.6 Current sense

Table 10 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
OCP1 turn-off threshold	V_{OCP1}	570	610	650	mV	
OCP1 leading-edge blanking time	t_{LEB}	240	295	350	ns	Pulse width when $V_{CS} > V_{OCP1}$; no production test.
Over current blanking and propagation delay	t_{CSOff}	–	290	–	ns	Propagation delay = 50 ns; no production test.
OCP2 turn-off threshold	V_{OCP2}	1140	1210	1260	mV	
OCP2 trigger time	t_{OCP2}	–	150	–	ns	Pulse width when $V_{CS} > V_{OCP2}$; no production test.
CS pull-up current	$-I_{CSPU}$	0.5	1	1.5	µA	

4.3.7 PWM generation

Table 11 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Initial on-time [1)]	$t_{ON\_initial}$	1.75	6.0	10.64	µs	Depending on input voltage, not tested in production.
Maximal on-time [2)]	t_{ON_max}	16	20	-	µs	For I_{ZCDclp} = 1.2 mA, not tested in production.
Minimum on-time	t_{ON_min}	–	200	–	ns	Depends on MOSFET gate capacitance. Pulses are minimum 800 ns, but can be shortened due to pre-charging, not tested in production.
Repetition time [1)]	t_{Rep}	47	52	60	µs	V_{ZCD} = 0 V, not tested in production.
Off-time	t_{Off}	42	47	52.5	µs	Not tested in production.

1 When missing zero crossing signal.
2 At the maximum of the AC line input voltage in RUN mode.

4.3.8 Gate driver

Table 12 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
GD source current	$-I_{source}$	125	–	–	mA	The parameter is not subject to production testing – verified by design/ characterization.
GD sink current	I_{sink}	250	–	–	mA	The parameter is not subject to production testing – verified by design/ characterization.
GD voltage	V_{GD}	10.4	11.0	11.6	V	V_{CC} > 11.5 V
Reduced *GD* voltage during start-up and burst mode	V_{GDred}	6.5	7.0	7.5	V	V_{CC} > 7.7 V

4.3.9 Clock oscillators

Table 13 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Restart time	$t_{restart}$	–	200	–	ms	Not tested in production.
Fast restart time	$t_{restart,fast}$	–	25	–	ms	Only for *VIN* under voltage event; not tested in production.

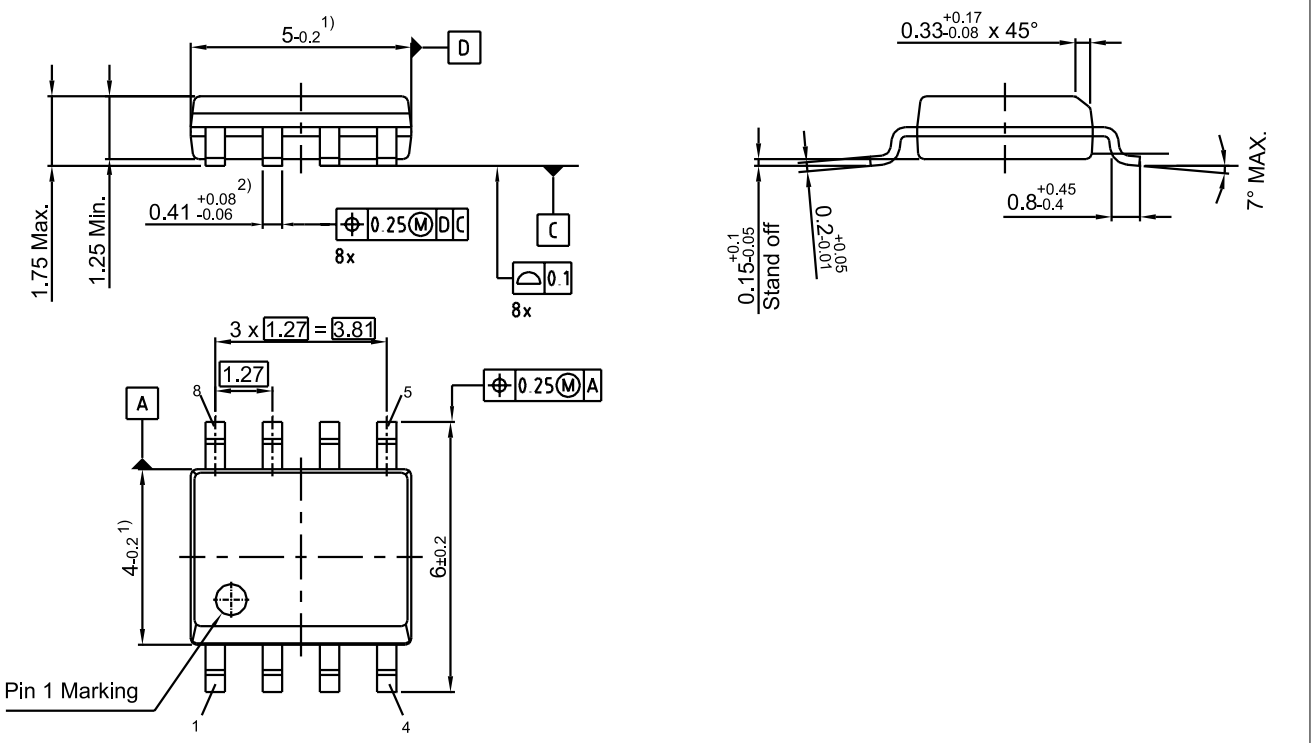
4.3.10 Temperature sensor

Table 14 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Relative accuracy of the temperature sensor	ΔT	-6	–	+6	°C	
End temperature for power limitation and shutdown temperature	T	–	130	–	°C	

5 Package dimensions

The package dimensions of PG-DSO-8 are provided.



1) Does not include plastic or metal protrusion
2) Does not include dambar protrusion of 0.127 Max. in excess of the lead width dimension
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 22 Package dimensions for PG-DSO-8

5 Package dimensions

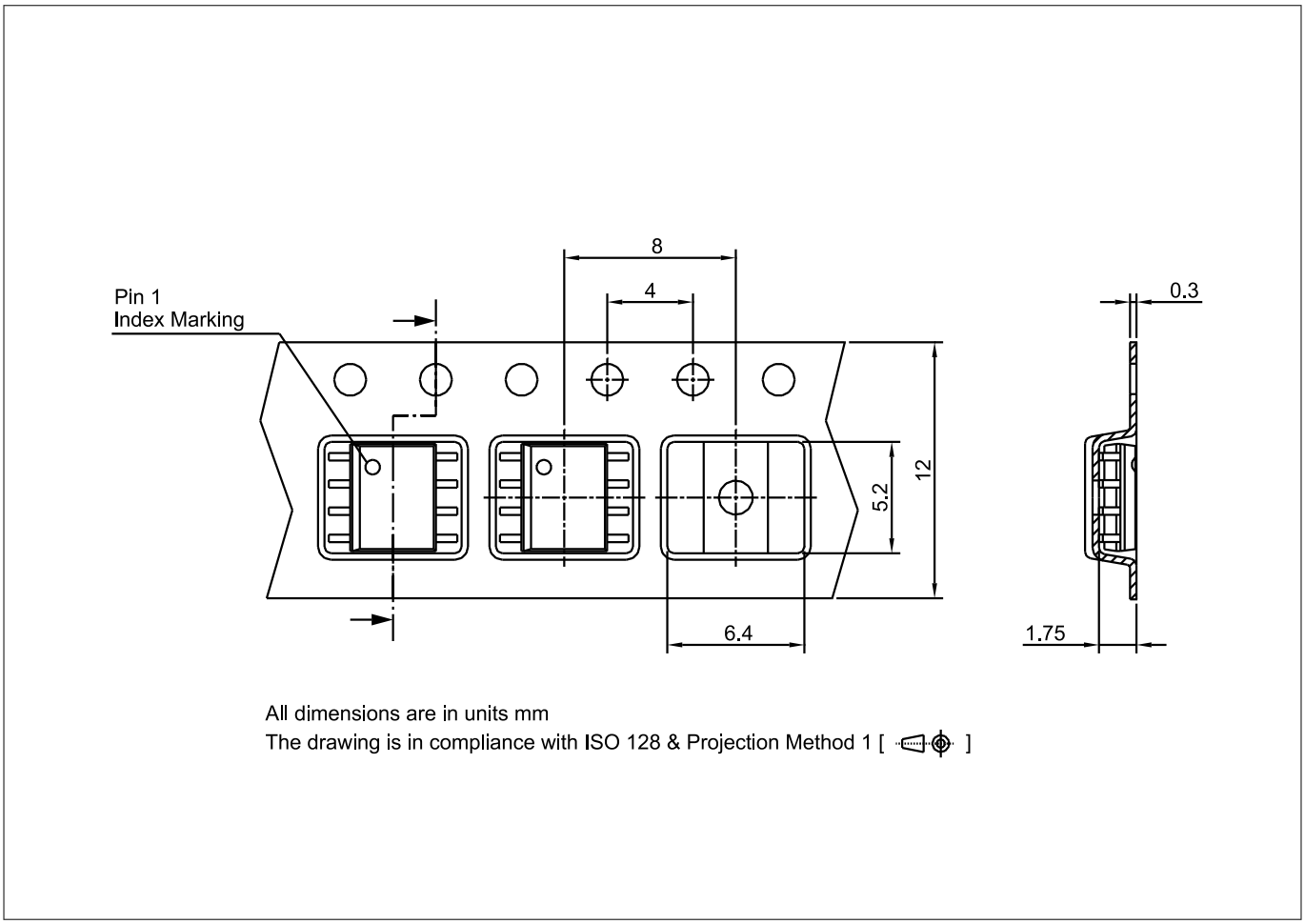


Figure 23 Tape and reel for PG-DSO-8

Note: You can find all of our packages, packing types and other package information on our Infineon Internet page “Products”: http://www.infineon.com/products.

6 Glossary

AC	Alternating current
ADC	Analog-to-digital converter
BM	Burst mode
CV	Constant voltage
CCM	Continuous conduction mode
DC	Direct current
DCM	Discontinuous conduction mode
EMI	Electromagnetic interference
ESD	Electrostatic discharge
LED	Light emitting diode
OCP	Overcurrent protection
OTP	Overtemperature protection
OVP	Overvoltage protection
PF	Power factor
PFC	Power factor correction
PSR	Primary side regulated
QR	Quasi-resonant
QRM	Quasi-resonant mode
SSR	Secondary side regulation
THD	Total harmonic distortion
UVLO	Under voltage lockout unit

7 Revision history

Revision	Date	Changes
1.0	2021-03-17	Initial release

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