15 V/1.2 A isolated PSR Flyback converter based on VIPER31

Introduction

The STEVAL-VP318L2F implements a 15 V/18 W power supply with a wide (90 to 265 V_{AC}) input voltage range, set in isolated flyback topology with primary side regulation (PSR).

The power supply has the following characteristics:

- 4-point average active mode efficiency at full load: >83%
- 4-point average active mode efficiency at 10% full load: >78%
- input power consumption at 0.01 A/230 V_{AC}: < 200 mW (efficiency >80%)
- Compliant with IEC55022 Class B conducted EMI, even with reduced EMI filter
- Independently settable input undervoltage/overvoltage protections
- RoHS compliant

The evaluation board is based on the VIPER318LDTR off-line high voltage converter with the following features:

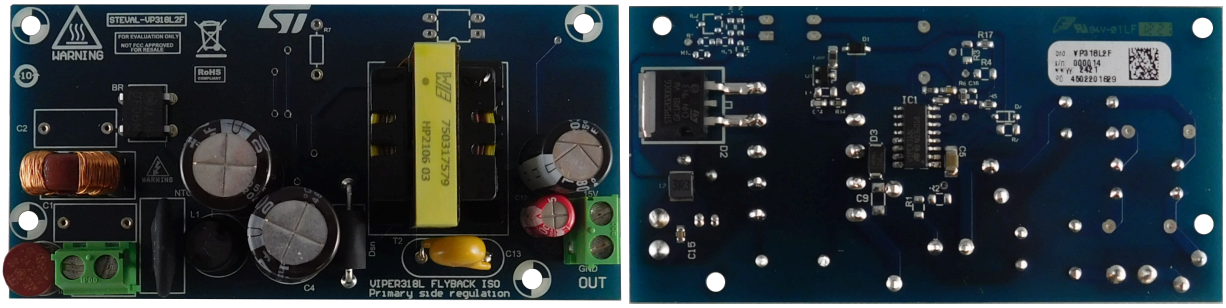
- 800 V avalanche rugged Power MOSFET
- Embedded HV start-up
- On-board trans-conductance error amplifier internally referenced to 1.2 V ±2%
- Current mode PWM controller with drain current limit protection for easy compensation
- Pulse frequency modulation (PFM) and ultra-low stand-by consumption of the internal circuitry under light load condition
- 60 kHz fixed switching frequency with jittering

Enhanced system reliability through built-in soft start function and the following set of protections:

- pulse skip mode to avoid flux-runaway
- delayed overload protection (OLP)
- input overvoltage protection
- input undervoltage protection
- thermal shutdown protection

Excluding pulse-skip mode, all protections are auto restart mode.

Figure 1. STEVAL-VP318L2F evaluation board top and bottom



RELATED LINKS

To configure the board for PSR operation, see STEVAL-VP318L1F

1 Circuit description

The PCB is designed to accommodate primary side regulation (PSR) or secondary side regulation (SSR), which is determined by specific BOM component choices. The STEVAL-VP318L2F specifically implements PSR operation.

FB is the inverting input of the VIPER318LDTR internal error amplifier and is an accurate 1.2 V voltage reference. The VCC to GND voltage value (V_{CC} in the equation below) is accurately set through a voltage divider connected across VCC, FB and GND, according to:

$$V_{CC} = \left(1 + \frac{R1}{R2}\right) \cdot 1.2\,V \quad (1)$$

where R1 is the high side resistor and R2 is the low side resistor.

V_{CC} and V_{OUT} (output voltage) should be related to each other through the N_S/N_{AUX} turn ratio only, according to:

$$V_{OUT} = \frac{N_S}{N_{AUX}} \cdot \left[\left(1 + \frac{R1}{R2}\right) \cdot 1.2V + V_{dAUX}\right] - V_{dOUT} \quad (2)$$

where V_{dAUX} and V_{dOUT} are the forward voltage drops of the auxiliary and output rectifiers, respectively.

Different non-idealities, mainly transformer parasitic, might cause the actual ratio to deviate from the ideal one. The most effective way to improve regulation is to use the circuit composed by Q1, C14 and R14 (see Section 1.2 Schematic diagrams), which blanks the spike appearing at the leading edges of the voltage generated by the auxiliary winding. This spike is due to the transformer leakage inductance and is the major responsible for poor load regulation.

Resistors R1, R2, R3 and R4 form a voltage divider from the rectified input mains to implement input undervoltage and overvoltage protections. By default, these resistors are disconnected and a 0 Ω R17 is mounted to minimize board consumption in no-load and light-load conditions. In this way, the OVP pin is connected to GND and UVP pin is left floating to disable their functions.

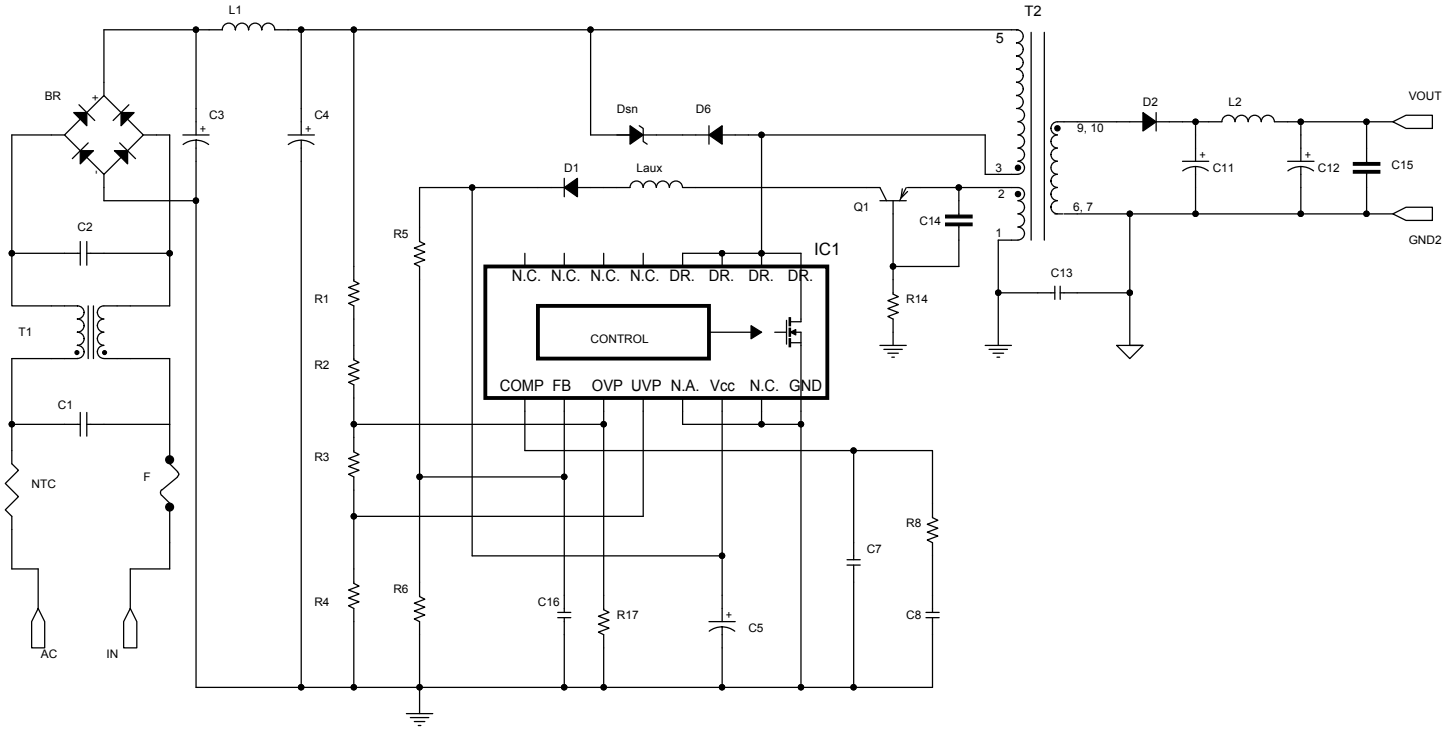
1.1 Specifications

Table 1. Electrical specs

Parameter	Symbol	Value
Input voltage range	V_{IN}	90 - 265 V_{AC}
Output voltage	V_{OUT}	15 V
Max. output current	I_{OUTmax}	1.2 A
Min. output current	I_{OUTmin}	0.01 A
Max. output power	P_{OUT}	18 W
Precision of output regulation	Δ_{VOUT_LF}	±5%
High frequency output voltage ripple	Δ_{VOUT_HF}	50 mV
Max. ambient operating temperature	T_{AMB}	60 °C
Switching frequency	F_{OSC}	60 kHz

1.2 Schematic diagrams

Figure 2. **STEVAL-VP318L2F circuit schematic**



1.3 Bill of materials

Table 2. **STEVAL-VP318L2F bill of materials**

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	1	BR	DF06M, DF-M, 600V, 1A	Diode bridge	Vishay	DF06M-E3/45
2	1	D1	1N4148, SOD-123, 100V, 0.3A	Small signal diode	DiodesZetex	1N4148W-7-F
3	1	D2	STPS20200CG-TR, D2PAK, 200V, 20A	Power Schottky diode	ST	STPS20200CG-TR
4	1	D3	STTH1L06A, DO-214AC (SMA), 600V, 1A	Ultrafast high voltage rectifier	ST	STTH1L06A
5	1	Dsn	1.5KE300A, D0-201 (through hole), 1500W	TRANSIL	ST	1.5KE300A
6	1	C1	Not connected, through hole, 13mmx7mm, p.10mm, Ø 0.6mm	X2 cap	Any	
7	1	C2	Not connected, through hole, 13mmx7mm, p.10mm, Ø 0.6mm	X2 cap	Any	
8	1	C3	22uF, through hole, d=12.5mm, p=5mm, h=20mm, 450Vcc, +/-20%	Electrolytic capacitor, BXF series	Rubycon	450BXF22M12.5X20
9	1	C4	22uF, through hole, d=12.5mm, p=5mm, h=20mm 450Vcc, +/-20%	Electrolytic capacitor, BXF series	Rubycon	450BXF22M12.5X20
10	1	C5	4.7uF, 1206, 50Vcc, +/-10%	Multi-layer ceramic capacitor	KEMET	C1206C475K5PACTU
11	1	C7	0.22nF, 0603, 50Vcc, +/-10%	Multi-layer ceramic capacitor	Wurth Elektronik	885012206079
12	1	C8	33nF, 0603, 50Vcc, +/-10%	Multi-layer ceramic capacitor	Wurth Elektronik	885012206092

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
13	1	C11	680uF, through hole, d=10mm, p=5mm, h=22mm, 25Vcc, +/-20%	Electrolytic capacitor, ZL series	Rubycon	25ZL680MEFC10X20
14	1	C12	100uF, through hole, d=6.3mm, p=2.5mm, h=11mm 35Vcc, +/-20%	Electrolytic capacitor	Wurth Elektronik	860020573008
15	1	C13	2.2nF through hole, d=9.5mm, p=10mm, h=13.5mm, 500Vac, +/-20%	Y1 capacitor	Vishay	VY1222M37Y5VQ63V0
16	1	C14	100pF, 0603, 50Vcc, +/-10%	Multi-layer ceramic capacitor	Wurth Elektronik	885012206077
17	1	C15	100nF, 0603, 25Vdc, +/-10%	Multi-layer ceramic capacitor	Wurth Elektronik	885012206071
18	1	C16	not connected, 0603	Multi-layer ceramic capacitor	Any	
19	1	L1	1mH, through hole, d=9.5mm, p=5mm, h=11.5mm, 0.5A, +/-10%	Power inductor, RFB series	Coilcraft	RFB0810-102L
20	1	L2	3.3uH, SMD (4mm x 4mm), 3.23A	Shielded power inductor	Wurth Elektronik	74404043033A
21	1	Laux	3.3uH, 0805, 0.03A, +/-10%	Small signal inductance	Murata	LQM21NN3R3K10L
22	1	T1	20mH, through hole, 15 x 7.5 x 17.5mm, 0.5A, +/-30%	Common mode choke	Wurth Elektronik	744821120
23	1	T2	750317579 rev03, EE25/10/6 through hole	Flyback transformer	Wurth Elektronik	750317579 rev03
24	1	NTC	10 ohm, through hole, 15 x 7 x 22mm, p=7.5mm, +/-20%	Thermistor	EPCOS	B57237S0100M000

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
25	1	F	2A/250V, through hole, d=8.5mm, p=5mm, h=8mm, 250Vac, 2A	Fuse	Wickmann	3821200041
26	1	R1	not connected, 0805	UVP-OVP resistor	Any	
27	1	R2	not connected, 0805	UVP-OVP resistor	Any	
28	1	R3	not connected, 0805	UVP-OVP resistor	Any	
29	1	R4	not connected, 0805	UVP-OVP resistor	Any	
30	1	R5	100kohm, 0603, 0.1W, +/-1%	Resistor	Panasonic	ERJ3EKF1003V
31	1	R6	12kohm, 0603, 0.1W, +/-1%	Resistor	Panasonic	ERJ3EKF1202V
32	1	R8	200kohm, 0603, 0.1W, +/-1%	Resistor	Yageo	AC0603FR-07200KL
33	1	R14	10kohm, 0603, 0.1W, +/- 5%	Resistor	Panasonic	ERJ3GEYJ103V
34	1	R17	0 ohm, 0603	OVP disable resistor	Any	
35	1	IC1	VIPer318LDTR, SO16N	High voltage power switch	ST	VIPER318LDTR
36	1	Q1	BC807,SOT-23	Small signal p-n-p BJT	ON Semiconductor	BC807-40LT1G
37	1	IN	l=11.36mm, w=10mm, d=8.1mm, p=5.08mm, 250Vac, 14A	Through hole input connector	Wurth Elektronik	691213510002
38	1	OUT	l=11.36mm, w=10mm, d=8.1mm, p=5.08mm, 250Vac, 14A	Through hole output connector	Wurth Elektronik	691213510002

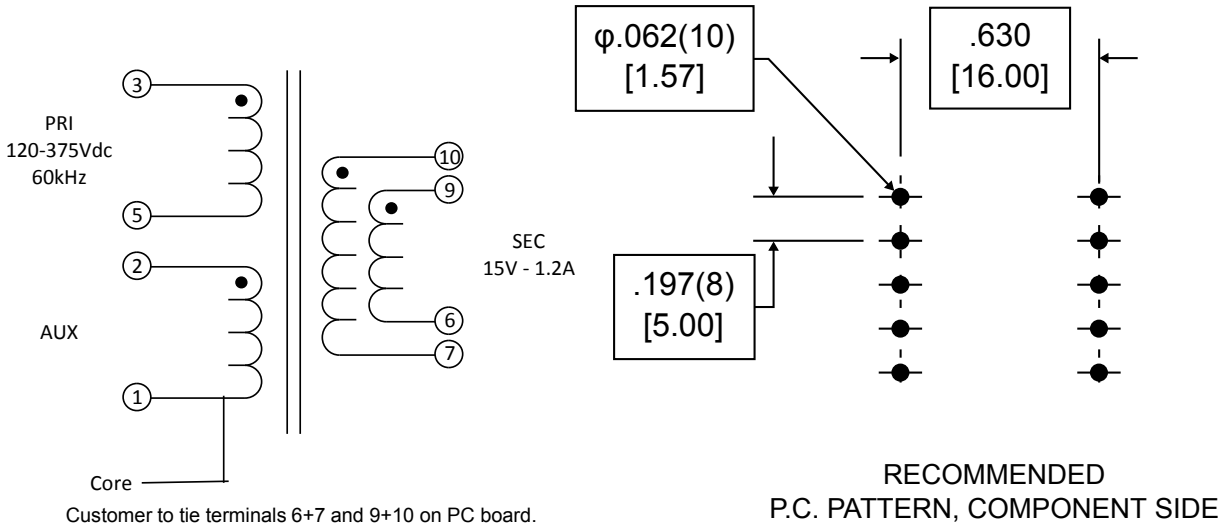
1.4 Transformer

Table 3. Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	Wurth Elektronik	-
Part number	750317579 rev03	-
Primary inductance (pins 3 - 5)	1.5 mH ±10%	10 kHz, 100 mV, Ls
Leakage inductance	90 µH typ., 120 µH max.	tie(1+2, 6+7+9+10),100 kHz, 100 mV, Ls
Primary to sec turn ratio	5:1, ± 1%	(3-5):(10-6), tie(6+7, 9+10)
Primary to aux turn ratio	6.82 ± 1%	(3-5):(2-1)
Reflected voltage	78 V	-
Saturation current	1.5 A max.	20% roll-off from initial
Operating current	0.8 A max.	-
DC-DC resistance 3-5	3.100 Ω ±10%	20°C
DC-DC resistance 2-1	0.645 Ω ±10%	20°C
DC-DC resistance 10-6	0.120 Ω ±10%	20°C, tie(6+7, 9+10)

Figure 3. Electrical and pin diagrams

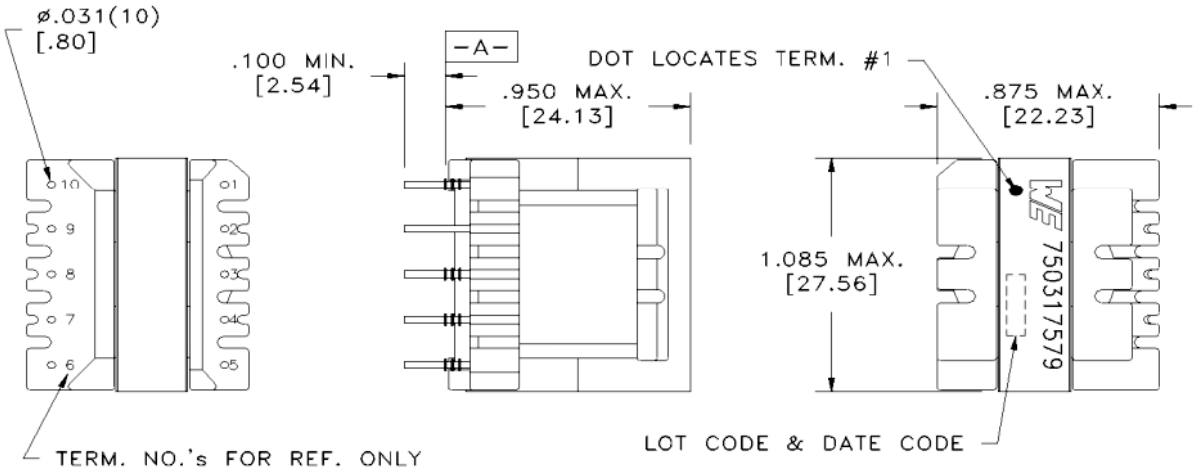
left: electrical diagram
right: pin distances (bottom view)



Customer to tie terminals 6+7 and 9+10 on PC board.

RECOMMENDED
P.C. PATTERN, COMPONENT SIDE

Figure 4. **Transformer dimensions (bottom, side and top view)**



2 Performance

2.1 Line and load regulation

The following figures respectively show line regulation in the entire output load range (0.01 A to 1.2 A) and load regulation in the entire input voltage range (90 V_{AC} to 265 V_{AC}).

Figure 5. STEVAL-VP318L2F line regulation

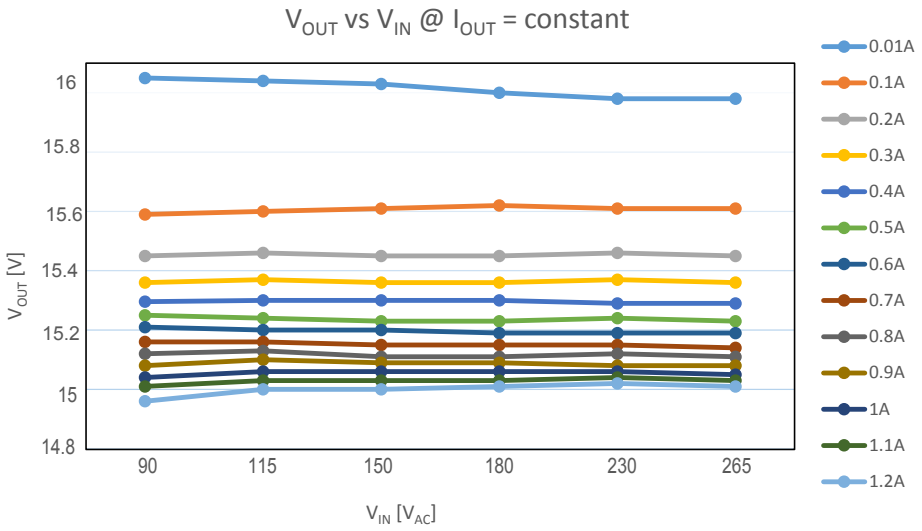
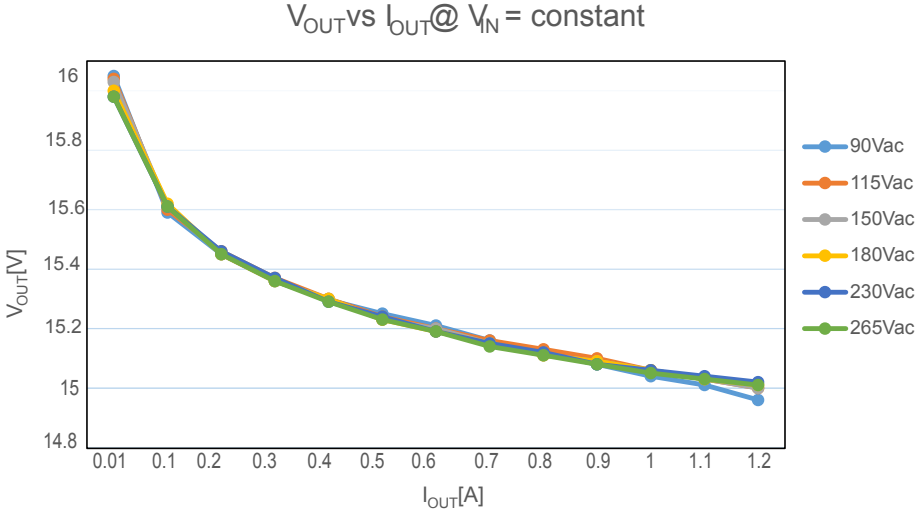


Figure 6. STEVAL-VP318L2F load regulation



2.2 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of the maximum load, at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

Table 4. **Active mode efficiency**

V_{IN} [V_{AC}]	Active mode efficiency [%]
115	83.5
230	84.8

2.3 Light load performance

V_{IN} [V_{AC}]	I_{out} [A]	Efficiency [%]
115	0.01 (minimum load)	83.7
230		78.1
115	0.12 (10% of max. load)	84.5
230		78.6

2.4 Typical waveforms

The following figures show typical waveforms in full load condition for the two nominal input voltages.

Figure 7. **Typical waveform at 115 V_{AC}, max. load**

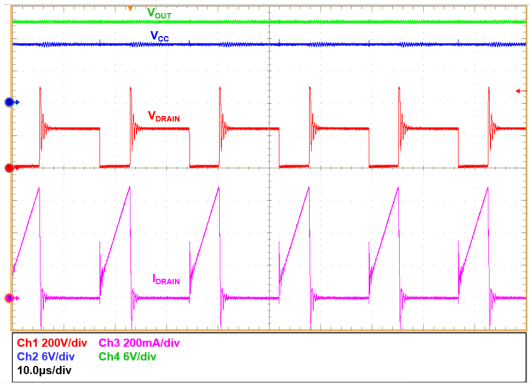
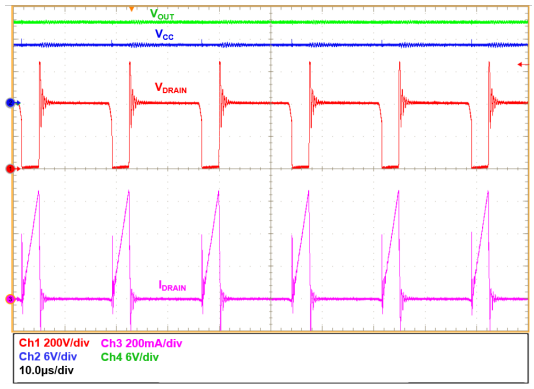


Figure 8. **Typical waveform at 230 V_{AC}, max. load**



The following figures show typical waveforms in full load condition for the minimum and maximum input voltages.

Figure 9. Typical waveform at 90 V_{AC}, max. load

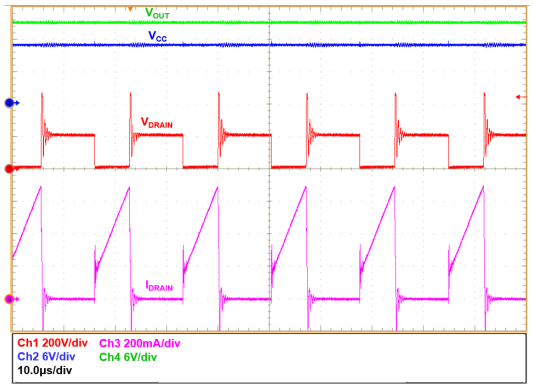
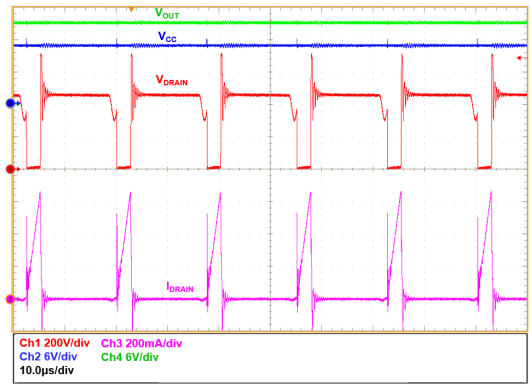


Figure 10. Typical waveform at 265 V_{AC}, max. load



3 Functional check

3.1 Soft start

As V_{DRAIN} exceeds $V_{HVSTART}$ at power-up, the internal HV current generator charges the V_{CC} capacitor C5 to V_{CCon}, the Power MOSFET starts switching, the current generator is turned off, and the IC is powered by the energy stored in C5.

An internal soft-start function progressively increases the cycle-by-cycle current limitation set point from zero up to I_{DLIM} in 8 steps. In this way, the DRAIN current is limited during output voltage increase, thus reducing the stress on the secondary diode. The soft-start time t_{SS} needed for the current limitation set-point to reach its final value is internally fixed at 8 ms. This function is activated on any converter start-up attempt and after a fault event. The soft start phase is shown in the following figures during the startup at full load at 90 V_{AC} and 265 V_{AC}, respectively.

Figure 11. Startup at 90 V_{AC}, max. load

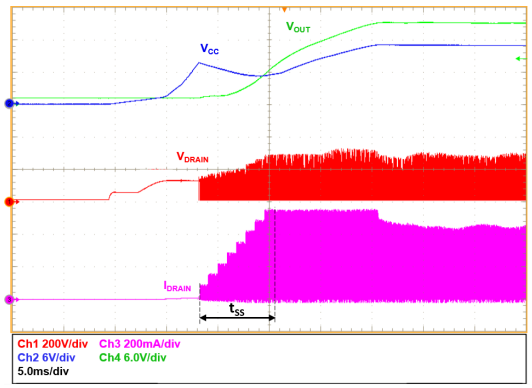
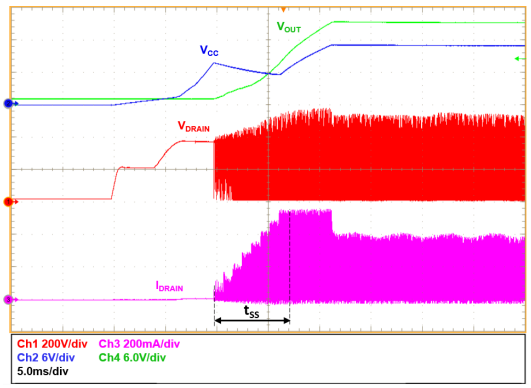


Figure 12. Startup at 265 V_{AC}, max. load



3.2 Overload protection

In an overload or short-circuit event, the drain current value reaches I_{DLIM}. Every cycle this condition is met, an internal OCP counter is incremented, and if the overload is maintained continuously for time t_{OVL} (50 ms typical, internally fixed), the counter reaches its end-of-count and the protection is tripped (Figure 13). The power section is turned off and the converter is disabled for a $t_{RESTART}$ time (1 s typical, Figure 14. Fault maintained - OVL steady state). After this time has elapsed, the IC resumes switching and, if the fault is still present, the protection continues triggering indefinitely. This lowers the repetition rate of converter restart attempts so that it works safely with extremely low power throughput and avoids IC overheating in case of repeated overload events.

Figure 13. Fault applied during steady state operation - OVL triggering

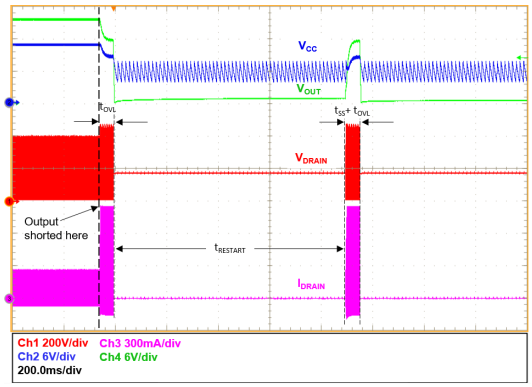
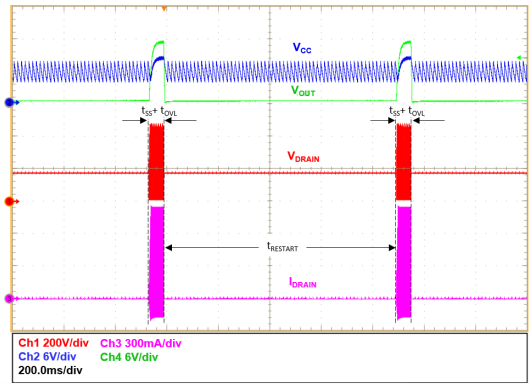


Figure 14. Fault maintained - OVL steady state



Furthermore, at startup after any protection tripping, the internal soft start-up function is invoked (Figure 15), in order to reduce the stress on the secondary diode.

After fault removal, the IC resumes working normally. If the fault is removed during t_{SS} or t_{OVL} (i.e., before protection tripping), the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short circuit is removed during $t_{RESTART}$, the IC has to wait for $t_{RESTART}$ to elapse before switching resumes (Figure 16).

Figure 15. Fault maintained -OVL steady state, t_{ss} and t_{OVL}

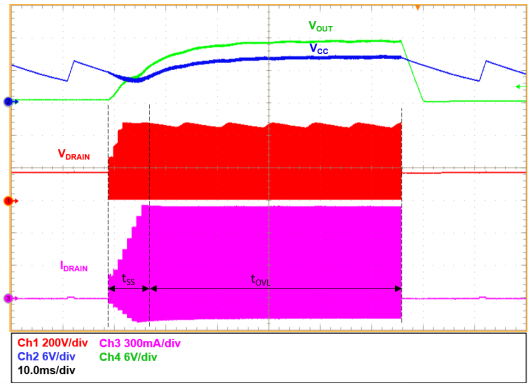
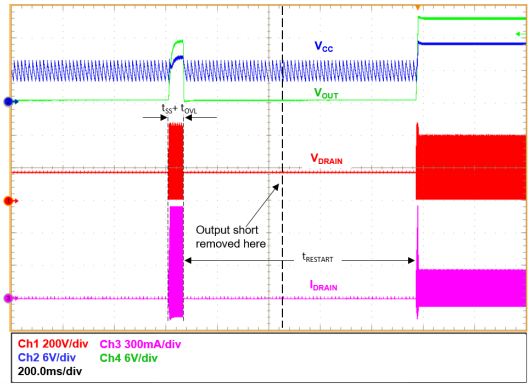


Figure 16. Fault removed and auto-restart from OLP



3.3 Pulse skip mode

Any time the drain peak current, I_{DRAIN} exceeds I_{DLIM} within the minimum on-time t_{ON_MIN}, one switching cycle is skipped. The check is made on a cycle-by-cycle basis and the cycles can be skipped until the F_{OSC_MIN} minimum switching frequency (15 kHz, typ.) is reached.

If the above condition persists and the internal OCP counter reaches its end-of-count, the IC is stopped for $t_{RESTART}$ (1 s, typ.) and activated again through a soft-start.

Any time I_{DRAIN} does not exceed I_{DLIM} within t_{ON_MIN}, one switching cycle is restored. The check is made on a cycle-by-cycle basis and the cycles can be restored until the nominal switching frequency F_{OSC} is reached.

This protection provides, when required, more time for inductor discharge than what allowed at nominal switching frequency, thus helping limiting the "flux runaway" effect, often occurring at converter startup and consisting in a net increase of the average inductor current when the primary MOSFET, charged during the minimum on-time through the input voltage, cannot discharge the same amount during the off-time, due to a very low output voltage. This current has to be limited as it could reach dangerously high values for the power components during the startup first cycles , until the output capacitor is not charged enough to ensure the inductor discharge rate needed for the volt-second balance.

We captured a startup sequence at 265 V_{AC} to test the protection. The figures below show the initial pulse skipping phase, with alternating switching cycles at 15 kHz, 30 kHz for a certain period, until the nominal 60 kHz F_{OSC} is restored.

Figure 17. Start-up at 265 V_{AC}, full load – pulse skipping

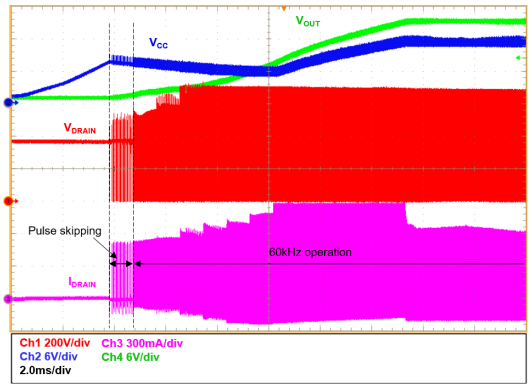
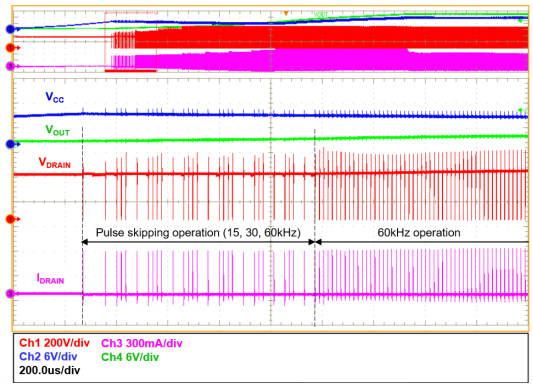


Figure 18. Start-up at 265 V_{AC}, full load – pulse skipping (zoom)



3.4 Input undervoltage/overvoltage

Input undervoltage and overvoltage protections are available on the respective UVP and OVP pins and can be enabled or disabled independently. By default, the protections are both disabled, but the voltage divider R1, R2, R3 and R4 is available to allow UVP and OVP implementation.

The input voltage divider high-side resistor selection should be a high value in order to limit the power consumption from the mains and should be divided in two to withstand high input voltage values. In our example, 3 MΩ values are selected for R1 and R2.

The medium-side and low-side resistors, R3 and R4, are selected through the following formulas:

$$R4 = \frac{V_{in\_UVP} + I_{UVP\_pull-up} \cdot RH - \sqrt{\left(V_{in\_UVP} + I_{UVP\_pull-up} \cdot RH\right)^2 - 4 \cdot V_{UVP\_th} \cdot I_{UVP\_pull-up} \cdot RH}}{2 \cdot I_{UVP\_pull-up}} \quad (3)$$

$$R3 = \left(V_{OVP\_th} - R4 \cdot I_{UVP\_pull-up}\right) \cdot \frac{RH}{V_{in\_OVP}} - R4 \quad (4)$$

where RH = R1 + R2; V_{UVP_th} and V_{OVP_th} are the UVP and OVP pin thresholds reported in the VIPER318LDTR datasheet (0.4 V and 4 V typical respectively); V_{in_UVP} and V_{in_OVP} are the required input UVP and OVP thresholds (i.e., the input voltage values corresponding to V_{UVP_th} on UVP pin, and V_{OVP_th} on OVP pin, respectively); $I_{UVP\_pull-up}$ is the internal pull-up current on the UVP pin.

As an example, if we select V_{IN_UVP} = 50 V_{DC} and V_{IN_OVP} = 380 V_{DC} in equations (3) and (4), then we obtain: R3 = 20 kΩ and R4 = 43 kΩ.

Input undervoltage protection behaves in the following way:

- when the input voltage drops below V_{IN_UVP}, the UVP pin voltage falls below V_{UVP_th} and an internal counter is activated;
- if V_{UVP} remains lower than V_{UVP_th} for more than t_{UVP_DEB} (30 ms typ.), the IC is stopped with no restart attempts, as shown in Figure 19, where V_{IN_UVP} measures about 51 V as expected;
- as long as V_{UVP} remains below V_{UVP_th}, most of the internal blocks are disabled and the internal consumption is reduced to ultra-low values, while V_{CC} is maintained between V_{CSon} and V_{CCon} by the periodical activation of the internal HV-current source, as shown in Figure 20.

Figure 19. V_{IN} from 60 to 50 V_{DC}: UVP triggering

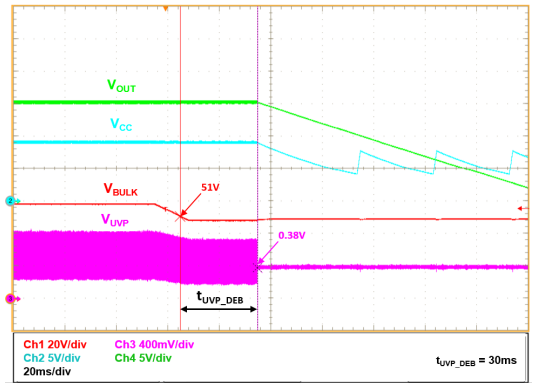
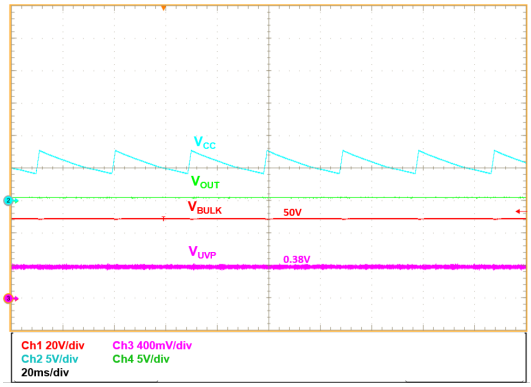


Figure 20. V_{IN} 50 V_{DC}: UVP steady-state



When V_{IN} exceeds V_{IN_UVP}, the UVP pin voltage exceeds V_{UVP_th}. If this condition is maintained for more than t_{UVP_REST} (30 ms, typ.), normal operation is restored (Figure 21).

Input overvoltage protection behaves in the following way:

- when the input voltage rises above V_{IN_OVP}, the OVP pin voltage exceeds V_{OVP_th} and an internal counter is activated;
- if V_{OVP} remains higher than V_{OVP_th} for more than t_{OVP_DEB} (250 µs typ.), the IC is stopped, as shown in Figure 22, where V_{IN_OVP} measures about 381 V as expected.

Figure 21. V_{IN} from 50 to 60 V_{DC}: resuming from UVP

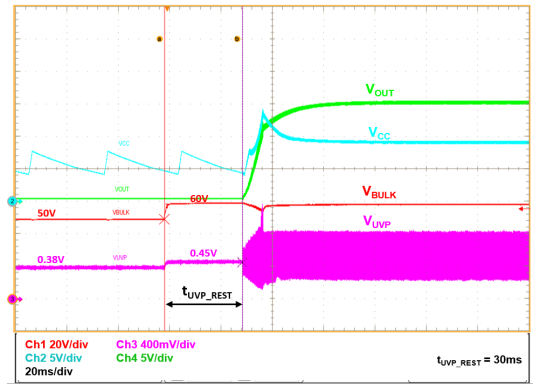
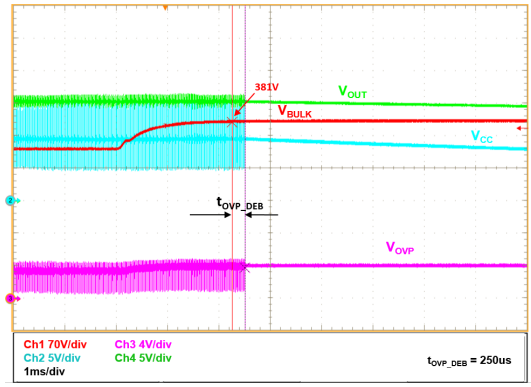


Figure 22. V_{IN} from 325 to 385 V_{DC}: OVP triggering



- OVP stops the device in auto-restart for t_{OVP_REST} (500 ms, typ.), the duration of restart attempts is t_{OVP_DEB}, as shown in Figure 23 and Figure 24.

Figure 23. V_{IN} 385 V_{DC}: OVP steady state

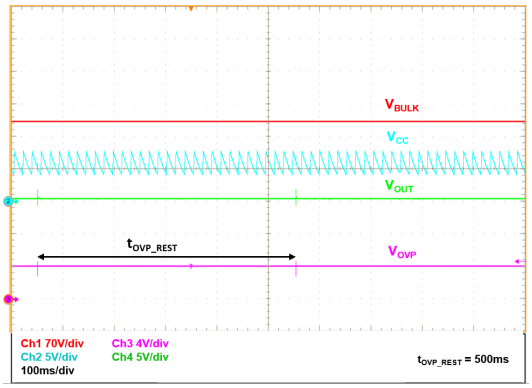
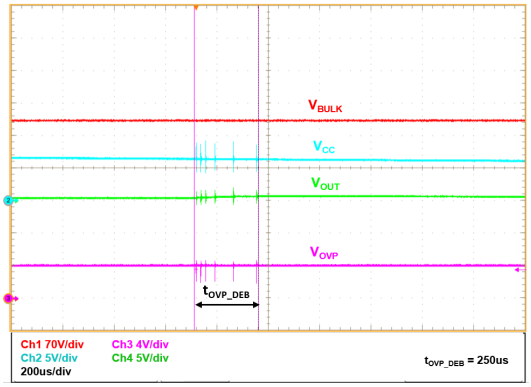


Figure 24. V_{IN} 385 V_{DC}: OVP steady state (zoom)



- When V_{IN} falls below V_{IN_OVP}, the OVP pin voltage goes below V_{OVP_th}.
- If this condition is maintained for more than t_{OVP_DEB}, the VIPER318LDTR restarts switching with soft-start phase and normal operation is restored (Figure 25. V_{IN} from 385 to 320 V_{DC}: resuming from OVP and Figure 26. V_{IN} from 385 to 320 V_{DC}: resuming from OVP (zoom)).

Figure 25. V_{IN} from 385 to 320 V_{DC}: resuming from OVP

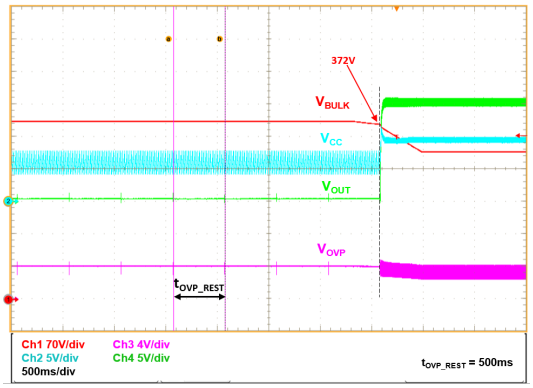
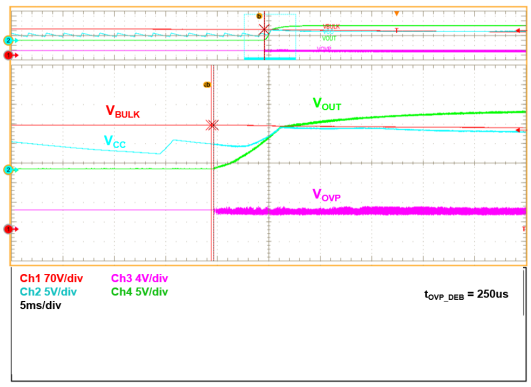


Figure 26. V_{IN} from 385 to 320 V_{DC}: resuming from OVP (zoom)



The power consumption of the input undervoltage/overvoltage network can be calculated as:

$$PIN_{UVP\_OVP}\left(V_{IN}\right) = \frac{V_{IN}^2}{(R1 + R2 + R3 + R4)} \quad (5)$$

This results in less than 18 mW consumption at 230 V_{AC} (~325 V_{DC})

If the undervoltage and overvoltage protections are not required, the OVP pin should be connected to GND pin (selecting R17 = 0 Ω), the UVP pin should be left floating, and the R1, R2, R3, R4 voltage divider should be disconnected.

3.5 Overtemperature protection

The Power MOSFET junction temperature is sensed during the MOSFET on- time through a diode integrated in the HV section of the chip. If a junction temperature higher than T_{SD} (160 °C, typ.) is measured, the PWM is disabled for $t_{RESTART}$.

In order to increase robustness against electromagnetic noise, the protection is triggered only if the condition is met for n_{th} = 3 consecutive switching cycles. After $t_{RESTART}$, the IC resumes switching with the soft start phase and if a junction temperature above T_{SD} is still measured for three consecutive switching cycles, the protection is triggered and PWM is disabled again for $t_{RESTART}$; otherwise, normal operation is restored.

During $t_{RESTART}$, V_{CC} is maintained between V_{CSon} and V_{CCon} by the HV current source periodical activation.

A 1 nF/1000 V capacitor has been soldered between DRAIN and GND in order to increase device temperature with increased switching losses. In this way, the protection is tripped at 230 V_{DC}/ 300 mA at a measured case temperature of 165 °C.

Figure 27. Thermal shutdown at T_{SD} = 165 °C (thermal image)

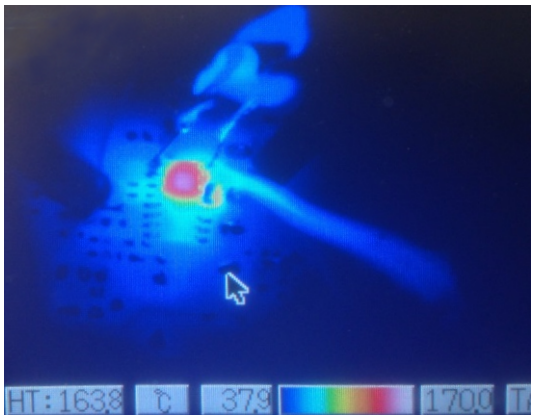
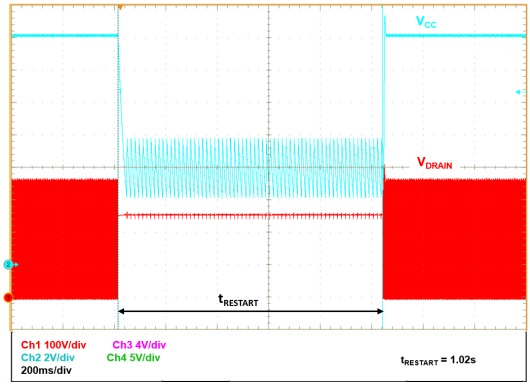


Figure 28. Thermal shutdown at T_{SD} = 165 °C



4 Thermal measurements

A thermal analysis of the board was performed using an IR camera for 90 V_{AC}, 115 V_{AC}, 230 V_{AC} and 265 V_{AC} mains input at full load condition. The results are shown in the following figures.

Figure 29. Thermal image at 90 V_{AC}, full load, T_{AMB} = 25 °C (1 of 2)

A: Dsn (1.5KE300)

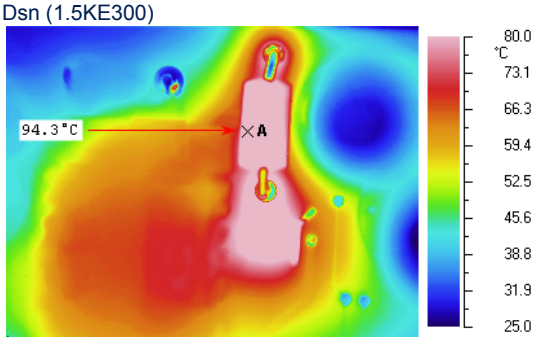


Figure 30. Thermal image at 115 V_{AC}, full load, T_{AMB} = 25 °C (2 of 2)

A: IC1 (VIPER318LDTR); B: D3 (STTH1L06)

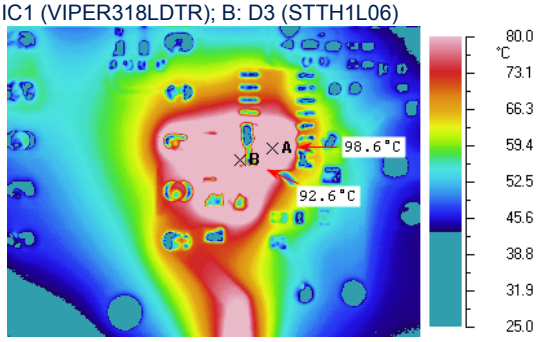


Figure 31. Thermal image at 115 V_{AC}, full load, T_{AMB} = 25 °C (1 of 2)

A: Dsn (1.5KE300)

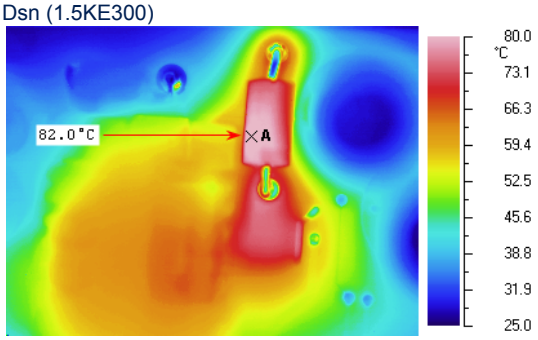


Figure 32. Thermal image at 115 V_{AC}, full load, T_{AMB} = 25 °C (2 of 2)

A: IC1 (VIPER318LDTR); B: D3 (STTH1L06)

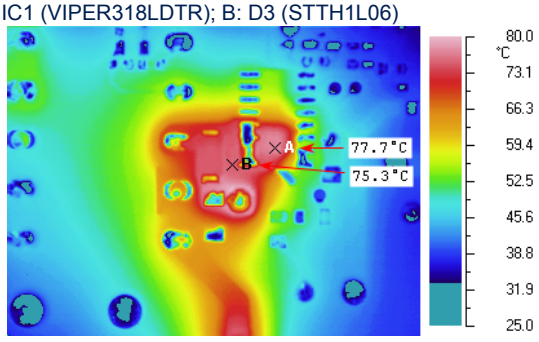


Figure 33. Thermal image at 230 V_{AC}, full load, T_{AMB} = 25 °C (1 of 2)

A: Dsn (1.5KE300)

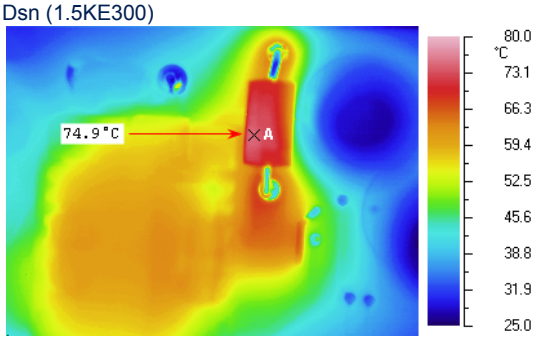


Figure 34. Thermal image at 230 V_{AC}, full load, T_{AMB} = 25 °C (2 of 2)

A: IC1 (VIPER318LDTR); B: D3 (STTH1L06)

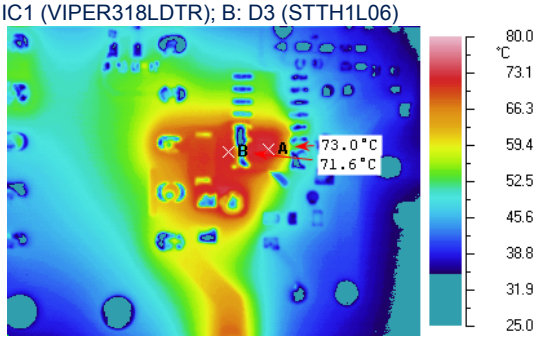


Figure 35. Thermal image at 265 V_{AC}, full load, T_{AMB} = 25 °C (1 of 2)

A: Dsn (1.5KE300)

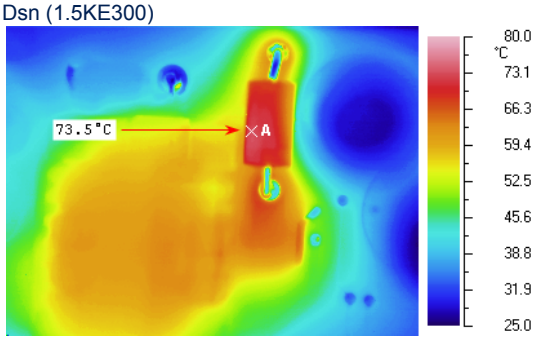
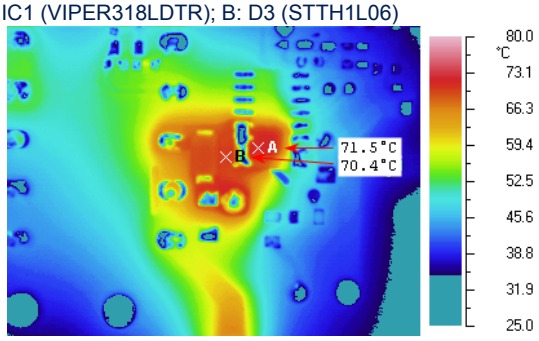


Figure 36. Thermal image at 265 V_{AC}, full load, T_{AMB} = 25 °C (2 of 2)

A: IC1 (VIPER318LDTR); B: D3 (STTH1L06)



5 EMI measurements

Pre-compliance tests regarding EN55022 (Class B) European normative with average detector were performed using an EMC analyzer and a LISN. The results are shown in the following figures.

Figure 37. Average measurements at 115 V_{AC}, full load, T_{AMB} = 25 °C

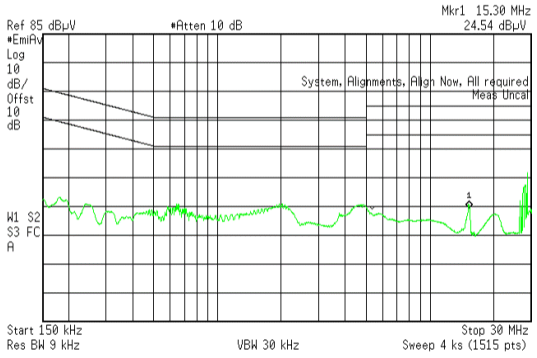
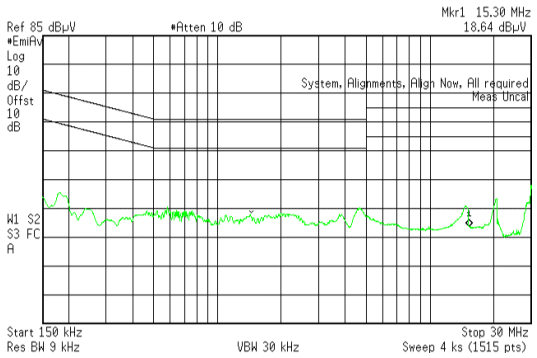


Figure 38. Average measurements at 230 V_{AC}, full load, T_{AMB} = 25 °C



6 Board layout

Figure 39. **Board layout - top layer**

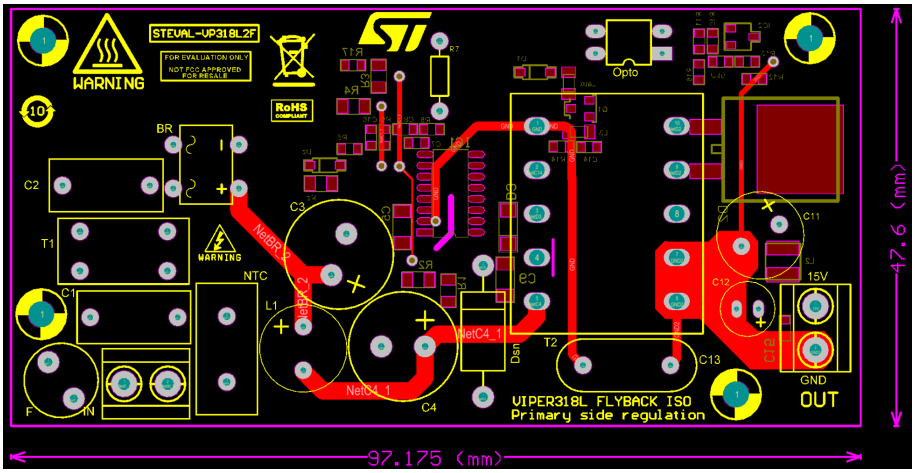
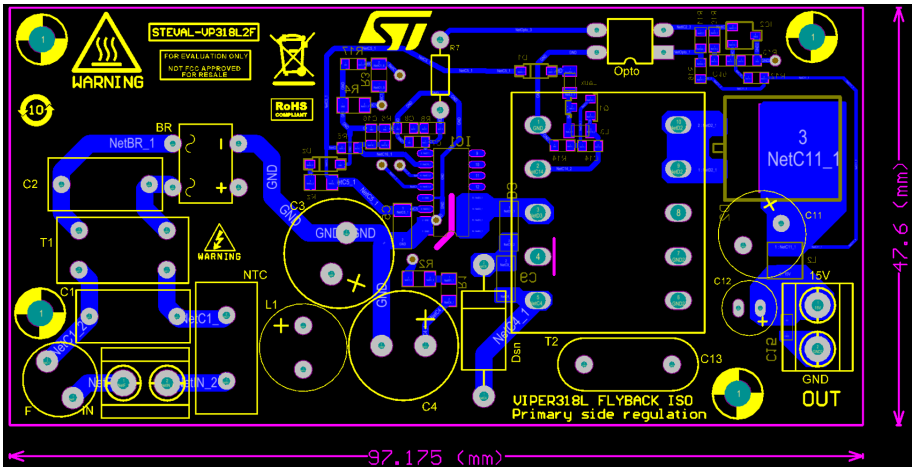


Figure 40. **Board layout - bottom layer**



7 Conclusions

We tested the STEVAL-VP318L2F and demonstrated how VIPER318LDTR can support SMPS converter designs in Flyback isolated PSR with very good line/load regulations, and reduce size, complexity and BoM requirements.

The 800 V, avalanche rugged Power MOSFET and the embedded protections render the VIPER318LDTR ideal for applications requiring robust, reliable and energy efficient performance.

Appendix A CCM flyback converter transfer function

The control-to-output transfer function of the flyback converter in CCM, $G_{vc}(s)$, is given by the approximation:

$$G_{vc}(s) \approx H_O \cdot \frac{\left(1+\frac{s}{\omega_{Z1}}\right)\cdot\left(1-\frac{s}{\omega_{Z2}}\right)}{1+\frac{s}{\omega_{P1}}} \quad (6)$$

Gain, poles and zero are defined below:

$$H_O = \frac{n \cdot R_O}{H_{COMP}} \cdot \frac{1-D}{1+D} \quad (7)$$

$$\omega_{Z1} = \frac{1}{R_C \cdot C_O} \quad (8)$$

$$\omega_{Z2} = -\frac{\left[n^2 \cdot (1-D)^2 \cdot R_O\right]}{D \cdot L} \quad (9)$$

$$\omega_{P1} = \frac{1+D}{R_O \cdot C_O} \quad (10)$$

Where:

- n = primary to secondary turns ratio
- $R_0 = V_{OUT}/I_{OUT}$ = nominal output resistance
- C_0 = capacitance of the output capacitor
- R_C = ESR of the output capacitor
- D = converter duty cycle
- L = primary inductance of the transformer
- $H_{COMP} = \Delta V_{COMP}/\Delta I_{DRAIN}$ (from device datasheet)

A.1 Compensator design

A.1.1 CCM flyback type-2 compensator design

To compensate the CCM flyback, we use a type-2 compensator featuring the integrator effect that provides high DC gain to minimize static error, as well as a pole-zero pair to boost the phase according to the phase margin target.

$$G_{c(s)} = G_{co} \cdot \frac{1+\frac{s}{\omega_{zc}}}{s\cdot\left(1+\frac{s}{\omega_{pc}}\right)} \quad (11)$$

The compensator is determined using a manual pole-zero placement technique in which the zero is placed in the vicinity of the power stage dominant pole to cancel its effect and the pole position is adjusted to achieve the required phase margin.

Follow the procedure below to design compensation with a type 2 compensator:

Step 1. Select the crossover frequency f_C and the phase margin Φ_m :

For CCM flyback, the crossover frequency must be selected as low as possible with respect to the RHP zero ω_{Z2} in order to limit the phase degradation that it introduces.

As a general rule, you should set f_C to below 20% of the RHP zero.

Step 2. Evaluate the gain and phase of the plant at crossover frequency:

$$G_{vc}(f_C) = \left|G_{vc}(2\cdot\pi\cdot f_C)\right| \quad (12)$$

$$\Phi_{vc}(f_C) = arg\left[G_{vc}(2\cdot\pi\cdot f_C)\right] \quad (13)$$

Step 3. The compensated open-loop gain must attain the unit gain at f_C , with the required phase margin, therefore the compensator must have following gain and phase at f_C :

$$G_c(f_C) = |G_c(2 \cdot \pi \cdot f_C)| = \frac{1}{G_{vc}(f_C)} \quad (14)$$

$$\Phi_c(f_C) = arg[G_c(2 \cdot \pi \cdot f_C)] = 90 - 180 + \Phi_m - \Phi_{vc}(f_C) \quad (15)$$

Step 4. Cancel the pole of the plant $f_{P1} = \omega_{P1}/(2 \cdot \pi)$ by placing the zero of the compensator, f_{zc} in the neighborhood ($\alpha = 1$ to 5):

$$f_{zc} = \frac{\omega_{zc}}{2 \cdot \pi} = \alpha \cdot f_{P1} \quad (16)$$

Step 5. Place the pole of the compensator to boost the phase and to obtain the desired phase margin:

$$f_{pc} = \frac{\omega_{pc}}{2 \cdot \pi} = \frac{f_C}{tan\left[tan^{-1}\left(\frac{f_C}{f_{zc}}\right) - \Phi_c(f_C)\right]} \quad (17)$$

Step 6. Calculate the gain G_{co} :

$$G_{co} = G_c(f_C) \cdot \frac{\omega_C \cdot \sqrt{1 + \left(\frac{f_C}{f_{pc}}\right)^2}}{\sqrt{1 + \left(\frac{f_C}{f_{zc}}\right)^2}} \quad (18)$$

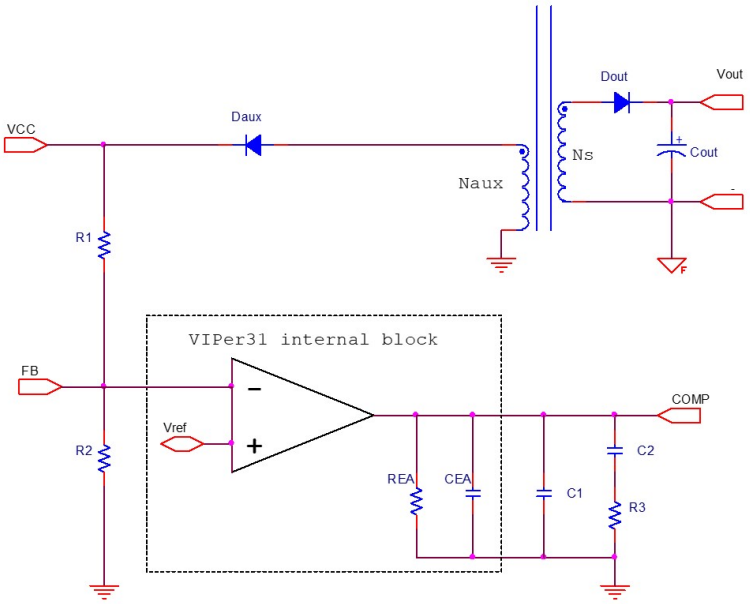
$G_C(s)$ is thus determined.

A.1.2 Compensator network implementation

The figure below shows the complete schematic arrangement for the type 2 error amplifier in primary side regulation.

The resistors R1 and R2 define the V_{CC} setpoint according to equation 1; V_{OUT} is regulated through the secondary-to-auxiliary turns ratio according to equation 2; C1, C2 and R3 implement the compensation network; CEA is the output capacitance of the VIPER318LDTR internal error amplifier, in the order of 10 pF; REA is the output resistance of the VIPER318LDTR internal error amplifier, which is in the order of several Mohms, much higher than R3 (~ tens of kohms), and will be ignored in the following calculation, with the effect of turning a pole at few or fractions of Hz into a pole in the origin.

Figure 41. **Primary feedback implementation and compensation network**



With reference to the implementation of figure above, the compensator gain, pole and zero indicated in equation 11 have the following expressions:

$$G_{co} = \frac{Naux}{Ns} \cdot \frac{Gm \cdot R2}{R1 + R2} \cdot \frac{1}{CEA + C1 + C2} \quad (19)$$

$$\omega_{zc} = 2 \cdot \pi \cdot f_{zc} = \frac{1}{R3 \cdot C2} \quad (20)$$

$$\omega_{pc} = 2 \cdot \pi \cdot f_{pc} = \frac{CEA + C1 + C2}{(CEA + C1) \cdot R3 \cdot C2} \quad (21)$$

where Gm is the transconductance of the error amplifier (its value is reported in the VIPER318LDTR datasheet).

A.1.3 Compensator network calculation

The target value of G_{co} is defined by equation 18, so the sum C1 + C2 can be calculated from equation 19:

$$C1 + C2 = \frac{Naux}{Ns} \cdot \frac{Gm \cdot R2}{R1 + R2} \cdot \frac{1}{G_{co}} - CEA \quad (22)$$

The target value of f_{zc} is defined by equation 16, so the product R3·C2 can be calculated from equation 20:

$$R3 \cdot C2 = \frac{1}{2 \cdot \pi \cdot f_{zc}} \quad (23)$$

The target value of f_{pc} is defined by equation 17, so C1 can be calculated from equations 21, 22 and 23:

$$C1 = \frac{Naux}{Ns} \cdot \frac{Gm \cdot R2}{R1 + R2} \cdot \frac{1}{G_{co}} \cdot \frac{f_{zc}}{f_{pc}} - CEA \quad (24)$$

C2 can be immediately calculated from equation 22 and R3 from equation 23.
In case of negative values, a lower crossover frequency should be selected and the procedure repeated.
The table below shows a summary of formulas and the results from calculation in the hypothesis f_C = 1 kHz and $\Phi_m = 76^0$. Last column lists the commercial values selected for the STEVAL-VP318L2F.

Table 5. Summary of compensator component calculations and results

Part	Ref. equation	Theoretical value	Selected value
R1	Arbitrarily selected	Hundreds kohm	100 kohm
R2	$\sim \frac{R1}{\frac{\frac{Naux}{Ns} \cdot V_{OUT}}{1.2V} - 1}$	12.2 kΩ	12 kohm
C1	$\frac{Naux}{Ns} \cdot \frac{Gm \cdot R2}{R1 + R2} \cdot \frac{1}{G_{co}} \cdot \frac{f_{zc}}{f_{pc}} - CEA$	275 pF	220 pF
C2	$\frac{Naux}{Ns} \cdot \frac{Gm \cdot R2}{R1 + R2} \cdot \frac{1}{G_{co}} - (CEA + C1)$	36.5 nF	33 nF
R3	$\frac{1}{2 \cdot \pi \cdot f_{zc} \cdot C2}$	201.4 kohm	200 kohm

The actual crossover frequency f_C and phase margin Φ_m are:

$$f_C \sim 1.1kHz$$

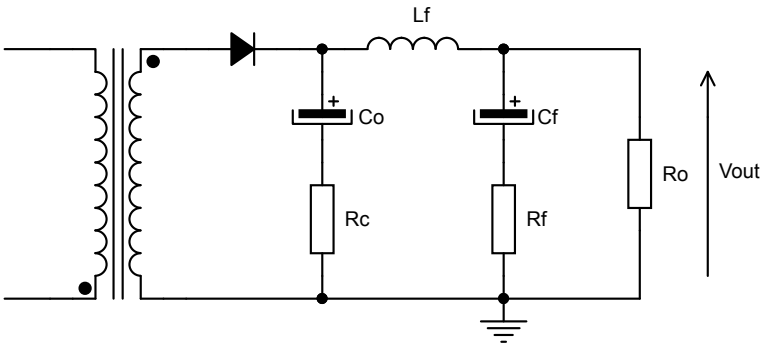
$$\theta_m \sim 76.8^0$$

Appendix B Effect of output LC post filter stage in flyback converters

Large capacitors are usually used in flyback converters to build the output filter, and it is important to factor in the RMS ripple rating and the parasitic resistance ESR when determining the size of the capacitor to satisfy the output ripple specification.

When the requirement of the ripple is very tight, a simple low cost LC filter can be used to attenuate the ripple to the desired level instead of using a large number of capacitors that increase the cost.

Figure 42. Output LC post filter for ripple reduction



Although this solution is very simple and cost effective, it changes the behavior of the plant and extra care must be placed to deal with the compensation design.

Assuming that C_O is much larger than C_f , the total transfer function of the plant in presence of the LC filter can be expressed as:

$$G'_{vc}(s) = G_{vc}(s) \cdot \frac{1 + \frac{s}{\omega_f}}{1 + \frac{s}{\omega_f \cdot Q_f} + \left(\frac{s}{\omega_f}\right)^2} \quad (25)$$

Where:

$$\omega_f = \frac{1}{\sqrt{L_f \cdot C_f}} \quad (26)$$

$$Q_f = \frac{1}{\frac{1}{R_O} \cdot \sqrt{\frac{L_f}{C_f}} + (R_f + R_c) \cdot \sqrt{\frac{C_f}{L_f}}} \quad (27)$$

Where $G_{vc}(s)$ is the transfer function of the plant without the filter.

The presence of the LC output post filter introduces a further zero and a pair of poles in the transfer function. This causes a peak at frequency $\omega_f/(2\pi)$ to appear in the amplitude diagram and a sudden 180° reduction of the phase to occur at the same frequency. Therefore, when you use an LC post filter, it is necessary to design its resonance frequency well above the crossover frequency to keep the resonance peak outside the converter band and to avoid eroding the phase margin or going as far as making the system unstable.

In our board, the LC filter in designed to have the pole pair at frequency $f_f = 8.76kHz$, with a quality factor equal to $Q_f = 0.074$, ensuring negligible phase margin erosion at the crossover frequency.

The following figures show steady-state output voltage ripple at full load and the system response to a step output load change from 0.01 A (minimum load) to 1.2 A (maximum load).

Figure 43. V_{OUT} AC ripple at 230 V_{AC}, full load

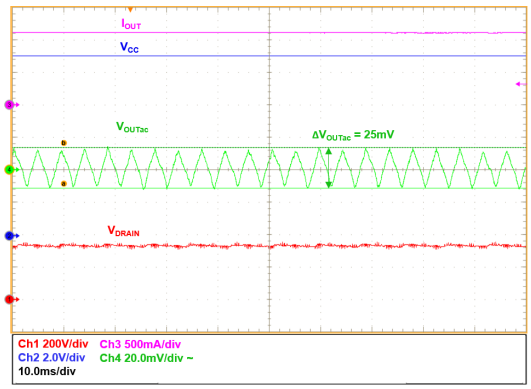
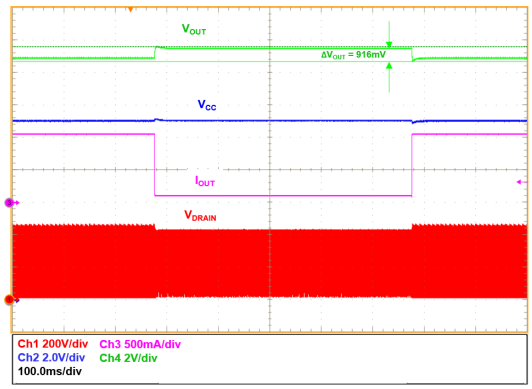


Figure 44. Step load from 0.01 A to 1.2 A at 230 V_{AC}, full load

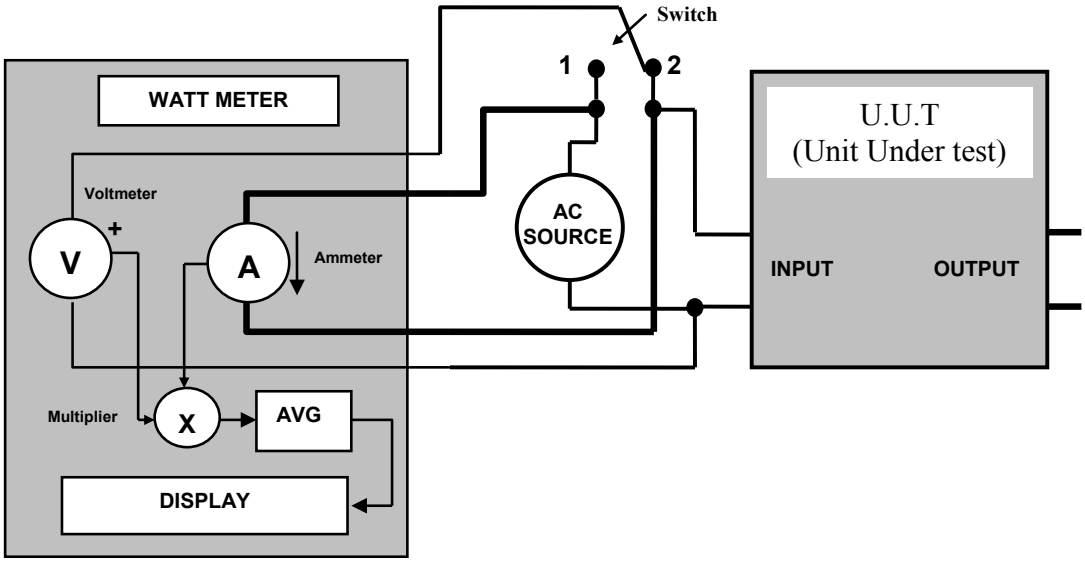


Appendix C Test equipment and measurement of efficiency and light load performance

The converter input power is measured with a wattmeter, taking simultaneous readings of the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument, so it samples the current and voltage and converts them into digital forms. The digital samples are then multiplied to give the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher, depending on the instrument used). The reading gives the average measured power over a short time interval short period of time (1 s typ.).

The following figure shows the wattmeter connected to the UUT (unit under test) and the AC source, as well as the wattmeter internal block diagram.

Figure 45. Connections of the UUT to the wattmeter for power measurements



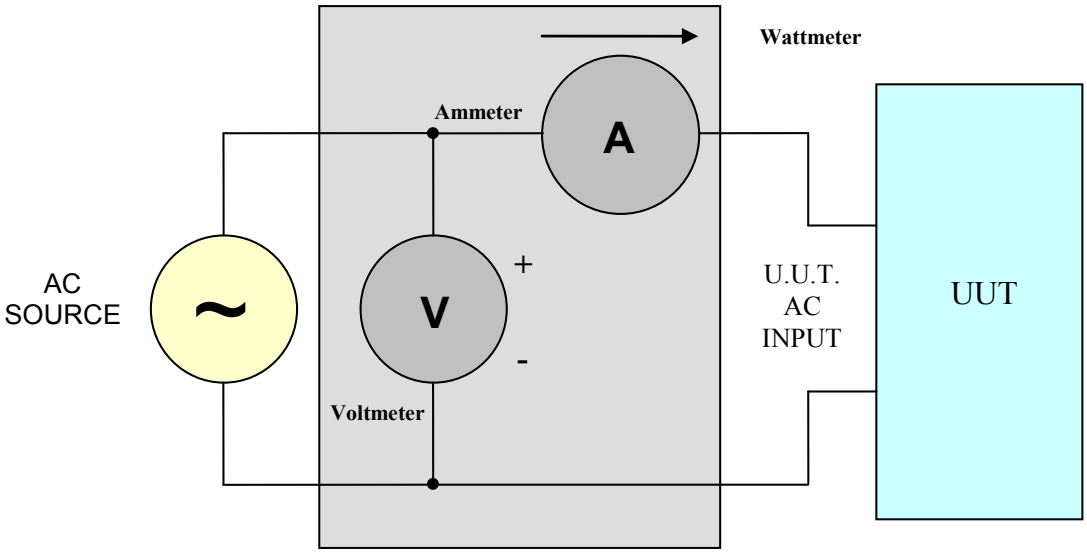
An electronic load is connected to the output of the power converter (UUT), allowing the setting and measurement of the load current of the converter, while the output voltage is measured by a voltmeter. The output power is the product of the load current and output voltage.

The ratio between the output power and the input power measured by the wattmeter is the efficiency of the converter. It is measured under different input and output conditions acting on the AC source and on the electronic load.

With reference to Figure 45. Connections of the UUT to the wattmeter for power measurements, the UUT input current causes a voltage drop across the ammeter internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

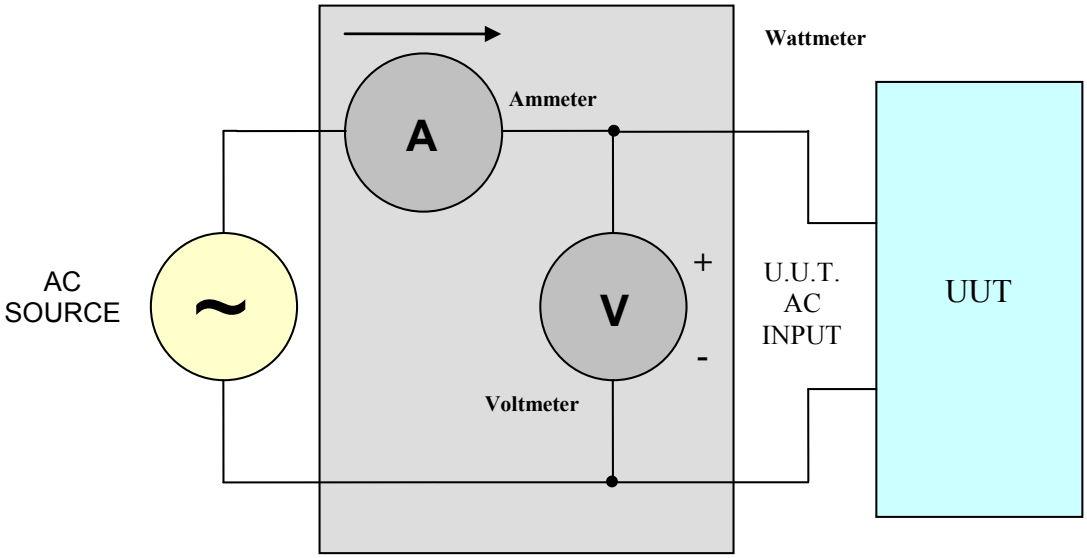
If the switch in Figure 45. Connections of the UUT to the wattmeter for power measurements is in position 1 (see the simplified scheme in Figure 46. Switch in position 1 - setting for standby measurements) this voltage drop causes a measured input voltage higher than the input voltage at the UUT input that obviously affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example, when we are measuring the input power of a UUT in the light-load condition).

Figure 46. **Switch in position 1 - setting for standby measurements**



For high UUT input currents, the voltage drop can be relevant (compared to the UUT real input voltage), so in this case the switch in Figure 45. Connections of the UUT to the wattmeter for power measurements can be set to position 2 (see simplified scheme in Figure 47. Switch in position 2 - setting for efficiency measurements) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 47. **Switch in position 2 - setting for efficiency measurements**



The voltage across the voltmeter causes a leakage current inside the voltmeter itself (that is not ideal). If the switch in Figure 45. Connections of the UUT to the wattmeter for power measurements is in position 2 (see simplified scheme in Figure 47. Switch in position 2 - setting for efficiency measurements), the voltmeter leakage current is measured by the ammeter together with the UUT input current, causing a measurement error. The error is negligible if the UUT input current is much higher than the voltmeter leakage. If the UUT input current is not much higher than the voltmeter leakage current, it is probably better to set the switch in Figure 45. Connections of the UUT to the wattmeter for power measurements to position 1.

If you are not sure which measurement scheme is more suitable, you can try both and record the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT shall be operated at 100% of nameplate output current output for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the ac input power shall be monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5-minute period.

If ac input power is not stable over a 5-minute period, the average power or accumulated energy shall be measured over time for both ac input and dc output.

Some wattmeter models allow integrating the measured input power over a time interval and then measuring the energy absorbed by the UUT during that time, from which the average input power is calculated.

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
30-Jun-2021	1	Initial release.

Contents

List of figures

List of tables