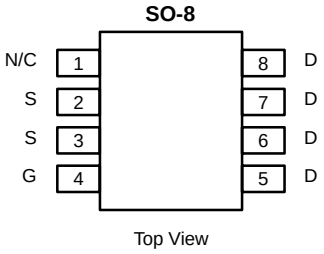
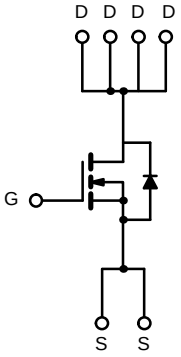
N-Channel Enhancement-Mode MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(ON)}$ (Ω)	I_D (A)
30	0.030 @ V_{GS} = 10 V	±7.0
	0.040 @ V_{GS} = 5 V	±6.0
	0.050 @ V_{GS} = 4.5 V	±5.4

Recommended upgrade: Si4410DY or Si4936DY
Lower profile/smaller size—see Si6434DQ





N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[A]	T_A = 25°C	I_D	±7.0	A
	T_A = 70°C		±5.8	
Pulsed Drain Current		I_{DM}	±30	
Continuous Source Current (Diode Conduction)[A]		I_S	2.8	
Maximum Power Dissipation[A]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Maximum Junction-to-Ambient[A]	R_{thJA}	50	°C/W

Notes
A. Surface Mounted on FR4 Board, t ≤ 10 sec.

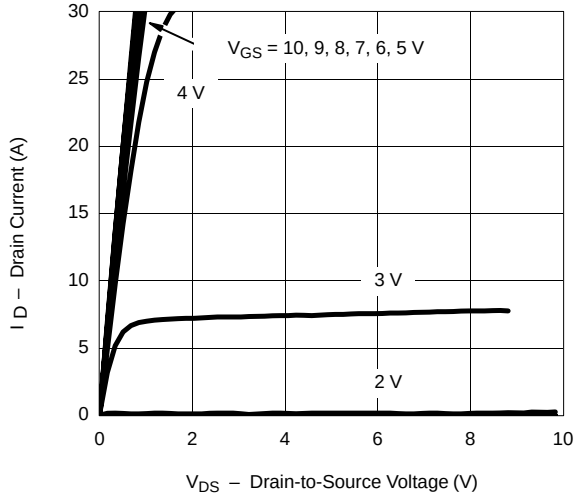
Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70122.
For SPICE model information via the Worldwide Web: http://www.siliconix.com/www/product/spice.htm

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
PARAMETER	**SYMBOL**	**TEST CONDITION**	**MIN**	**TYP[A]**	**MAX**	**UNIT**
STATIC						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.0			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			2	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[B]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	30			A
Drain-Source On-State Resistance[B]	$r_{DS(on)}$	V_{GS} = 10 V, I_D =7.0 A		0.024	0.030	Ω
		V_{GS} = 5 V, I_D = 4.0 A		0.030	0.040	
		V_{GS} = 4.5 V, I_D = 3.5 A		0.032	0.050	
Forward Transconductance[B]	g_{fs}	V_{DS} = 15 V, I_D = 7.0 A		15		S
Diode Forward Voltage[B]	V_{SD}	I_S = 2 A, V_{GS} = 0 V		0.72	1.1	V
DYNAMIC[A]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 2 A		24	50	nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			4.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 25 V, R_L = 25 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		14	30	ns
Rise Time	t_r			10	60	
Turn-Off Delay Time	$t_{d(off)}$			46	150	
Fall Time	t_f			17	140	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2 A, di/dt = 100 A/μs		60		

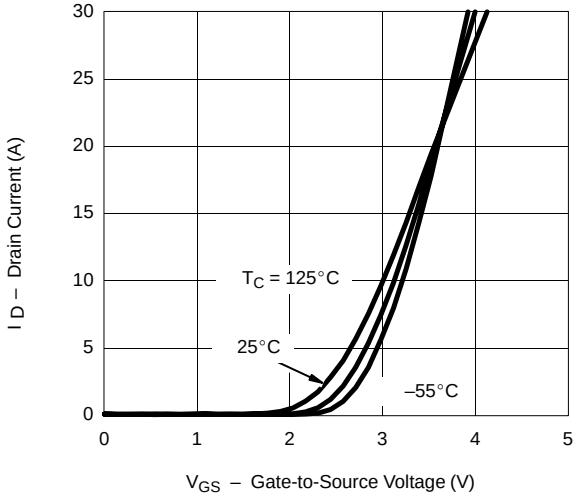
Notes
A. Guaranteed by design, not subject to production testing.
B. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

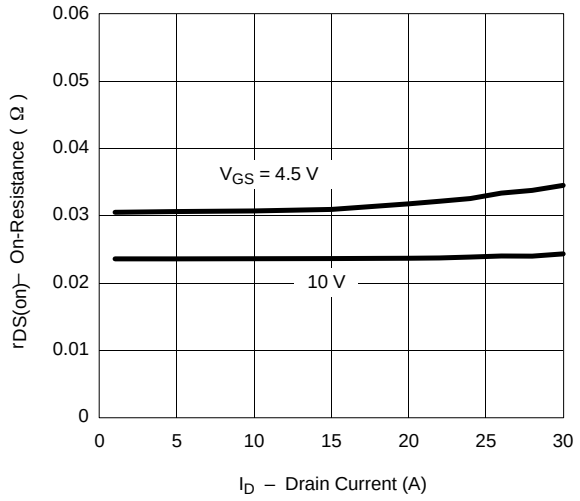
Output Characteristics



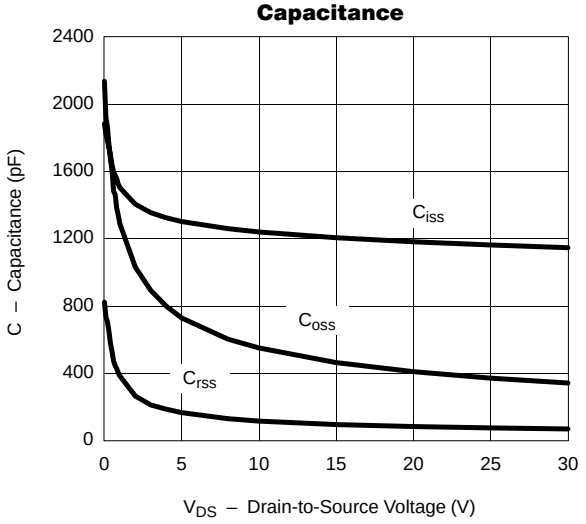
Transfer Characteristics



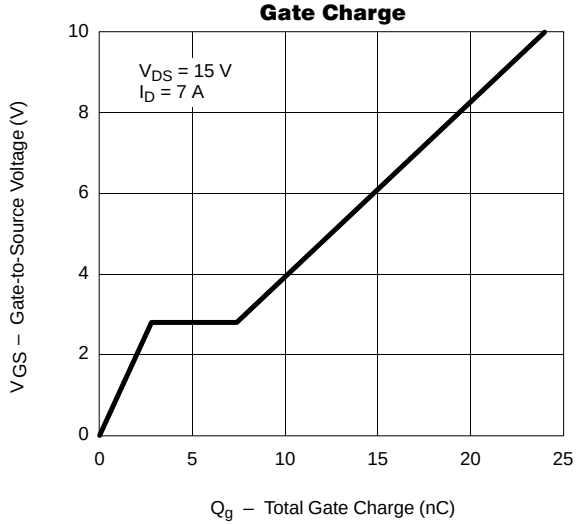
On-Resistance vs. Drain Current



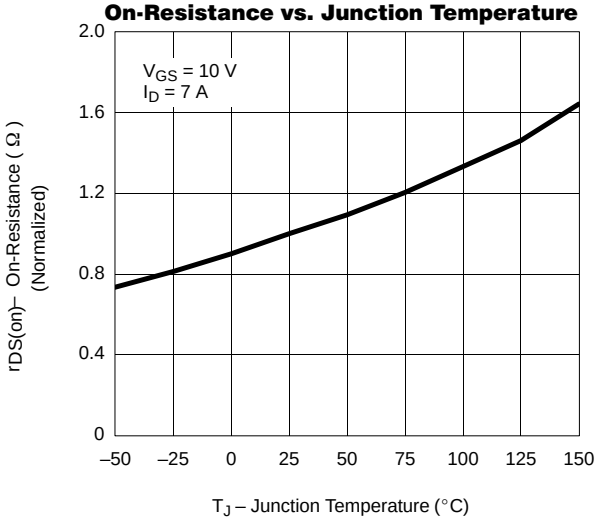
Capacitance



Gate Charge

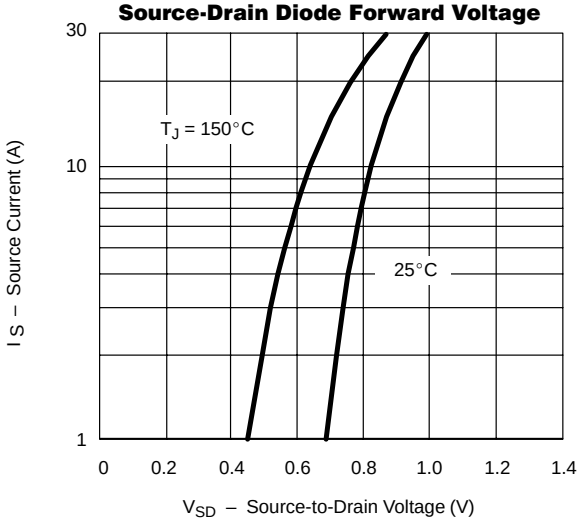


On-Resistance vs. Junction Temperature

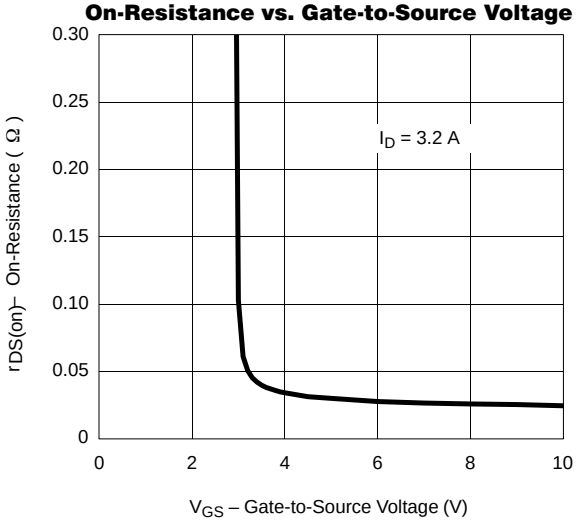


TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

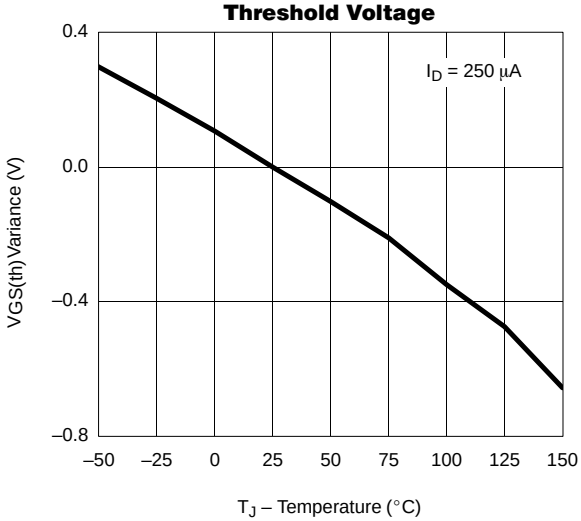
Source-Drain Diode Forward Voltage



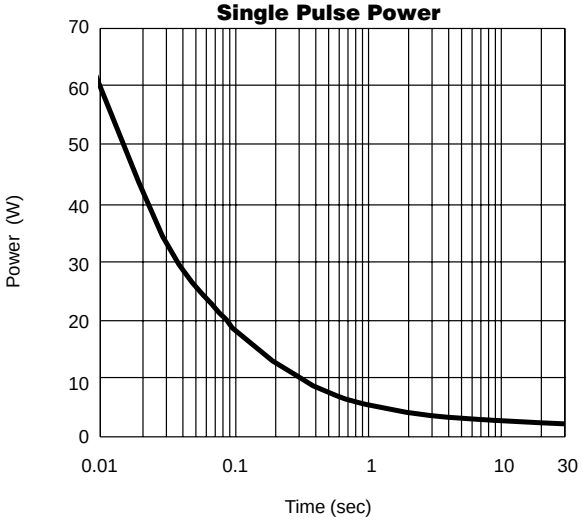
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient