

MOSFET - N-Channel Shielded Gate PowerTrench®

150 V, 7.3 mΩ, 101 A

NTB7D3N15MC

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)} = 7.3 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 62 \text{ A}$
- 50% Lower Q_{rr} than other MOSFET Suppliers
- Lowers Switching Noise/EMI
- 100% UIL Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	150	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Note 2)	I_D	101	A	
Power Dissipation $R_{\theta JC}$ (Note 2)				P_D
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	I_D	15.2	A	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)				P_D
Pulsed Drain Current	$T_C = 25^\circ\text{C}$, $t_p = 100 \mu\text{s}$	I_{DM}	488	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 20 \text{ A}_{pk}$, $L = 3 \text{ mH}$)	E_{AS}	600	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

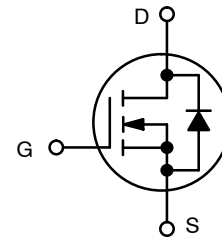
1. Surface-mounted on FR4 board using a 1 in², 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



ON Semiconductor®

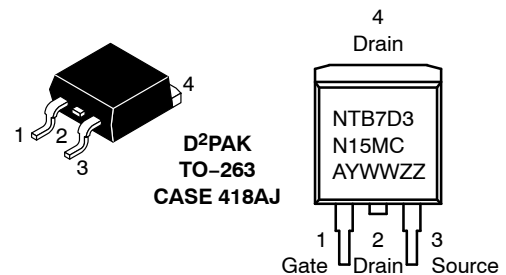
www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
150 V	7.3 mΩ @ 10 V	101 A



N-CHANNEL MOSFET

MARKING DIAGRAM



NTB7D3N15MC = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTB7D3N15MC	D ² PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.9	°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	40	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		71		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$			1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 342\ \mu\text{A}$	2.5		4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 342\ \mu\text{A}$, ref to 25°C		-7.3		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 62\text{ A}$		6.0	7.3	m Ω
		$V_{GS} = 8\text{ V}, I_D = 31\text{ A}$		6.5	8.4	
Forward Transconductance	g_{FS}	$V_{DS} = 10\text{ V}, I_D = 62\text{ A}$		119		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		4250		pF
Output Capacitance	C_{OSS}			1250		
Reverse Transfer Capacitance	C_{RSS}			15		
Gate-Resistance	R_G			0.8	1.6	Ω
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}; I_D = 62\text{ A}$		53		nC
Threshold Gate Charge	$Q_{G(TH)}$			14		
Gate-to-Source Charge	Q_{GS}			23		
Gate-to-Drain Charge	Q_{GD}			8.5		
Plateau Voltage	V_{GP}			5.8		
Output Charge	Q_{OSS}	$V_{DD} = 75\text{ V}, V_{GS} = 0\text{ V}$		133		nC

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 75\text{ V}, I_D = 62\text{ A}, R_G = 4.7\ \Omega$		27		ns
Rise Time	t_r			8.5		
Turn-Off Delay Time	$t_{d(OFF)}$			33		
Fall Time	t_f			5.8		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 62\text{ A}$	$T_J = 25^\circ\text{C}$		0.93	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}$ $di_S/dt = 300\text{ A}/\mu\text{s}, I_S = 62\text{ A}$			55		ns
Reverse Recovery Charge	Q_{RR}				247		nC
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}$ $di_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 62\text{ A}$			50		ns
Reverse Recovery Charge	Q_{RR}				720		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

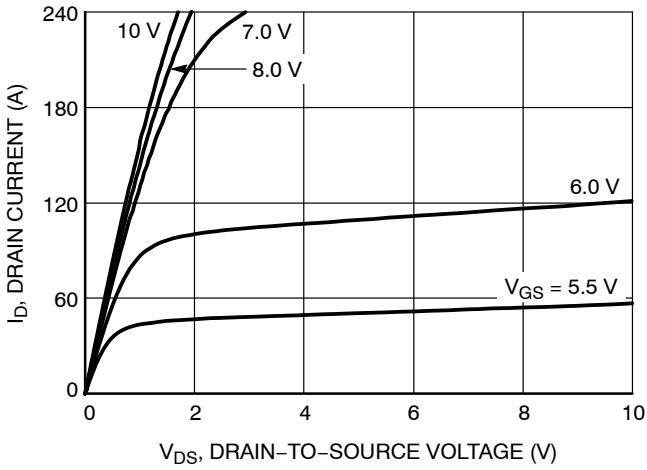


Figure 1. On-Region Characteristics

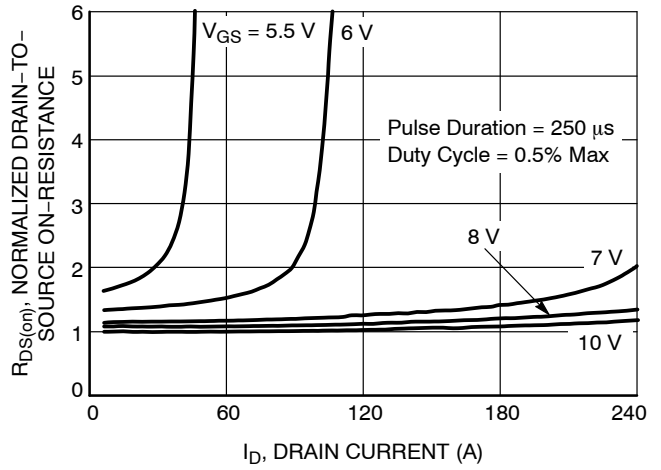


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

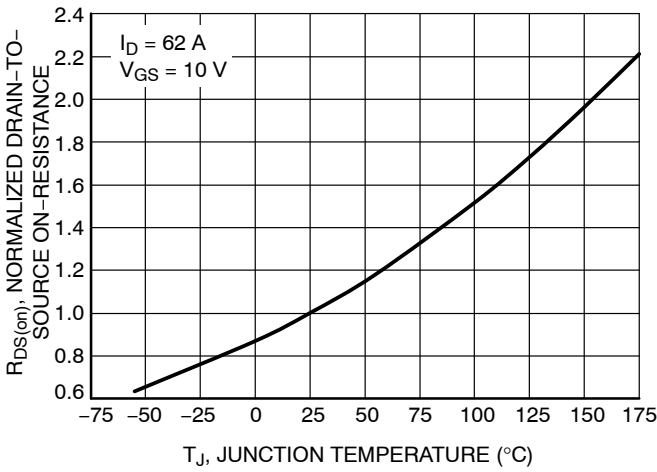


Figure 3. Normalized On-Resistance vs. Junction Temperature

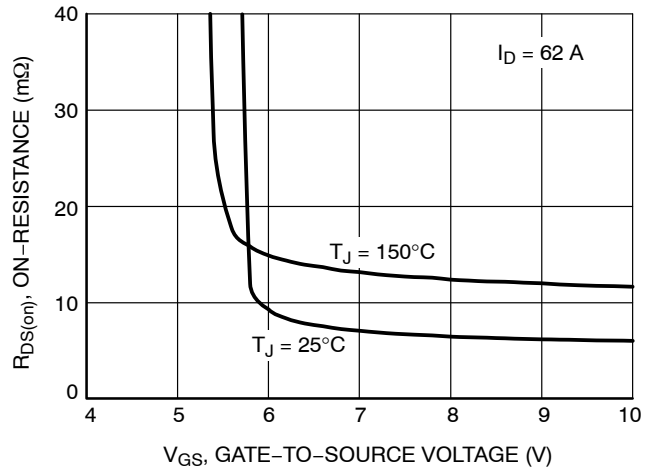


Figure 4. On-Resistance vs. Gate-to-Source Voltage

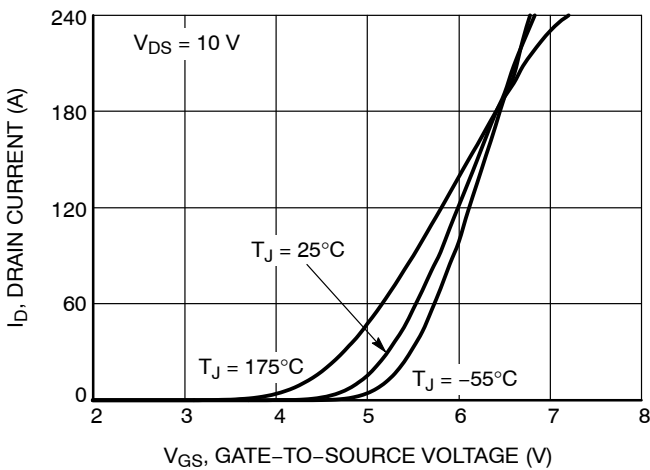


Figure 5. Transfer Characteristics

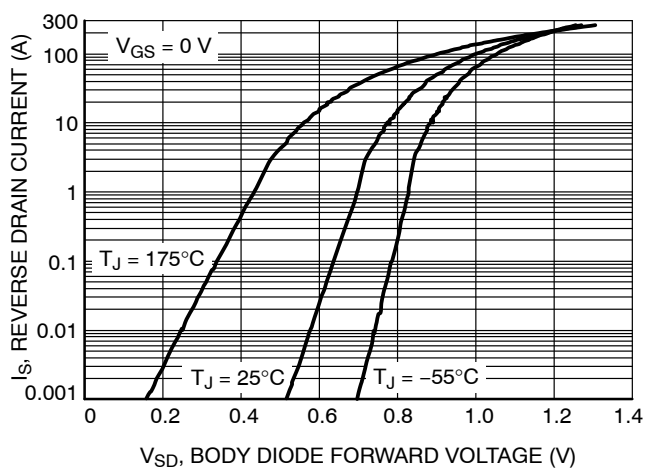


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS

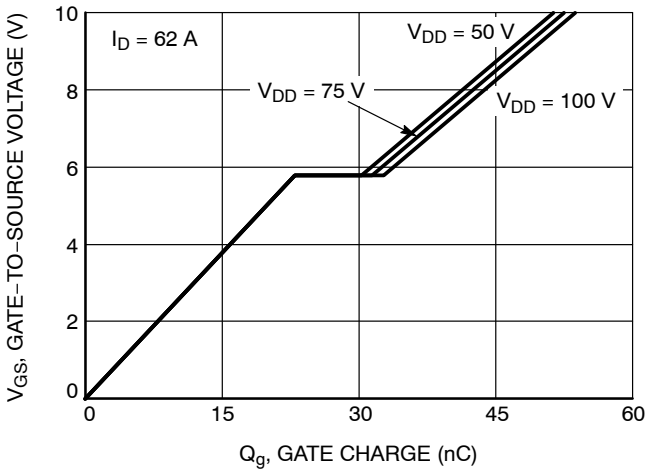


Figure 7. Gate Charge Characteristics

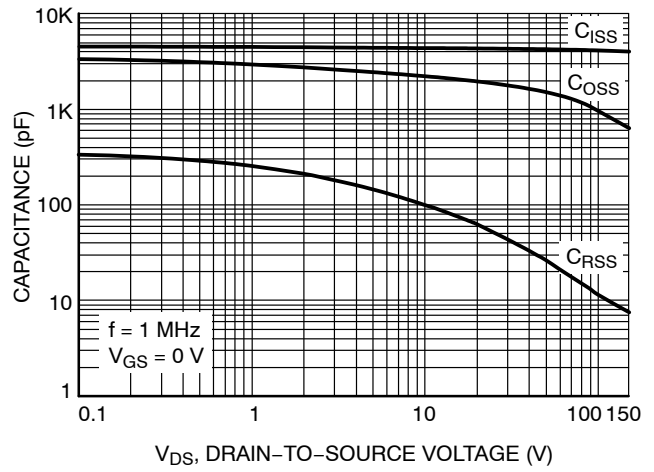


Figure 8. Capacitance vs. Drain-to-Source Voltage

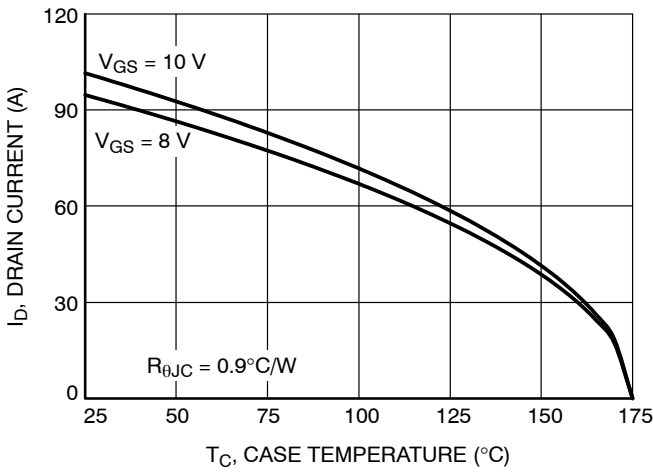


Figure 9. Drain Current vs. Case Temperature

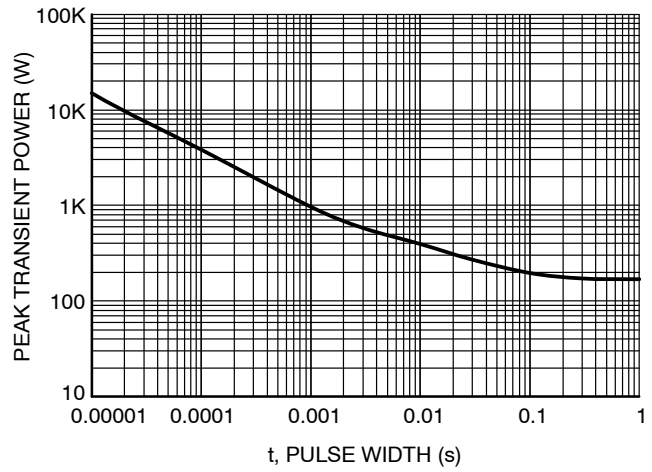


Figure 10. Peak Power

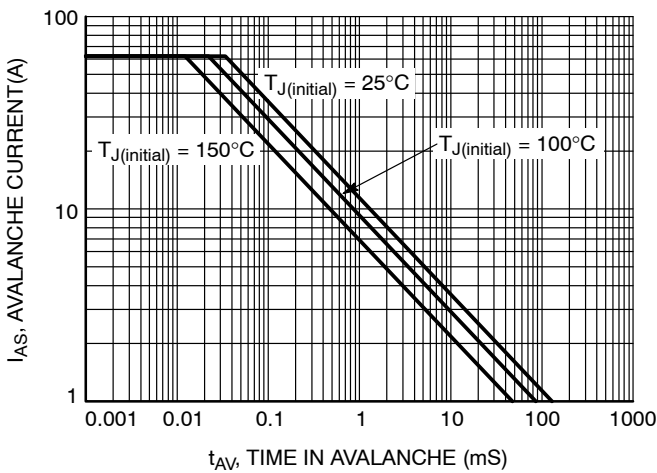


Figure 11. Unclamped Inductive Switching Capability

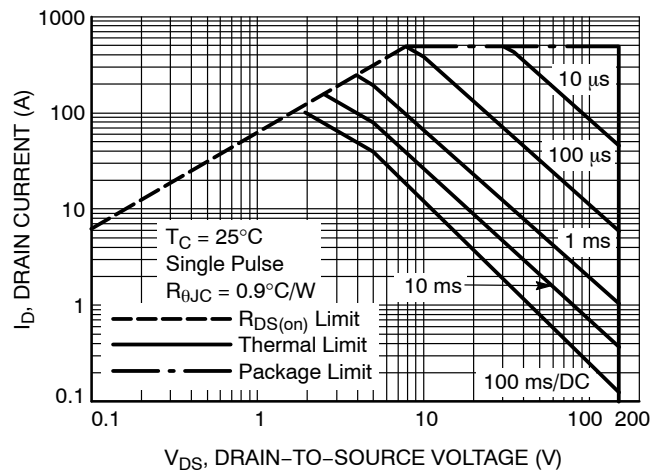


Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS

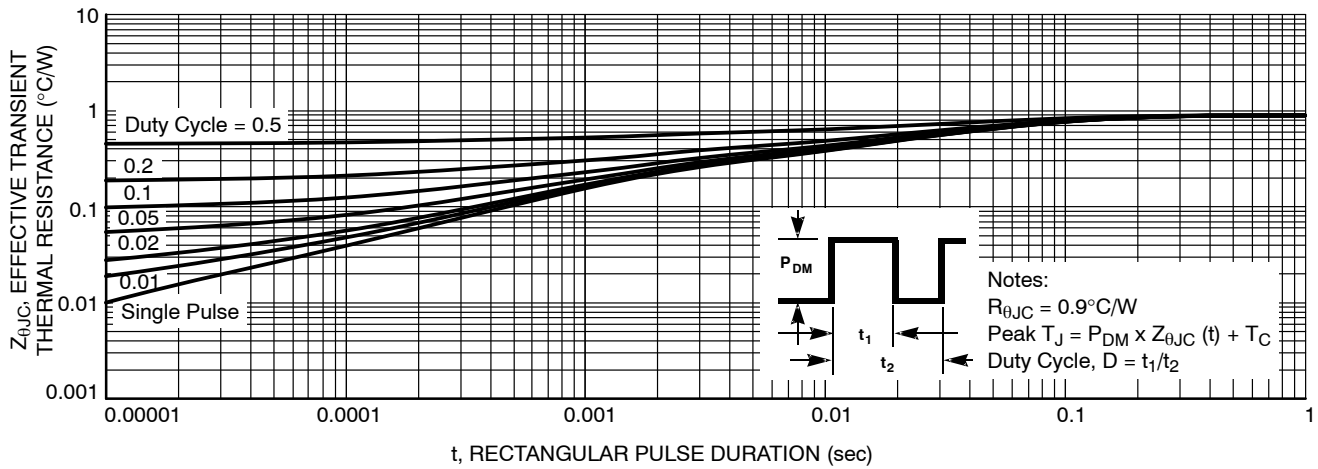
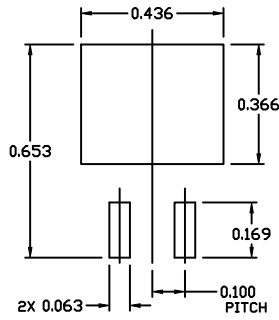


Figure 13. Transient Thermal Impedance

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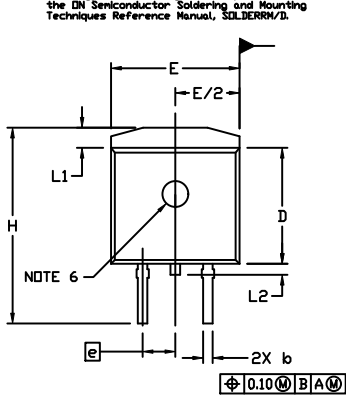
PACKAGE DIMENSIONS

D²PAK-3 (TO-263, 3-LEAD) CASE 418AJ ISSUE E



RECOMMENDED MOUNTING FOOTPRINT

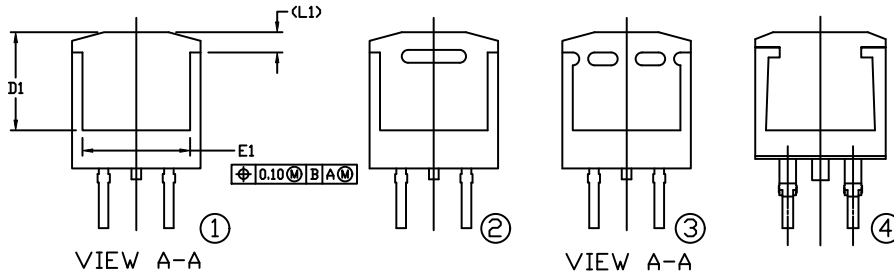
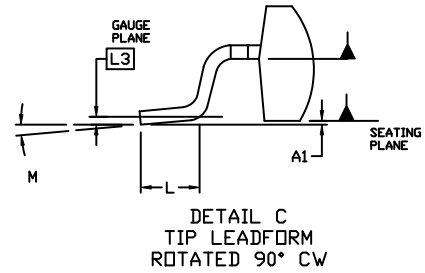
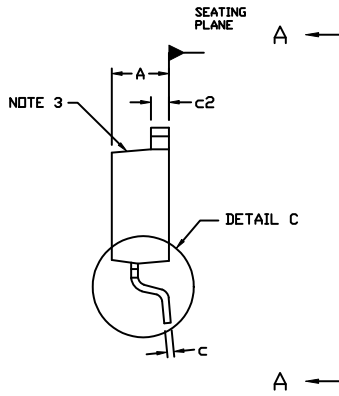
For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/T.



NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	-8°	8°	-8°	8°



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