swissbit®

Design-In Guideline

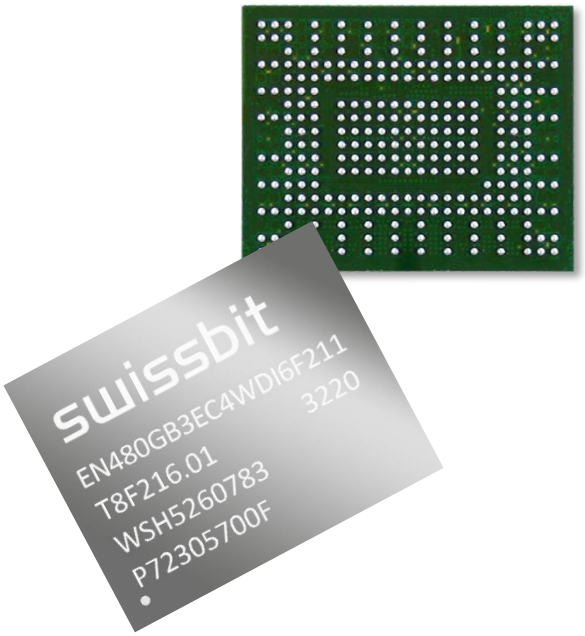
Industrial PCIe BGA SSD (M.2 1620 BGA)

EN-20 / EN-26 Series

PCIe Gen3, 3D TLC / 3D pSLC

Industrial Temperature Grade

Date: July 15, 2021
Revision: 1.00



Made in Germany

Contents

1. Overview

The Swissbit EN-2x Solid State Drive (SSD) leverages the M.2 BGA standard and NVMe standard to support a PCIe electrical interface. The NVMe controller and the newest 3D NAND flash technology provide a robust, nonvolatile storage solution for todays embedded computing applications. The EN-2x SSD combines a high performance NVMe controller and several 3D NAND flash devices into a 16 x 20mm BGA package.

Swissbit offers different product series based on the EN-20 / EN-26 (BGA SSD), such as N-20m2 / N-26m2 (m.2 module in lengths of 30/42/80mm) and G-20 / G-26 (CFExpress card).
For details about all these series, please see our Fact- and Datasheets on our website www.swissbit.com.

1.1 Scope

This application note provides information and suggestions on designing a printed circuit board (PCB) for the EN-2x BGA in order to achieve optimum performance for system applications.

2. References

1. NVM Express, Inc., "NVM Express Revision 1.3," [Online].
   Available: https://nvmexpress.org/wp-content/uploads/NVM_Express_Revision_1.3.pdf.
   [Accessed 22 03 2021].

2. „NVMe Command Line Interface," NVM Express, Inc., [Online].
   Available: https://nvmexpress.org/open-source-nvme-management-utility-nvme-command-line-interface-nvme-cli/.
   [Accessed am 22 03 2021].

3. „Active State Power Management," Wikipedia, [Online].
   Available: https://en.wikipedia.org/wiki/Active_State_Power_Management.
   [Accessed am 22 03 2021].

3. Hardware

3.1 Signal description

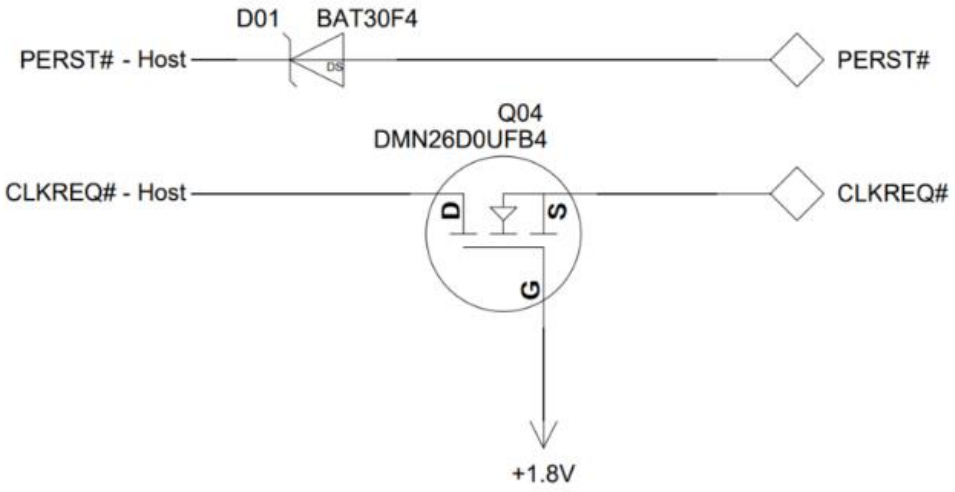
3.1.1 4 lanes, 2 lanes and 1 lane options

The EN-2x drives could be used with 1, 2 or 4 PCIe lanes. This will influence the performance and power consumption. The host must be connected with lane 0, lanes 0, 1 or lanes 0, 1, 2, 3. Unconnected lanes can be left floating.
The EN-2x supports the "lane reversal" option, e.g., if the host uses only lane 0, it should be connected to drive lane 0, but it may alternatively be connected to drive lane 3.
See https://teledynelecroy.com/doc/understanding-lane-reversal-and-polarity.

3.1.2 3V3 and 1v8 signals (PERST# and CLKREQ#)

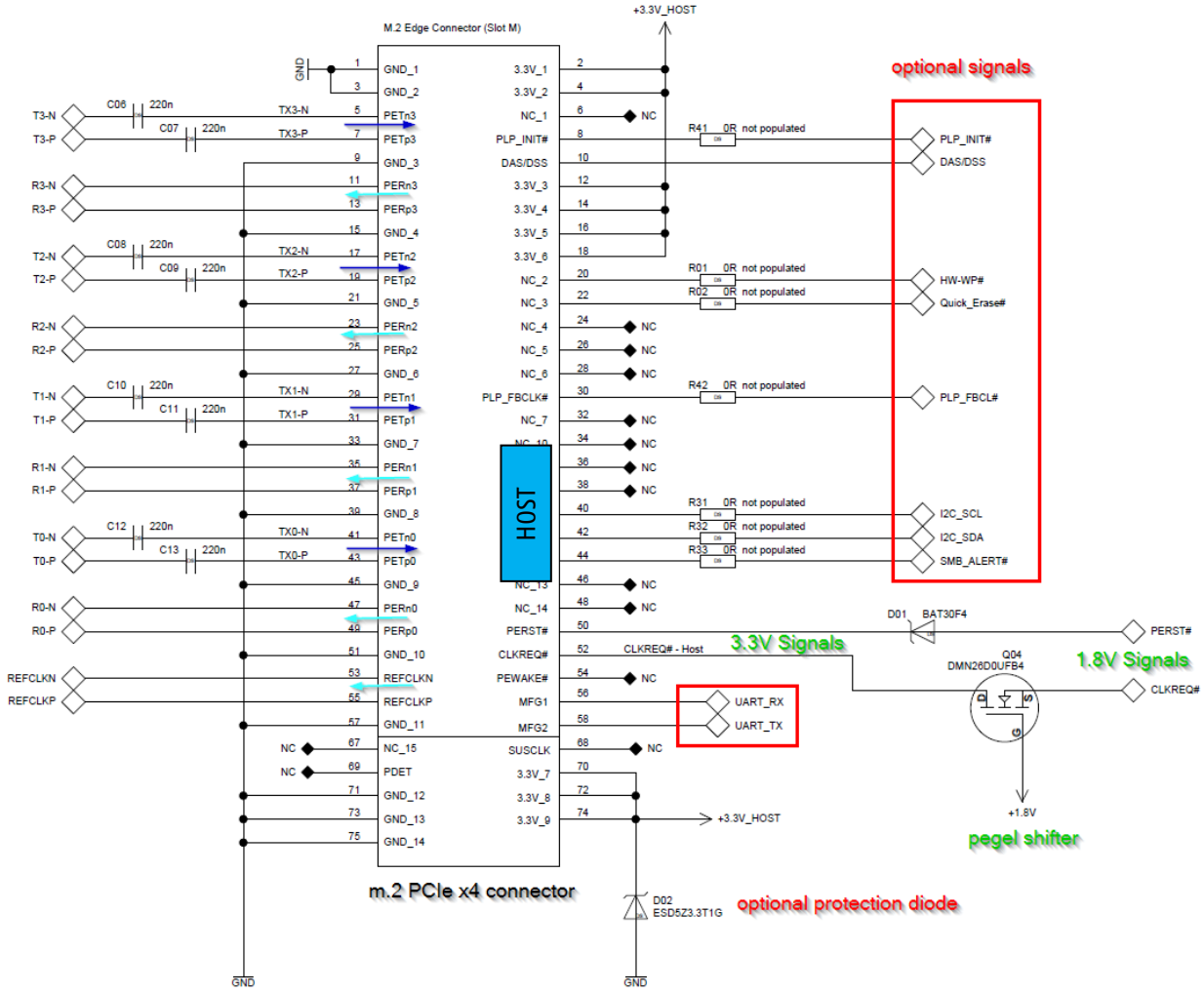
The standard EN-2x BGAs use a signal level of 1.8V at PERST# and at CLKREQ# signal as specified in the PCIe standard. If a host needs 3.3V signal level for these signals, the level can be shifted by a diode and a FET transistor, respectively, see Figure 1.

Figure 1: Level shifter for PERST# input and CLKREQ# output



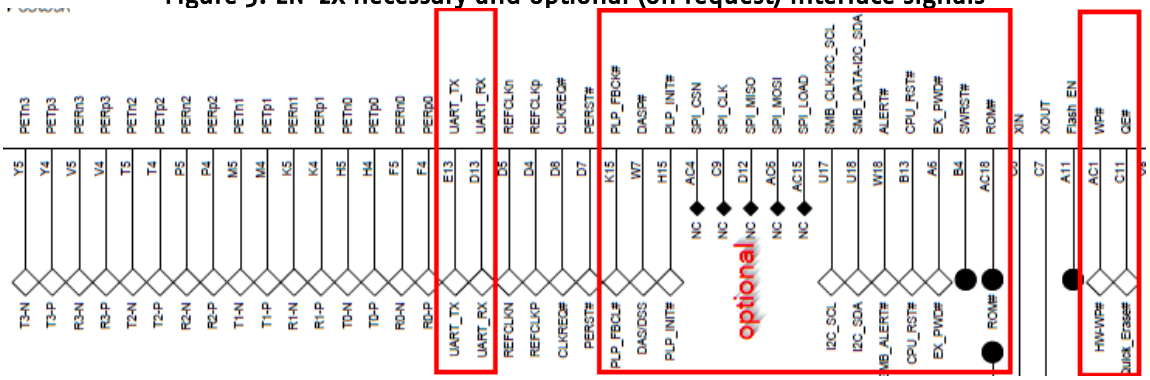
3.1.3 Interface to the host (e.g. m.2 PCIe drive)

Figure 2: PCIe interface e.g. m.2 with 4 lanes



The EN-2x BGA must be connected to the host (e.g. m.2 interface) with the Reference Clock (REFCLKx), 4 PCIe lanes Tx-x (Transmitting from the EN-2x BGA), and Rx-x (Receiving from the BGA). The 220nF capacitors must be at the transmitting side.
Either 1, 2 or 4 lanes can be connected in the right order (host lane 0, 1, 2, 3)
Host lane 0 must be connected to device lane 0 (or might be connected to device lane 3 if it simplifies the routing).
According to the PCIe standard, voltage levels for the signals PERST# and CLKREQ# are specified as 1.8V for BGA and 3.3V for m.2, respectively. Therefore, level shifter (e.g. diode or FET transistor) should be used for both of these input and output signals.
The DAS/DSS signal indicates the transfer state of the drive. Other signals are optional, see Figure 3.

Figure 3: EN-2x necessary and optional (on request) interface signals

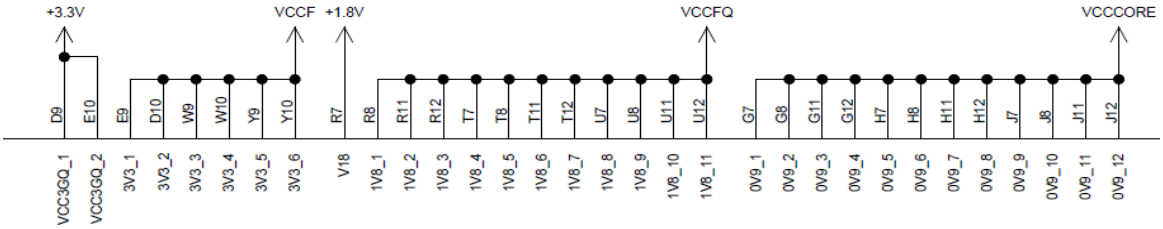


3.1.4 Voltages

Table 1: The EN-2x BGA needs 3 to 5 voltages (+/-5%)

Voltage	Pins	Description	Voltage V	Max current mA	Recommended caps µF
PWR_1 VCCF	D10, E9, W9, W10, Y9, Y10	Flash supply (6 pins) can be switched off by controller pin A6 (EX_PWD#)	2.9...3.3V	700	22
PWR_1.1 +3.3V	D9, E10	+3.3V supply (2 pins) permanent	3.3V	100	1
PWR_2 VCCFQ	R8, R11, R12, T7, T8, T11, T12, U7, U8, U11, U12	VCCFQ supply (11 pins) can be switched off by VCCF	1.8V	800	22
PWR_2.1 +1.8V	R7	+1.8V supply permanent	1.8V	150	10
PWR_3 VCCCORE	G7, G8, G11, G12, H7, H8, H11, H12, J7, J8, J11, J12	+core supply (12 pins) can be reduced to 0.75V by controller pin A6 (EX_PWD#)	0.9V	1500	2X 22

Figure 4: EN-2x Pins of the different voltages



Remarks

- To save power (temperature rise of the BGA), VCCF can be reduced to 2.9V.
  The internal flash chips have the same current consumption for 2.9V or 3.3V.
  With VCCF=2.9V 12% of the flash voltage is saved.

- To save energy in low power state (PS4), the controller switches pin A6 (EX_PWD#) low in this state.
  With EX_PWD following can be switched:
  - VCCCORE Core voltage can be reduced from 0.9V to 0.75V
  - bVCCF Flash voltage can be switched off.
  - The VCCFQ flash interface can be switched off with the Flash voltage VCCF.

  If PS4 mode is not used or extremely low power in PS4 is not necessary, the 3 voltages can stay on all time.

Figure 5: EN-2x simple power supply

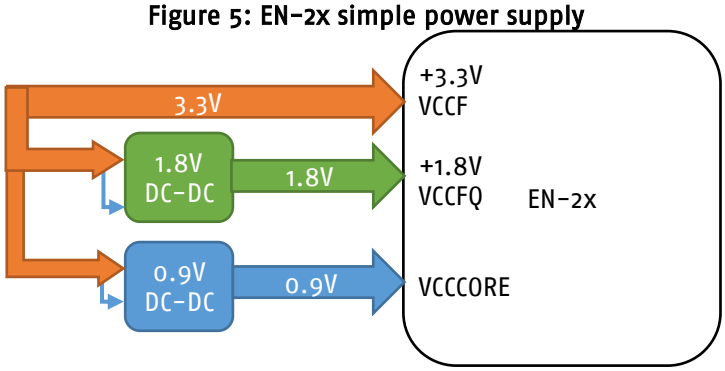


Figure 6: EN-2x to save operation power (heating) for high temperature heavy load application

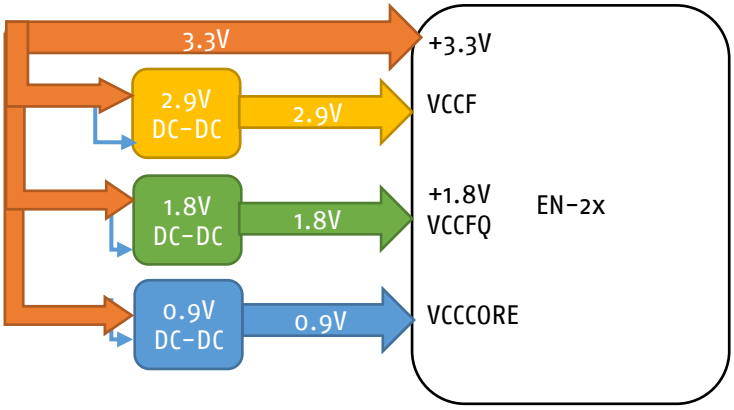
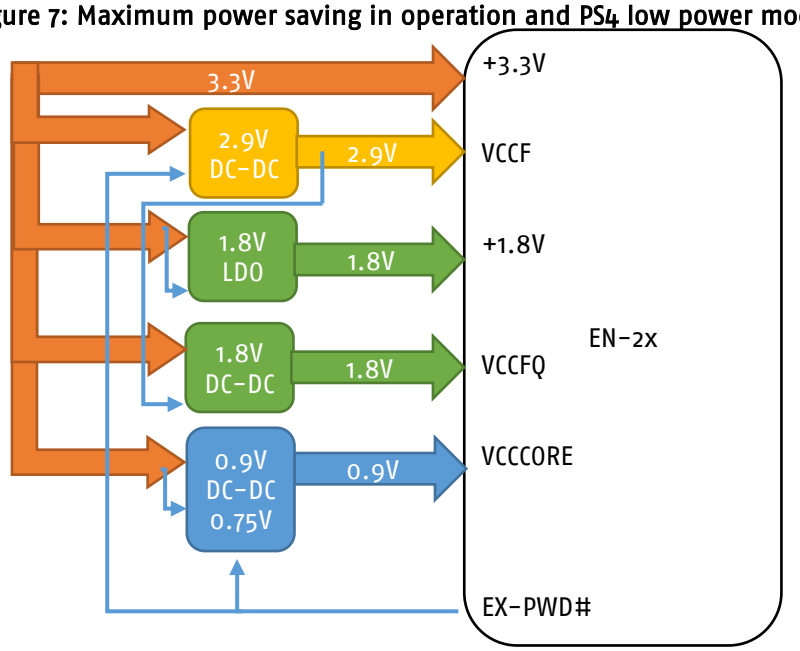
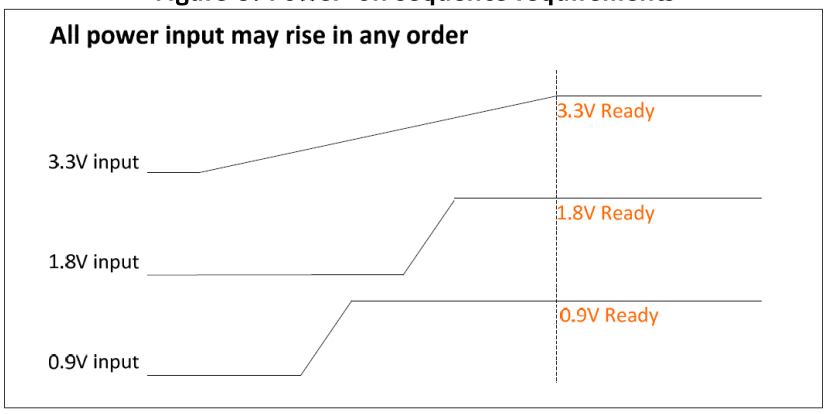


Figure 7: Maximum power saving in operation and PS4 low power mode



The voltages 3...5 can be applied in any order. The ramp time should be min 50µs.
If the drive is power cycled, all voltages should be <0.5V for >1ms (discharge, if necessary), see Figure 8.

Figure 8: Power-on sequence requirements

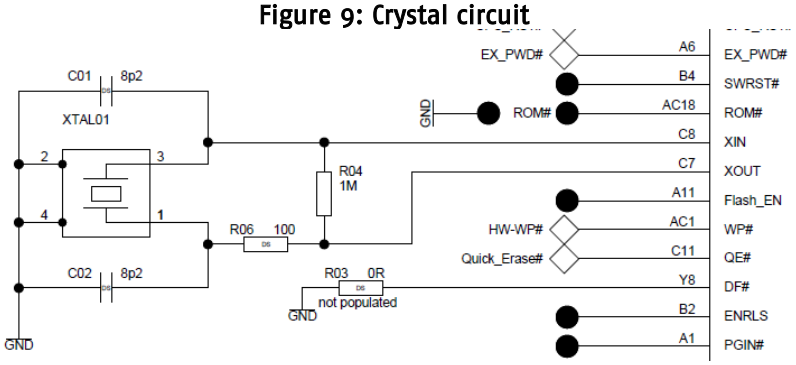


For extreme power saving in PS4 mode:

- VCCF and VCCFQ can be switched off by the EX_PWD# controller output in PS4 mode.
- VCCCORE can be reduced from 0.9V to 0.75V by the EX_PWD# controller output in PS4.

3.1.5 Crystal circuit

Figure 9: Crystal circuit



The 25.000MHz Crystal must be connected between XIN and XOUT, e.g., Murata XRCFD25M000F2N51R0.
The 1MOhm (R04) parallel resistor helps to start the oscillator.
The serial resistor (R06, here 100Ohm) reduces the driving level.
The value of both capacitors (C01 & C02) should be C01=C02=2*(C_L-C_Stray) in which C_L is defined in the crystal specification and C_Stray is the capacity of the BGA Pins and the PCB (C_Stray=1...3pF). Larger capacitors reduce the frequency slightly and damp the signal.

Frequency, amplitude, wave form

In Figure 10 / Figure 11 / Figure 12, characteristics of the Swissbit N-2x drive with EN-2x BGA with Murata XRCFD25M000F2N51R0, 100 Ohm serial resistor, 1MOhm parallel resistor and 2x 8.2pF capacitors with active probe are shown.

Figure 10: XOUT controller

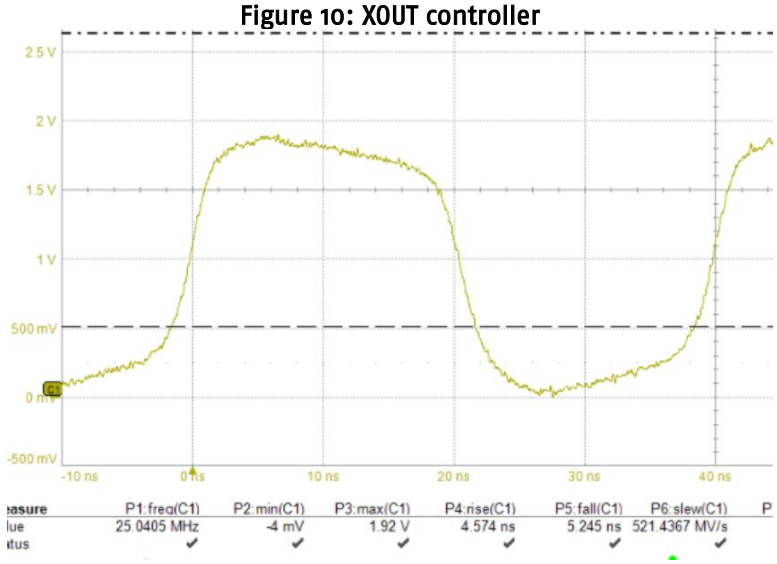


Figure 11: XDRV after 100Ohm

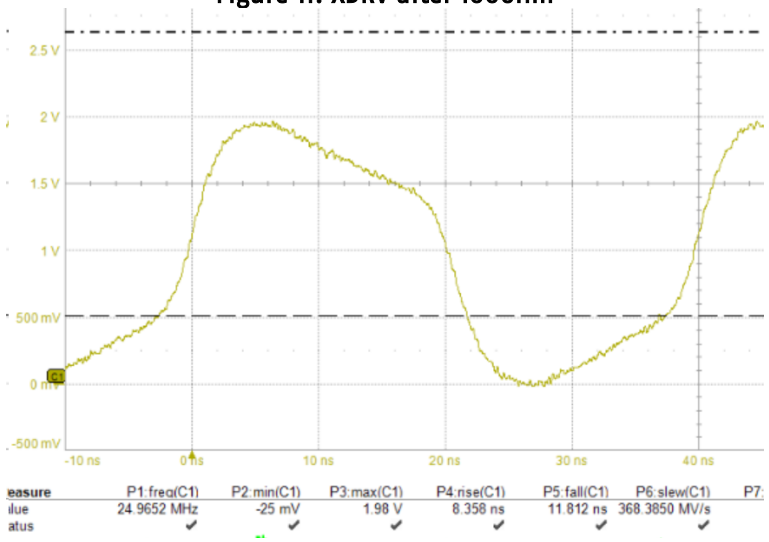
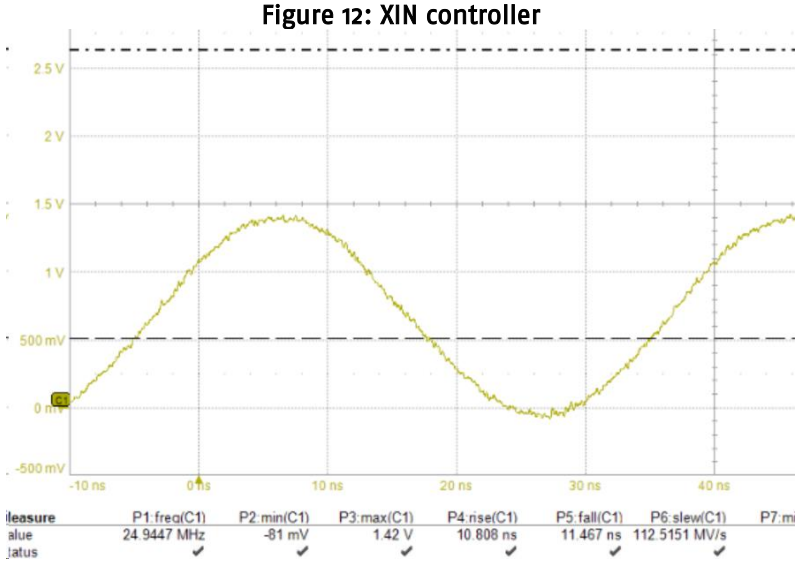


Figure 12: XIN controller



The driving resistor should be dimensioned, such that the oscillation margin is >5 and the driving strength is not larger than the maximum value specified by the crystal manufacturer.

For the optimization of the driving strength and oscillation margin, the serial resistor should be adapted. More information can be found via the following links:
https://www.murata.com/en-us/products/timingdevice/crystalu/basic/margin
https://video.murata.com/en-sg/detail/video/6180352806001

3.1.6 Other optional signals

If the signals are not used, keep them unconnected. Configurable signals can be activated in the Firmware on special customer request.

- DAS/DSS show Transfer activity, low active, LED with serial 1k0hm can be connected to 3.3V.
- HW-WP# Hardware Write protect (if configured, low active)
- Quick_Erase# Quick erase (if configured, low active)
- DF# host can initialize flush data before power off (if configured, low active)
- PLP_INIT# host can initialize flush data before power off (if configured, low active)
- PLP_FBCK# Drive signals, when data has been flushed after PLP_init (if configured, low active)
- I2C_SCL/I2C_SDA/SMB_ALERT# SMBus connection (if configured)
- UART_RX/UART_TX if possible route it to test pads, accessible for debugging
- JTDI/JTMS/JRST/JTCK/JTDO if possible route it to test pads, accessible for debugging

3.2 Layout recommendations

3.2.1 PCB Stackup

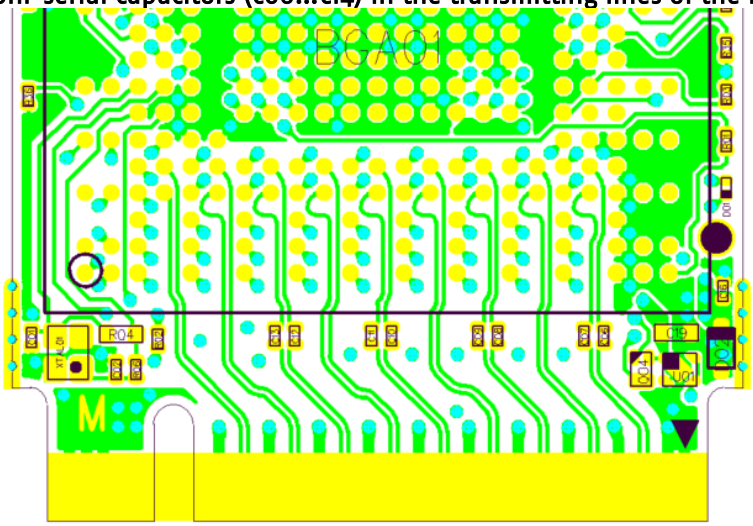
It is recommended to use a 4 layer FR4-based PCB. The ground plane should be the plane next to the assembly layer of the EN-2x BGA. The stack-up should provide a target differential impedance of the PCIe signals of 85 Ω ± 10%.

3.2.2 Routing Differential Signals

The PCIe interface supports transfer rates of 8 Gbps.

- Recommend to route differential signal traces on the board first.
- The length match intra pair needs to match under 5 mil (0.12mm)
- Keep the differential signal traces between the EN-2x chip and the connector or host chip with equal length, but no longer than 3 inch (76mm) if possible. Isolate the differential traces from other circuitry and signals. A minimum spacing of 50 mils (1.3mm) is required to ensure no interference to these traces.
- Do not route differential signal traces under crystal, oscillator, clock synthesizers, magnetic devices or ICs. It will cause interference.
- Place AC coupled 220nF capacitors (type 0201 recommended) at the Device transmitting lines (PETxx) as close as possible to the connector and without common mode filter (see Figure 13). In case of no connector in the embedded system, place the AC coupled 220nF capacitors (type 0201) close to the EN-2x chip. It should be noted that the capacitors mentioned above are necessary components to measure the differential signals and to detect the device.
- For the Device receiving lines (PERxx) and (REFCLKx) that are transmitted by the host, place the 220nF capacitors next to the host connector or in embedded system next to the host chip.

Figure 13: 220nF serial capacitors (C06…C14) in the transmitting lines of the EN-2x drives.



Other 5 differential pair high speed lines must have 220nF at the host side.

- Avoid right angle signal trace. When it is necessary to turn 90°, use two 45° turns or an arc instead of making a single 90°. In this way, it reduces reflections on the signal traces by minimizing impedance discontinuities.
- Avoid using vias in routing the trace of PCIe differential signals if possible. It can reduce signal reflection and impedance change. If it cannot be avoided make sure to keep both traces of the differential pair equal in length and symmetrical to prevent the problems mentioned above.

3.2.3 Controlled impedance

For good signal quality, the differential signal traces shall provide the impedance controlled at 85Ω±10% for differential pair and 50Ω ± 10% for single ended to match the transmitter and receiver impedance. Figure 14 shows a board stack-up and routing example (all length values in mil).

- Material: FR4, with Dielectric constant (Er) of 4.2
- The stack can provide the specified impedance: 85Ω ± 10% and signal end 50Ω ± 10%

Figure 14: Differential Controlled Impedance (PCIe signals)

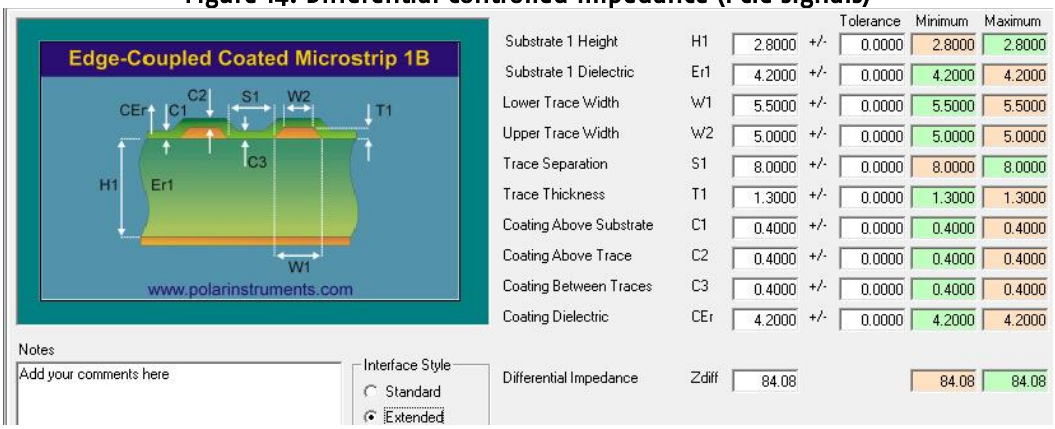
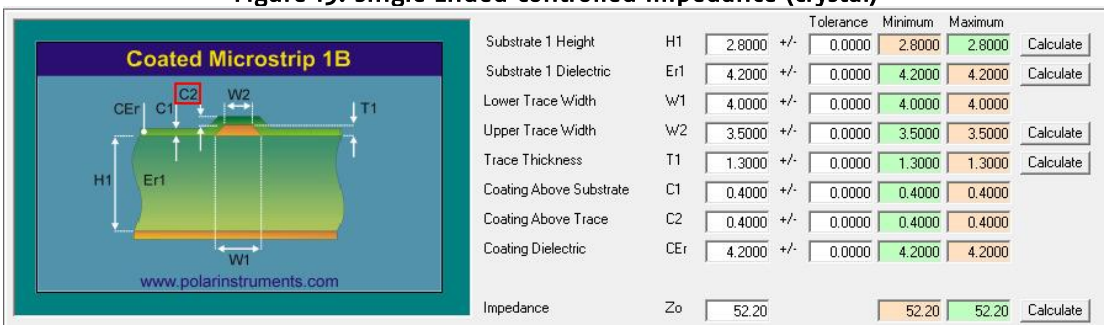


Figure 15: Single Ended Controlled Impedance (Crystal)



3.2.4 Power and ground plane Guidelines

The following recommendations apply to the design and layout of power and ground planes:

- Try to keep the power plane and ground plane as large as possible for good thermal and EMI performance.
- Route high speed signals (PCIe differential signal) above a continuous and unbroken ground plane.
- The trace width of VCC3F, VCCFQ, VCC3GQ, V18 and VCCK signals must be as wide as possible, keeping a minimum of 25 mils (0.63mm) width on the board. In addition, the above mentioned signals must keep a spacing of at least 8 mils (0.2mm) width to the EN-2x chip and 10 mils (0.25mm) width to the flash to minimize crosstalk.
- Avoid vias while placing capacitors, especially for the bypass capacitors located close to VCC3F, VCCFQ, VCC3GQ, V18 and VCCK signals.
- The power components (DC-DC or LDO) need to be close to the EN-2x Chip. Avoid long connections between the power component and EN-2x. It can prevent noise or interference.

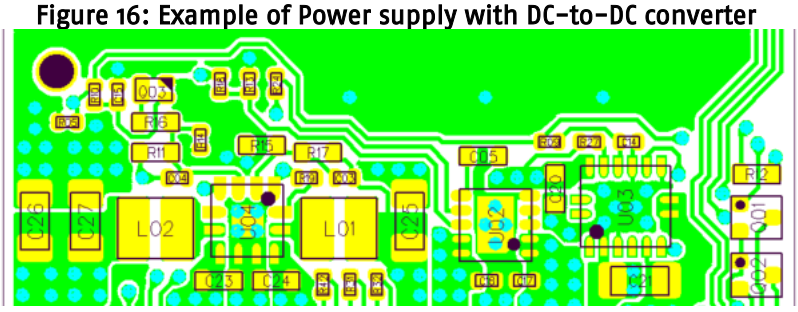
3.2.5 DC-to-DC Converter

The EN-2x works at power supply voltage of 3.3V/1.8V/0.9V. It is recommended to use a DC-to-DC converter for power supply rather than a LDO voltage regulator. The drop voltage of DC-DC converter is less than that of regulator; thereby it enhances the power stability in the system.

The following guidelines should be used to help ensure a proper layout.

- The input capacitor should be connected as closely as possible to VIN and GND
- The output capacitor and inductor should be connected as closely as possible. The connection of the inductor to the LX pin should be as short as possible.
- The feedback trace or OUT pin should be separate from any power trace and connected as closely as possible to the load point.
- Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the OUT pin to minimize the length of the high impedance feedback trace.
- The resistance of the trace from the load return to the GND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

Figure 16: Example of Power supply with DC-to-DC converter



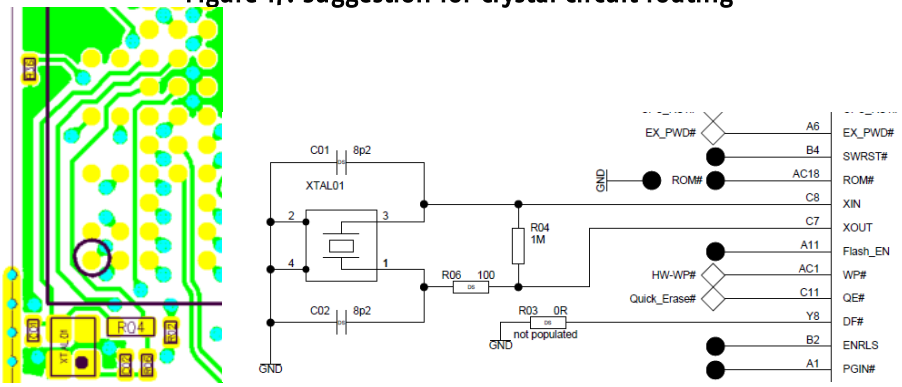
3.2.6 Crystal

XIN and XOUT must be connected to a 25MHz crystal with the typical external components. Because of the crystal gain characteristics and frequency stability, the 25MHz crystal is extremely sensitive to power supply noise and to electromagnetic coupling to nearby high-speed signals. Noise coupling can significantly degrade the frequency stability of the crystal. The objective of this section is to present general guidelines that can be applied to improve the performance of the crystal and to prevent any critical issues.

For the best performance, observe the following guidelines:

- The Crystal and its components should be placed close to EN-2x chip on the same layer.
- 25MHz clock trace should be protected by ground plane to avoid the impact of other signals.
- For good 25MHz clock quality, set 50Ω ± 10% impedance for signal ended (see Figure 17).

Figure 17: Suggestion for Crystal circuit routing



Additional recommendations: https://www.nxp.com/docs/en/application-note/AN12864.pdf

3.2.7 BGA ball break-out

Suggestion for the BGA solder pads:

- not solder mask defined (NSMD)
- copper pad size 0.45mm
- solder mask opening 0.55mm

3.3 Temperature characteristics

The EN-2x has a metalized surface for heat dissipation. In temperature-critical application, an additional heat spreader should be mounted.

3.3.1 Temperature sensors and reported temperatures

The EN-2x has a temperature sensor inside the controller. A normalized "Composite temperature" is calculated, which is 6...12 degrees lower than measured (dependent on the operation). This should represent the surface temperature of the BGA.
Composite temperature and NAND flash temperatures are reported in the Telemetry log and the SMART log.

3.3.2 Throttling

To prevent over heating at high temperature and heavy load the EN-2x has two throttling stages that reduce the bandwidth, power consumption and self-heating.
The standard drives have following throttling temperature thresholds of the composite temperature:

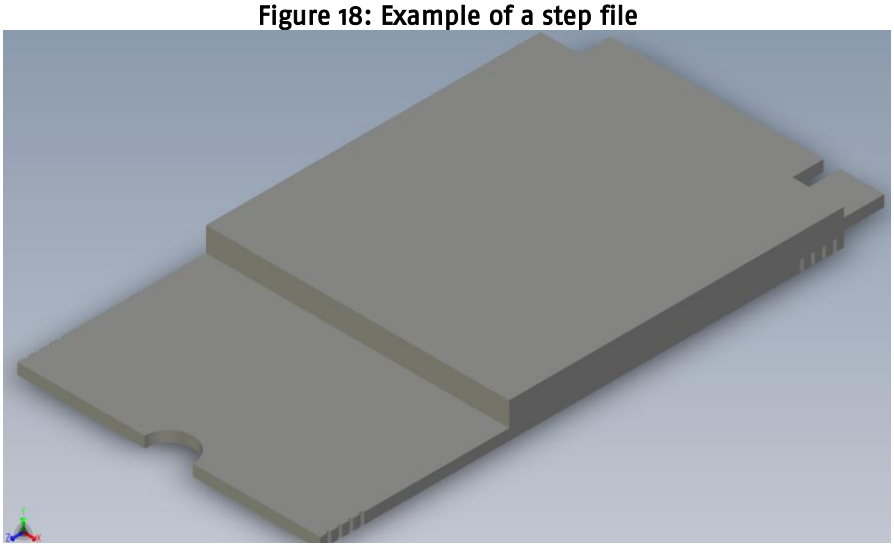
Table 2: Throttling mode temperature and performance

Mode	Throttling temperature	Release temperature	Sequential read performance
Normal operation			100%
Light Throttling	90°C	80°C	~60%
Heavy Throttling	105°C	95°C	~20%
Thermal Shutdown	125°C		Thermal shutdown

3.4 Step file (reference to availability)

STEP Model of the Swissbit m.2 N-2x module with EN-2x BGA available on request.

Figure 18: Example of a step file



4. Software

The EN-2x series complies with the NVM express base specification revision 1.3 (1). The following commands and concepts are based on the NVMe specification.

4.1 NVMe Management Utility

For Linux, there is an open source tool available for managing NVMe drives, the NVMe Command Line Interface (NVMe-CLI) (2).
This tool can be used for executing firmware updates, configuring features, read out drive and lifetime information and more.

4.2 Power and heat management

The EN-2x series supports several features to reduce power consumption and heat generation.

4.2.1 Active-state power management (ASPM)

Active-state power management (ASPM) is a power management mechanism for PCI Express devices to garner power savings while otherwise in a fully active state. Predominantly, this is achieved through active-state link power management; i.e., the PCI Express serial link is powered down when there is no traffic across it.
ASPM is usually managed by the operating system's power management software or through the BIOS. While ASPM brings a reduction in power consumption, it can also result in increased latency as the serial bus needs to be 'woken up' from low-power mode, possibly reconfigured and the host-to-device link re-established. This is known as ASPM exit latency (3).

Swissbit recommends enabling ASPM on the host system to reduce the power consumption of the drive.

4.2.2 NVMe Power Management

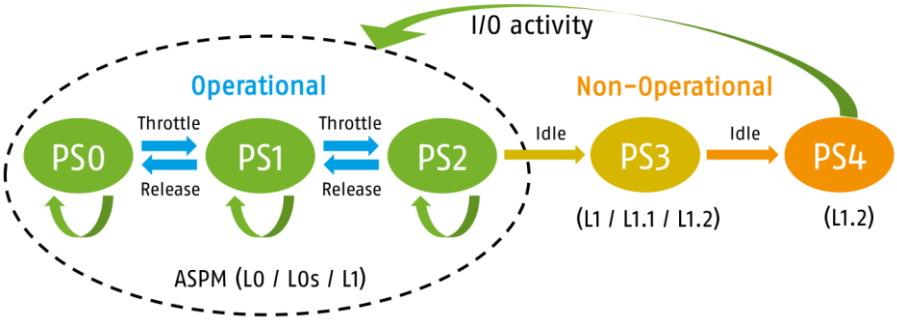
The EN-2x series supports 5 different NVMe power states. For each power state there is a descriptor which indicates the maximum power that may be consumed in that state, entry, and exit latency for non-operational power states and more. These power state descriptors can be found in the "Identify Controller" data structure.

Table 3: EN-2x Power States

NVMe Power State	PCIe Link State	Operational	Max Power [W][1]	Entry Latency [ms][1]	Exit Latency [ms][1]	Note
PS0	L0 / L0s / L1	Yes	3.5	-	-	Full-speed
PS1	L0 / L0s / L1	Yes	2.5	-	-	Light Throttle
PS2	L0 / L0s / L1	Yes	1.5	-	-	Heavy Throttle
PS3	L1 / L1.1 / L1.2	No	0.2	2.2	3	Light Sleep
PS4	L1.2	No	0.1	15	12	Deep Sleep

The power states can be checked and controlled by the NVMe "Get Features" or "Set Features" command (Feature ID 02h).

Figure 19: NVMe Power State Overview



4.2.3 Autonomous Power State Transitions (APST)[2]

Autonomous power state transitions provide a mechanism for the host to configure the drive to automatically transition between power states on certain conditions without software intervention. The entry condition to transition to the Idle Transition Power State is that the drive has been in idle for a continuous period of time exceeding the Idle Time Prior to Transition time specified. The controller is idle when there are no commands outstanding to any I/O Submission Queue. An autonomous power state transition is only possible to a non-operational power state.

The current APST status can be checked and controlled by the NVMe "Get Features" or "Set Features" command (Feature ID 0Ch).

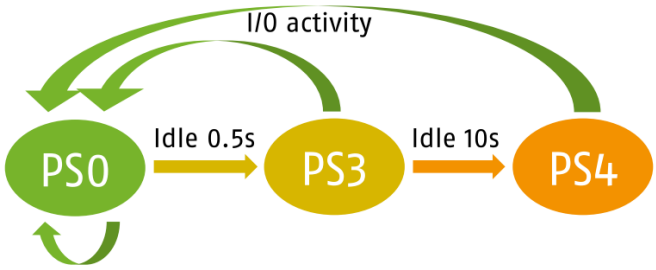
Table 4: Example of a possible APST configuration

Power State Table	
NVMe Power State	Operational
PS0	Yes
PS1	Yes
PS2	Yes
PS3	No
PS4	No

APST Table	
Idle Time Prior to Transition [ms]	Idle Transition Power State
500	PS3
500	PS3
500	PS3
10'000	PS4
-	-

[1] Depends on density and firmware revision
[2] APST support depends on product revision and density, see APSTA field in the "Identify Controller data structure"

Figure 20: APST Overview



4.2.4 Thermal Throttling Management

The EN-2x provides a mechanism to automatically transition between active power states in order to attempt to meet thermal management requirements. There are three throttling stages:

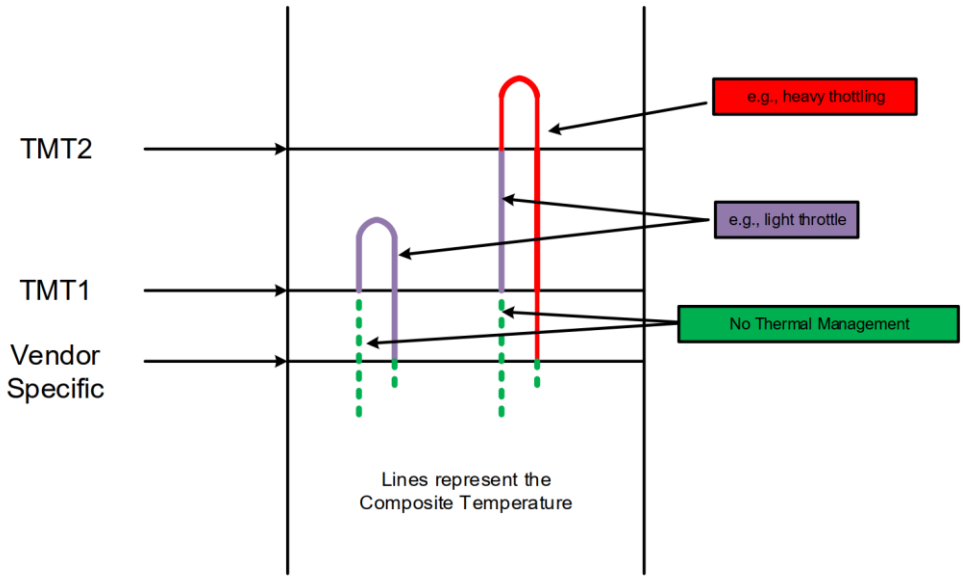
Table 5: Thermal Stages

Thermal Stage	Power State	Thermal Management Temperature (TMT)[3]	Note
Light Throttle	PS1	TMT1 (90°C)	
Heavy Throttle	PS2	TMT2(105°C)	
Shutdown	-	TMT3 (125°C)	Non-operative, reset required

The thermal throttling mechanism is enabled by default and cannot be disabled.

If the Composite Temperature, see chapter Temperature Sensors, is at or above TMT1 and below TMT2, the drive starts transitioning to Power State 1. If the Composite Temperature is at or above TMT2 the drive starts transitioning to PS2. The temperature at which the drive stops being in a lower power state is slightly lower than the respective TMT because (hysteresis), please see Table 2 for details.
If the Composite Temperature is at or above TMT3, the drive shuts down to prevent permanent damage. However, TMT3 should never be reached if the maximum ambient temperatures specified in the data sheet are respected[4].

Figure 21: NVMe Throttling



[3] Management temperature depends on product revision and density
[4] Adequate airflow or cooling is required to ensure the drive temperature does not exceed the specified maximum operating temperature.

4.2.4.1 Host Controlled Thermal Management (HCTM)

HCTM provides an option to adjust the EN-2x drive to the thermal characteristics of the host systems. With this feature, the thermal management stages described in Table 5, can be adjusted within a specific range. The "Maximum Thermal Management Temperature" (MXTMT) and the "Minimum Thermal Management Temperature" (MNTMT) which both can be found in the "Identify Controller" data structure limit this range.

TMT1 and TMT2 can be checked and controlled by the NVMe "Get Features" or "Set Features" command (Feature ID 0Ch).

4.2.4.2 Temperature Sensors

The EN-2x reports thee different temperatures in the "SMART / Health Information" log page.

Table 6: Temperature Sensors

Temperature	Unit	Note
Composite Temperature	°K	Represents the whole BGA and may differ from the actual temperature reported for sensor 1&2. This temperature is used for all thermal management actions.
Temperature Sensor 1	°K	Sensor that is located near the PCIe PHY
Temperature Sensor 2	°K	Sensor that is located near the NAND

4.2.4.3 Temperature Monitoring

The drive temperature should always be monitored by the host system. Therefore, several temperature thresholds can be used. Each temperature allows to set an under and over threshold.
Apart from the thresholds of each temperature, there are two more thresholds; the Warning Composite Temperature Threshold (WCTEMP) and the Critical Composite Temperature Threshold (CCTEMP). These thresholds are defined in the "Identify Controller" data structure. The drive reports the time it was over CCTEMP or WCTEMP in the "SMART / Health Information" log page, see "Warning Composite Temperature Time" or "Critical Composite Temperature Time" field.

If the temperature is over or under of one of the above mentioned thresholds, a warning is displayed in the "Critical Warning" field in the "SMART / Health Information" log page. It is recommended to closely monitor this field. The temperature thresholds and the host system environment should be configured so that the CCTEMP temperature is never reached. The WCTEMP temperature should be reached for a very short time at most.

4.3 Firmware update

The EN-2x series supports in-field firmware update. The firmware update is implemented according to the firmware update process described in the NVMe specification. The EN-2x supports firmware updates without requiring a reset.

Swissbit provides and recommends the "SBFirmwareUpdate" tool for executing firmware updates. This tool is available for Windows and as a live Linux version (bootable image).

4.4 Host Memory Buffer (HMB)

The Host Memory Buffer feature allows the controller to utilize an assigned portion of host memory exclusively. The use of the host memory resources is vendor specific. Host software may not be able to provide any or a limited amount of the host memory resources requested by the controller.

The HMB feature can be en/disabled with the NVMe Set Features command. Modern operating systems like Windows 10 or Linux do enable HMB by default. The current HMB status can be checked with NVMe Get Features command.

The EN-2x supports the use of 64MB HMB, as indicated in HMPRE/HMMIN fields in the "Identify Controller data structure". Enabled HMB will result in higher performance and endurance. Therefore, Swissbit recommends the use of HMB.

5. Features on request

The following features are only available on special customer request and are not available for *-STD products.

5.1 Quick erase

The quick erase feature provides a hardware controlled method to erase all user data.
For the quick erase feature, the signals shown in Table 7 have to be connected.

Table 7: Quick Erase Signals

Description	Direction (I/O)	Signal
QEE (Quick Erase Enable)	I	QE#
QEB (Quick Erase Busy)	O	DASP#

Procedure:

QE0: Normal:
Normal operating state

- **Transition QE0:QE1:** When the QEE signal is asserted for more than 1s, the drive transitions to QE1.

QE1: Quick Erase Init:
In this state, the device completes previous queued tasks and resets related hardware registers. The maximum processing time will be less than 600ms.

- **Transition QE1:QE0:** If a power cycle event occurs during this state, the drive will give up the current Quick Erase action and transition back to QE0.
- **Transition QE1:QE2:** When all initialization tasks finished successfully, the drive transitions to QE2

QE2: Quick Erase Execute:
In this state, the device starts to search all data blocks and erases them. When this state is entered, the QEB- is asserted to indicate the drive is busy.

- **Transition QE2:QE2:** If a power cycle event occurs in this state, the drive shall resume erase process after boot process finished.
- **Transition QE2:QE3:** Once all data blocks have been successfully erased, the drive enters QE3.

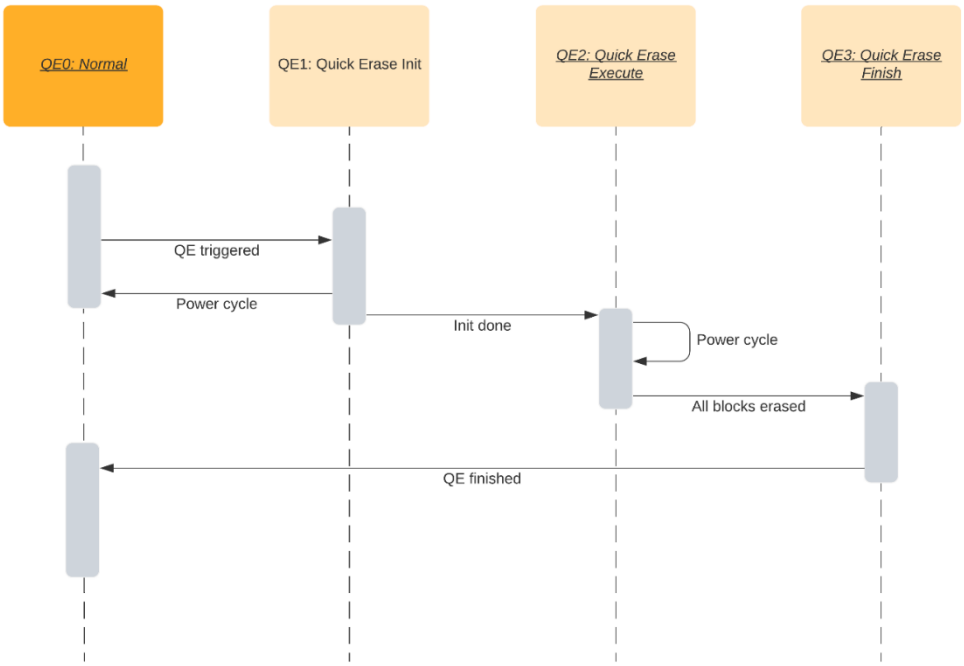
QE3: Quick Erase Finish:
In this state, the QEB- will be de-asserted and the CSTS.CFS controller register bit will be set to indicate that device is ready again.

Transition QE3:QE0: After QEB- and CSTS.CFS have been successfully modified, the drive enters QE0.

Notes:

- After a quick erase has been triggered it has highest priority, so any other command like a NVMe reset will not be executed.
- 0x00 will be returned for all user data after a successful quick erase operation.
- After the quick erase procedure the host is required to reset the drive (NVMe reset or power cycle).
- The busy time varies depending on density and firmware of the drive. The maximum busy time is expected ~10s.

Figure 22: Quick Erase Sequence



5.2 Write protect

The write protect feature provides a hardware controlled method to prevent any unexpected writes to the drive. For the write protect feature, the signal shown in Table 8 has to be connected.

Table 8: Write Protect Signals

Description	Direction (I/O)	Signal
WPE (Write Protect Enable)	I	WP#

Procedure:

WP0: Sample WPE:
This state is entered when the host issued any commands, then device shall sample the WPE- signal

- **Transition WP0:WP1:** When the drive has detected an issued write command but WPE is de-asserted, the drive enters WP1 (normal command execution).
- **Transition WP0:WP2/3:** When the drive has detected an issued write command and WPE is asserted for >10ms, the drive enters WP2 or WP3. On default WP2 (dummy write) will be entered.
- **WP3:** Return_Error(optional)

WP1: Command Execute:
Commands will be executed as usual in this state.

- **Transition WP1:WP4:** The drive returns to idle state after successful command execution.

WP2: Dummy Write:
In this state all write commands return successful. However, no data will be actually written to the flash.

- **Transition WP2:WP4:** The drive will immediately successfully complete the write command and return to idle.

WP3: Return Error:
In this state all write commands return with an error, no data will be actually written to the flash.

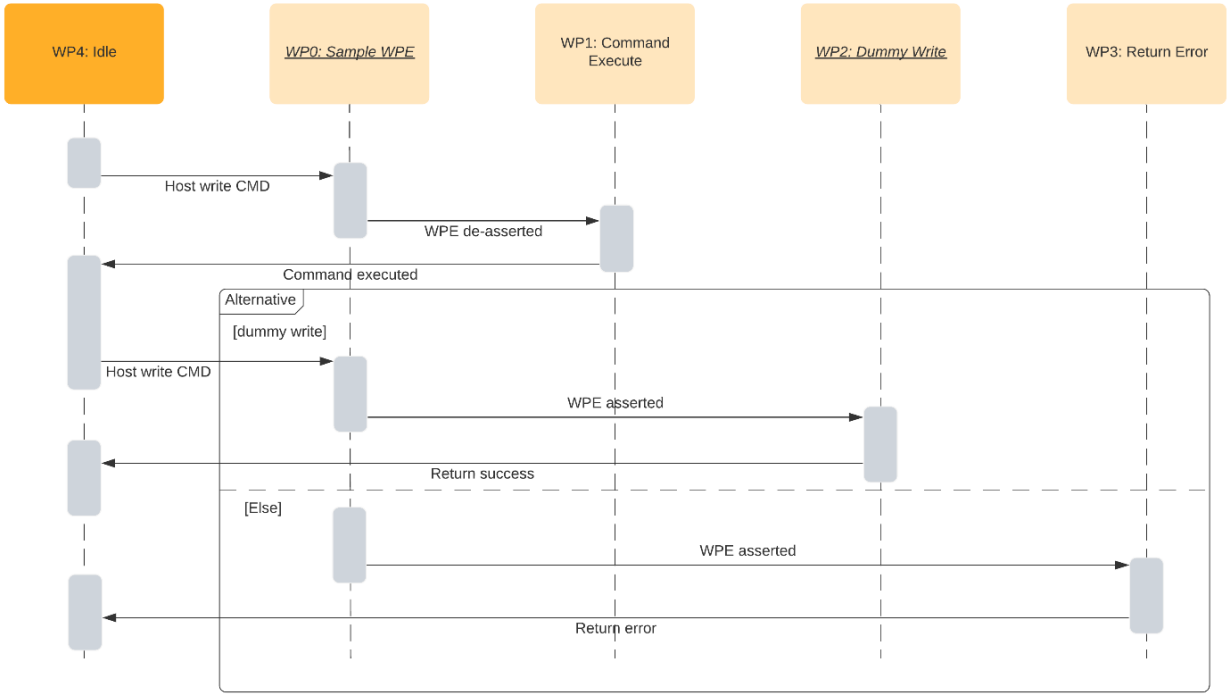
- **Transition WP3:WP4:** The drive will immediately return an error on the write command and return to idle.

WP4: Idle: Idle state.

Notes:
The following commands are considered as "write command":

- NVMe Write
- NVMe Write Uncorrectable
- NVMe Write Zeroes
- NVMe Format
- NVMe Sanitize

Figure 23: Write Protect Sequence



5.3 Data flush before power off

The last data in the cache can be written to the NAND flash (flushed) before power off by setting DF# low.
All voltages must be stable at least 20ms after the DF# trigger.
After the DF# trigger was detected the PCIe interface will become inactive and all queued commands are discarded. Only data that already is internally cached will be flushed.
After this operation, the device is inactive and must be power cycled.

6. Revision History

Table 9: Document Revision History

Date	Revision	Description	Revision Details
July 15, 2021	1.00	Initial release	Doc. req. no. 4766