LAN8670/1/2

10BASE-T1S Ethernet PHY Transceiver

Description

The LAN8670/1/2 is a high-performance 10BASE-T1S single-pair Ethernet PHY transceiver for 10 Mbit/s half-duplex networking over a single pair of conductors. Utilizing standard Ethernet technology in sensor/actuator networks reduces application costs by eliminating gateways necessary with legacy networking technologies. The ability to connect multiple PHYs onto a common mixing segment further saves implementation costs by reducing cabling and switch ports. The LAN8670/1/2 is designed for use in high-reliability cost sensitive industrial, backplane, and building automation sensor/actuator applications.

Highlights

- High-performance 10BASE-T1S Ethernet PHY
- Designed according to IEEE Std 802.3cg-2019™
  - 10 Mbit/s over single balanced pair
  - Half-duplex point-to-point link segments up to at least 15m
  - Half-duplex multidrop mixing segments up to at least 25m with up to at least 8 PHYs
- Media Independent Interface (MII) and Reduced Media Independent Interface (RMII)
  - 2.5 MHz MII clock mode
  - 50 MHz RMII clock mode
  - Serial Management Interface (SMI) for rapid register access
  - Comprehensive status interrupt support
- Carrier Sense Multiple Access / Collision Detection (CSMA/CD) media access control
- Physical Layer Collision Avoidance (PLCA)
  - Allows for high bandwidth utilization by avoiding collisions on the physical layer
  - Burst mode for transmission of multiple packets for high packet rate latency-sensitive applications
- Enhanced electromagnetic compatibility / electromagnetic interference (EMC/EMI) performance
  - Low RF emissions
  - Robust against injected currents and network cable shorts to ground or battery
  - Simple low cost analog front-end
- Single 3.3V supply with integrated 1.8V regulator
- Small footprint VQFN packaging with wettable flanks
  - LAN8670 32-pin (5 x 5 mm)
  - LAN8671 24-pin (4 x 4 mm)
  - LAN8672 36-pin (6 x 6 mm)
- -40°C to +125°C extended temperature range
- Microchip Functional Safety Ready

Target Applications

- Sensor/actuator networks operating at high bandwidth
- Microphone networks delivering audio streams for beamforming, hands-free microphones, etc.
- Backplane communication
- Industrial control cabinets and machine control
- Building automation

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Conformity

Table 1 shows the conformity relationship between data sheet, silicon, and product revisions. This data sheet applies to silicon revision 2 (0010b) as shown below.

Table 1. Conformity Table

Product Revision[1]	Silicon Revision[2]	Data Sheet Revision
A0	Rev 0 (0000b)	DS60001573A
B1	Rev 2 (0010b)	DS60001573B
B1	Rev 2 (0010b)	DS60001573C

Notes:

1. The product revision is noted in the package top marking.
2. The silicon revision is obtained by reading the Manufacturer's Model Revision from the PHY Identifier 1 register.

Related Links

9. Package Marking Information

5.1.4 PHY_ID1

Table of Contents

1. Preface

1.1 General Terms

Table 1-1. General Terms

Term	Description
10BASE-T	10 Mbit/s Ethernet over twisted pair, IEEE Std 802.3™ Clause 14
10BASE-T1L	10 Mbit/s Ethernet over long-reach single pair of conductors, IEEE Std 802.3 Clause 146
10BASE-T1S	10 Mbit/s Ethernet over short-reach single pair of conductors, IEEE Std 802.3 Clause 147
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
CSR	Control and Status Register
BT	Bit Time, 100 ns for 10 Mbps Ethernet
LDO	Low Dropout Regulator
MAC	Media Access Controller
MDI	Medium Dependent Interface
MII	Media Independent Interface, IEEE Std 802.3 Clause 22
PCS	Physical Coding Sublayer
PLCA	Physical Layer Collision Avoidance, IEEE Std 802.3 Clause 148
PMA	Physical Medium Attachment sublayer
PMD	Physical Medium Dependent sublayer
POR	Power-on Reset
RS	Reconciliation Sublayer
SMI	Serial Management Interface, also known as MII Management Interface, IEEE Std 802.3 Clause 22
STA	Station management entity
RMII	Reduced Media Independent Interface

1.2 Buffer Types

Table 1-2. LAN8670/1/2 Buffer Type Descriptions

Buffer	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-directional
ICLK	Oscillator input
OCLK	Crystal oscillator output
P	Power
PD	55 kΩ (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
PU	55 kΩ (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
VIS-VDDP	3.3V Schmitt-triggered input (VDDP power domain)
VO-VDDP	3.3V output (VDDP power domain)
VOH-VDDP	3.3V high-speed output (VDDP power domain)
VOD-VDDP	3.3V open-drain output (VDDP power domain)

Note: Digital signals are not 5V tolerant unless specified.

1.3 Register Bit Types

The following table describes the register bit attributes used throughout this document.

Table 1-3. Register Bit Types

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RO	**Read Only:** A register of bit with this attribute is read only; writing has no effect.
WO	**Write Only:** If a register or bit is write-only, reads will return unspecified data.
W1S	**Write One to Set:** Writing a one sets the value. Writing a zero has no effect.
W1C	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect.
WAC	**Write Anything to Clear:** Writing anything clears the value.
RC	**Read to Clear:** Content is cleared after the read. Writes have no effect.
SC	**Self Clearing:** A bit with this attribute will be cleared to '0' after being written as '1'. Hardware often clears such bits following the completion of some action initiated by the write.
NASR	**Not Affected by Software Reset:** The state of NASR bits do not change on assertion of a software reset.
STKY	This field is "Sticky" in that it is neither initialized nor modified by hot reset or Function Level Reset.
RESERVED	**Reserved Field:** Reserved fields must be written with the same default values as specified. The value of reserved bits is not guaranteed on a read.

Many of these register bit notations can be combined. Some examples of this are:

- R/W: Can be written. Will return current setting on a read.
- R/W1C: Will return current setting on a read. Writing a '1' clears the bit.

1.4 Reference Documents

1. IEEE Std 802.3™-2018, IEEE Standard for Ethernet.
   standards.ieee.org/standard/802_3-2018.html
2. IEEE Std 802.3cg™-2019, IEEE Standard for Ethernet, Amendment 5: Physical Layer Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors.
   standards.ieee.org/standard/802_3cg-2019.html
3. RMII Specification Revision 1.2.

2. Introduction

2.1 General Description

The Microchip LAN8670/1/2 is a compact, low power, and cost-effective single-port 10BASE-T1S Ethernet physical layer transceiver designed according to the IEEE Std 802.3cg-2019 specification. The device provides 10 Mbit/s half-duplex transmit and receive capability over single-balanced pair medium such as Unshielded Twisted Pair (UTP) cable. The LAN8670/1/2 is designed for use in applications requiring extended temperature range (-40°C to +125°C). The device is also compliant to industrial EMC and EMI requirements. The single power supply and simple analog front end simplifies its integration into small form factor applications.

The LAN8670/1/2 allows for the creation of both multidrop and point-to-point network topologies. Point-to-point link segments of up to at least 15m in length are supported. The multidrop mode supports up to at least 8 PHYs connected to a common mixing segment of up to at least 25m in length. The ability to connect multiple PHYs to a common mixing segment reduces weight and implementation costs by reducing cabling and switch ports.

The LAN8670/1/2 supports communication with an Ethernet MAC via standard MII/RMII interfaces. An integrated serial management interface (SMI) provides rapid register access and configuration at up to 4 MHz.

Access to the physical medium is managed by CSMA/CD and optionally supplemented by Physical Layer Collision Avoidance (PLCA).

The LAN8670/1/2 is designed to be used in functional safety related applications.

The Microchip LAN8670/1/2 family includes the following devices:

- LAN8670
- LAN8671
- LAN8672

Device specific features that do not pertain to the entire LAN8670/1/2 family are called out independently throughout this document. Table 2-1 below provides a summary of the feature differences between family members.

Table 2-1. LAN8670/1/2 Family Feature Matrix

Part Number	Package	MII Support	RMII Support	PLCA Support	-40^{O} to +125^{O}C
LAN8670	32-VQFN	X	X	X	X
LAN8671	24-VQFN		X	X	X
LAN8672	36-VQFN	X		X	X

A system-level block diagram and internal block diagram of the LAN8670/1/2 are shown in the following figures.

Figure 2-1. LAN8670/1/2 System-Level Block Diagram

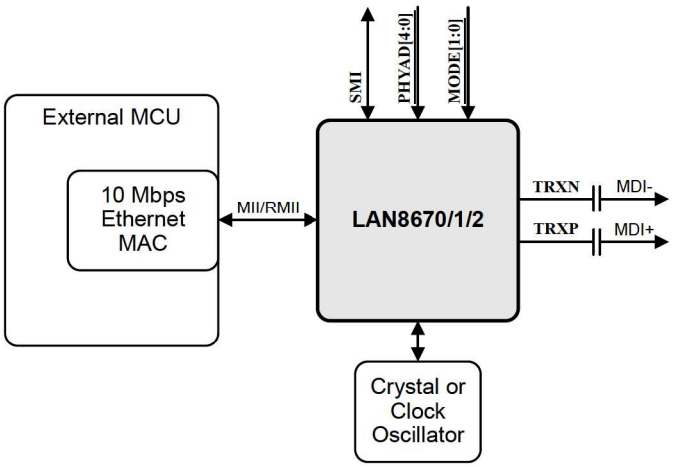
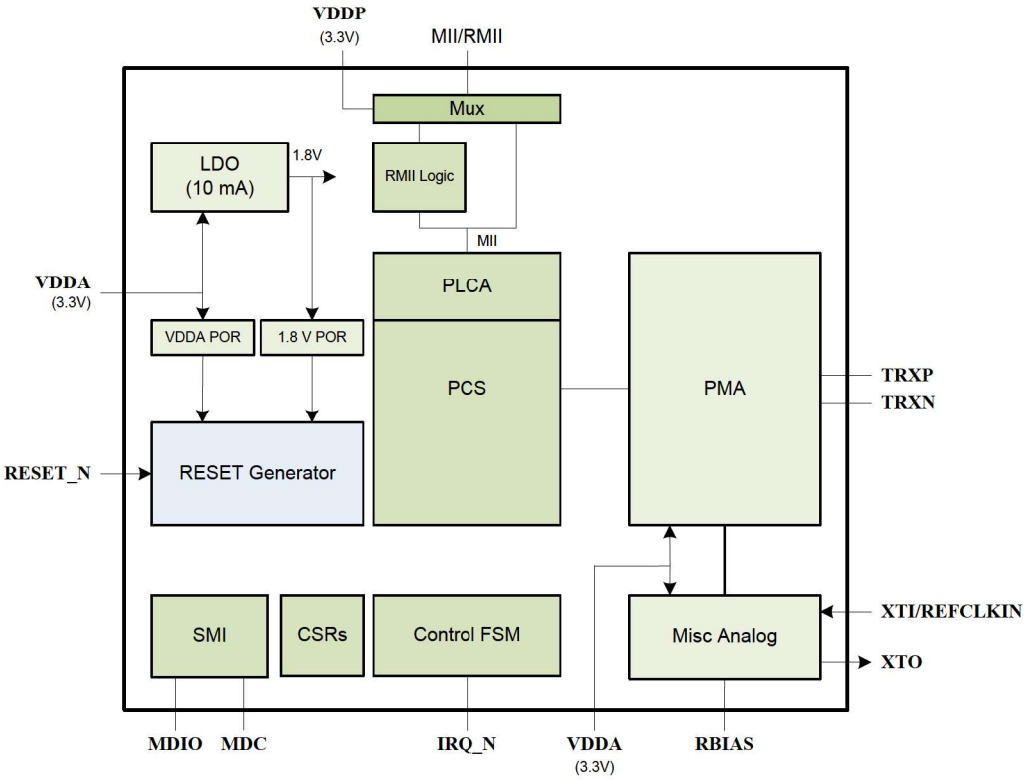


Figure 2-2. LAN8670/1/2 Internal Block Diagram



3. Pin Description and Configuration

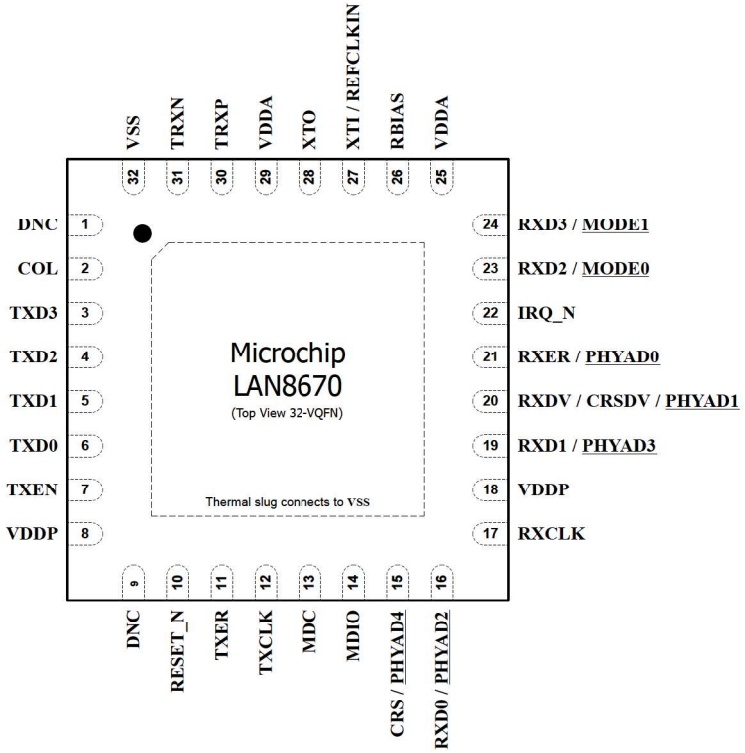
The pin assignments and descriptions for the LAN8670/1/2 are detailed in the following sections. Pin buffer type definitions are detailed in the Buffer Types section.

Related Links

1.2 Buffer Types

3.1 LAN8670 Pin Assignments

Figure 3-1. LAN8670 32-VQFN Pin Assignments



Note: Exposed pad (VSS) on bottom of package must be connected to ground.

Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor.

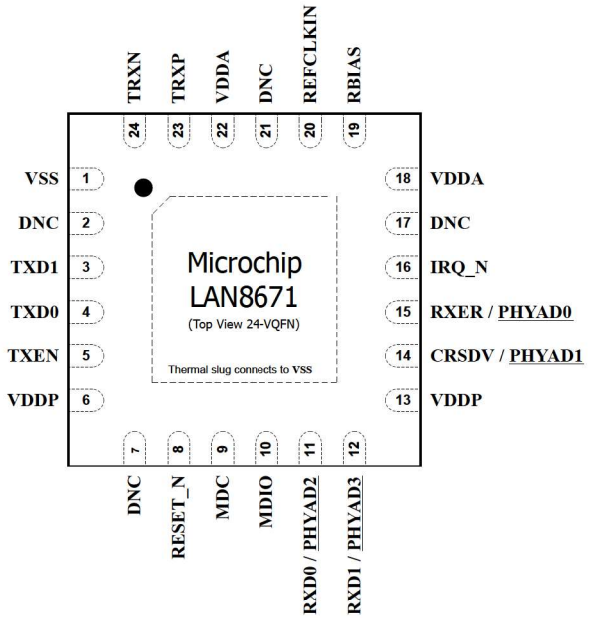
Table 3-1. LAN8670 32-VQFN Pin Assignments

Pin Num	Pin Name	Pin Num	Pin Name
1	DNC	17	RXCLK
2	COL	18	VDDP
3	TXD3	19	RXD1/PHYAD3
4	TXD2	20	RXDV/CRSDV/PHYAD1
5	TXD1	21	RXER/PHYAD0
6	TXD0	22	IRQ_N
7	TXEN	23	RXD2/MODE0
8	VDDP	24	RXD3/MODE1
9	DNC	25	VDDA
10	RESET_N	26	RBIAS
11	TXER	27	XTI/REFCLKIN
12	TXCLK	28	XTO
13	MDC	29	VDDA
14	MDIO	30	TRXP
15	CRS/PHYAD4	31	TRXN
16	RXD0/PHYAD2	32	VSS

Note: Exposed Pad (VSS) must be connected to ground.

3.2 LAN8671 Pin Assignments

Figure 3-2. LAN8671 24-VQFN Pin Assignments



Note: Exposed pad (VSS) on bottom of package must be connected to ground.

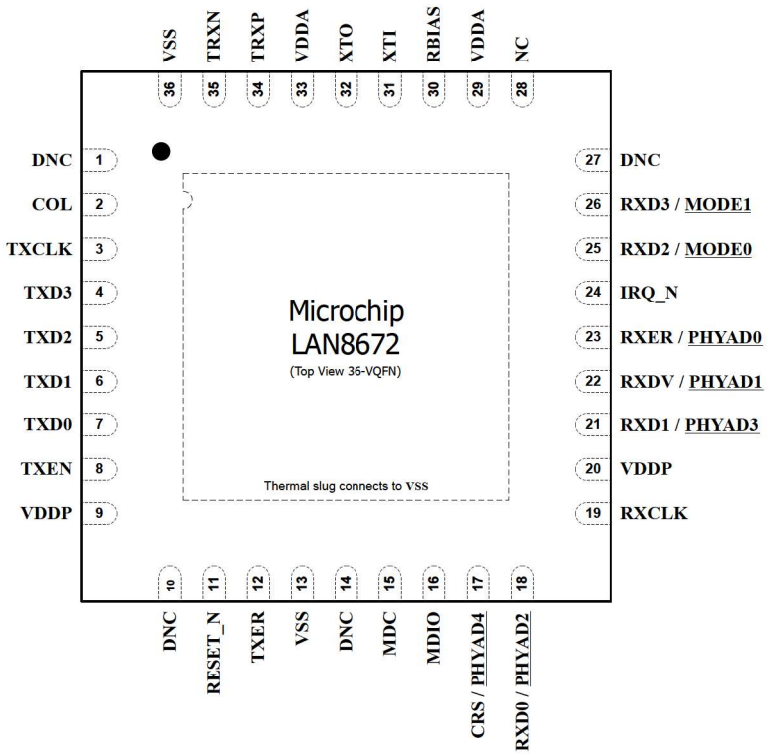
Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor.

Table 3-2. LAN8671 24-VQFN Pin Assignments

Pin Num	Pin Name	Pin Num	Pin Name
1	VSS	13	VDDP
2	DNC	14	CRSDV/PHYAD1
3	TXD1	15	RXER/PHYAD0
4	TXD0	16	IRQ_N
5	TXEN	17	DNC
6	VDDP	18	VDDA
7	DNC	19	RBIAS
8	RESET_N	20	REFCLKIN
9	MDC	21	DNC
10	MDIO	22	VDDA
11	RXD0/PHYAD2	23	TRXP
12	RXD1/PHYAD3	24	TRXN
Note: Exposed Pad (VSS) must be connected to ground.			

3.3 LAN8672 Pin Assignments

Figure 3-3. LAN8672 36-VQFN Pin Assignments



Note: Exposed pad (VSS) on bottom of package must be connected to ground.

Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor.

Table 3-3. LAN8672 36-VQFN Pin Assignments

Pin Num	Pin Name	Pin Num	Pin Name
1	DNC	19	RXCLK
2	COL	20	VDDP
3	TXCLK	21	RXD1/PHYAD3
4	TXD3	22	RXDV/PHYAD1
5	TXD2	23	RXER/PHYAD0
6	TXD1	24	IRQ_N
7	TXD0	25	RXD2/MODE0
8	TXEN	26	RXD3/MODE1
9	VDDP	27	DNC
10	DNC	28	NC
11	RESET_N	29	VDDA
12	TXER	30	RBIAS
13	VSS	31	XTI
14	DNC	32	XTO
15	MDC	33	VDDA
16	MDIO	34	TRXP
17	CRS/PHYAD4	35	TRXN
18	RXD0/PHYAD2	36	VSS

Note: Exposed Pad (VSS) must be connected to ground.

3.4 Pin Descriptions

This section contains descriptions of the various LAN8670/1/2 pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, RESET_N indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Pin buffer type definitions are detailed in the Buffer Types section.

Table 3-4. MII/RMII Signals

Name	Symbol	Buffer Type	Description
Transmit Data 0	TXD0	VIS-VDDP	Transmit data bus bit 0 (all modes)
Transmit Data 1	TXD1	VIS-VDDP	Transmit data bus bit 1 (all modes)
Transmit Data 2 (MII Mode)	TXD2	VIS-VDDP	Transmit data bus bit 2 (MII mode) In RMII mode, this signal is not used and is internally pulled-down to VSS.
Transmit Data 3 (MII Mode)	TXD3	VIS-VDDP	Transmit data bus bit 3 (MII mode) In RMII mode, this signal is not used and is internally pulled-down to VSS.
Transmit Error (MII Mode)	TXER	VIS-VDDP	This signal is asserted to indicate that an error was detected somewhere in the packet presently being transferred to the transceiver. This pin is unused in RMII mode and should be connected to VSS.
Transmit Enable	TXEN	VIS-VDDP	Indicates that valid transmission data is present on TXD[3:0]. In RMII mode, only TXD[1:0] provide valid data. **Note:** A pull-down resistor is recommended to prevent incidental transmission if the MAC does not actively pull-down or drive this pin low at all times during its reset and initialization.
Transmit Clock (MII Mode)	TXCLK	VO-VDDP	2.5 MHz clock used to latch data from the MAC into the transceiver. In RMII mode, this pin is unused and is driven low. It should be left unconnected.
Receive Data 0	RXD0	VOH-VDDP	Receive data bus bit 0 (all modes)
Receive Data 1	RXD1	VOH-VDDP	Receive data bus bit 1 (all modes)
Receive Data 2 (MII Mode)	RXD2	VO-VDDP	Receive data bus bit 2 (MII mode) In RMII mode, this pin is unused and is driven low.
Receive Data 3 (MII Mode)	RXD3	VO-VDDP	Receive data bus bit 3 (MII mode) In RMII mode, this pin is unused and is driven low.
Receive Error	RXER	VOH-VDDP	This signal is asserted to indicate that an error was detected somewhere in the packet presently being transferred from the transceiver. This signal is optional in RMII mode.

.....continued

Name	Symbol	Buffer Type	Description
Receive Data Valid (MII Mode)	RXDV	VOH-VDDP	Indicates that recovered and decoded data is available on the RXD[3:0] pins. This signal is not used in RMII mode.
Receive Clock (MII Mode)	RXCLK	VO-VDDP	In MII mode, this pin is the 2.5 MHz receive clock output. In RMII mode, this pin is unused and is driven low. It should be left unconnected.
Carrier Sense / Receive Data Valid (RMII Mode)	CRSDV	VOH-VDDP	This signal is asserted to indicate the receive medium is non-idle in RMII mode. This signal is not used in MII mode.
Collision Detect (MII Mode)	COL	VO-VDDP	Collision Detect. In RMII mode, this pin is unused and is driven low.
Carrier Sense (MII Mode)	CRS	VO-VDDP	Carrier Sense. In RMII mode, this pin is unused and is driven low.

Table 3-5. Ethernet Transceiver Pins

Name	Symbol	Buffer Type	Description
Ethernet TX/RX Positive Terminal	TRXP	AIO	Positive terminal for transmit/receive signal.
Ethernet TX/RX Negative Terminal	TRXN	AIO	Negative terminal for transmit/receive signal.

Table 3-6. Serial Management Interface (SMI) Pins

Name	Symbol	Buffer Type	Description
SMI Data Input/Output	MDIO	VIS-VDDP / VO-VDDP	Serial Management Interface data input/output.
SMI Clock	MDC	VIS VDDP	Serial Management Interface clock.

Table 3-7. Miscellaneous Pins

Name	Symbol	Buffer Type	Description
External 25 MHz Crystal Input	XTI	ICLK	External 25 MHz crystal input.
External Clock Input	REFCLKIN	ICLK	Single-ended clock oscillator input. A frequency of 25 MHz shall be used in all modes except RMII, which requires 50 MHz. **Note:** When using a single-ended clock oscillator, XTO must be left unconnected with <10 pF stray capacitance.
External 25 MHz Crystal Output	XTO	OCLK	External 25 MHz crystal output. **Note:** When using a single-ended clock oscillator on XTI/REFCLKIN, this pin must be left unconnected with <10 pF stray capacitance.
Interrupt	IRQ_N	VOD-VDDP	Device interrupt. Active low and open drain. **Note:** When used, this pin requires a 10 kΩ (typical) pull-up to VDDP. **Note:** This pin is to be unconnected when unused.
System Reset	RESET_N	VIS-VDDP	System reset. This pin is active low. If unused, this pin must be pulled-up to VDDP.

.....continued			
Name	**Symbol**	**Buffer Type**	**Description**
Bias Resistor	RBIAS	AIO	External bias resistor connection pin. This pin requires connection of a 12.4 kΩ resistor to ground. **Note:** The resistor must be within ± 1% tolerance across the entire expected operating temperature range.
Do Not Connect	DNC	-	Pin is internally connected. The pin must be left floating externally.
No Connect	NC	-	Pin is not connected internally. The pin should be left floating externally.

Table 3-8. Configuration Straps

Name	Symbol	Buffer Type	Description
Operating Mode Configuration Straps 1-0	MODE[1:0]	VIS-VDDP	These configuration straps are used to select the device's default mode of operation. See Section 3.5, Configuration Straps for additional information.
PHY Address Configuration Straps 4-0	PHYAD[4:0]	VIS-VDDP	These configuration straps are used to select the device's default PHY SMI address. See Section 3.5, Configuration Straps for additional information.

Table 3-9. Power Pins

Name	Symbol	Buffer Type	Description
+3.3V Switched I/O Power Supply Input	VDDP	P	+3.3V switched I/O power supply input.
+3.3V Switched Analog Power Supply Input	VDDA	P	+3.3V switched analog power supply input.
Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

3.5 Configuration Straps

Configuration straps allow various features of the device to be automatically configured to user defined values. Configuration straps are identified by an underlined symbol name in the pin assignment lists and are latched on Power-On Reset (POR) and pin reset (RESET_N). Configuration straps do not have internal resistors to prevent the signal from floating when unconnected.

Important: External pull-up or pull-down resistors must be sized appropriately (10 kΩ, typical) to ensure that the configuration straps reach the required voltage level prior to latching at reset.

3.5.1 Device Mode (MODE[1:0])

The MODE[1:0] configuration straps control various device modes. When the RESET_N pin is negated, the associated register bit values are loaded according to the MODE[1:0] configuration straps and the device is configured. When a soft reset occurs via the Soft Reset bit of the Basic Control Register, the configuration of the device is controlled by the register bit values and the MODE[1:0] configuration straps have no affect.

The device's mode may be configured using the hardware configuration straps as summarized in Table 3-10 below.

Note: As the LAN8672 only supports operation in MII mode, the MODE[1:0] configuration straps must be set to 01b.

Table 3-10. MODE[1:0] Configuration Straps

MODE[1:0]	Definition
00b	Reserved
01b	PHY is placed in MII mode with 25 MHz crystal
10b	PHY is placed in RMII mode with 50 MHz REFCLKIN
11b	Reserved

3.5.2 PHY Address (PHYAD[4:0])

The PHYAD[4:0] configuration straps are driven high or low to give each PHY a unique SMI address. This address is latched into an internal register at the end of a hardware reset. In a multi-transceiver application (such as a switch), the controller is able to manage each transceiver via the unique address. Each transceiver checks each management data frame for a matching address in the relevant bits. When a match is recognized, the transceiver responds to that particular frame.

The LAN8670/2 SMI address must be configured using the PHYAD[4:0] hardware configuration straps to any value between 0x00 and 0x1F. The LAN8671 SMI address must be configured using the PHYAD[3:0] hardware configuration straps to any value between 0x00 and 0x0F.

4. Functional Descriptions

4.1 Media Independent Interface (MII)

The integrated Media Independent Interface (MII) provides a common interface between physical layer and MAC layer devices, adhering to IEEE Std 802.3-2018 *IEEE Standard for Ethernet*.

The MII includes the following interface signals:

- Transmit Data - TXD[3:0]
- Transmit Enable - TXEN
- Transmit Clock - TXCLK
- Transmit Error - TXER
- Receive Data - RXD[3:0]
- Receive Data Valid - RXDV
- Receive Clock - RXCLK
- Receive Error - RXER
- Carrier Sense - CRS
- Collision Detect - COL

In MII mode, on the transmit path, the transceiver drives the transmit clock, TXCLK, to the controller. The controller synchronizes the transmit data to the rising edge of TXCLK and drives TXEN high to indicate valid transmit data on TXD[3:0]. The transceiver will synchronously capture TXEN, TXER, and TXD[3:0] on the falling edge of TXCLK.

On the receive path, the transceiver drives both the receive data, RXD[3:0], and the receive clock, RXCLK. The controller captures in the receive data on the rising edge of RXCLK when the transceiver drives RXDV high. The transceiver drives RXER high when a receive error is detected (e.g., an uncorrectable decoding error). The transceiver synchronizes RXD[3:0], RXDV, and RXER to change on the falling edge of RXCLK.

The CRS and COL signals are asserted asynchronously to the clocks.

For timing information, refer to the MII Timing section. Refer to Clause 22 of the IEEE Std 802.3-2018 IEEE Standard for Ethernet specification for additional MII information.

Note: Many modern controllers, often found on switches, implement a reduced pin MII assuming full-duplex point-to-point operation. These interfaces, known as MII-Lite, do not include the required CRS and COL signals for 10BASE-T1S half-duplex operation. Back-to-back connection of two half-duplex transceivers is also not supported due to the CRS and COL requirement.

Note: The connection of a 10 kΩ pull-down resistor on TXEN is recommended to prevent incidental transmission if the MAC does not actively pull-down or drive this pin low at all times during its reset and initialization.

Related Links

7.6.6 MII Timing

4.2 Reduced Media Independent Interface (RMII)

The integrated Reduced Media Independent Interface (RMII) provides a common low pin count interface between the physical layer and MAC layer devices, adhering to the RMII Specification Revision 1.2. RMII reduces the pin count of MII while retaining a serial management interface (MDIO/MDC) identical to MII. PLCA is fully supported through the RMII.

The RMII has the following characteristics:

- A single 50 MHz clock reference is used for both transmit and receive
- It provides independent 2-bit (di-bit) wide transmit and receive data paths

The RMII includes the following interface signals:

- Transmit Data - TXD[1:0]
- Transmit Enable - TXEN
- Receive Data - RXD[1:0]
- Receive Error - RXER
- Carrier Sense / Data Valid - CRSDV

For timing information, refer to the RMII Timing section. Refer to the RMII Specification Revision 1.2 for additional information.

When operating in RMII mode, the LAN8670/1 REFCLKIN pin must be connected to a 50 MHz reference clock source. This clock source may be driven by the MAC or from a common oscillator driving both the MAC and LAN8670/1. When a common oscillator is utilized, it is recommended to match the length of the PCB traces from the source to the LAN8670/1 and MAC to within 0.5 inches (13 mm). Care should be taken when laying out the board to prevent the LAN8670/1 clock from becoming a victim of crosstalk as any noise introduced to the clock input of the LAN8670/1 could become radiated onto the network.

The CRSDV pin combines both carrier sense and receive data valid. On carrier sense, the CRSDV pin is asserted asynchronously to the 50 MHz reference clock. Thereafter, CRSDV is only negated synchronously to the reference clock. Carrier sense is indicated by the assertion of CRSDV during which the first di-bit of a data nibble is presented on RXD[1:0]. Similarly, receive data valid is indicated by the assertion of CRSDV when the second di-bit of a data nibble is presented on RXD[1:0]. See the RMII Specification Revision 1.2.

A collision is signaled on RMII by the assertion of carrier sense when the MAC is asserting TXEN. A half-duplex RMII MAC must be able to properly derive the collision indication from CRSDV and TXEN.

Note: The connection of a 10 kΩ pull-down resistor on TXEN is recommended to prevent incidental transmission if the MAC does not actively pull-down or drive this pin low at all times during its reset and initialization.

Related Links

7.6.7 RMII Timing

4.3 Serial Management Interface (SMI)

The Serial Management Interface (SMI) is used to control the device and obtain its status. This interface supports the standard PHY registers required by Clause 22 of IEEE Std 802.3, as well as “vendor-specific” registers allowed by the specification. Unimplemented registers will be read as hexadecimal “0000”. Device registers are detailed in the Register Descriptions section.

At the system level, SMI provides two signals: MDIO and MDC. The MDC signal is an aperiodic clock provided by the station management entity (STA). MDIO is a bi-directional data SMI input/output signal that receives serial data (commands) from the STA and sends serial data (status) to the STA. The minimum time between edges of the MDC is 100 ns. There is no maximum time between edges. The minimum cycle time (i.e., the time between two consecutive rising or two consecutive falling edges) is 250 ns. These modest timing requirements allow this interface to be easily driven by the I/O port of a microcontroller.

The data on the MDIO line is latched on the rising edge of the MDC. The management frame structure and timing is shown in the following figures. The timing relationships of the MDIO signals are further described in the SMI Timing section of the Operational Characteristics AC Specifications.

Figure 4-1. SMI Timing and Frame Structure - READ Cycle

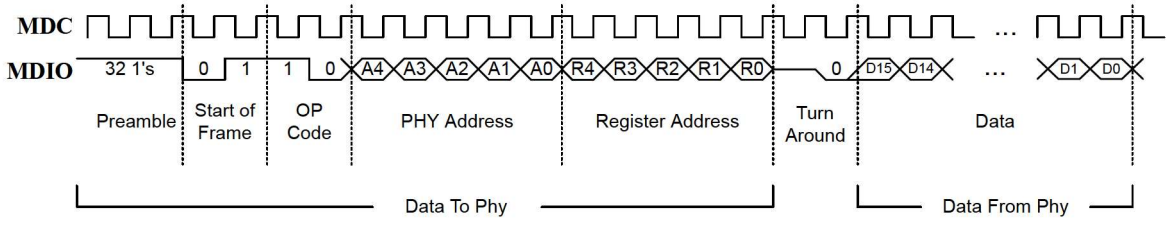
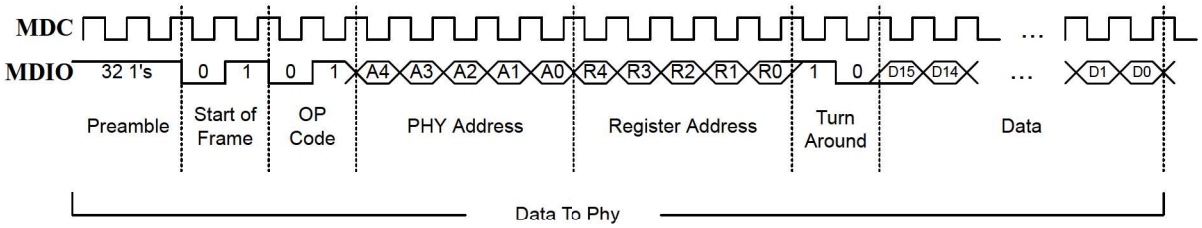


Figure 4-2. SMI Timing and Frame Structure - WRITE Cycle



Related Links

5. Register Descriptions

7.6.8 SMI Timing

4.3.1 Clause 45 Register Access

The LAN8670/1/2 only supports the MDIO management frame protocol defined in IEEE Std 802.3 Clause 22. Registers mapped into IEEE Std 802.3 Clause 45 MDIO Managed Devices (MMD) are accessed indirectly through the MMD Access Control (MMDCTRL) and MMD Access Address/Data (MMDAD) registers as described in IEEE Std 802.3 Annex 22D.

MMD Register Read

The following process is used to indirectly read Clause 45 registers using the Clause 22 access mechanism.

1. Write the MMD Access Control register with the MMD Function (FNCTN) field set to `00b` and the Device Address (DEVID) field with the MDIO Management Device (MMD) address.
2. Write the address of the desired register to be read into the MMD Access Address/Data register.
3. Write the MMD Access Control register with the MMD Function field set to `01b`, `10b`, or `11b`.
4. Read the contents of the MMD's selected register from the MMD Access Address/Data register.

Subsequent reads from the MMD Access Address/Data register will continue to reread and return the value of the selected MMD register when the MMD Function field is set to `01b` or `11b`. When the MMD Function field is set to `10b`, the MMD register address will be incremented following every read causing subsequent reads from the MMD Access Address/Data register to return data from the next higher MMD register.

MMD Register Write

The following process is used to indirectly write Clause 45 registers using the Clause 22 access mechanism.

1. Write the MMD Access Control register with the MMD Function (FNCTN) field set to `00b` and the Device Address (DEVID) field with the MDIO Management Device (MMD) address.
2. Write the address of the desired register to be written into the MMD Access Address/Data register.
3. Write the MMD Access Control register with the MMD Function field set to `01b`, `10b`, or `11b`.

Subsequent writes to the MMD Access Address/Data register will continue to write to the selected MMD register when the MMD Function field is set to `01b`. When the MMD Function field is set to `10b` or `11b`, the MMD register address will be incremented following every write causing subsequent writes to the MMD Access Address/Data register to write data to the next higher MMD register.

Related Links

5.1.5 MMDCTRL

5.1.6 MMDAD

4.4 Interrupt Management

The LAN8670/1/2 supports multiple interrupt capabilities which are not part of the IEEE 802.3 specification. An active low asynchronous interrupt signal may be generated on the IRQ_N pin when selected status events are detected as configured by the Interrupt Mask Registers.

To assert an interrupt for a given event in the Status 1 (STS1) and Status 2 (STS2) registers, the corresponding mask bit in the Interrupt Mask 1 (IMASK1) and Interrupt Mask 2 (IMSK2) registers must be written to '0' to enable the interrupt. When the associated event occurs setting the status bit, the IRQ_N pin will also be asserted. When the event to negate the status bit is true, or the corresponding bit in the Interrupt Mask Register is set disabling the interrupt, the IRQ_N pin will be deasserted.

All interrupts are disabled (masked) following a reset with the exception of the Reset Complete interrupt mask bit. The Reset Complete interrupt mask is '0' by default such that the IRQ_N pin will be asserted following a reset event setting the Reset Complete status bit. This may be used to alert the station management entity that the LAN8670/1/2 has been reset and is available for configuration.

Related Links

5.4.2 STS1
5.4.3 STS2
5.4.5 IMSK1
5.4.6 IMSK2

4.5 Resets

The device provides the chip-level reset sources described in the following sections.

4.5.1 Power-On Reset (POR)

A Power-On Reset occurs whenever power is initially applied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset for approximately 2 ms. Configuration straps are loaded by this reset and must adhere to the timing requirements specified in Power-On Configuration Strap Timing when not using the external pin reset (RESET_N).

After power-on, the POR initially negates after the rising threshold is passed. In the event that the supply drops below the falling threshold, the POR asserts. The POR stays asserted until the rising threshold is once again crossed. The rising and falling thresholds are listed in Table 4-1.

Table 4-1. POR Supply Thresholds

POR	Rising Threshold[1]	Falling Threshold[1]
VDDA	2.5V	2.4V
1.8V[2]	1.6V	1.3V

Notes:
1. Rising and falling threshold voltages are design parameters and are neither tested nor characterized.
2. The internal 1.8V supply cannot be monitored externally.

Related Links

7.6.3 Power-On Configuration Strap Timing

4.5.2 External Pin Reset (RESET_N)

A hardware reset will occur when the RESET_N pin is asserted. The RESET_N pin must be connected externally to VDDP if unused. If used, the RESET_N pin must be driven for a minimum period as defined in the RESET_N Configuration Strap Timing section. Configuration straps are loaded by the reset.

Related Links

7.6.4 RESET_N Configuration Strap Timing

4.5.3 Software Reset

The software reset is available via the PHY Soft Reset (SW_RESET) bit in the Basic Control register.

Configuration straps are not loaded by a software reset.

Related Links
5.1.1 BASIC_CONTROL

4.6 Power Management

A summary of the device's available power states is provided in the table below.

Table 4-2. Power Management States

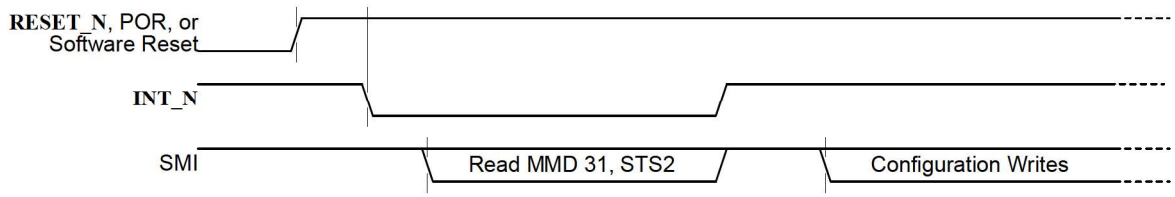
State	Description
RESET	• The device is in this state when the RESET_N pin is asserted
ACTIVE	• The device is fully active

4.7 Initialization

When the device is in a reset state, the IRQ_N interrupt pin is high-impedance and will be pulled high through an external pull-up resistor. Once all device reset sources are deasserted, the device will begin its internal initialization. The device will assert the Reset Complete (RESETC) bit in the Status 2 (STS2) register to indicate that it has completed its internal initialization and is ready for configuration. As the Reset Complete status is non-maskable, the IRQ_N pin will always be asserted and driven low following a device reset.

At the system level, the station management entity should respond to all assertions of the IRQ_N pin with a read of critical status registers through the Serial Management Interface (SMI), including the Status 2 register. Upon reading of the Status 2 register, the pending Reset Complete status bit will be automatically cleared causing the IRQ_N pin to be released and pulled high again. The station management entity may then continue to configure the device registers through the Serial Management Interface. See Figure 4-3 for an illustration of the device reset, initialization, and configuration process.

Figure 4-3. Initialization and Configuration Sequence



Related Links
5.4.3 STS2
4.5 Resets

4.8 Clock Manager

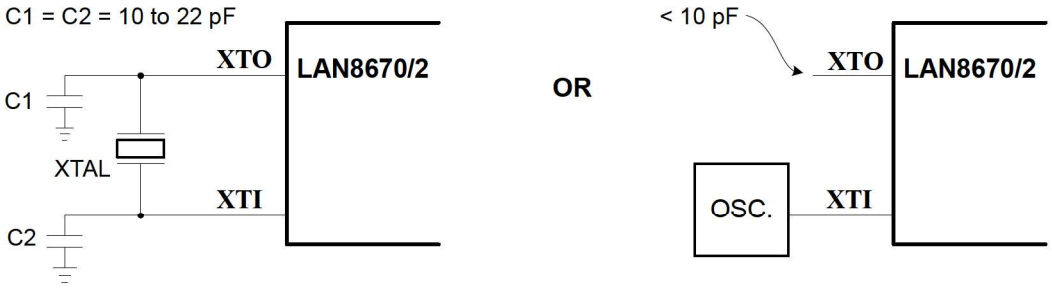
The Clock Manager generates the internal clocks from an external reference source.

4.8.1 Crystal Pins (XTI/XTO)

The XTI and XTO crystal oscillator pins are used to connect a 25.0 MHz clock source for MII operation. The crystal oscillator should be in a fundamental, parallel resonant mode. Figure 4-4 depicts the external circuitry connected to the LAN8670/1/2 oscillator circuit. Since the internal inverter/amplifier is operated in its linear region, external series resistors should not be used as they will lower the gain and could cause start-up problems. Several factors must be considered when selecting a crystal including load capacitance, oscillator margin, cut, and operating temperature. The crystal frequency must be 25.0 MHz.

If an external clock oscillator is used in lieu of a crystal oscillator, it must be connected to the XTI pin. The clock must be stable prior to the negation of reset and remain stable for proper operation. In addition, the XTO pin should float and have minimal capacitance (see Figure 4-4).

Figure 4-4. Crystal Oscillator Input



Related Links

6.4 Crystal Oscillator Selection

7.8.1 Crystal Specifications

4.8.2 Reference Clock (REFCLKIN)

The REFCLKIN pin is used to connect an external 50.0 MHz reference clock source for RMII operation. The clock source must be stable prior to the negation of reset and remain stable for proper operation. In addition, the LAN8670 XTO pin should float and have minimal capacitance (<10 pF).

Reference clock requirements are found in the RMII REFCLKIN Requirements section.

Related Links

7.8.2 RMII REFCLKIN Requirements

4.9 Physical Layer Collision Avoidance (PLCA)

PLCA operates in conjunction with a CSMA/CD MAC to actively avoid collisions among half-duplex stations (known as PLCA *nodes*) allowing for greater network utilization. Each node on the network segment (i.e., collision domain) is assigned a unique *Local ID*. *Transmit opportunities* are then granted to each node in sequence based on their Local ID. The node configured as Local ID = 0 is known as the *PLCA coordinator*. The role of the PLCA coordinator is to transmit a periodic synchronizing BEACON onto the physical media. All other nodes are referred to as a *PLCA follower* as they follow the synchronization of the coordinator. Once the BEACON has been received on the segment, all nodes begin counting transmit opportunities beginning with zero. Nodes detect their assigned transmit opportunity by counting the number of opportunities that have passed since the transmission of the BEACON by the PLCA coordinator. Each node may transmit when the number of transmit opportunities counted since the BEACON matches the Local ID assigned to the node. Within each transmit opportunity, the node assigned the current opportunity may either transmit a packet or yield. Once the node has transmitted a packet (or yielded), each node increments the transmit opportunity counter and the transmit opportunity goes to the next node. The first transmit opportunity of zero allows node with Local ID = 0 to transmit. Once a fixed number of transmit opportunities has been provided, the PLCA coordinator will transmit another BEACON starting the cycle over again. A BEACON followed by a fixed number of transmit opportunities is known as a *PLCA bus cycle*.

On multidrop topologies with multiple nodes connected to a shared media mixing segment, PLCA enables a fairness in opportunity to transmit such that one node cannot transmit more than one frame without each of the other nodes also being granted an opportunity to transmit. An exception to this is that PLCA also allows individual nodes, if desired within the engineered network segment, to be configured to transmit a burst of frames within a single transmit opportunity.

PLCA is enabled by setting the PLCA Enable bit in the PLCA Control 0 (PLCA_CTRL0) register. The node Local ID is configured within the PLCA Local ID (ID) field of the PLCA Control 1 (PLCA_CTRL1) register and must be unique within the PLCA network segment to successfully avoid collisions. Additionally, the Local ID must be less than the number of transmit opportunities in each bus cycle in order to be granted a transmit opportunity (see the Node Count field of the PLCA Control 1 register). When the node is configured as the PLCA coordinator, then the number of transmit opportunities within each PLCA bus cycle (period between successive BEACON transmissions) is configured in the Node Count (NCNT) field of the PLCA Control 1 register.

The time for each transmit opportunity is configured within the PLCA Transmit Opportunity Timer (PLCA_TOTMR) register. The transmit opportunity timer must be set equal among all nodes in the PLCA collision domain to maintain

synchronization among the nodes. The default transmit opportunity timer value is appropriate for segments specified in IEEE 802.3 Clause 147 and should only be changed in special circumstances.

When PLCA has been enabled on a node, the PLCA Status bit in the PLCA Status (PLCA_STS) register will indicate if the node is actively receiving a periodic PLCA BEACON. This may be useful for diagnosing a misbehaving PLCA network segment.

Related Links

4.9.1 PLCA Burst Mode
5.4.14 PLCA_CTRL0
5.4.15 PLCA_CTRL1
5.4.17 PLCA_TOTMR
5.4.16 PLCA_STS

4.9.1 PLCA Burst Mode

Some applications, such as sensors or audio, may require the transmission of frequent small frames with a limited latency. As PLCA enables only one transmit opportunity for each node in each bus cycle, these applications may experience significant latency when they are connected onto a multidrop mixing segment with applications that transmit large packets. For example, an audio application may require the transmission of eight stereo 16-bit audio samples as 64 byte packets every 167 µs with minimal latency. When another node on the segment transmits a 1500 byte packet it will occupy the channel for 1.2 ms. The audio application will therefore buffer seven audio packets during the time that the channel is occupied. With standard PLCA, the audio application will only be able to transmit one of its audio packets during the next PLCA bus cycle. The result is that each successive audio packet the audio application needs to transmit is delayed with increasing latency.

One solution to this problem is to allow specific nodes to transmit more than one packet during its transmit opportunity. This ability to transmit a burst of multiple packet allows the audio application in the above example to empty its buffers and transmit all audio packets that it has queued, preventing the latency of the audio packets to grow beyond a tolerable limit.

The ability to transmit packets in a burst is configurable individually for each node on the segment. The Maximum Burst Count (MAXBC) field in the PLCA Burst Mode (PLCA_BURST) register configures the maximum number of additional packets allowed to transmit in each of the node's transmit opportunities. This is in addition to the initial packet that may be transmitted by the node in its transmit opportunity. Additionally, the Burst Timer (BTMR) field configures the amount of time the node may transmit (COMMIT) to maintain a hold on its current transmit opportunity after transmitting a packet to allow the MAC to transmit an additional packet. Once this timer expires, the node will then yield the transmit opportunity to the next node.

Related Links

5.4.18 PLCA_BURST

4.9.2 Physical Layer Collision Avoidance (PLCA) Diagnostics

The LAN8670/1/2 PHY implements a number of features useful to the detection of PLCA misconfiguration on the network segment. These features include error status indications and event counters.

The PLCA error status indicators are located in the Status 1 (STS1) register. Each indication also has an associated interrupt mask bit in the Interrupt Mask 1 (IMSK1) register to enable an assertion on the IRQ_N interrupt pin when the event is detected.

Each node of a PLCA segment must be assigned a unique node ID to properly avoid collisions. The device has the ability to detect that another node is assigned the same Local ID by detecting the reception of a packet from the network during its assigned transmit opportunity. When this condition occurs, the Receive in Transmit Opportunity (RXINTO) status bit is set. Additionally, should a collision be detected while the device is transmitting in its assigned transmit opportunity, the Transmit Collision (TXCOL) status bit will be set.

Multiple nodes configured and acting as PLCA Coordinators also cause problems. Multiple Coordinators on the mixing segment will each transmit a BEACON according to its own PLCA bus cycle and timing. The result is that each Coordinator will receive BEACONs that it did not transmit. When configured as a PLCA Coordinator, it will set the Unexpected BEACON Received (UNEXPB) status bit to indicate the presence of another Coordinator on the network segment.

The PLCA Coordinator must be configured with the correct number of nodes on the segment to permit the proper number of transmit opportunities per bus cycle. If the Coordinator is configured to allow for too few transmit opportunities between BEACONs, Follower nodes may not receive their assigned transmit opportunity. When the device is operating as a PLCA Follower, if it detects a BEACON before its assigned transmit opportunity occurs then the BEACON Received Before Transmit Opportunity (BCNBFTO) status bit is set to indicate that the configured PLCA bus cycle is too small to allow the Follower to transmit.

When configured as a PLCA Follower, the PLCA Status (PST) bit in the PLCA Status (PLCA_STS) register will be set as long as BEACONs are regularly being received from a Coordinator. If BEACONs are not received by the device it will continue incrementing its transmit opportunity counter. When the transmit opportunity counter reaches the maximum count of 255, it will then stop incrementing and a 13 ms timer started. If no BEACON is received after the timer expires, the PLCA Status bit will be cleared. When the PLCA Status bit is zero, the device will revert to CSMA/CD operation with PLCA deactivated. Once a BEACON is received the device will set the PLCA Status bit and return to normal PLCA operation. Refer to Clause 148 of the IEEE 802.3cg specification for additional details.

Note: The PLCA Status (PST) bit cannot generate an interrupt assertion on the IRQ_N pin and must therefore be polled by reading the PLCA Status (PLCA_STS) register.

Two event counters are implemented to aid the station controller in monitoring PLCA on the segment. These counters include a transmit opportunity counter and a BEACON counter. Each counter is enabled by setting the corresponding enable bit in the Counter Control (CTRCTRL) register. Writing a '1' to the Transmit Opportunity Counter Enable (TOCTRE) bit enables the transmit opportunity counter. The BEACON Counter Enable (BCNCTRE) bit enables the BEACON counter when set.

When enabled, the Transmit Opportunity Count High/Low (TOCNTH/TOCNTL) registers will contain the number of transmit opportunities the local PHY could have used to transmit since the last read. By polling the counter, the station controller can monitor that PLCA is active and that the PHY can transmit packets when needed.

Similarly, the BEACON Count High/Low (BCNCNTH/BCNCNTL) register contains the number of received BEACONs since the last read. The station controller can poll this counter to monitor the health of the PLCA Coordinator.

Related Links

5.4.2 STS1
5.4.5 IMSK1
5.4.16 PLCA_STS
5.4.7 CTRCTRL
5.4.8 TOCNTH
5.4.9 TOCNTL
5.4.10 BCNCNTH
5.4.11 BCNCNTL

5. Register Descriptions

This chapter describes the various device registers, which are categorized as follows:

- SMI Basic Control and Status Registers (Clause 22)
- PMA/PMD Registers (MMD 1)
- PCS Registers (MMD 3)
- Miscellaneous Registers (MMD 31)

For details on register bit attribute notation, refer to the section Register Bit Types.

Related Links

1.3 Register Bit Types

5.1 SMI Basic Control and Status Registers

The section describes the various SMI Control and Status Registers (CSRs). The SMI CSRs follow the IEEE 802.3 (Clause 22.2.4) management register set. All functionality and bit definitions comply with these standards.

⚠WARNING RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in adverse operation and unexpected results.

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	BASIC_CONTROL	15:8	SW_RESET	LOOPBACK	SPD_SEL[0]	AUTO_NEG_EN	PD	ISOLATE	RE_AUTO_NEG	DUPLEX_MODE
		7:0	COL_TEST	SPD_SEL[1]						
0x01	BASIC_STATUS	15:8	100BASE-T4	100BASE-TX Full Duplex	100BASE-TX Half Duplex	10BASE-T Full Duplex	10BASE-T Half Duplex	100BASE-T2 Full Duplex	100BASE-T2 Half Duplex	Extended Status
		7:0		MF_PRE_SUP	AUTO_NEG_COMP	RMT_FAULT	AUTO_NEG	LINK_STAT	JAB_DET	EXT_CAP
0x02	PHY_ID0	15:8	OUI[2:9]							
		7:0	OUI[10:17]							
0x03	PHY_ID1	15:8	OUI[18:23]						MODEL[5:4]	
		7:0	MODEL[3:0]				REV[3:0]			
0x05 ... 0x0C	Reserved									
0x0D	MMDCTRL	15:8	FNCTN[1:0]							
		7:0				DEVAD[4:0]				
0x0E	MMDAD	15:8	ADR_DATA[15:8]							
		7:0	ADR_DATA[7:0]							
0x10 ... 0x11	Reserved									
0x12	STRAP_CTRL0	15:8								MITYP[1]
		7:0	MITYP[0]	PKGTYP[1:0]		SMIADR[4:0]				

5.1.1 Basic Control

Name: BASIC_CONTROL
Address: 0x00

Clause 22 Basic Control Register

Bit	15	14	13	12	11	10	9	8
	SW_RESET	LOOPBACK	SPD_SEL[0]	AUTO_NEG_EN	PD	ISOLATE	RE_AUTO_NEG	DUPLEX_MODE
Access	R/W SC	R/W	RO	RO	R/W	R/W	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COL_TEST	SPD_SEL[1]						
Access	R/W	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – SW_RESET PHY Soft Reset
Writing a '1' to this bit will initiate a software reset of the PHY. A software reset will restore all registers to their default state, except for those fields identified as "NASR".
Note: This bit is self-clearing. When setting this bit, do not set other bits in this register.

Value	Description
0	Normal operation
1	PHY software reset

Bit 14 – LOOPBACK Near-End Loopback
When set, this bit enables a Near-End Loopback. When enabled, transmit data (TXD) pins from the MAC will be looped back onto the receive data (RXD) pins to the MAC. In this mode, no signal is transmitted onto the network media.

Value	Description
0	Normal operation
1	Enable near-end loopback mode

Bit 13 – SPD_SEL[0] PHY Speed Select
Together with SPD_SEL[1], sets the network communication speed.
Note: Only 10 Mbit/s is supported. This bit is always '0'.

Value	Description
00	10 Mbit/s
01	100 Mbit/s
10	1000 Mbit/s
11	Reserved

Bit 12 – AUTO_NEG_EN Auto-Negotiation Enable
Note: Auto-negotiation is not supported. This bit is always '0'.

Value	Description
0	Disable auto-negotiate process
1	Enable auto-negotiate process

Bit 11 – PD Power Down
Setting this bit will power down the PMA transceiver leaving the remainder of the device functional.
Note: This bit is the same as the Low Power Enable bit in the 10BASE-T1S PMA Control register.

Value	Description
0	Normal operation
1	PMA is powered down

Bit 10 – ISOLATE Electrical isolation of PHY from MII/RMII
When this bit is set, the PHY will electrically isolate its data paths from the MII/RMII.

Value	Description
0	Normal operation (PHY is not electrically isolated from MII/RMII)
1	Electrical isolation of PHY from MII/RMII

Bit 9 – RE_AUTO_NEG Restart Auto-Negotiation
Note: Auto-negotiation is not supported. This bit is always '0'.

Value	Description
0	Normal operation
1	Restart auto-negotiate process

Bit 8 – DUPLEX_MODE Duplex Mode
This bit configures the PHY for full-duplex or half-duplex network communication.
Note: Only half duplex operation is supported. This bit is always '0'.

Value	Description
0	Half duplex
1	Full duplex

Bit 7 – COL_TEST Collision Test
When the Near-End Loopback is enabled (LOOPBACK), setting this bit will allow the COL pin to be tested. When the Collision Test is enabled, asserting TXEN will cause the COL output to go high within 512 bit times. Negating TXEN will cause the COL output to go low within 4 bit times. The Collision Test should only be enabled when Near-End Loopback is enabled.

Value	Description
0	Normal operation. Collision test is disabled.
1	Enable collision test

Bit 6 – SPD_SEL[1] PHY Speed Select
See description for SPD_SEL[0] for details.
Note: Only 10 Mbit/s operation is supported. This bit is always '0'.

5.1.2 Basic Status

Name: BASIC_STATUS
Address: 0x01

Clause 22 Basic Status Register

Bit	15	14	13	12	11	10	9	8
	100BASE-T4	100BASE-TX Full Duplex	100BASE-TX Half Duplex	10BASE-T Full Duplex	10BASE-T Half Duplex	100BASE-T2 Full Duplex	100BASE-T2 Half Duplex	Extended Status
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
		MF_PRE_SUP	AUTO_NEG_COMP	RMT_FAULT	AUTO_NEG	LINK_STAT	JAB_DET	EXT_CAP
Access	RO	RO	RO	RO	RO	RO	RC	RO
Reset	1	0	0	0	0	1	0	1

Bit 15 – 100BASE-T4 100BASE-T4 Ability
Note: 100BASE-T4 operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 100BASE-T4
1	PHY able to operate at 100BASE-T4

Bit 14 – 100BASE-TX Full Duplex 100BASE-TX Full Duplex Ability
Note: 100BASE-TX operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to perform Full-Duplex 100BASE-TX
1	PHY able to perform Full-Duplex 100BASE-TX

Bit 13 – 100BASE-TX Half Duplex 100BASE-TX Half Duplex Ability
Note: 100BASE-TX operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to perform Half-Duplex 100BASE-TX
1	PHY able to perform Half-Duplex 100BASE-TX

Bit 12 – 10BASE-T Full Duplex 10BASE-T Full Duplex Ability
Note: Full duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to at 10 Mbit/s in Full-Duplex
1	PHY able to at 10 Mbit/s in Full-Duplex

Bit 11 – 10BASE-T Half Duplex 10BASE-T Half Duplex Ability
Note: Half duplex operation is supported. This bit is always '1'.

Value	Description
0	PHY not able to at 10 Mbit/s in Half-Duplex
1	PHY able to at 10 Mbit/s in Half-Duplex

Bit 10 – 100BASE-T2 Full Duplex 100BASE-T2 Full Duplex Ability
Note: 100BASE-T2 operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 100BASE-T2 in Full-Duplex
1	PHY able to operate at 100BASE-T2 in Full-Duplex

Bit 9 – 100BASE-T2 Half Duplex 100BASE-T2 Half Duplex Ability
Note: 100BASE-T2 operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 100BASE-T2 in Half-Duplex
1	PHY able to operate at 100BASE-T2 in Half-Duplex

Bit 8 – Extended Status Extended status information ability
Note: Extended status information is not available. This bit is always '0'.

Value	Description
0	No extended status information in register 0x0F
1	Extended status information in register 0x0F

Bit 6 – MF_PRE_SUP Management Frame Preamble Suppression Ability
Note: Management frame preamble suppression is not supported. This bit is always '0'.

Value	Description
0	PHY will not accept management frames with preamble suppressed
1	PHY will accept management frames with preamble suppressed

Bit 5 – AUTO_NEG_COMP Auto-Negotiation Complete
Note: Auto-negotiation is not supported. This bit is always '0'.

Value	Description
0	Auto-negotiation process has not completed
1	Auto-negotiation process has completed

Bit 4 – RMT_FAULT Remote Fault Detection
Note: Remote fault detection is not supported. This bit is always '0'.

Value	Description
0	No remote fault condition detected
1	Remote fault condition detected

Bit 3 – AUTO_NEG Auto-Negotiation Ability
Note: Auto-negotiation is not supported. This bit is always '0'.

Value	Description
0	PHY is not able to perform auto-negotiation
1	PHY is able to perform auto-negotiation

Bit 2 – LINK_STAT Link Status
Note: Link status indication is not supported. This bit is always '1'.

Value	Description
0	Network link is down
1	Network link is up

Bit 1 – JAB_DET Jabber Detection Status
This bit is set on detection of a jabber condition.

Value	Description
0	No jabber condition detected
1	Jabber condition detected

Bit 0 – EXT_CAP Extended Capabilities Ability
Note: Extended capabilities registers are supported. This bit is always '1'.

Value	Description
0	Extended capabilities registers not supported. Basic capabilities registers only.
1	Extended capabilities registers supported in addition to basic capabilities registers.

5.1.3 PHY Identifier 0 Register

Name: PHY_ID0
Address: 0x02

Bit	15	14	13	12	11	10	9	8
	OUI[2:9]							
Acccss	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OUI[10:17]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	1	1	1

Bits 15:8 – OUI[2:9] Organizationally Unique Identifier
This field contains the 3rd through the 10th bits of the Organizationally Unique Identifier (OUI) as specified in IEEE Std 802.3 Clause 22. OUI = 00800Fh

Bits 7:0 – OUI[10:17] Organizationally Unique Identifier
This field contains the 11th through the 18th bits of the Organizationally Unique Identifier (OUI) as specified in IEEE Std 802.3 Clause 22. OUI = 00800Fh

5.1.4 PHY Identifier 1 Register

Name: PHY_ID1
Address: 0x03

Bit	15	14	13	12	11	10	9	8
	OUI[18:23]						MODEL[5:4]	
Acccss	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
	MODEL[3:0]				REV[3:0]			
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	1	1	0	0	0	1	0

Bits 15:10 – OUI[18:23] Organizationally Unique Identifier
This field contains the 19th through the 24th bits of the Organizationally Unique Identifier (OUI) as specified in IEEE Std 802.3 Clause 22. OUI = 00800Fh

Bits 9:4 – MODEL[5:0] Manufacturer's Model Number
Six-bit manufacturer's model / product identification number

Value	Description
010110	LAN8670/1/2

Bits 3:0 – REV[3:0] Manufacturer's Revision Number
Four-bit manufacturer's silicon revision identification number
Note: The default value of the this field varies dependent on the silicon revision number.

Value	Description
0000	Silicon revision 0
0010	Silicon revision 2

5.1.5 MMD Access Control Register

Name: MMDCTRL
Address: 0x0D

Bit	15	14	13	12	11	10	9	8
	FNCTN[1:0]							
Acccss	R/W	R/W	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				DEVAD[4:0]				
Access	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:14 – FNCTN[1:0] MMD Function
This field specifies the action to be performed when reading or writing the MMD Access Address/Data register.

Value	Description
00	Address
01	Data - No post increment
10	Data - Post increment on reads and writes
11	Data - Post increment on writes only

Bits 4:0 – DEVAD[4:0] Device Address
Address of the MDIO Manageable Device to access.

Value	Description
00001	PMA/PMD
00010	PCS
11111	Vendor Specific 2
Others	Reserved - do not access

5.1.6 MMD Access Address/Data Register

Name: MMDAD
Address: 0x0E

Bit	15	14	13	12	11	10	9	8
	ADR_DATA[15:8]							
Acccss	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADR_DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADR_DATA[15:0] MMD Address / Data
Functionality depends on the MMD Function (FNCTN) bits in the MMD Access Control (MMDCTRL) register as specified in IEEE Std 802.3 Annex 22D:

- `00b` = Writing this field sets the offset of the register within the MMD to access
- `01b`, `10b`, `11b` = When written, the contents are written into the MMD register
- `01b`, `10b`, `11b` = When read, the contents from the MMD register are returned

Related Links
5.1.5 MMDCTRL

5.1.7 Strap Control 0 Register

Name: STRAP_CTRL0
Address: 0x12

Bit	15	14	13	12	11	10	9	8
								MITYP[1]
Acccss	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	x

Bit	7	6	5	4	3	2	1	0
	MITYP[0]	PKGTYP[1:0]		SMIADR[4:0]				
Access	R/W	R/W NASR	R/W NASR	R/W NASR	R/W NASR	R/W NASR	R/W NASR	R/W NASR
Reset	x	x	x	x	x	x	x	x

Bits 8:7 – MITYP[1:0] Media Interface Type
This field indicates the media interface type as defined by the product package and state of the MODE configuration straps at reset.
Note: The default is determined by the MODE[1:0] configuration strap pins. This bit field defaults to 01b on the LAN8671 as the device may only be configured for use in RMII mode. Similarly, this bit field defaults to 10b on the LAN8672 as the device may only be configured for use in MII mode. Refer to the section on configuration straps for additional information.

Important: This field shall not be written to any value except its default value on reset.

Value	Description
00b	Undefined
01b	RMII with 50 MHz REFCLKIN
10b	MII with 25 MHz crystal
11b	Undefined

Bits 6:5 – PKGTYP[1:0] Package Type
This field indicates the product and package type.
Note: The default value is specific to the product.

Important: This field shall not be written to any value except its default value on reset.

Value	Description
00b	Undefined
01b	32-pin LAN8670
10b	24-pin LAN8671
11b	36-pin LAN8672

Note: This register is not affected by soft reset (SW_RESET).

Bits 4:0 – SMIADR[4:0] Serial Management Interface Address
Note: The default value is determined by the state of the PHYADn PHY Address configuration strap pins at reset. Refer to the section on configuration straps for additional information.

Note: This register is not affected by soft reset (SW_RESET).

⚠ CAUTION When writing to other fields of this register, be sure to read this field and write it with the read value (i.e., read-modified write).

Related Links

3.5 Configuration Straps

5.2 PMA/PMD Registers

The PMA/PMD registers are located at MDIO Manageable Device (MMD) address 0x01.

WARNING RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in adverse operation and unexpected results.

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x11	Reserved									
0x12	PMA_PMD_EXT_ABILITY	15:8								
		7:0					T1SABL	T1LABL		
0x14 ... 0x0833	Reserved									
0x0834	T1PMAPMDCTL	15:8								
		7:0					TYPSEL[3:0]			
0x0836 ... 0x08F8	Reserved									
0x08F9	T1SPMACTL	15:8	RST	TXD			LPE	MDE		
		7:0								LBE
0x08FA	T1SPMASTS	15:8			LBA		LPA	MDA	RXFA	
		7:0							RXFD	
0x08FB	T1STSTCTL	15:8	TSTCTL[2:0]							
		7:0								

5.2.1 BASE-T1 PMA/PMD Extended Ability

Name: PMA_PMD_EXT_ABILITY
Address: 0x0012

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					T1SABL	T1LABL		
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	1	0	0	0

Bit 3 – T1SABL 10BASE-T1S Ability

Value	Description
0	PMA/PMD is not able to perform 10BASE-T1S operation
1	PMA/PMD is able to perform 10BASE-T1S operation

Note: This bit is always 1.

Bit 2 – T1LABL 10BASE-T1L Ability

Value	Description
0	PMA/PMD is not able to perform 10BASE-T1Loperation
1	PMA/PMD is able to perform 10BASE-T1L operation

Note: 10BASE-T1L operation is not supported. This bit is always 0.

5.2.2 BASE-T1 PMA/PMD Control

Name: T1PMAPMDCTL
Address: 0x0834

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					TYPSEL[3:0]			
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	1	1

Bits 3:0 – TYPSEL[3:0] Type Selection
Note: Only 10BASE-T1S operation is supported. This field is always 0011b.

Value	Description
0000b	100BASE-T1
0001b	1000BASE-T1
0010b	10BASE-T1L
0011b	10BASE-T1S
01xxb	Reserved
1xxxb	Reserved

5.2.3 10BASE-T1S PMA Control

Name: T1SPMACTL
Address: 0x08F9

Bit	15	14	13	12	11	10	9	8
	RST	TXD			LPE	MDE		
Acccss	R/W SC	R/W	RO	RO	R/W	R/W	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								LBE
Access	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – RST PMA Reset
Note: This bit is self-clearing. When setting this bit, do not set other bits in this register.

Value	Description
0	Normal Operation
1	PMA Reset

Bit 14 – TXD Transmit Disable

Value	Description
0	Normal operation
1	Transmit disable

Bit 11 – LPE Low Power Enable
Setting this bit will power down the PMA transceiver.
Note: This bit has the same effect as the Power Down bit in the Clause 22 BASIC_CONTROL register.

Value	Description
0	Normal operation
1	Place PMA into low-power mode

Bit 10 – MDE Multidrop Enable

Value	Description
0	Disable mixing segment operation (point-to-point mode)
1	Enable PMA multidrop (mixing segment) operation

Bit 0 – LBE PMA Loopback Enable

Value	Description
0	Disable PMA loopback mode
1	Enable PMA loopback mode

5.2.4 10BASE-T1S PMA Status

Name: T1SPMASTS
Address: 0x08FA

Bit	15	14	13	12	11	10	9	8
			LBA		LPA	MDA	RXFA	
Acccss	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	1	0	1	1	0	0

Bit	7	6	5	4	3	2	1	0
							RXFD	
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 13 – LBA PMA Loopback Ability

Value	Description
0	PHY does not support PMA loopback mode
1	PHY supports PMA loopback mode

Bit 11 – LPA Low Power Ability

Value	Description
0	PMA does not have low power ability
1	PMA has low power ability

Bit 10 – MDA Multidrop Ability

Value	Description
0	PMA does not support mixing segment operation (point-to-point only)
1	PMA supports multidrop (mixing segment) operation

Bit 9 – RXFA Receive Fault Ability

Value	Description
0	PHY does not have the ability to detect PMA faults
1	PHY has the ability to detect faults in the PMA receive path

Bit 1 – RXFD Receive Fault Detection

Value	Description
0	No PMA fault detected
1	PMA fault condition detected

5.2.5 T1S Test Mode Control

Name: T1STSTCTL
Address: 0x08FB

Bit	15	14	13	12	11	10	9	8
	TSTCTL[2:0]							
Acccss	R/W	R/W	R/W	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:13 – TSTCTL[2:0] Test Mode Control
Note: For a description of the test modes, refer to Clause 147.5.2 of the IEEE 802.3cg™-2019 *Amendment 5: Physical Layers Specifications and Management Parameters for 10 Mb/s Operation and Associated Power Delivery over a Single Balanced Pair of Conductors*.

Value	Description
000	Normal (non-test) operation
001	Test mode 1
010	Test mode 2
011	Test mode 3
100	Test mode 4
101	Reserved
11x	Reserved

5.3 PCS Registers

The PCS registers are located at MDIO Manageable Device (MMD) address 0x03.

⚠WARNING RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in adverse operation and unexpected results.

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x08F2	Reserved									
0x08F3	T1SPCSCTL	15:8	RST	LBE						DUPLEX
		7:0								
0x08F4	T1SPCSSTS	15:8								
		7:0	FAULT							
0x08F5	T1SPCSDIAG1	15:8	RMTJABCNT[15:8]							
		7:0	RMTJABCNT[7:0]							
0x08F6	T1SPCSDIAG2	15:8	CORTXCNT[15:8]							
		7:0	CORTXCNT[7:0]							

5.3.1 10BASE-T1S PCS Control

Name: T1SPCSCTL
Address: 0x08F3

Bit	15	14	13	12	11	10	9	8
	RST	LBE						DUPLEX
Access	R/W SC	R/W	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – RST PCS Reset
Note: This bit is self-clearing. When setting this bit, do not set other bits in this register.

Value	Description
0	Normal Operation
1	PCS reset

Bit 14 – LBE PCS Loopback Enable

Value	Description
0	Disable PCS loopback mode
1	Enable PCS loopback mode

Bit 8 – DUPLEX Duplex Mode
Note: Only half-duplex operation is supported.

Value	Description
0	Full-duplex operation
1	Half-duplex operation

5.3.2 10BASE-T1S PCS Status

Name: T1SPCSSTS
Address: 0x08F4

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FAULT							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 7 – FAULT PCS Fault Indication

Value	Description
0	No PCS fault detected
1	PCS fault condition detected

5.3.3 10BASE-T1S PCS Diagnostic 1

Name: T1SPCSDIAG1
Address: 0x08F5

Bit	15	14	13	12	11	10	9	8
	RMTJABCNT[15:8]							
Acccss	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RMTJABCNT[7:0]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RMTJABCNT[15:0] Remote Jabber Count
Field counting the number of remote jabber errors (ESDJAB) received since the last read of the register. This field will saturate at 0xFFFF.

5.3.4 10BASE-T1S PCS Diagnostic 2

Name: T1SPCSDIAG2
Address: 0x08F6

Bit	15	14	13	12	11	10	9	8
	CORTXCNT[15:8]							
Acccss	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CORTXCNT[7:0]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CORTXCNT[15:0] Corrupted Transmit Count
Field containing the number of times a locally initiated transmission resulted in a corrupted signal at the MDI. Corruption during transmission would typically be due to collisions. This field is self-clearing when read. This field will saturate at 0xFFFF.

5.4 Miscellaneous Registers

The miscellaneous registers are located at MDIO Manageable Device (MMD) address 0x1F.

⚠WARNING RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in adverse operation and unexpected results.

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0F	Reserved									
0x10	CTRL1	15:8								
		7:0							DIGLBE	
0x12 ... 0x17	Reserved									
0x18	STS1	15:8						TXCOL	TXJAB	
		7:0	EMPCYC	RXINTO	UNEXPB	BCNBFTO		PLCASYM	ESDERR	DEC5B
0x19	STS2	15:8					RESETC			
		7:0								
0x1A	STS3	15:8								
		7:0	ERRTOID[7:0]							
0x1C	IMSK1	15:8						TXCOLM	TXJABM	
		7:0	EMPCYCM	RXINTOM	UNEXPBM	BCNBFTOM		PLCASYMM	ESDERRM	DEC5BM
0x1D	IMSK2	15:8					RESETCM			
		7:0								
0x1F	Reserved									
0x20	CTRCTRL	15:8								
		7:0							TOCTRE	BCNCTRE
0x22 ... 0x23	Reserved									
0x24	TOCNTH	15:8	TOCNT[31:24]							
		7:0	TOCNT[23:16]							
0x25	TOCNTL	15:8	TOCNT[15:8]							
		7:0	TOCNT[7:0]							
0x26	BCNCNTH	15:8	BCNCNT[31:24]							
		7:0	BCNCNT[23:16]							
0x27	BCNCNTL	15:8	BCNCNT[15:8]							
		7:0	BCNCNT[7:0]							
0x29 ... 0xCA	Reserved									
0xCB	PADCTRL3	15:8	PDRV4[1:0]		PDRV3[1:0]		PDRV2[1:0]		PDRV1[1:0]	
		7:0								
0xCD ... 0xC9FF	Reserved									
0xCA00	MIDVER	15:8	IDM[7:0]							
		7:0	VER[7:0]							
0xCA01	PLCA_CTRL0	15:8	EN	RST						
		7:0								
0xCA02	PLCA_CTRL1	15:8	NCNT[7:0]							
		7:0	ID[7:0]							
0xCA03	PLCA_STS	15:8	PST							
		7:0								
0xCA04	PLCA_TOTMR	15:8								
		7:0	TOTMR[7:0]							

.....continued

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xCA05	PLCA_BURST	15:8	MAXBC[7:0]							
		7:0	BTMR[7:0]							

5.4.1 Control 1 Register

Name: CTRL1
Address: 0x0010

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
							DIGLBE	
Access	RO	RO	RO	RO	RO	RO	R/W	RO
Reset	0	0	0	0	0	0	0	0

Bit 1 – DIGLBE Digital Loopback Enable
Enables a digital loopback from the differential Manchester encoder to the decoder.

Value	Description
0	Normal operation
1	Digital loopback enabled

5.4.2 Status 1 Register

Name: STS1
Address: 0x0018

Bit	15	14	13	12	11	10	9	8
						TXCOL	TXJAB	
Acccss	RO	RO	RO	RO	RO	RC	RC	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EMPCYC	RXINTO	UNEXPB	BCNBFTO		PLCASYM	ESDERR	DEC5B
Access	RC	RC	RC	RC	RO	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit 10 – TXCOL Transmit Collision Status
Physical collision on the network was detected. This does not include logical collisions due to normal operation of PLCA.

Value	Description
0	No collision detected during transmit
1	Collision detected during transmit

Bit 9 – TXJAB Transmit Jabber Status
This bit indicates the occurrence of a transmit jabber condition. A jabber condition occurs when the PHY detects that the PCS has remained in the transmit state longer than 2 ms.

Value	Description
0	No transmit jabber detected
1	Transmit jabber detected

Bit 7 – EMPCYC PLCA Empty Cycle Status
This bit indicates the detection of an empty PLCA bus cycle. An empty bus cycle occurs when the node detects no transmissions in any of the possible transmit opportunities between two successive BEACONs.

Value	Description
0	An empty PLCA cycle has not been detected
1	An empty PLCA cycle has been detected

Bit 6 – RXINTO Receive in Transmit Opportunity
This bit indicates the detection of another node transmitting in this node's local assigned transmit opportunity. This could indicate multiple nodes being assigned the same Local ID.

Value	Description
0	Another node has not been detected transmitting in this node's TO
1	Another node has been detected transmitting in this node's TO

Bit 5 – UNEXPB Unexpected BEACON Received
When configured as the PLCA coordinator in charge of transmitting the periodic coordinating BEACONs, this bit indicates the detection of an unexpected BEACON on the segment. This condition may be due to the configuration of multiple PLCA coordinators on the segment.

Value	Description
0	Another node on the segment has not been detected transmitting a BEACON
1	Another node on the segment has been detected transmitting a BEACON

Bit 4 – BCNBFTO BEACON Received Before Transmit Opportunity
This bit indicates the detection of a BEACON before the node's assigned transmit opportunity. This condition could indicate the configuration of multiple PLCA coordinators on the segment. Other conditions that may cause this to occur include a PLCA coordinator with an incorrectly configured maximum node count resulting in a PLCA cycle that is too short, or a PLCA Local ID that is configured beyond the PLCA cycle.

Value	Description
0	A BEACON has not been detected before local transmit opportunity
1	A BEACON was detected before local transmit opportunity

Bit 2 – PLCASYM PLCA Symbols Detected
This bit indicates the detection of PLCA BEACON symbols when PLCA is not enabled. This condition may indicate the local node is operating with PLCA disabled on a segment with PLCA enabled nodes.

Value	Description
0	PLCA BEACON symbols have not been detected from the network with PLCA disabled
1	PLCA BEACON symbols have been detected from the network with PLCA with disabled

Bit 1 – ESDERR End-of-Stream Delimiter Error
This bit indicates the reception of an End-of-Stream Delimiter Error (ESDERR) or End-of-Stream Jabber (ESDJAB) symbol.

Value	Description
0	ESD error has not been detected
1	ESD error has been detected

Bit 0 – DEC5B 5B Decode Error
This bit indicates a 5B decoder encountered an unknown or reserved 5B codeword that could not be decoded.

Value	Description
0	5B decoder error has not occurred
1	5B decode error has occurred

5.4.3 Status 2 Register

Name: STS2
Address: 0x0019

Bit	15	14	13	12	11	10	9	8
					RESETC			
Acccss	RO	RO	RO	RO	RC	RO	RO	RO
Reset	0	0	0	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 11 – RESETC Reset Complete Status
This bit is asserted upon completion of a reset due to power-on, assertion of the RESET_N pin, or setting of the SW_RESET bit.

Value	Description
0	Reset has not occurred
1	Reset has occurred

5.4.4 Status 3 Register

Name: STS3
Address: 0x001A

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ERRTOID[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ERRTOID[7:0] PLCA Error Transmit Opportunity ID
This field captures the local PLCA current transmit opportunity counter when any unmasked interrupt status bit in the Status 1 register is set.
Note: This field is only accurate if one unmasked interrupt status bit is set in the Status 1 register. If multiple interrupt status bits are set, then this field represents the transmit opportunity for only the most recent interrupt status bit.

5.4.5 Interrupt Mask 1 Register

Name: IMSK1
Address: 0x001C

Bit	15	14	13	12	11	10	9	8
						TXCOLM	TXJABM	
Acccss	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	EMPCYCM	RXINTOM	UNEXPBM	BCNBFTOM		PLCASYMM	ESDERRM	DEC5BM
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 10 – TXCOLM Transmit Collision Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Transmit Collision (TXCOL) status bit is set.

Value	Description
0	Transmit collision interrupt enabled
1	Transmit collision interrupt disabled

Bit 9 – TXJABM Transmit Jabber Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Transmit Jabber (TXJAB) status bit is set.

Value	Description
0	Transmit jabber interrupt enabled
1	Transmit jabber interrupt disabled

Bit 7 – EMPCYCM PLCA Empty Cycle Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the PLCA Empty Cycle (EMPCYC) status bit is set.

Value	Description
0	PLCA empty cycle interrupt enabled
1	PLCA empty cycle interrupt disabled

Bit 6 – RXINTOM Receive in Transmit Opportunity Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Receive in Transmit Opportunity (RXINTO) status bit is set.

Value	Description
0	Receive in transmit opportunity interrupt enabled
1	Receive in transmit opportunity interrupt disabled

Bit 5 – UNEXPBM Unexpected BEACON Received Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Unexpected BEACON Received (UNEXPB) status bit is set.

Value	Description
0	Unexpected BEACON received interrupt enabled
1	Unexpected BEACON received interrupt disabled

Bit 4 – BCNBFTOM BEACON Received Before Transmit Opportunity Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the BEACON Received Before Transmit Opportunity (BCNBFTO) status bit is set.

Value	Description
0	BEACON received before transmit opportunity interrupt enabled
1	BEACON received before transmit opportunity interrupt disabled

Bit 2 – PLCASYMM PLCA Symbols Detected Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the PLCA Symbols Detected (PLCASYN) status bit is set.

Value	Description
0	PLCA BEACON symbols detected interrupt enabled
1	PLCA BEACON symbols detected interrupt disabled

Bit 1 – ESDERRM End-of-Stream Delimiter Error Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the End-of-Stream Delimiter Error (ESDERR) status bit is set.

Value	Description
0	ESD error interrupt enabled
1	ESD error interrupt disabled

Bit 0 – DEC5BM 5B Decode Error Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the 5B Decoder Error (DEC5B) status is set.

Value	Description
0	5B decode error interrupt enabled
1	5B decode error interrupt disabled

5.4.6 Interrupt Mask 2 Register

Name: IMSK2
Address: 0x001D

Bit	15	14	13	12	11	10	9	8
					RESETCM			
Acccss	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	0	0	1

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 11 – RESETCM Reset Complete Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the device reset has been completed.

Value	Description
0	Reset complete interrupt enabled
1	Reset complete interrupt disabled

5.4.7 Counter Control Register

Name: CTRCTRL
Address: 0x0020

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
							TOCTRE	BCNCTRE
Access	RO	RO	RO	RO	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 1 – TOCTRE Transmit Opportunity Counter Enable
Enables and disables the PLCA transmit opportunity counter in the Transmit Opportunity Count (High) and Transmit Opportunity Count (Low) registers.

Value	Description
0	PLCA transmit opportunity counter is disabled
1	PLCA transmit opportunity counter is enabled

Bit 0 – BCNCTRE PLCA BEACON Counter Enable
Enables and disables the PLCA BEACON counter in BEACON Count (High) and BEACON Count (Low) registers.

Value	Description
0	PLCA BEACON counter is disabled
1	PLCA BEACON counter is enabled

5.4.8 Transmit Opportunity Count (High)

Name: TOCNTH
Address: 0x0024

Bit	15	14	13	12	11	10	9	8
	TOCNT[31:24]							
Acccss	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOCNT[23:16]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TOCNT[31:16] Transmit Opportunity Count
This field maintains the upper 16 bits of the 32-bit count of the number of PLCA transmit opportunities the transceiver may have utilized since the previous read.
Note: When this register is read, the contents of the 32-bit transmit opportunity counter will be latched into the high and low counter register pair. The high counter register will be updated prior to be driven onto MDIO pin.

Note: The 32-bit counter will be reset when the contents are latched into the high and low counter register pair.

5.4.9 Transmit Opportunity Count (Low)

Name: TOCNTL
Address: 0x0025

Bit	15	14	13	12	11	10	9	8
	TOCNT[15:8]							
Acccss	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOCNT[7:0]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TOCNT[15:0] Transmit Opportunity Count
This field maintains the lower 16 bits of the 32-bit count of the number of PLCA transmit opportunities the transceiver may have utilized since the previous read.
Note: The contents of this register will be latched upon reading of the Transmit Opportunity Count (High) register.

5.4.10 BEACON Count (High)

Name: BCNCNTH
Address: 0x0026

Bit	15	14	13	12	11	10	9	8
	BCNCNT[31:24]							
Acccss	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BCNCNT[23:16]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BCNCNT[31:16] Beacon Count
This field maintains the upper 16 bits of the 32-bit counter of PLCA beacons received or transmitted since the previous read.
Note: When this register is read, the contents of the 32-bit beacon counter will be latched into the high and low counter register pair. The high counter register will be updated prior to be driven onto MDIO pin.

Note: The 32-bit beacon counter will be reset when the contents are latched into the high and low counter register pair.

5.4.11 BEACON Count (Low)

Name: BCNCNTL
Address: 0x0027

Bit	15	14	13	12	11	10	9	8
	BCNCNT[15:8]							
Acccss	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BCNCNT[7:0]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BCNCNT[15:0] Beacon Count
This field maintains the lower 16 bits of the 32-bit counter of PLCA beacons received or transmitted since the previous read.
Note: The contents of this register will be latched upon reading of the BEACON Count (High) register.

5.4.12 Pad Control 3 Register

Name: PADCTRL3
Address: 0x00CB

Bit	15	14	13	12	11	10	9	8
	PDRV4[1:0]		PDRV3[1:0]		PDRV2[1:0]		PDRV1[1:0]	
Acccss	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
Access	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	1

Bits 15:14 – PDRV4[1:0] Digital Output Pad Drive Strength
This field configures the output pad drive strength for pin group 4.

Value	Description
00	Low current drive
01	Medium-low current drive
10	Medium-high current drive
11	High current drive (default)

Bits 13:12 – PDRV3[1:0] Digital Output Pad Drive Strength
This field configures the output pad drive strength for pin group 3.

Value	Description
00	Low current drive
01	Medium-low current drive
10	Medium-high current drive
11	High current drive (default)

Bits 11:10 – PDRV2[1:0] Digital Output Pad Drive Strength
This field configures the output pad drive strength for pin group 2.

Value	Description
00	Low current drive
01	Medium-low current drive
10	Medium-high current drive
11	High current drive (default)

Bits 9:8 – PDRV1[1:0] Digital Output Pad Drive Strength
This field configures the output pad drive strength for pin group 1.

Value	Description
00	Low current drive
01	Medium-low current drive
10	Medium-high current drive
11	High current drive (default)

5.4.13 OPEN Alliance Map ID and Version Register

Name: MIDVER
Address: 0xCA00

Bit	15	14	13	12	11	10	9	8
	IDM[7:0]							
Acccss	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	1	0	1	0

Bit	7	6	5	4	3	2	1	0
	VER[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	1	0	0	0	0

Bits 15:8 – IDM[7:0] Register Map ID
This field uniquely identifies the OPEN Alliance address space for register mapping.

Value	Description
0x0A	OPEN Alliance register map

Bits 7:0 – VER[7:0] Register Map Version
This field specifies the register map version. The version number is represented in binary-coded-decimal.

Value	Description
0x10	OPEN Alliance register map version 1.0

5.4.14 PLCA Control 0 Register

Name: PLCA_CTRL0
Address: 0xCA01

Bit	15	14	13	12	11	10	9	8
	EN	RST						
Access	R/W	R/W SC	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – EN PLCA Enable

Value	Description
0	The PLCA reconciliation sublayer is disabled and the PHY operates in normal CSMA/CD mode without the performance enhancements of PLCA.
1	The Physical Layer Collision Avoidance (PLCA) reconciliation sublayer functionality is enabled.

Bit 14 – RST PLCA Reset
Note: This bit is self-clearing. When setting this bit, do not set other bits in this register.

Value	Description
0	Normal operation
1	PLCA reconciliation sublayer is reset

5.4.15 PLCA Control 1 Register

Name: PLCA_CTRL1
Address: 0xCA02

Bit	15	14	13	12	11	10	9	8
	NCNT[7:0]							
Acccss	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
	ID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 15:8 – NCNT[7:0] Node Count
This field configures the maximum number of nodes supported on the multidrop network. Proper operation requires that this field be set to at least the number of nodes that may exist on the network. The number of transmit opportunities in a given PLCA cycle.
Valid range: 0x01-0xFF
Note: This field must be configured correctly on the node with ID=0.

Bits 7:0 – ID[7:0] PLCA Local ID
This field configures the node's PLCA Local ID and the transmit opportunity within the PLCA cycle which it will transmit. A value of zero configures the node as the PLCA coordinator responsible for the periodic transmission of the PLCA BEACON and the number of transmit opportunities available per PLCA bus cycle. When set to 0xFF, the PLCA operation will be disabled and the node will revert to CSMA/CD.
Note: This parameter shall be configured unique across the multidrop network to ensure proper collision-free operation.

Value	Description
0	PLCA Coordinator node Local ID
1-0xFE	PLCA Follower node Local ID
0xFF	PLCA Disabled

5.4.16 PLCA Status Register

Name: PLCA_STS
Address: 0xCA03

Bit	15	14	13	12	11	10	9	8
	PST							
Acccss	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – PST PLCA Status
This field indicates that the PLCA reconciliation sublayer is active and a BEACON is being regularly transmitted or received.

Value	Description
0	The PLCA reconciliation sublayer is not regularly receiving or transmitting the BEACON
1	The PLCA reconciliation sublayer is regularly receiving or transmitting the BEACON

5.4.17 PLCA Transmit Opportunity Timer Register

Name: PLCA_TOTMR
Address: 0xCA04

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOTMR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

Bits 7:0 – TOTMR[7:0] PLCA Transmit Opportunity Timer
Configures the PLCA Transmit Opportunity time allowed for each node to begin transmitting to capture the network. The time is represented in increments of 100 ns (i.e., 1 BT).

Important: This field must be configured identically across all nodes on the multidrop network.

⚠ CAUTION Improper configuration of Transmit Opportunity timer may result in reduced network performance or collisions. It is recommended to leave this field at its default value unless a full evaluation of network delays has been performed.

5.4.18 PLCA Burst Mode Register

Name: PLCA_BURST
Address: 0xCA05

Bit	15	14	13	12	11	10	9	8
	MAXBC[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BTMR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

Bits 15:8 – MAXBC[7:0] Maximum Burst Count
This field configures the maximum number of additional frames that the node may transmit in a single transmit opportunity. When set to 0, the PLCA burst mode is disabled and only one frame will be transmitted per transmit opportunity.

Value	Description
0	Burst mode disabled. Only one frame will be transmitted per Transmit Opportunity.
1-0xFF	Number of additional frames that may be transmitted in a burst.

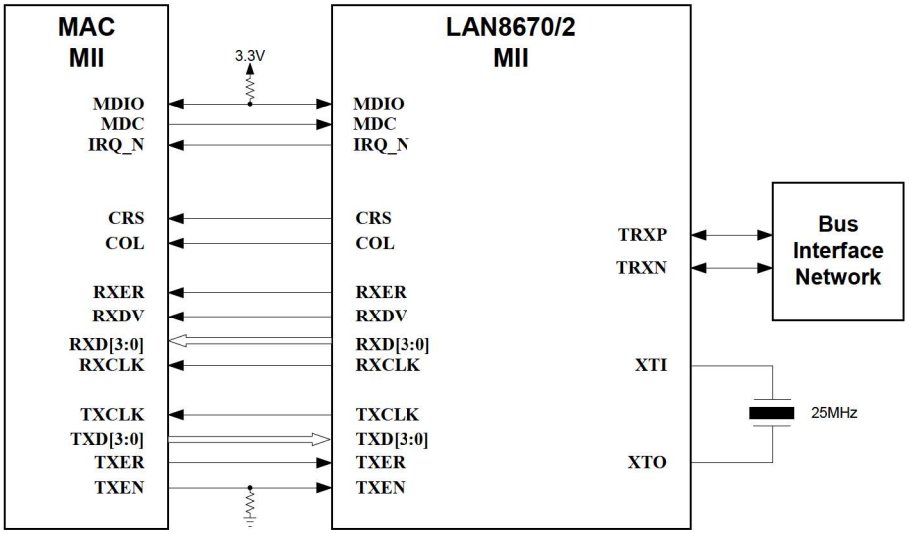
Bits 7:0 – BTMR[7:0] Burst Timer
When burst mode is enabled, this field configures the amount of time allowed following the transmission of a frame which the node will continue to transmit and hold the multidrop network waiting for the MAC to transmit an additional frame. Should the timer expire before the MAC transmits an additional frame, or if the maximum number of frames allowed to be transmitted in a single burst has been exceeded, the node will stop transmitting and yield the network to the next transmit opportunity.
The time is represented in increments of 100 ns (i.e., 1 BT).
Note: The minimum value should be equal to the MAC inter-frame gap (IFG) plus margin for the latency between the MAC and PHY.

6. Application Information

6.1 MII Operation

Figure 6-1 illustrates device connectivity in MII mode.

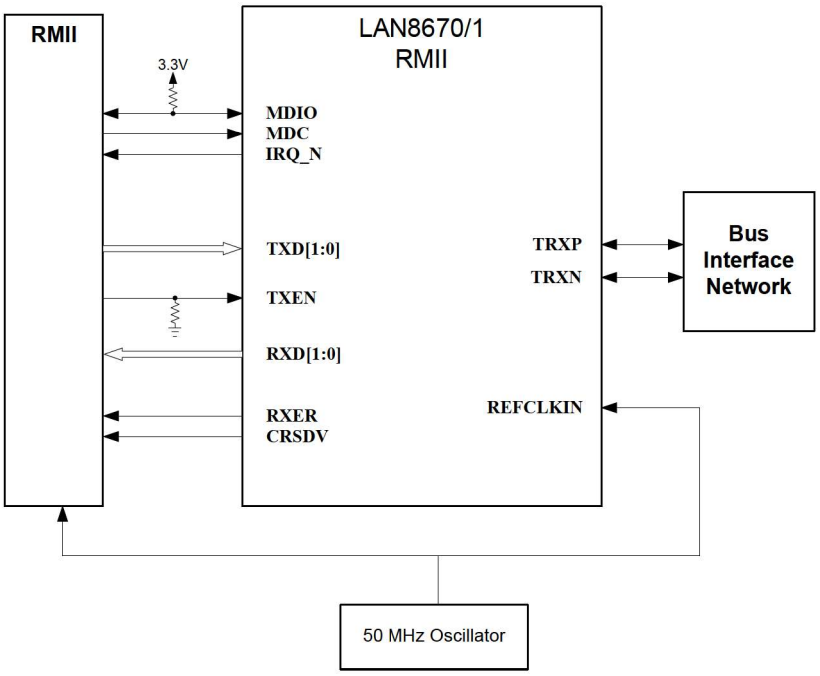
Figure 6-1. MII Connectivity



6.2 RMII Operation with Reference Clock

The figure below illustrates device connectivity in RMII mode with a 50 MHz reference clock.

Figure 6-2. RMII Connectivity with Reference Clock



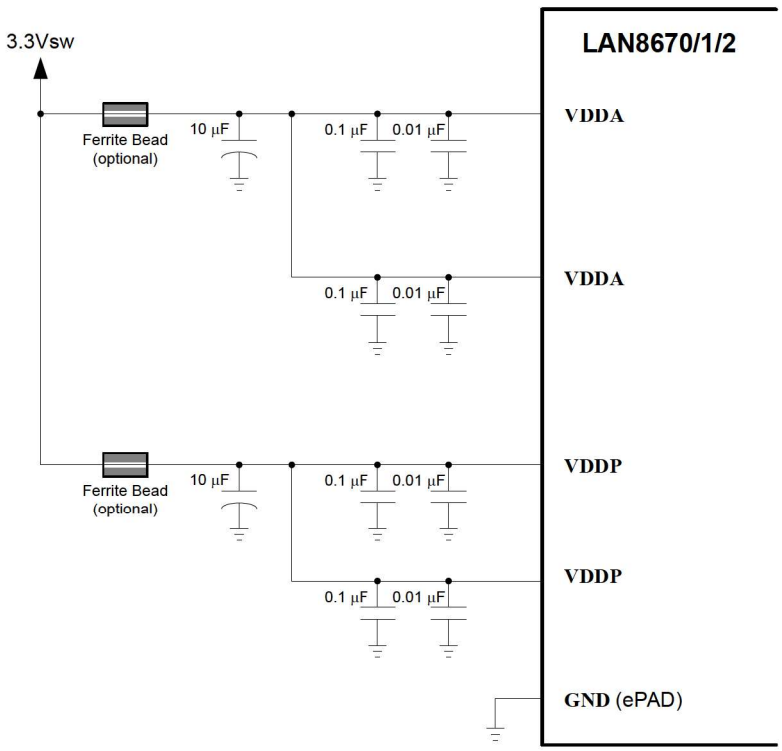
6.3 Power Connectivity

Figure 6-3 illustrates a typical power configuration for the LAN8670/1/2 with the power supply architecture and recommended decoupling. The LAN8670/1/2 requires at minimum only a single 3.3V power supply.

The analog pins (TRXP, TRXN, XTI/REFCLKIN, and XTO) pins must never be driven to more than the VDDA supply. Furthermore, all other digital pins must never be driven to more than the VDDP supply. These requirements are applicable to power-up and power-down as well as normal operating conditions.

A ferrite bead may optionally be added to the VDDA and VDDP supplies for increased noise immunity in EMI-sensitive applications. Depending on the properties of the ferrite bead, its combination with the decoupling capacitors may cause resonance peaking at lower frequencies leading to an undesired amplification of low-frequency noise in the system resulting in increased electromagnetic radiation. Since the ferrite bead selection is highly dependent on the noise in the system, which varies from design to design, the large bulk capacitor, typically 10 µF, is recommended to be placed on the device side of the ferrite bead. During the prototype phase, it is recommended to include the option for the ferrite beads should the need arise to populate it to improve noise immunity.

Figure 6-3. Power Connectivity



6.4 Crystal Oscillator Selection

Oscillator margin is a measure of the stability of an oscillator circuit, and is defined in Equation 6-1 as the ratio of the oscillator's negative resistance (R_{NEG}) to the crystal's ESR (R_{ESR}).

Equation 6-1. Crystal Oscillator Margin Measurement

$$\text{Margin} = \frac{|R_{\text{NEG}}|}{R_{\text{ESR}}} = \frac{|R_{\text{VAR}}| + R_{\text{ESR}}}{R_{\text{ESR}}}$$

The negative resistance can be measured by placing a variable resistor (R_{VAR}) in series with the crystal and finding the largest resistor value where the crystal still starts up properly. This point would be just below where the oscillator does not start-up or where the start-up time is excessively long. Ideally, oscillator margin should be greater than 10, and should be at least 5. Smaller oscillator margin can affect the ability of the oscillator to start up.

The load capacitance, specified when ordering the crystal, is the series combination of the capacitance on each leg of the crystal. This capacitance includes not only the added capacitors, but also PCB trace (shunt) capacitance and chip pin capacitance. Larger capacitors also have a negative effect on oscillator margin. It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XTI/XTO). The transconductance gain (g_m) of the internal inverting amplifier is nominally 18.2 mS.

The crystal cut and tolerance value listed in the Crystal Specifications section are typical values and may be changed to suit differing system requirements. Higher ESR values (than those listed in Crystal Specifications) run the risk of having start-up problems and should be thoroughly tested before being used. Contact the crystal manufacturer for more information.

Related Links

7.8.1 Crystal Specifications

6.5 Electromagnetic Compatibility (EMC) Considerations

6.5.1 Output Drive Strength Control

The LAN8670/1/2 digital outputs are configurable to one of four drive strengths. By changing the digital output impedance in combination with the output load, the rise and fall time of driven output signals may be adjusted to meet timing requirements while reducing the sharp transitions and ringing that can be a source of unwanted radiated emissions. The pin output drive strength is configurable in groups based on their application as defined in the table below. The output drive level for each pin group is configured within the Pad Control 3 (PADCTRL3) register. The output drive currents are specified in the DC Specifications section.

Table 6-1. Digital Output Drive Pin Groups

Pin Name	Pin Number		
	LAN8670	LAN8671	LAN8672
Pin Group 1 - Application			
TXCLK	12	-	-
IRQ_N	22	16	24
Pin Group 2 - Serial Management Interface			
MDIO	14	10	16
Pin Group 3 - MII			
COL	2	-	2
CRS	15	-	17
RXCLK	17	-	19
RXD2	23	-	25
RXD3	24	-	26
TXCLK	-	-	3
Pin Group 4 - MII/RMII			
RXD0	16	11	18
RXD1	19	12	21
RXDV/CRSDV	20	-	-
CRSDV	-	14	-
RXDV	-	-	22
RXER	21	15	23

Related Links

5.4.12 PADCTRL3
7.5 DC Specifications (other than 10BASE-T1S PMA)

6.6 Reference Schematics

The schematics on the following pages contain example reference implementations of the LAN8670/1/2. Engineers may wish to include series termination resistors near digital output pins to aid in matching the driver and PCB trace impedance. At a minimum, a series 100 nF coupling capacitor (not shown) is needed on each of the TRXP and TRXN pins. Additional bus interface network (BIN) details are contained in a separate Application Note.

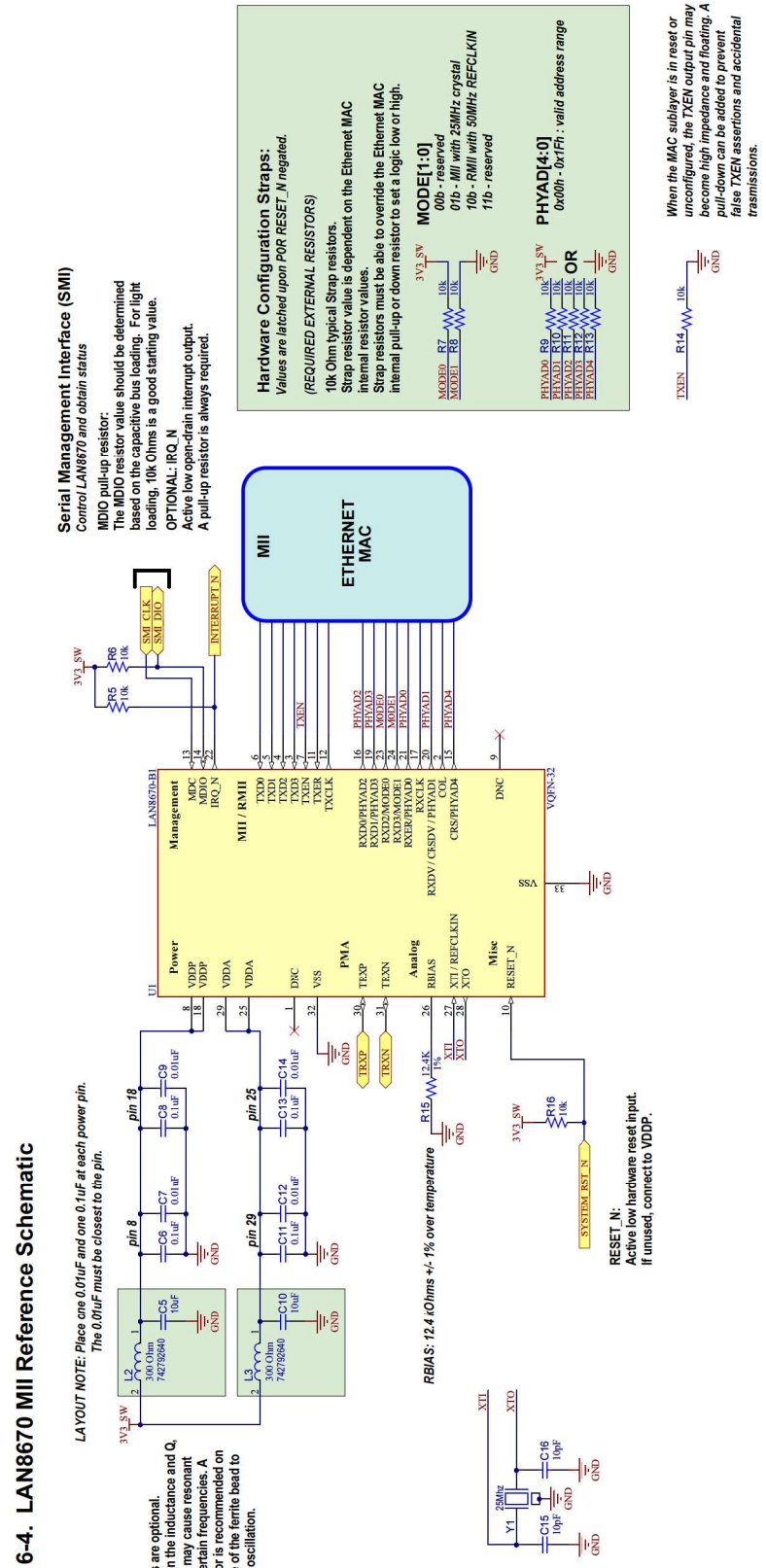
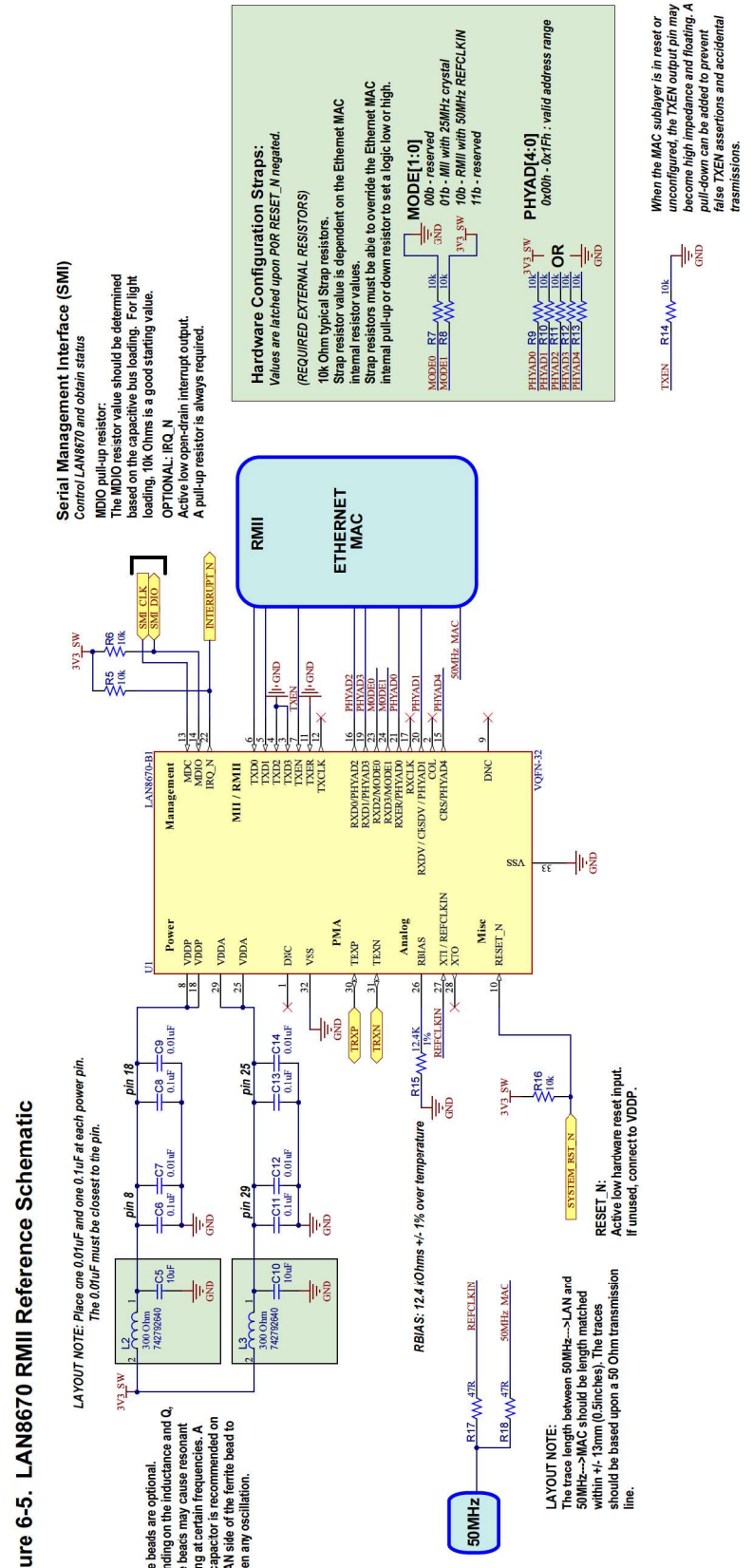


Figure 6-4. LAN8670 MII Reference Schematic

Figure 6-5. LAN8670 RMII Reference Schematic



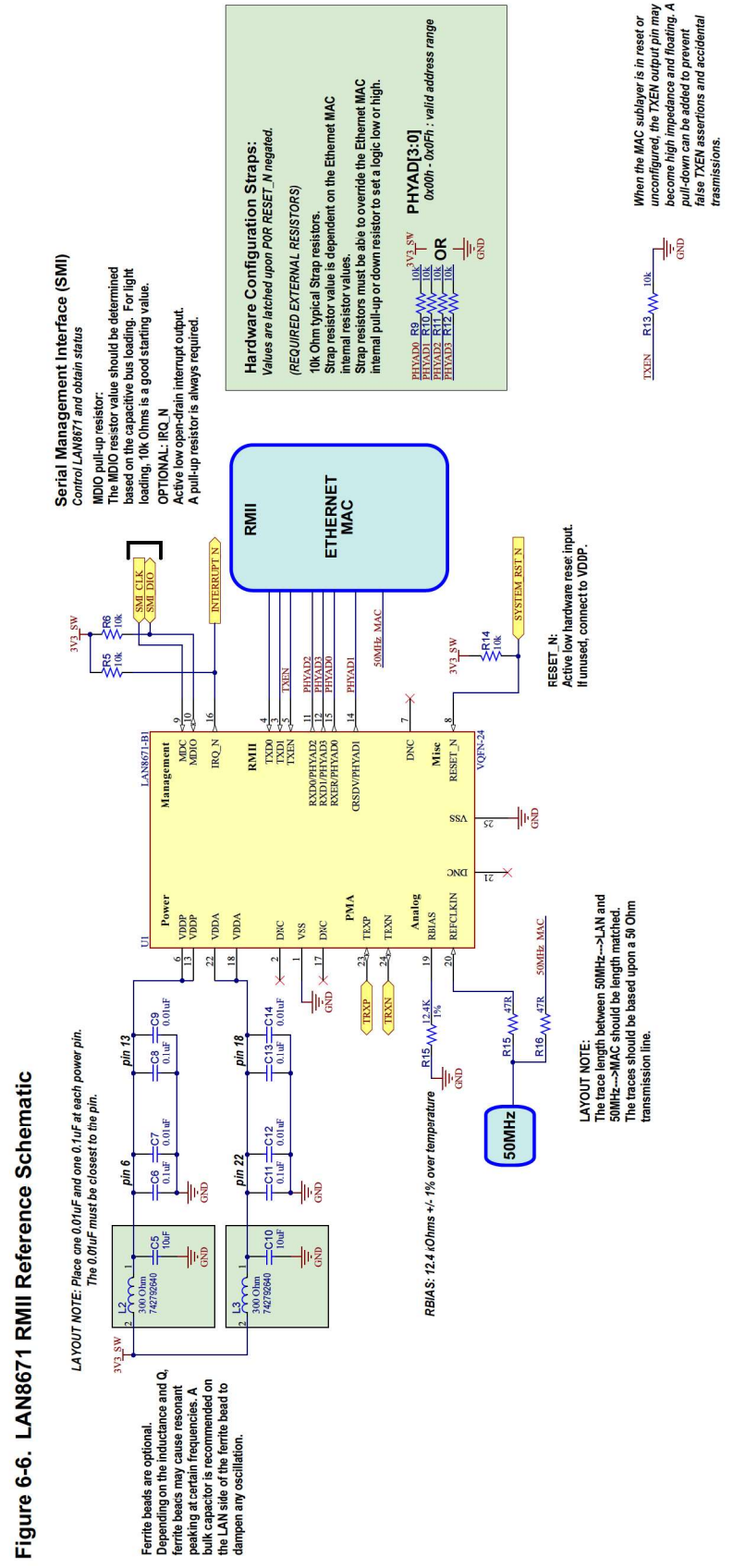


Figure 6-6. LAN8671 RMII Reference Schematic

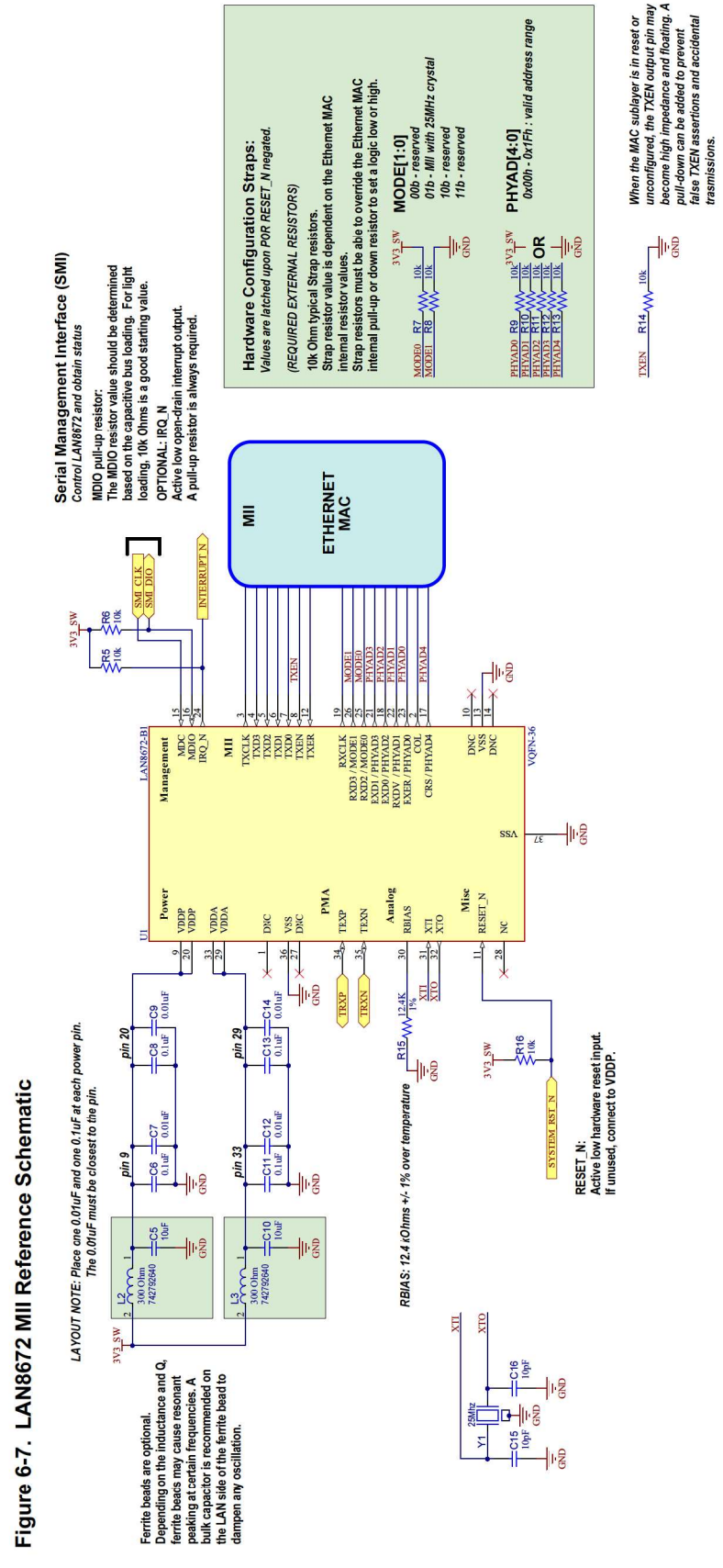


Figure 6-7. LAN8672 MII Reference Schematic

7. Operational Characteristics

7.1 Absolute Maximum Ratings

Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Operating Conditions, DC Specifications, or any other applicable section of this specification is not implied.

Attention: Exposure at or above these limits may damage the device.

Table 7-1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Power Supply Voltage:					Note 1
Digital I/O (VDDP)		-0.5	3.9	V	
Analog (VDDA)		-0.5	3.9	V	
Voltage applied to pins:					
TRXP, TRXN	$V_{TRXP/N}$	-27	42	V	
TRXP/TRXN (differential)	V_{DIFF}	-25	25	V	
XTI/REFCLKIN, RBIAS		-0.5	VDDA + 0.5	V	Note 2
All other pins		-0.5	VDDP + 0.5	V	Note 2
Junction Temperature Under Bias	T_J	-40	150	°C	
Storage Temperature	T_{stg}	-55	150	°C	
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020				
ESD Human Body Model					Note 3
TRXP, TRXN (to VSS)		-8	+8	kV	
All other pins		-2	+2	kV	
ESD Machine Model		-400	+400	V	JESD22-A115
ESD Charge Device Model		-750	+750	V	AEC-Q100-011

Notes:

1. When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.
2. Voltage applied to pins must remain below 3.9V.
3. Test specification following JESD22-A114/AEC-Q100-002: (1.5 kΩ/100 pF)

7.2 Operating Conditions

Proper operation of the device is guaranteed only within the ranges specified in this section.

Table 7-2. Operating Conditions

Description	Symbol	Min	Max	Units	Notes
Power Supply Voltage:					
Digital I/O (VDDP)		3.135	3.465	V	
Analog (VDDA)		3.135	3.465	V	
Maximum Input Voltage:					
XTI/REFCLKIN, RBIAS		-0.3	VDDA + 0.3	V	
All other pins		-0.3	VDDP + 0.3	V	
Power Supply Ramp Rate		300		µs/V	
Ambient Operating Temperature (Still Air)	T_A	-40	+125	°C	

7.3 Power Consumption

This section details the device power measurements taken over various operating conditions. Unless otherwise noted, all measurements were taken with power supplies at nominal values. All values are typical.

Table 7-3. Current Consumption and Power Dissipation

Mode		VDDA Current @3.3V (mA)	VDDP Current @3.3V (mA)	Total Device Power (mW)
RESET	RESET_N pin low	21	5	86
ACTIVE	Receive	21	5	86
ACTIVE	Transmit	31	5	120

7.4 Package Thermal Specifications

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESD51.

Table 7-4. LAN8670 Package Thermal Parameters (32-VQFN)

Parameter	Symbol	Value	Units	Notes
Junction-to-Ambient	Θ_{JA}	43	°C/W	Still air
Junction-to-Top-of-Package	Ψ_{JT}	0.6	°C/W	Still air
Junction-to-Case	Θ_{JC}	7.6	°C/W	

Table 7-5. LAN8671 Package Thermal Parameters (24-VQFN)

Parameter	Symbol	Value	Units	Notes
Junction-to-Ambient	Θ_{JA}	54	°C/W	Still air
Junction-to-Top-of-Package	Ψ_{JT}	0.9	°C/W	Still air
Junction-to-Case	Θ_{JC}	8.3	°C/W	

Table 7-6. LAN8672 Package Thermal Parameters (36-VQFN)

Parameter	Symbol	Value	Units	Notes
Junction-to-Ambient	Θ_{JA}	35	°C/W	Still air
Junction-to-Top-of-Package	Ψ_{JT}	0.4	°C/W	Still air
Junction-to-Case	Θ_{JC}	5.0	°C/W	

7.5 DC Specifications (other than 10BASE-T1S PMA)

Table 7-7. DC Electrical Characteristics (other than 10BASE-T1S PMA)

Parameter	Symbol	Min	Typ	Max	Units	Notes
VIS-VDDP Type Input Buffers						
Low-Level Input Voltage	V_{IL}	-0.3		0.8	V	
High-Level Input Voltage	V_{IH}	2.0		VDDP+0.3	V	
Input Hysteresis	ΔV_{hys}	25		230	mV	
Input Leakage	I_L	-10		10	µA	V_{IN} = VSS or VDDP
Input Capacitance	C_{IN}			3	pF	
VO-VDDP Type Output Buffers						
Low-Level Output	V_{OL}			0.4	V	Note 1
	I_{OL-L}	-0.6			mA	Low drive
	I_{OL-ML}	-1.7			mA	Medium-low drive
	I_{OL-MH}	-2.8			mA	Medium-high drive
	I_{OL-H}	-4.0			mA	High drive
High-Level Output	V_{OH}	VDDP-0.4			V	Note 2
	I_{OH-L}	0.45			mA	Low drive
	I_{OH-ML}	1.2			mA	Medium-low drive
	I_{OH-MH}	2.0			mA	Medium-high drive
	I_{OH-H}	2.9			mA	High drive
VOD-VDDP Type Output Buffers						
Low-Level Output	V_{OL}			0.4	V	Note 1
	I_{OL-L}	-0.6			mA	Low drive
	I_{OL-ML}	-1.7			mA	Medium-low drive
	I_{OL-MH}	-2.8			mA	Medium-high drive
	I_{OL-H}	-4.0			mA	High drive
VOH-VDDP Type Output Buffers						
Low-Level Output	V_{OL}			0.4	V	Note 1
	I_{OL-L}	-1.3			mA	Low drive
	I_{OL-ML}	-2.7			mA	Medium-low drive
	I_{OL-MH}	-4.0			mA	Medium-high drive
	I_{OL-H}	-5.3			mA	High drive
High-Level Output	V_{OH}	VDDP-0.4			V	Note 2
	I_{OH-L}	1.0			mA	Low drive
	I_{OH-ML}	2.0			mA	Medium-low drive
	I_{OH-MH}	2.8			mA	Medium-high drive
	I_{OH-H}	3.5			mA	High drive

.....continued

Parameter	Symbol	Min	Typ	Max	Units	Notes
ICLK Type Input Buffer						Note 3
Low-Level Input Voltage	V_{IL}	-0.3		0.45	V	
High-Level Input Voltage	V_{IH}	VDDA-0.35		VDDA+0.3	V	
Input Leakage	I_L	-10		10	µA	V_{IN} = VSS or VDDA
Input Capacitance	C_{IN}			3	pF	

Notes:

1. I_{OL} is configurable to four levels of sink current.
2. I_{OH} is configurable to four levels of source current.
3. REFCLKIN, and optionally XTI, can be driven from a single-ended clock oscillator to which these specifications apply.

7.6 AC Specifications

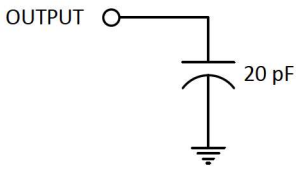
This section details the various AC timing specifications of the device.

Note: The Ethernet TRXP/TRXN pin timing adheres to IEEE Std 802.3cg. Refer to the IEEE Std 802.3cg specification for detailed Ethernet timing information.

7.6.1 Equivalent Test Load

Output timing specifications assume a 20 pF equivalent test load, unless otherwise noted, as illustrated below.

Figure 7-1. Output Equivalent Test Load



7.6.2 General Signals and Clocks

Table 7-8. AC Electrical Characteristics (other than Ethernet PMA)

Parameter	Symbol	Min	Typ	Max	Units	Notes
VO-VDDP Type Output Buffers						
Output Rise Time	t_r					10% to 90%, C_L = 20 pF
			23		ns	Low drive
			8		ns	Medium-low drive
			5		ns	Medium-high drive
			3		ns	High drive
Output Fall Time	t_f					90% to 10%, C_L = 20 pF
			23		ns	Low drive
			8		ns	Medium-low drive
			5		ns	Medium-high drive
			3		ns	High drive
VOD-VDDP Type Output Buffers						
Output Fall Time	t_f					90% to 10%, C_L = 20 pF
			23		ns	Low drive
			7		ns	Medium-low drive
			5		ns	Medium-high drive
			3		ns	High drive
VOH-VDDP Type Output Buffers						
Output Rise Time	t_r					10% to 90%, C_L = 20 pF
			10		ns	Low drive
			5		ns	Medium-low drive
			4		ns	Medium-high drive

.....continued						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
			3		ns	High drive
Output Fall Time	t_f					90% to 10%, C_L = 20 pF
			10		ns	Low drive
			5		ns	Medium-low drive
			4		ns	Medium-high drive
			3		ns	High drive

7.6.3 Power-On Configuration Strap Timing

The timing diagram below illustrates the configuration strap timing requirements, in relation to power-on, for applications where RESET_N is not used at power-on. The operational level (V_{opp}) for the external power supply is defined as the minimum operational supply voltage as detailed in the Operating Conditions section.

Figure 7-2. Power-On Configuration Strap Timing

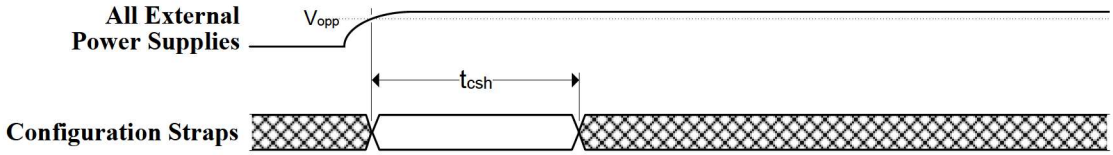


Table 7-9. Power-On Configuration Strap Timing

Description	Symbol	Min	Typ	Max	Units
Configuration strap hold after external power supply at operational level	t_{csh}	4			ms

7.6.4 RESET_N Configuration Strap Timing

The following diagram illustrates the RESET_N timing requirements and its relation to the configuration straps. Assertion of RESET_N is not a requirement. However, if used, it must be asserted for the minimum period specified.

Figure 7-3. RESET_N Configuration Strap Timing

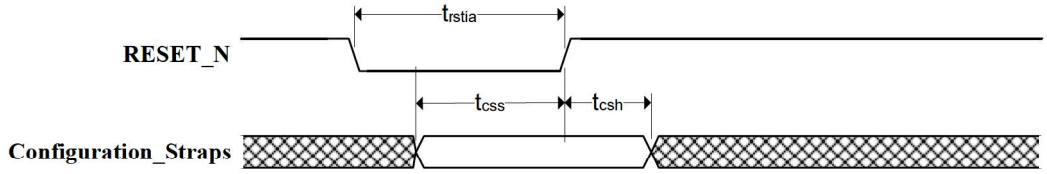


Table 7-10. RESET_N Configuration Strap Timing

Description	Symbol	Min	Typ	Max	Units
RESET_N input assertion time	t_{rstia}	5			µs
Configuration strap setup before RESET_N negation	t_{css}	200			ns
Configuration strap hold after RESET_N negation	t_{csh}	10			ns

7.6.5 Power Sequence Timing

Power supplies must adhere to the following rules:

- There is no power-up sequencing requirement, however all power supplies must reach operational levels within the time periods specified in Table 7-11.
- VDDA must not be powered for an extended period of time without VDDP also at operational levels.

- Following initial power-on, or if a power supply brownout occurs (i.e., either of the VDDA or VDDP supplies drops below operational limits), an internal power-on reset will be performed once all power supplies reach operational levels. Refer to the section Power-On Configuration Strap Timing for power-on reset requirements.
- Do not drive input signals without power supplied to the device.

Attention: Violation of these specifications may damage the device.

Figure 7-4. Power Sequence Timing

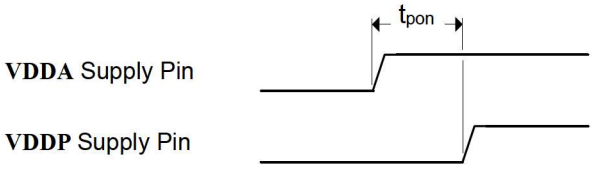


Table 7-11. Power Sequence Timing

Description	Symbol	Min	Typ	Max	Units
VDDP supply turn-on time relative to VDDA	t_{pon}	0		5	ms

Related Links

7.6.3 Power-On Configuration Strap Timing

7.6.6 MII Timing

This section specifies the MII transmit and receive timing.

Figure 7-5. MII Transmit Timing

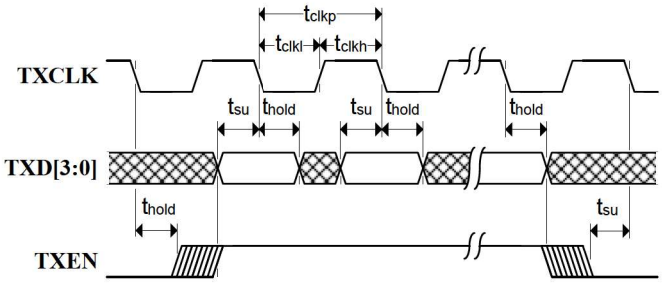


Table 7-12. MII Transmit Timing

Description	Symbol	Min	Typ	Max	Units
TXCLK period	t_{clkp}	400			ns
TXCLK high time	t_{clkh}	t_{clkp} * 0.4		t_{clkp} * 0.6	ns
TXCLK low time	t_{clkl}	t_{clkp} * 0.4		t_{clkp} * 0.6	ns
TXD[3:0], TXEN setup time to falling edge of TXCLK	t_{su}	26.0			ns
TXD[3:0], TXEN hold time after falling edge of TXCLK	t_{hold}	0			ns

Note: Timing was designed for system load between 5 pF and 20 pF.

Figure 7-6. MII Receive Timing

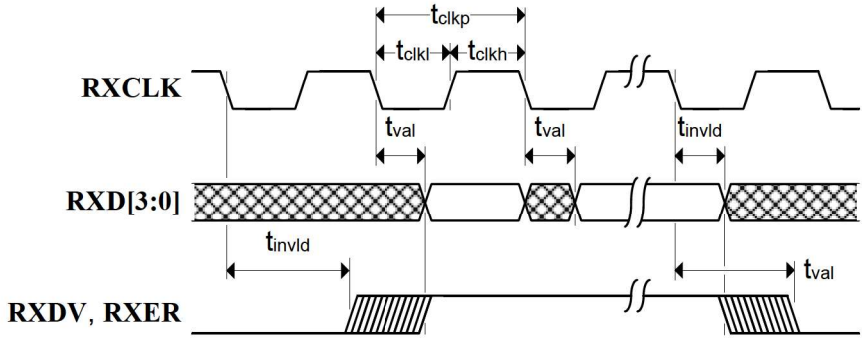


Table 7-13. MII Receive Timing

Description	Symbol	Min	Typ	Max	Units
RXCLK period	t_{clkp}	400			ns
RXCLK high time	t_{clkh}	t_{clkp} * 0.4		t_{clkp} * 0.6	ns
RXCLK low time	t_{clkl}	t_{clkp} * 0.4		t_{clkp} * 0.6	ns
RXD[3:0], RXDV, RXER output valid from falling edge of RXCLK	t_{val}			28.0	ns
RXD[3:0], RXDV, RXER output invalid from falling edge of RXCLK	t_{invld}	10.0			ns

Note:
Timing was designed for system load between 5 pF and 20 pF.

7.6.7 RMII Timing

This section specifies the RMII interface transmit and receive timing.

In this mode, a 50 MHz clock must be input on the REFCLKIN pin. Refer to the RMII REFCLKIN Requirements section for clock additional details.

Note: The CRSDV pin performs both carrier sense and data valid functions. CRSDV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. If the PHY has additional bits to be presented on RXD[1:0] following the initial negation of CRSDV, then the device will assert CRSDV on cycles of REFCLKIN which present the second di-bit of each nibble and negate CRSDV on cycles of REFCLKIN which present the first di-bit of a nibble. For additional information, refer to the RMII specification.

Figure 7-7. RMII Timing

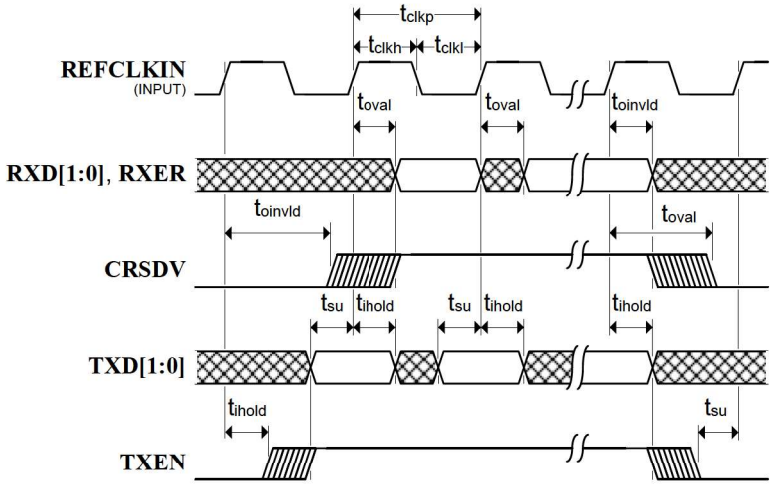


Table 7-14. RMII Timing

Description	Symbol	Min	Typ	Max	Units
REFCLKIN period	t_{clkp}	20			ns
REFCLKIN high time	t_{clkh}	t_{clkp} * 0.35		t_{clkp} * 0.65	ns
REFCLKIN low time	t_{clkl}	t_{clkp} * 0.35		t_{clkp} * 0.65	ns
RXD[1:0], RXER, CRSDV output valid from rising edge of REFCLKIN	t_{oval}			16	ns
RXD[1:0], RXER, CRSDV output invalid from rising edge of REFCLKIN	t_{oinvld}	3.0			ns
TXD[1:0], TXEN setup time to rising edge of REFCLKIN	t_{su}	4.0			ns
TXD[1:0], TXEN hold time after rising edge of REFCLKIN	t_{ihold}	1.5			ns

Note: Timing was designed for system load between 5 pF and 20 pF.

7.6.8 SMI Timing

This section specifies the serial management interface timing of the device.

Figure 7-8. SMI Timing

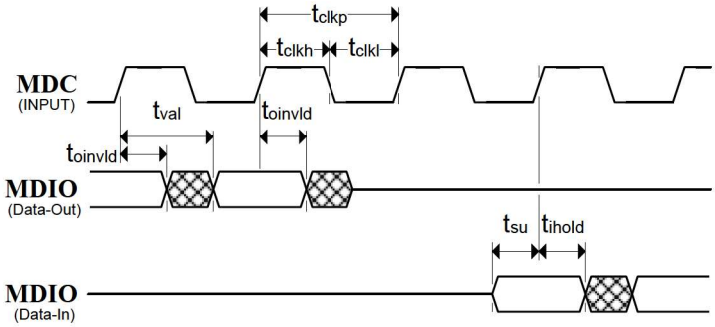


Table 7-15. SMI Timing

Description	Symbol	Min	Typ	Max	Units
MDC period	t_{clkp}	250			ns
MDC high time	t_{clkh}	t_{clkp} * 0.4			ns
MDC low time	t_{clkl}	t_{clkp} * 0.4			ns
MDIO (read from PHY) output valid from rising edge of MDC	t_{val}			130	ns
MDIO (read from PHY) output invalid from rising edge of MDC	t_{oinvld}	0			ns
MDIO (write to PHY) setup time to rising edge of MDC	t_{su}	10			ns
MDIO (write to PHY) input hold time after rising edge of MDC	t_{ihold}	10			ns

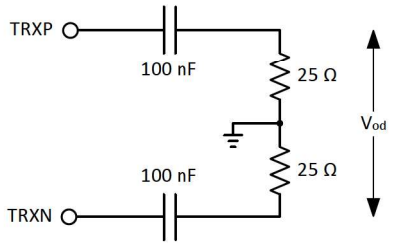
7.7 10BASE-T1S PMA

Table 7-16. 10BASE-T1S PMA Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential capacitance	C_d		9		pF	1 MHz Note 1
Transmit Driver Output						
Differential driver output	V_{od}	0.8	1.0	1.2	V	Figure 7-9
Change in differential steady state output for complementary states	ΔV_{od}	-0.2		0.2	V	Figure 7-9
Receiver Input						
Receiver differential sensitivity	V_{th}	600			mV	
Differential input resistance	R_{id}		10		kΩ	Note 1

Note:
1. Design parameter (not tested).

Figure 7-9. Differential Output Test Fixture



7.8 Clock Circuit

The device can accept either a 25 MHz crystal (preferred) or a 25 MHz single-ended clock oscillator (± 100 ppm) input. If the single-ended clock oscillator method is implemented, XTO should be left unconnected and XTI (REFCLKIN) should be driven with a nominal 0-3.3V clock signal.

Note: In RMII mode, a 50 MHz single-ended clock oscillator input must be driven onto REFCLKIN which adheres to the requirements detailed in the RMII REFCLKIN Requirements section.

7.8.1 Crystal Specifications

See the following table for recommended crystal specifications.

Table 7-17. Crystal Oscillator Specifications

Parameter	Min	Typ	Max	Units	Notes
Crystal Cut		AT (typical)			
Crystal Oscillation Mode		Fundamental			
Crystal Calibration Mode		Parallel Resonant Mode			
Frequency		25.000		MHz	
Tolerance			±100	ppm	Note 1, 2
Recommended Maximum Shunt Capacitance			6	pF	
Recommended Matched Load Capacitance		10-22		pF	Note 3
Drive Level		50		µW	
Recommended Maximum Equivalent Series Resistance (ESR)			100	Ω	
XTI/XTO Pin Capacitance		2		pF	Note 4

Notes:

1. The total deviation for the transmitter clock frequency is specified by IEEE 802.3cg as ±100 ppm.
2. This parameter must include increased variation over the expected operational lifetime of the application (aging).
3. Load capacitance per crystal terminal.
4. This number includes the pad, the bond wire and the lead frame. Printed circuit board trace capacitance is not included in this value. The XTI/XTO pin and PCB trace capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

7.8.2 RMII REFCLKIN Requirements

The following table details the RMII REFCLKIN timing requirements.

Table 7-18. RMII REFCLKIN Timing Requirements

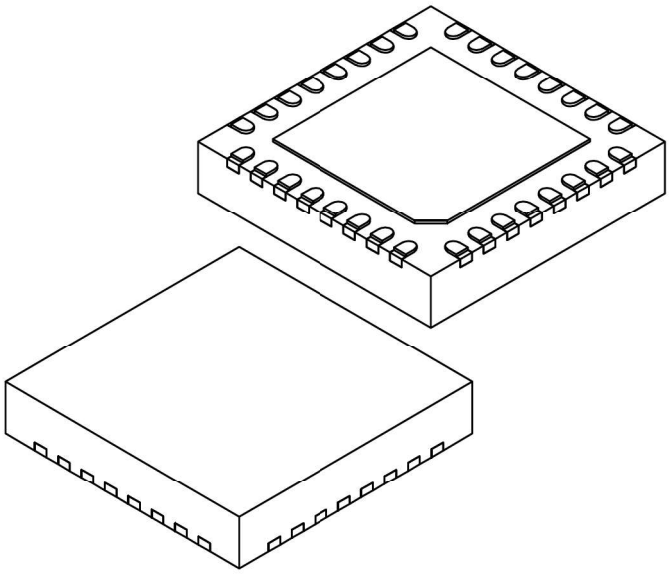
Parameter	Min	Typ	Max	Units	Notes
REFCLKIN frequency		50		MHz	
REFCLKIN Frequency Stability			±100	ppm	Including aging
REFCLKIN Duty Cycle	35		65	%	
REFCLKIN Jitter			840	ps	peak-to-peak (not RMS)

8. Packaging Information

8.1 32-VQFN (LAN8670 Only)

32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN] With 3.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.30	3.40	3.50
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.30	3.40	3.50
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-
Exposed Pad Corner Chamfer	CH		0.35 REF	
Step Height	A4	0.10	-	0.19
Step Length	D3	0.035	0.060	0.085

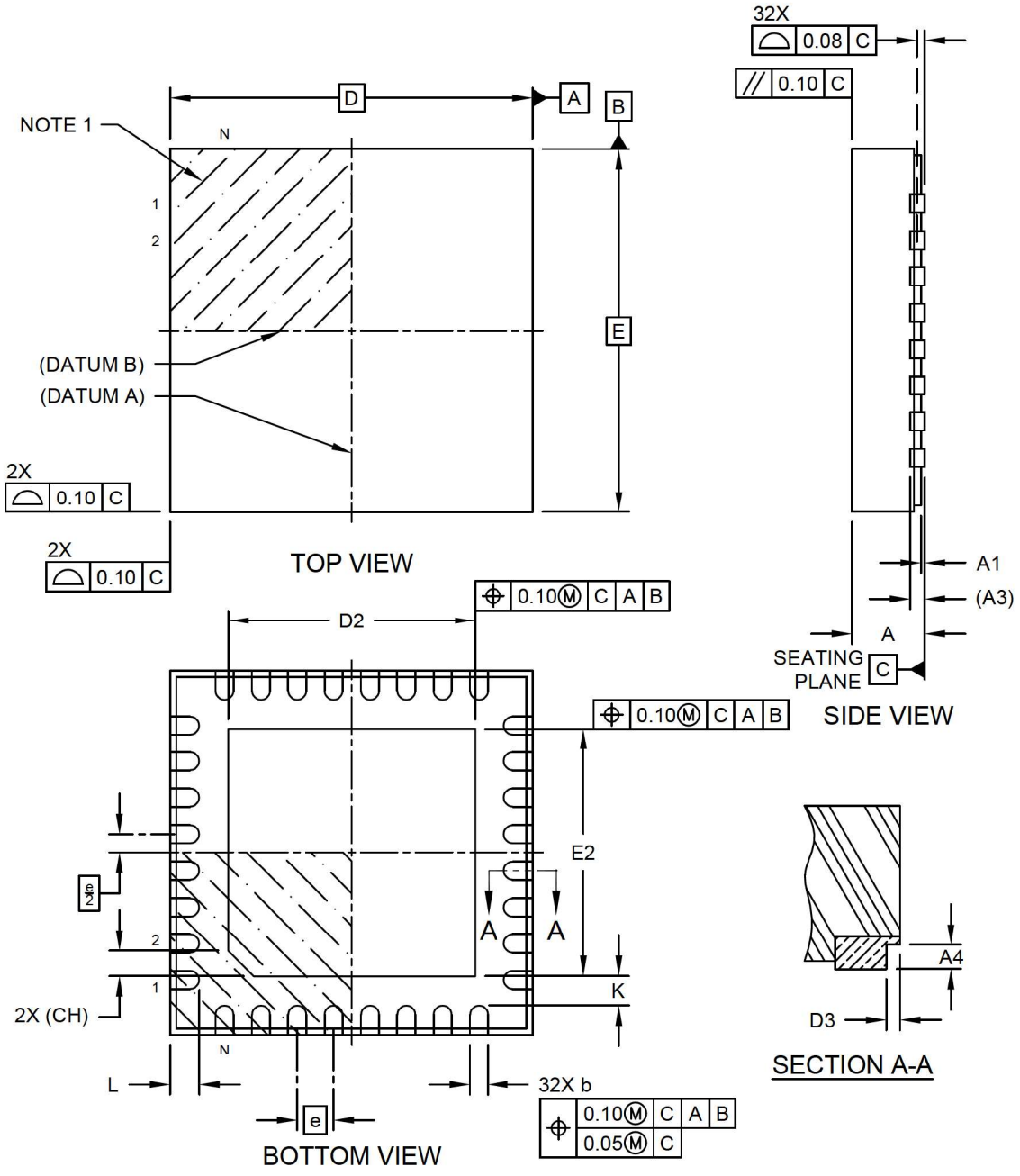
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-500 Rev B Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN] With 3.4 mm Exposed Pad and Stepped Wettable Flanks

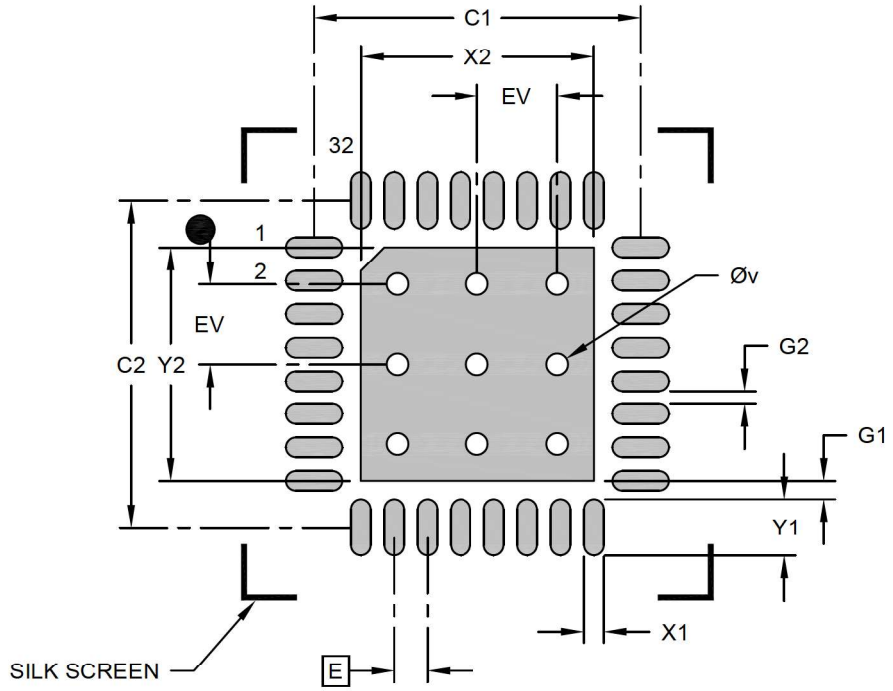
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-500 Rev B Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN] With 3.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.50
Center Pad Length	Y2			3.50
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (32)	X1			0.30
Contact Pad Length (32)	Y1			0.85
Contact Pad to Center Pad (32)	G1	0.20		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

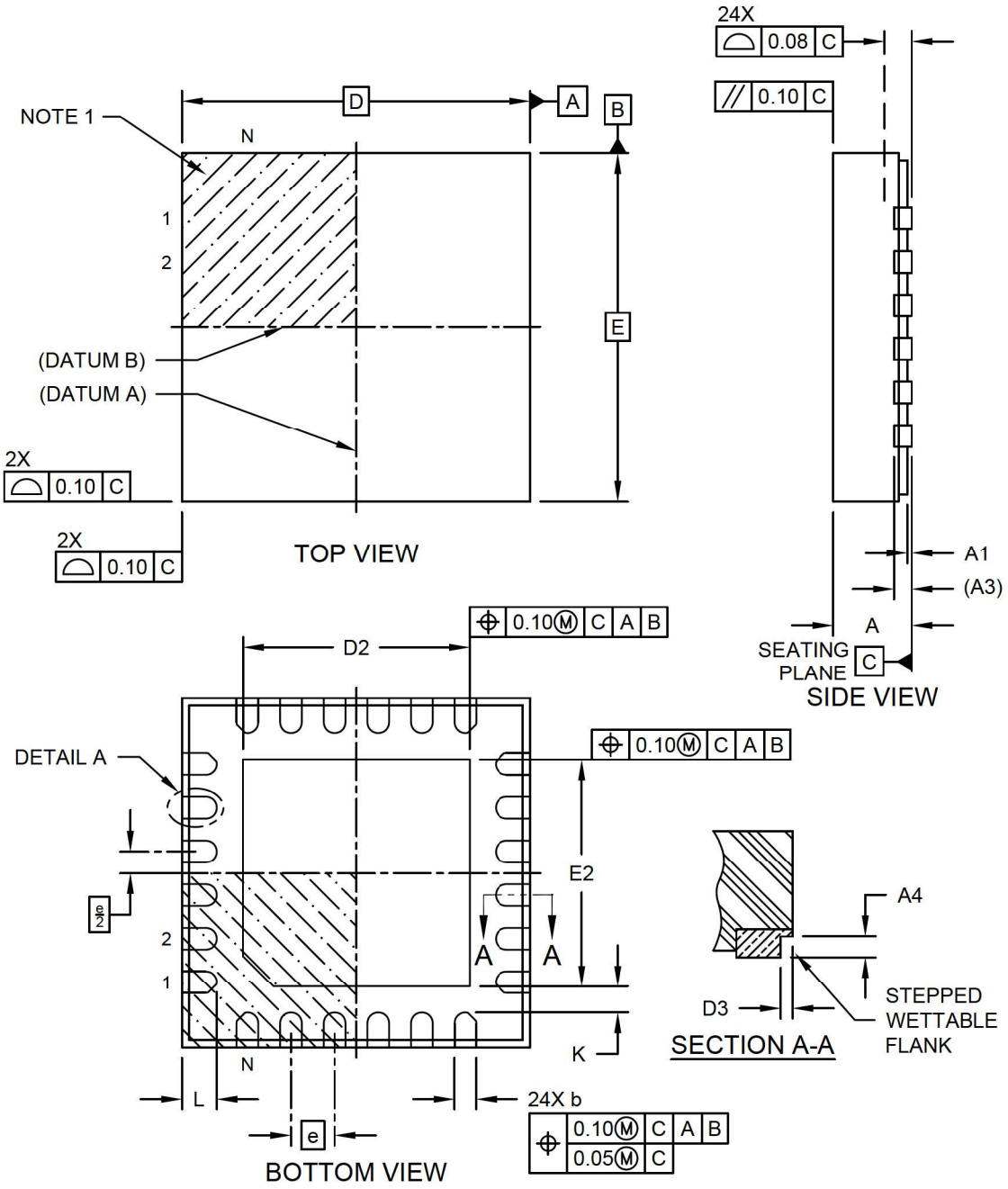
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2500 Rev B

8.2 24-VQFN (LAN8671 Only)

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

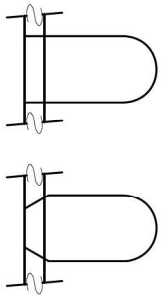
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



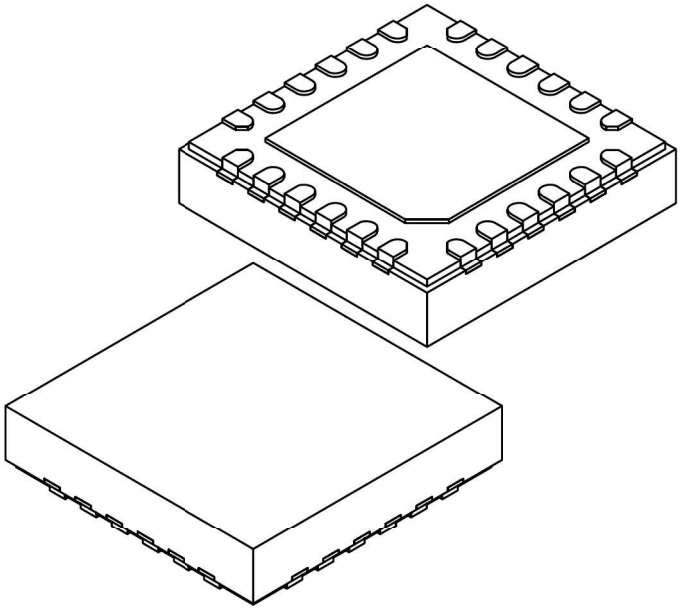
Microchip Technology Drawing C04-21483 Rev A Sheet 1 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		24	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.60	2.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Length	D3	-	-	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

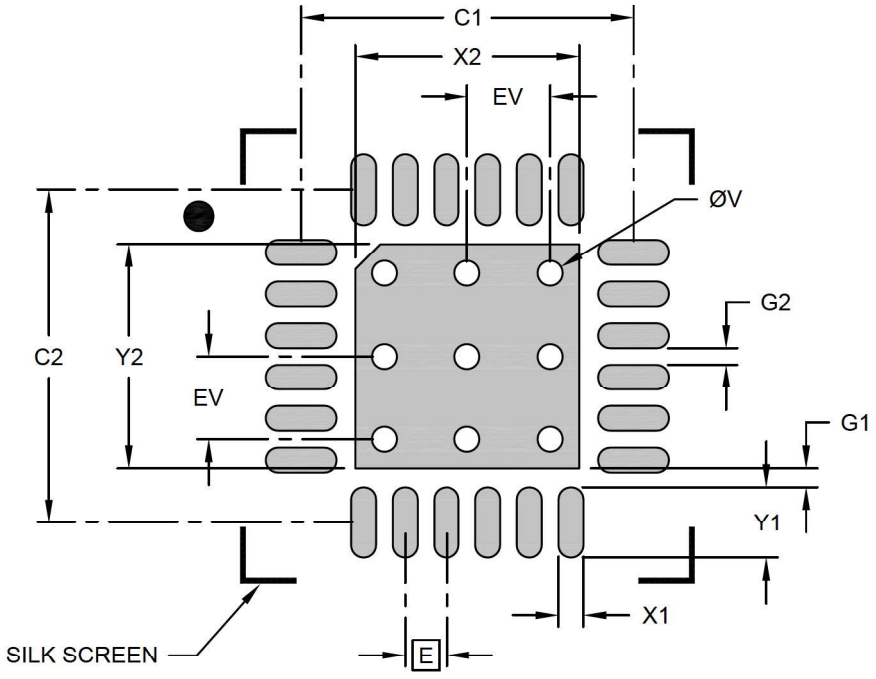
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21483 Rev A Sheet 2 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.70
Optional Center Pad Length	Y2			2.70
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X24)	X1			0.30
Contact Pad Length (X24)	Y1			0.85
Contact Pad to Center Pad (X24)	G1	0.23		
Contact Pad to Contact Pad (20)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

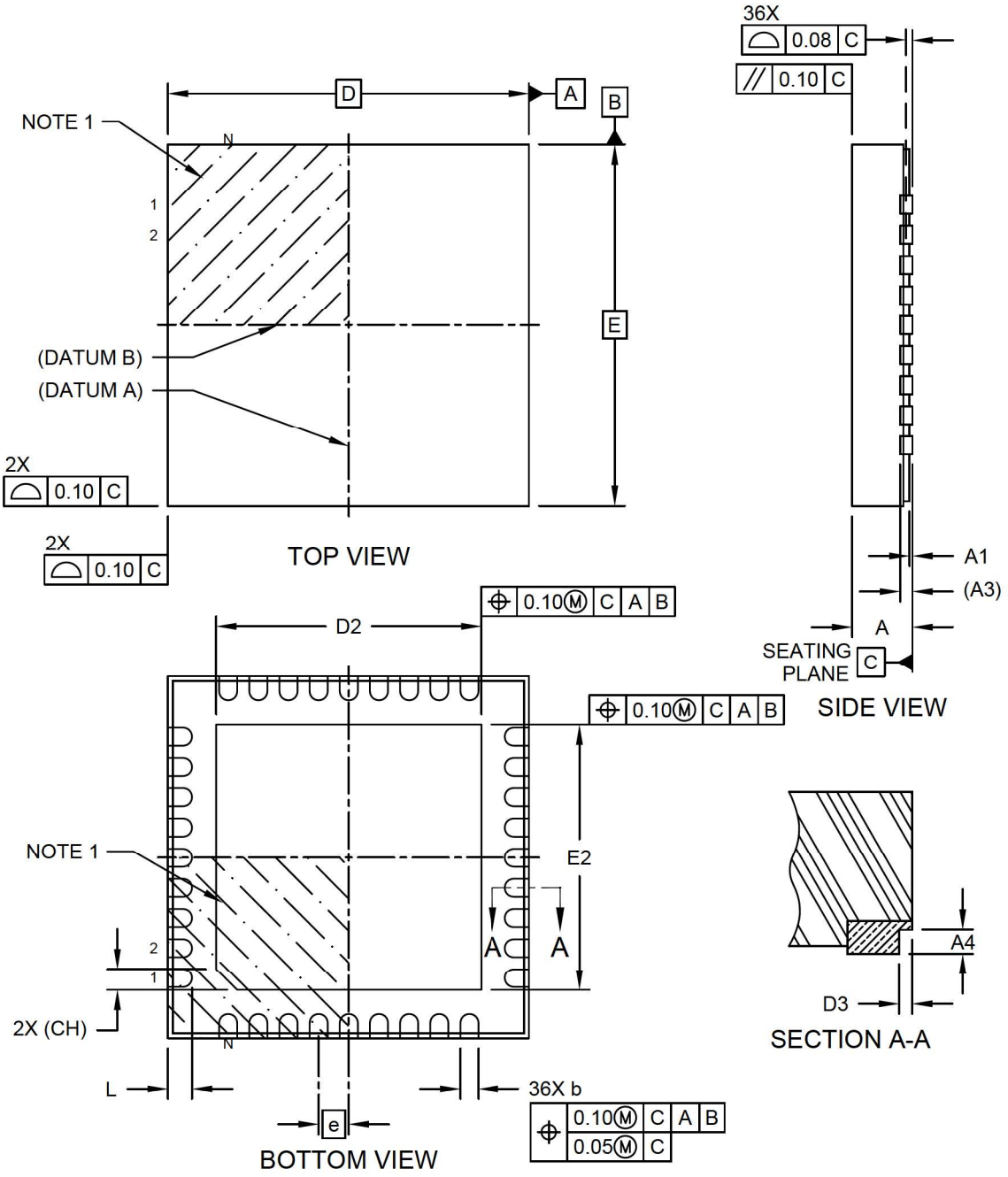
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23483 Rev A Sheet 1 of 2

8.3 36-VQFN (LAN8672 Only)

36-Lead Very Thin Plastic Quad Flat, No Lead Package (LNX) - 6x6x1.0 mm Body [VQFN] With 4.4 mm Exposed Pad and Stepped Wettable Flanks

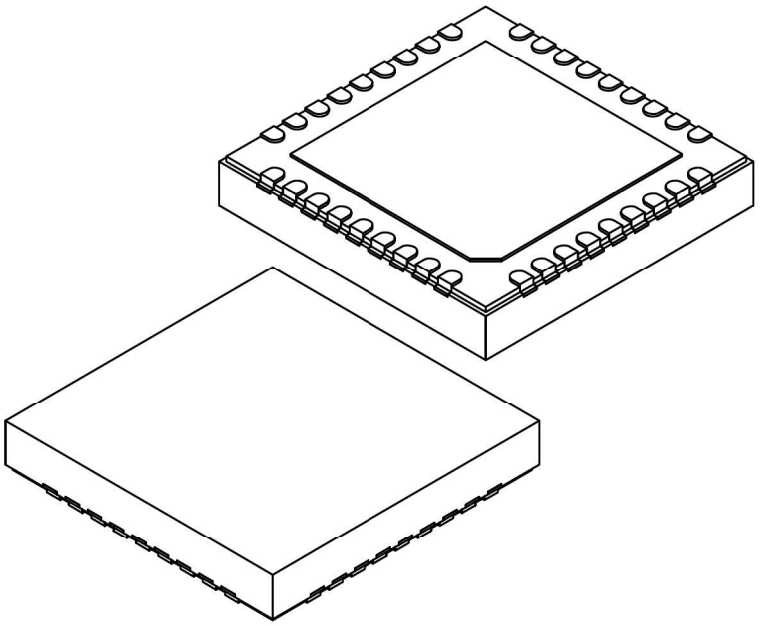
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-501 Rev B Sheet 1 of 2

36-Lead Very Thin Plastic Quad Flat, No Lead Package (LNX) - 6x6x1.0 mm Body [VQFN] With 4.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.30	4.40	4.50
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.30	4.40	4.50
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-
Exposed Pad Corner Chamfer	CH		0.35 REF	
Step Height	A4	0.10	-	0.19
Step Length	D3	0.035	0.060	0.085

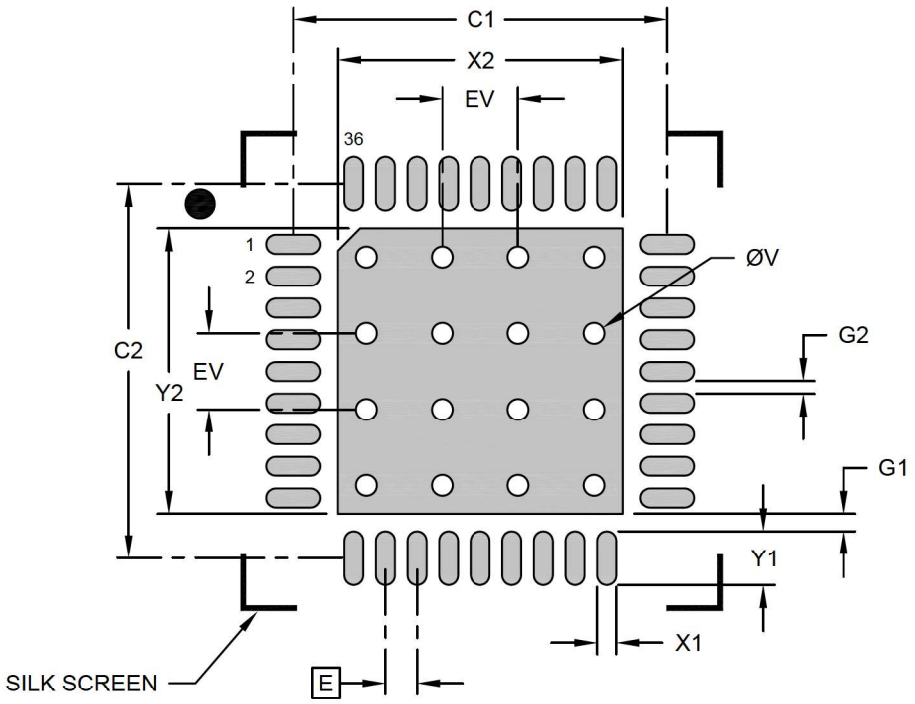
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-501 Rev B Sheet 2 of 2

36-Lead Very Thin Plastic Quad Flat, No Lead Package (LNX) - 6x6x1.0 mm Body [VQFN] With 4.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			4.50
Center Pad Length	Y2			4.50
Contact Pad Spacing	C1		5.90	
Contact Pad Spacing	C2		5.90	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.20		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

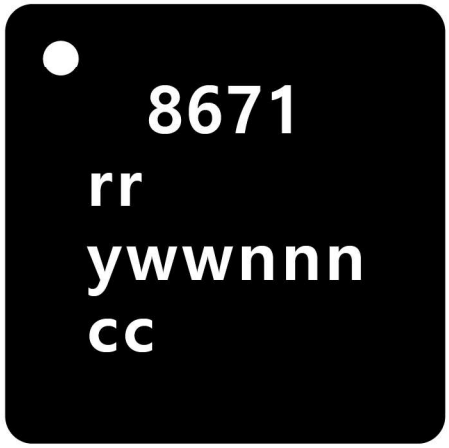
Microchip Technology Drawing C04-2501 Rev B

9. Package Marking Information

Figure 9-1. LAN8670 Top Mark

Legend:		
	LAN8670	Device Identifier
	rr	Product Revision Code
	yy	last two digits of Assembly Year
	ww	Assembly Work Week
	nnn	Tracking Number
	cc	Country of Origin Abbreviation (optional)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Figure 9-2. LAN8671 Top Mark



Legend:		
	8671	Device Identifier (LAN8671)
	rr	Product Revision Code
	y	last digit of Assembly Year
	ww	Assembly Work Week
	nnn	Tracking Number
	cc	Country of Origin Abbreviation (optional)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Figure 9-3. LAN8672 Top Mark

Legend:		
	LAN8672	Device Identifier
	rr	Product Revision Code
	yy	last two digits of Assembly Year
	ww	Assembly Work Week
	nnn	Tracking Number
	cc	Country of Origin Abbreviation (optional)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

10. Data Sheet Revision History

Table 10-1. Data Sheet Revision History

Revision Level & Date	Section/Figure/Entry	Correction
DS60001573A (Aug-2019)	All	Initial Release
DS60001573B (Feb-2021)	All	Updated Release for RevB1
DS60001573C (Jun-2021)	3	Separating unused pins that are internally connected (DNC) from those which are internally unconnected (NC)
	7.5	Updated VIS-VDDP input hysteresis; VO-VDDP, VOH-VDDP output high level drive currents; ICLK input voltage limits
	7.6.2	Updated typical rise/fall times
	7.6.6	Updated MII TXD/TXEN setup time
	7.6.7	Updated RMII RXD/RXER/CRSDV output valid time
	7.7	Updated 10BASE-T1S PMA Electrical Characteristics
	7.1	Updated ESD Machine Model rating
	4.7	Added initialization and configuration sequence
	4.9.2	Added PLCA diagnostics
	6.6	Added reference schematics
	All	Various editorial changes

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PART NO.	XX	[X](1)	-	X	/	XXX
Device	Product Revision	Tape and Reel Option		Temperature Grade		Package Type

Device:	LAN8670 10BASE-T1S Ethernet PHY Transceiver, MII/RMII LAN8671 10BASE-T1S Ethernet PHY Transceiver, RMII LAN8672 10BASE-T1S Ethernet PHY Transceiver, MII	
Product Revision:	xx	Two character code specifying product revision
Tape and Reel Option:	Blank	Standard packaging (tray)
	T	Tape and Reel(1)
Temperature Grade:	E	-40ºC to +125ºC Extended range
Package Type:	LMX	32-pin VQFN (LAN8670 only)
	U3B	24-pin VQFN (LAN8671 only)
	LNX	36-pin VQFN (LAN8672 only)

- LAN8670B1-E/LMX - 10BASE-T1S Ethernet PHY Transceiver, MII/RMII, Revision B1, Standard tray packaging, 32-VQFN package, -40ºC to +125ºC
- LAN8671B1-E/U3B - 10BASE-T1S Ethernet PHY Transceiver, RMII, Revision B1, Standard tray packaging, 24-VQFN package, -40ºC to +125ºC
- LAN8672B1-E/LNX - 10BASE-T1S Ethernet PHY Transceiver, MII, Revision B1, Standard tray packaging, 36-VQFN package, -40ºC to +125ºC
- LAN8670B1T-E/LMX - 10BASE-T1S Ethernet PHY Transceiver, MII/RMII, Revision B1, Tape and Reel packaging, 32-VQFN package, -40ºC to +125ºC

Note:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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