Tentative Product Specification

Module name: P0760WVLB-T

Issue date: 2008/12/15

Version: 1.7

Customer		
Approved by Customer		
Approved by CMEL		
PD Division	**ENG Division**	**QA Dept**

Note:

1. The information contained herein may be change without prior notice. It is therefore advisable to contact CHI MEI EL Corp. before designed your product based on this specification.
2. This tentative product specification is for reference, some item or setting maybe changed for evaluation.

Reversion History

Version	Date	Page	Description
Ver.1.0	2008/06/26	All	Tentative specification was first issued
Ver.1.1	2008/08/26	5,12~19	LVDS timing and command modify
Ver.1.2	2008/09/08	8	Modify Electro-Optical Characteristic
		21,22	Modify External Dimension Drawing
		24	Add Package Drawing
Ver.1.3	2008/09/16	8	Modify Electro-Optical Characteristic
Ver.1.4	2008/10/02	3	Modify Maximum ratings
		4	Modify Electrical Characteristic
		5	Modify AC Characteristic—LVDS
Ver.1.5	2008/11/04	8	Modify Electro-Optical Characteristic
		21,22	Modify External Dimension Drawing
Ver.1.6	2008/11/17	21,22	Modify External Dimension Drawing
Ver.1.7	2008/12/15	3	Change Absolute Maximum ratings description
		7	Add DC Characteristic—SPI
		11	Add connector type at note
		20	Add Brightness control
		23	Add Reliability Test
		24	Add Handling & Storage
		25	Modify Package Drawing

1. Purpose:

This documentation defines general product specification for OLED module supplied by CMEL. The information described in this technical specification is tentative. Please Contact CMEL's representative while your product is modified.

2. General Description:

- Driving Mode: Active Matrix
- Color Mode: Full Color (16.7M color)
- Support 3-wire SPI command setting
- Interface: LVDS interface and DE only mode.
- Auto-current limit function (ACL) for power saving mode.
- Application: Portable DVD, PMP, GPS, Photo Frame etc.
- RoHS Compatible

3. Mechanical Data:

No.	Items	Specification	Unit
1	**Diagonal Size**	7.6	Inch
2	**Resolution**	800 RGB x 480	
3	**Pixel Pitch**	207 x 207	um
4	**Active Area**	165.60 x 99.36	mm
5	**Outline Area**	177.30 x 118.32	mm
6	**Thickness**	Max 5.4	mm
7	**Weight**	150	g

4. Absolute Maximum ratings:

Absolute ratings of environment：

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-40	+80	ºC	(1)
Operating Ambient Temperature	T_{OP}	-20	+60	ºC	(2)

Note (1) The storage duration for both critical temperature (-40 & 80℃) meet reliability test criteria.

(2) The operating duration for both critical temperature (-20 & 60℃) meet reliability test criteria.

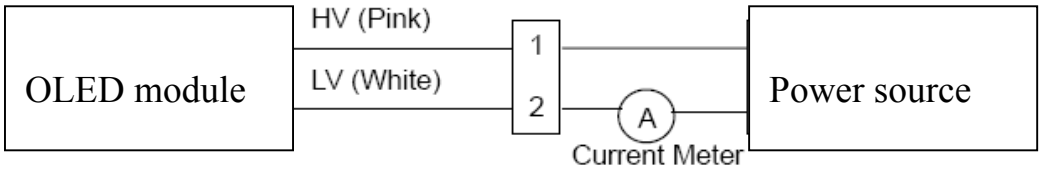
5. Electrical Characteristic:

5.1 DC Characteristic—module

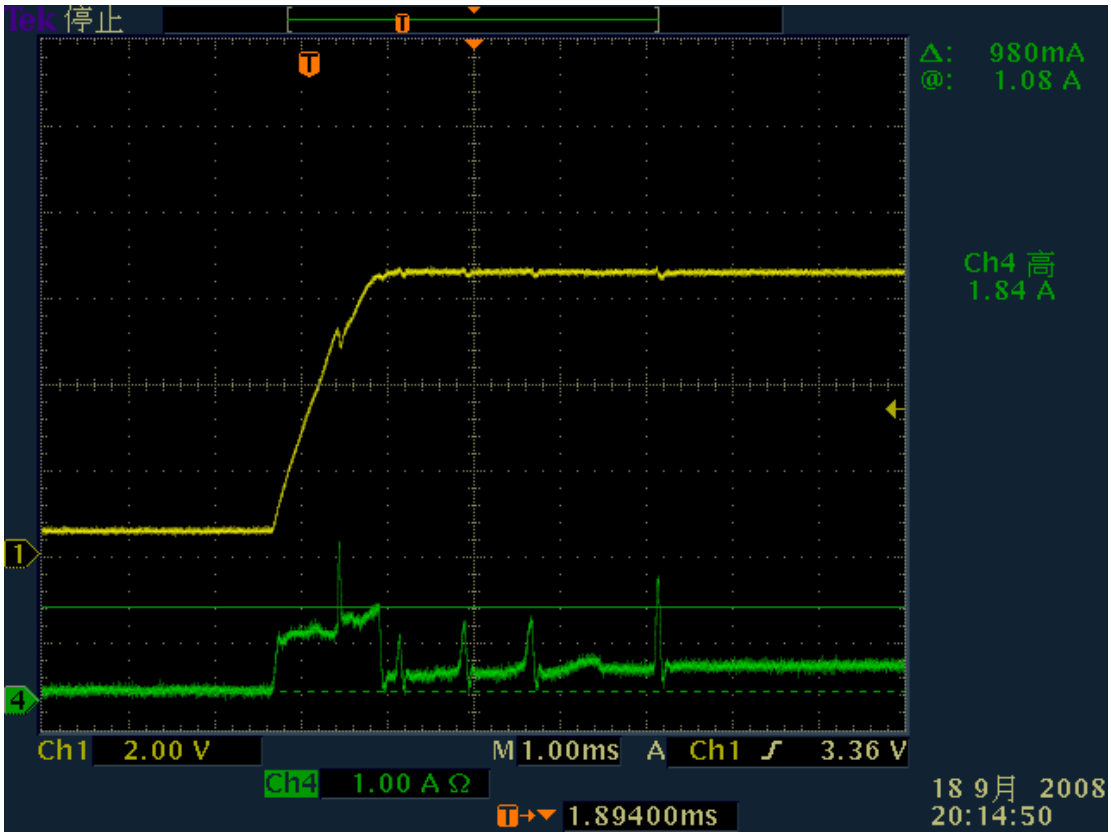
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VCI	4.5	5	5.5	V	-
Permissive Ripple Voltage	V_{PR}			100	mV	
Rush Current	I_{RUSH}		1.84		A	(2)
Initial Stage Current	I_{IS}		0.39		A	(2)

5.2 DC Characteristic—OLED

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Positive power	VDD	5.15	5.2	5.25	V	-
Negative power	VSS	-4.9	-4.8	-4.7	V	



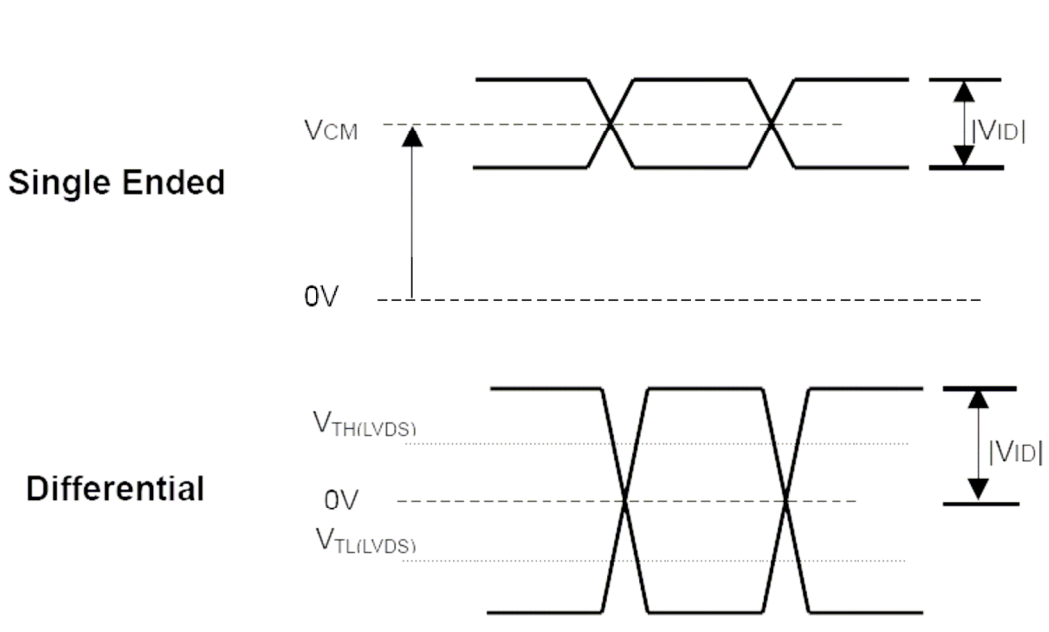
Note (2)



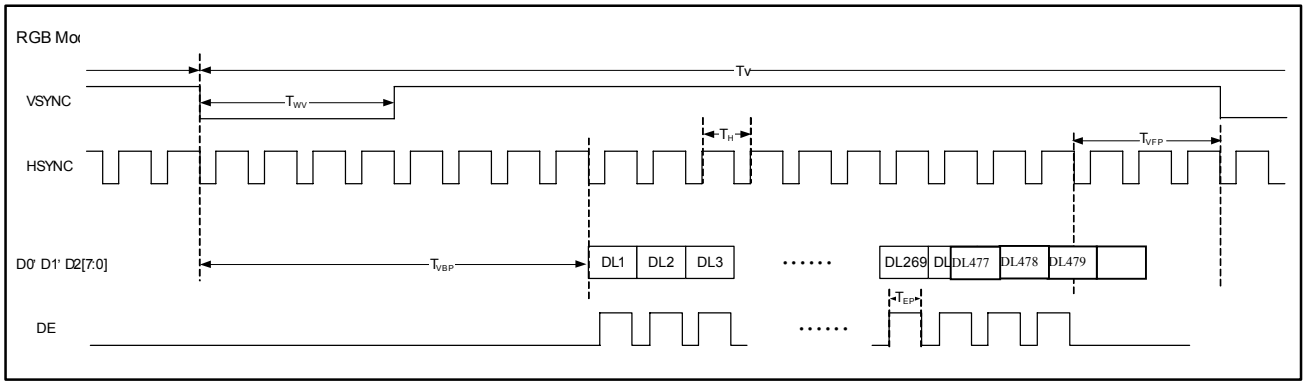
5.3 AC Characteristic—LVDS

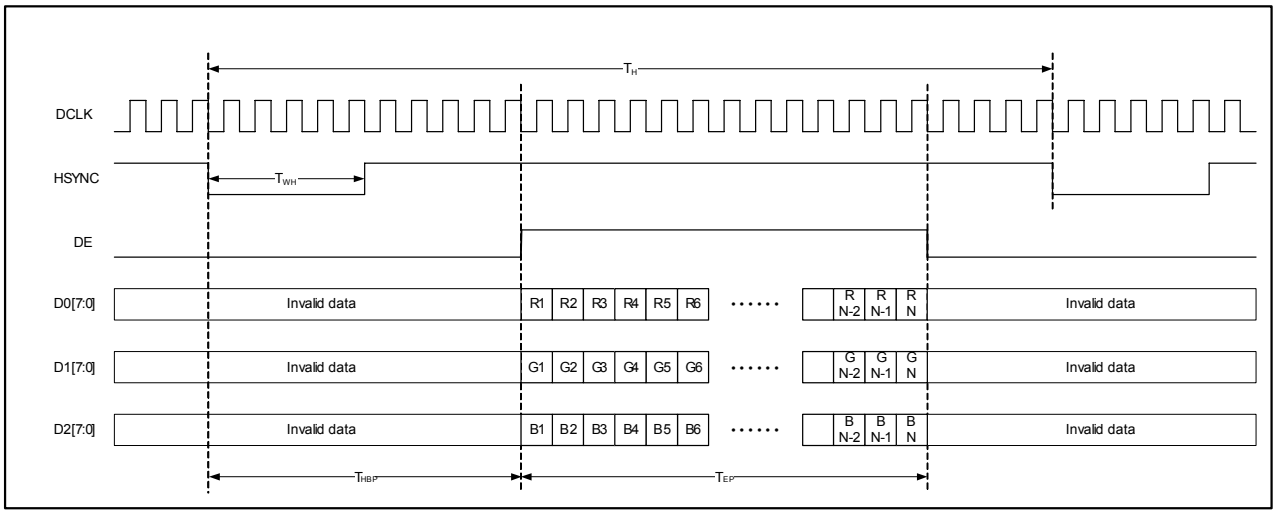
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$			+100	mV	(3)
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100			mV	(3)
LVDS Common Mode Voltage	V_{CM}	1.125	1.2	1.375	V	(3)
OLED Diode Refer Voltage	$\|V_{ID}\|$	100		600	mV	(3)
Terminating Resistor	R_T		100		Ohm	
DCLK frequency	F_{CPH}	27.08	30	-	MHz	(4)
DCLK period	T_{CPH}	-	33.3	36.93	ns	(4)
DCLK pulse duty	T_{CWH}	-	50	-	%	(4)
DE pulse width	T_{EP}	-	800	-	T_{CPH}	(4)
HSYNC pulse width	T_{WH}	10	40	-	T_{CPH}	(4)
HSYNC-first horizontal data time	T_{HBP}	100	198	-	T_{CPH}	(4)
HSYNC front porch	T_{HFP}	10	10	-	T_{CPH}	(4)
HSYNC period	T_H	910	1008	-	T_{CPH}	(4)
VSYNC pulse width	T_{WV}	3	3	-	T_H	(4)
VSYNC-1st Data input (DE) time	T_{VBP}	10	10	-	T_H	(4)
VSYNC front porch	T_{VFP}	6	6	-	T_H	(4)
VSYNC period	T_V	496	496	-	T_H	(4)

Note (3) The parameters of LVDS signals are defined as the following figures.



Note (4) The timing specification of LVDS signals are defined as the following figures.



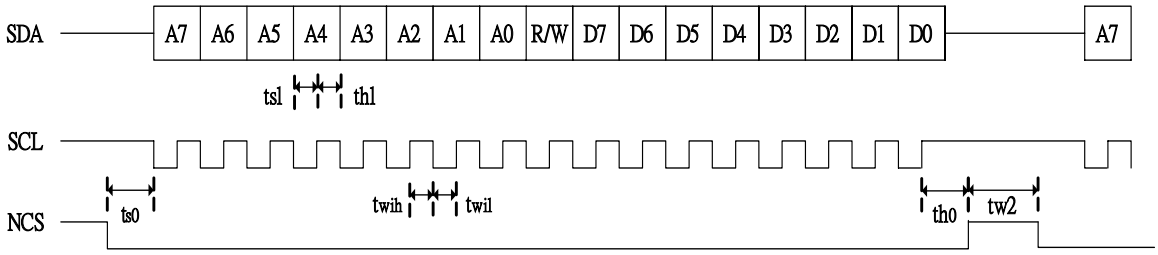


5.4 AC Characteristic—SPI

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Time from NCS to SCL	Ts0	40			ns	
Time from SCL to NCS	Th0	60			ns	
SCL low time	Twih		Tcyc/2		ns	
SCL high time	Twil		Tcyc/2		ns	
Setup time of SDA	Tsl	40			ns	
Hold time of SDA	Thl	40			ns	
NCS high pulse width	Tw2	500			ns	
Serial clocl cycle time	Tcyc	100	500		ns	
Time from NCS to SCL	Ts0	40			ns	
Time from SCL to NCS	Th0	60			ns	
SCL low time	Twih		Tcyc/2		ns	

5.5 DC Characteristic—SPI

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Logic High Input voltage	VIH	0.8*3.3		3.3	V	
Logic Low Input voltage	VIL	0		0.2*3.3	V	



6. Electro-Optical Characteristic:

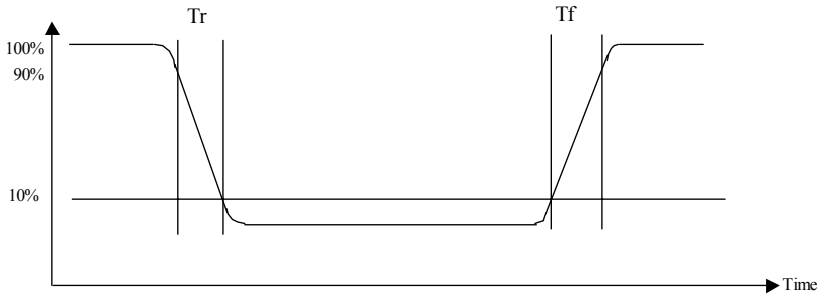
Items	Symbol	Min	Typ.	Max	Unit	Remark
Luminance	L	200		230	Cd/m^2	(1)(5)
Power Consumption	Pon			8	W	30% pixels on (1)
Maximum Current	Icc			1300	mA	(1)
Response Time	Tres			50	uS	(2)
Color Gamma	NTSC		70		%	(1)
CIEx (White)	Wx	0.25	0.28	0.31	-	(5)
CIEy (White)	Wy	0.27	0.30	0.33	-	(5)
Viewing Angle	VA	170			Degree	(3)
Contrast	CR	10000:1				(4)
Operation Lifetime	LTop	30000			Hrs	(1)(6)
Surface Reflectance				3	%	At 60 lux
Color Temperature			6500		K	
Uniformity		75	80		%	(7)

Note:
Measuring surrounding: dark room
Surrounding temperature: 25°C

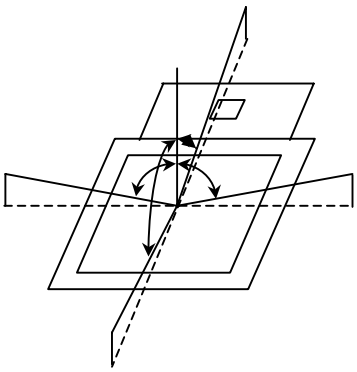
1. Test condition:
We turn on 4% area in the center of panel, and fix full white 200nits to adjust gamma code.

VDD= +5.2V, VSS= -4.8V

2. Response Time test condition



3. Viewing angle test condition:



ϕ =270°

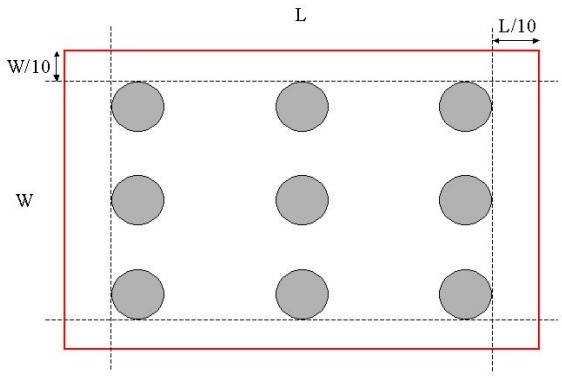
4. Contrast

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

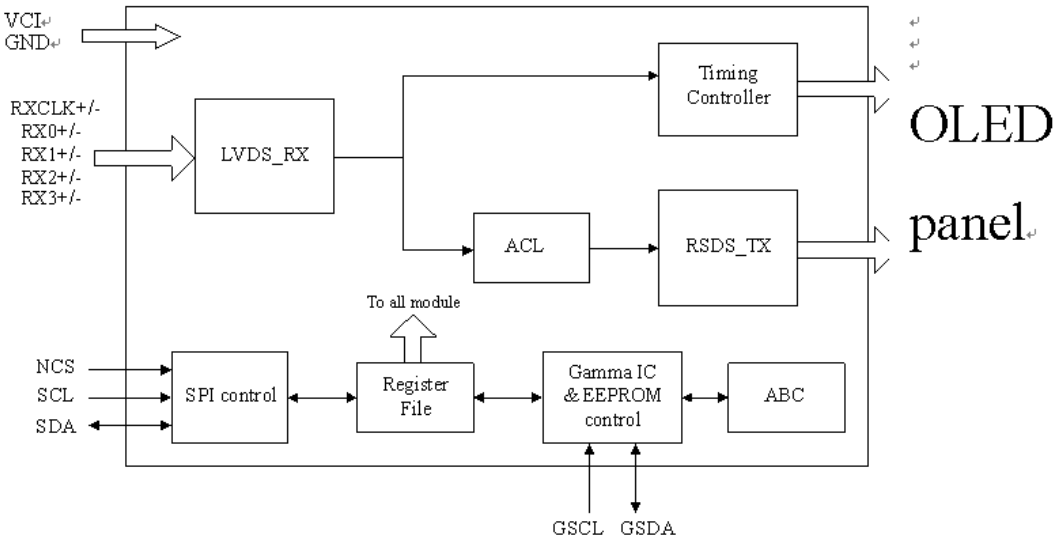
5. Optical tester: CA210 (In the display center)

6. Operation Life Time is defined when the luminance decay to less than 50% of the initial luminance during the average operation. The Luminance of the average operation is defined picture changing 30% power consumption at full on 200nits.

7. Follow VESA rule.



7. System Diagram:



8. Input Terminal Pin Assignment:

8.1 OLED module

PIN	Symbol	I/O	Description	Remarks
1	VCI	P	Power supply 5V (typical)	5V
2	GND	P	Ground	Ground
3	NC	-	Not connect	Open
4	NC	-	Not connect	Open
5	NC	-	Not connect	Open
6	NC	-	Not connect	Open
7	NC	-	Not connect	Open
8	RX0-	I	Negative LVDS differential data input, Channel 0	RX0-
9	RX0+	I	Positive LVDS differential data input, Channel 0	RX0+
10	GND	**P**	Ground	Ground
11	RX1-	I	Negative LVDS differential data input, Channel 1	RX1-
12	RX1+	I	Positive LVDS differential data input, Channel 1	RX1+
13	GND	**P**	Ground	Ground
14	RX2-	I	Negative LVDS differential data input, Channel 2	RX2-
15	RX2+	I	Positive LVDS differential data input, Channel 2	RX2+
16	GND	P	Ground	Ground
17	RXCLK-	I	Negative LVDS differential clock input	RXCLK-
18	RXCLK+	I	Positive LVDS differential clock input	RXCLK+
19	GND	P	Ground	Ground
20	RX3-	I	Negative LVDS differential data input, Channel 3	RX3-
21	RX3+	I	Positive LVDS differential data input, Channel 3	RX3+
22	GND	P	Ground	Ground
23	GND	P	Ground	Ground
24	GND	P	Ground	Ground
25	GND	P	Ground	Ground
26	SCL	I	Serial interface clock pin.	SCL
27	SDA	I/O	Serial interface data input and output line	SDA
28	NCS	I	Serial interface chip enable line	NCS
29	VCI	P	Power supply 5V (typical)	5V
30	VCI	P	Power supply 5V (typical)	5V

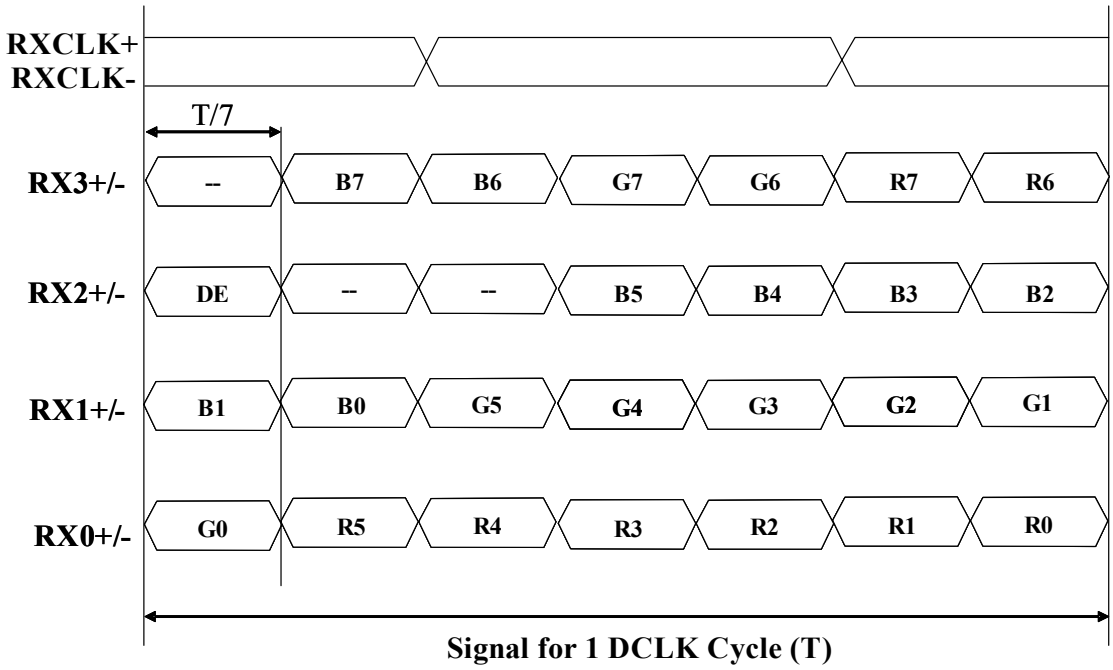
Note: (1) Connector Part No : FI-XPB30SL-HF10 or equivalent.

Note: (2) User's connector Part No : P2407P30 or equivalent.

8.2 OLED unit

PIN	Symbol	I/O	Description	Remarks
1	VDD	P	Positive power	Pink
2	VSS	P	Negative power	White

8.3 Timing Diagram of LVDS input signal



Signal for 1 DCLK Cycle (T)

8.4 Register description:

8.5

NAME	ADDR	R/W	Description
TCONCTL5	05h	R/W	[7:0] VBP: Vertical valid data start time select. 0x00: 3 HSYNC 0x01: 4 HSYNC ……. 0x07: 10 HSYNC (default) ……. 0xFE: 257 HSYNC 0xFF: 258 HSYNC Default: 07h
TCONCTL6	06h	R/W	[7:0] VFP: 0x00: 5HSYNC (default)

			0x01: 6HSYNC ……. 0xFE: 259 HSYNC 0xFF: 260 HSYNC Default: 00h
TCONCTL7	07h	R/W	[7:0] HBP: Horizontal valid data start time select. 0x00: 3 DCLK 0x01: 4 DCLK ……. 0x11: 20 DCLK (default) ……. 0xFE: 257 DCLK 0xFF: 258 DCLK Default: 11h
TCONCTL8	08h	R/W	[7:0] HFP: 0x00: 0 DCLK 0x01: 1 DCLK ……. 0x0A: 10 DCLK (default) ……. 0xFE: 254 DCLK 0xFF: 255 DCLK Default: 0Ah
TCONCTL13	0Dh	R/W	[7] PAT_SELEN: built-in pattern enable 0: disable 1: enable [6:0] PAT_SEL: built-in pattern select Default: 00h
TCONCTL14	0Eh	R/W	[5:0] R_CONSTRA: R constraint 0x00: R data x 0 0x01: R data x 1/32 …….. 0x20: R data x 32/32 …….. 0x3F: R data x 63/32

			Default: 20h
TCONCTL15	0Fh	R/W	[5:0] G_CONSTRA: G constraint 0x00: G data x 0 0x01: G data x 1/32 …….. 0x20: G data x 32/32 …….. 0x3F: G data x 63/32 Default: 20h
TCONCTL16	10h	R/W	[5:0] B_CONSTRA: B constraint 0x00: B data x 0 0x01: B data x 1/32 …….. 0x20: B data x 32/32 …….. 0x3F: B data x 63/32 Default: 20h
TCONCTL17	11h	R/W	[5:0] RGB_CONSTRA: RGB constraint 0x00: RGB data x 0 0x01: RGB data x 1/32 …….. 0x20: RGB data x 32/32 …….. 0x3F: RGB data x 63/32 Default: 20h
TCONCTL18	12h	R/W	[7:0] BRIGHT: RGB brightness 0x00: RGB data - 128 0x01: RGB data - 127 …….. 0x80: RGB data + 0 0x81: RGB data + 1 …….. 0xFF: RGB data + 127 Default: 80h
ACLCTL1	1Fh	R/W	[7:1] In-house command.

			[0] ACLEN: 0: disable ACL function 1: enable ACL function Default: 82h
SERCTL1	57h	R/W	[6:0] CNTR: GSCL frequency setting parameter GSCL frequency = DCLK / ((CNTR+1) x2) Ex. 24.7Mhz/((31+1) x2) = 24.7Mhz/64 = 386Khz Default: 1Fh
GAMCTL1	58h	R/W	[3:0] GAM_DLY: GSDA delay cycle from GSCL Default: 04h
GAMCTL2	59h	R/W	[7] BKSEL: select gamma IC memory bank 0: select bank 0 1: select bank 1 [6] A0 0: select gamma IC 1 1: select gamma IC 2 [5:0] STRADR: gamma output voltage selected address, when BUR_WRT (5Bh bit 4) is 1, STRADR represents gamma output voltage start address, other mode represent the selected address of gamma IC Default: 00h
GAMCTL3	5Ah	R/W	[7] GI2CBUSY (read only) : any action of gamma IC and EEPROM must check this bit 0: I2C bus not busy 1: I2C bus busy [5:0] ENDADR: this is useful only at BUR_WRT (5Bh bit 4) is 1, and represents the gamma output voltage end address Default: 17h
GAMCTL4	5Bh	WC	[6] GEN_RST: reset gamma IC [5] SIN_WRT: single write gamma DAC register [4] BUR_WRT: burst write gamma DAC register [3] WRT_MEM: single write gamma IC OTP [2] SIN_READ: single read gamma DAC register

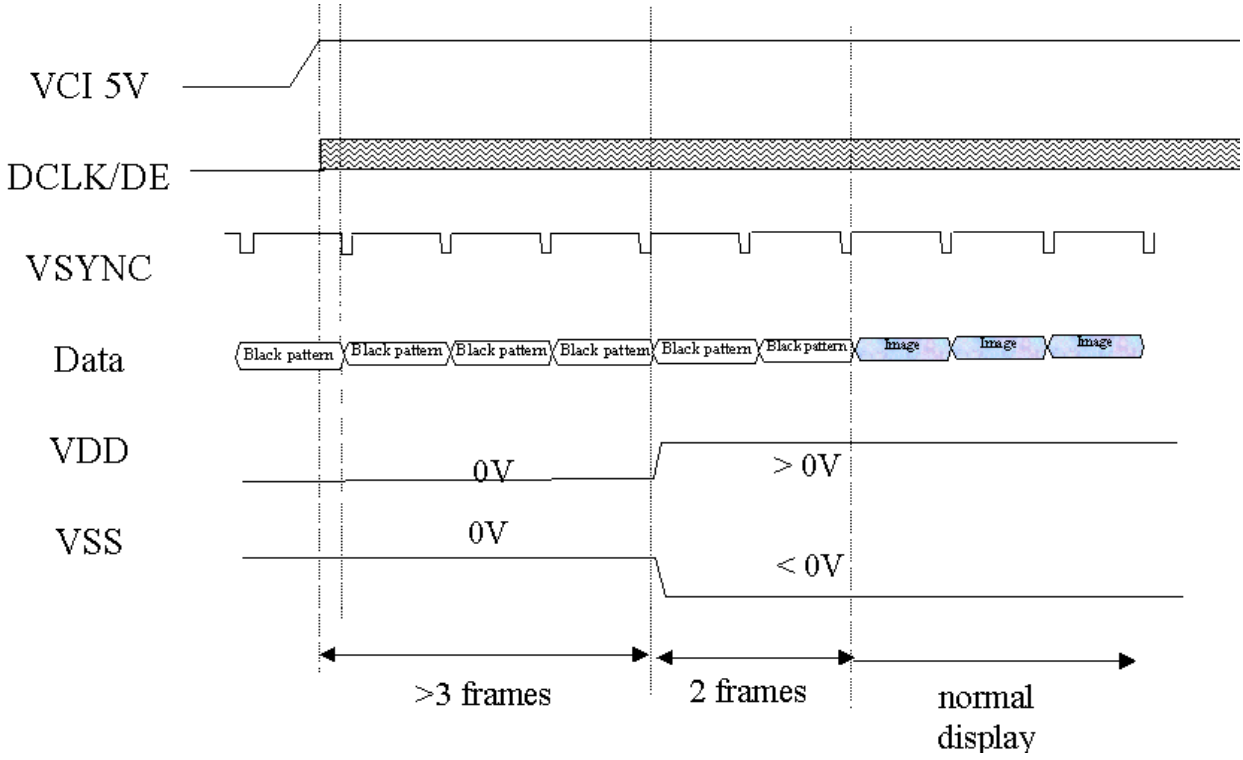
			[1] GEN_ACQ: general acquire gamma IC OTP to gamma DAC output [0] SIN_ACQ: single acquire gamma IC OTP to gamma DAC output Default: 00h
GAMCTL5	5Ch	R	[1:0] RDDATA [9:8]: high byte of read DAC register from gamma IC
GAMCTL 6	5Dh	R	[7:0] RDDATA [7:0]: low byte of read DAC register from gamma IC
EEPROM1	5Eh	R/W	[6:4] BANKSEL: select EEPROM read/write bank 000: write 5Fh ~ 86h to EEPROM bank 0 or read EEPROM bank 0 to 5Fh ~ 86h 001: write 5Fh ~ 86h to EEPROM bank 1 or read EEPROM bank 1 to 5Fh ~ 86h 010: write 5Fh ~ 86h to EEPROM bank 2 or read EEPROM bank 2 to 5Fh ~ 86h 011: write 5Fh ~ 86h to EEPROM bank 3 or read EEPROM bank 3 to 5Fh ~ 86h 1xx: write 00h ~ 5Eh to EEPROM bank4 or read EEPROM bank4 to 00h ~ 5Eh [1] EEPROM_WR (write & clear): EEPROM write [0] EEPROM_RD (write & clear): EEPROM read Default: 40h
RGAMMA01	5Fh	R/W	[7:6] DAC4 [9:8]: R_GAMMA30 high byte [5:4] DAC3 [9:8]: R_GAMMA15 high byte [3:2] DAC2 [9:8]: R_GAMMA5 high byte [1:0] DAC1 [9:8]: R_GAMMA0 high byte
RGAMMA02	60h	R/W	[7:0] DAC1 [7:0]: R_GAMMA0 low byte
RGAMMA03	61h	R/W	[7:0] DAC2 [7:0]: R_GAMMA5 low byte
RGAMMA04	62h	R/W	[7:0] DAC3 [7:0]: R_GAMMA15 low byte
RGAMMA05	63h	R/W	[7:0] DAC4 [7:0]: R_GAMMA30 low byte

RGAMMA06	64h	R/W	[7:6] DAC8 [9:8]: R_GAMMA255 high byte [5:4] DAC7 [9:8]: R_GAMMA168 high byte [3:2] DAC6 [9:8]: R_GAMMA84 high byte [1:0] DAC5 [9:8]: R_GAMMA50 high byte
RGAMMA07	65h	R/W	[7:0] DAC5 [7:0]: R_GAMMA50 low byte
RGAMMA08	66h	R/W	[7:0] DAC6 [7:0]: R_GAMMA84 low byte
RGAMMA09	67h	R/W	[7:0] DAC7 [7:0]: R_GAMMA168 low byte
RGAMMA10	68h	R/W	[7:0] DAC8 [7:0]: R_GAMMA255 low byte
GGAMMA01	69h	R/W	[7:6] DAC12 [9:8]: G_GAMMA30 high byte [5:4] DAC11 [9:8]: G_GAMMA15 high byte [3:2] DAC10 [9:8]: G_GAMMA5 high byte [1:0] DAC9 [9:8]: G_GAMMA0 high byte
GGAMMA02	6Ah	R/W	[7:0] DAC9 [7:0]: G_GAMMA0 low byte
GGAMMA03	6Bh	R/W	[7:0] DAC10 [7:0]: G_GAMMA5 low byte
GGAMMA04	6Ch	R/W	[7:0] DAC11 [7:0]: G_GAMMA15 low byte
GGAMMA05	6Dh	R/W	[7:0] DAC12 [7:0]: G_GAMMA30 low byte
GGAMMA06	6Eh	R/W	[7:6] DAC16 [9:8]: G_GAMMA255 high byte [5:4] DAC15 [9:8]: G_GAMMA168 high byte [3:2] DAC14 [9:8]: G_GAMMA84 high byte [1:0] DAC13 [9:8]: G_GAMMA50 high byte
GGAMMA07	6Fh	R/W	[7:0] DAC13 [7:0]: G_GAMMA50 low byte
GGAMMA08	70h	R/W	[7:0] DAC14 [7:0]: G_GAMMA84 low byte
GGAMMA09	71h	R/W	[7:0] DAC15 [7:0]: G_GAMMA168 low byte

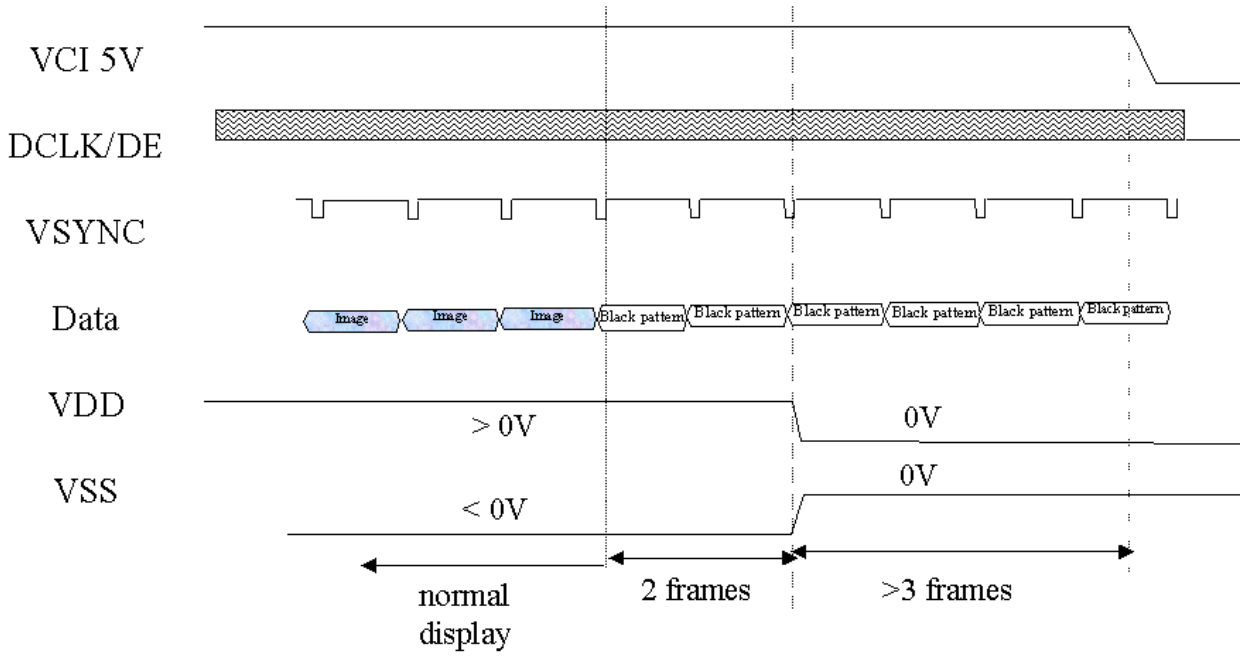
GGAMMA10	72h	R/W	[7:0] DAC16 [7:0]: G_GAMMA255 low byte
BGAMMA01	73h	R/W	[7:6] DAC20 [9:8]: B_GAMMA30 high byte [5:4] DAC19 [9:8]: B_GAMMA15 high byte [3:2] DAC18 [9:8]: B_GAMMA5 high byte [1:0] DAC17 [9:8]: B_GAMMA0 high byte
BGAMMA02	74h	R/W	[7:0] DAC17 [7:0]: B_GAMMA0 low byte
BGAMMA03	75h	R/W	[7:0] DAC18 [7:0]: B_GAMMA5 low byte
BGAMMA04	76h	R/W	[7:0] DAC19 [7:0]: B_GAMMA15 low byte
BGAMMA05	77h	R/W	[7:0] DAC20 [7:0]: B_GAMMA30 low byte
BGAMMA06	78h	R/W	[7:6] VCOM2 [9:8]: B_GAMMA255 high byte [5:4] VCOM1 [9:8]: B_GAMMA168 high byte [3:2] DAC22 [9:8]: B_GAMMA84 high byte [1:0] DAC21 [9:8]: B_GAMMA50 high byte
BGAMMA07	79h	R/W	[7:0] DAC21 [7:0]: B_GAMMA50 low byte
BGAMMA08	7Ah	R/W	[7:0] DAC22 [7:0]: B_GAMMA84 low byte
BGAMMA09	7Bh	R/W	[7:0] VCOM1 [7:0]: B_GAMMA168 low byte
BGAMMA10	7Ch	R/W	[7:0] VCOM2 [7:0]: B_GAMMA255 low byte
EEPROM2	FFh	R/W	[0] EE_RDEN: this bit have to use with EEPROM_WR (5Eh bit1), when this bit set high first and write EEPROM_WR = 1, the register 00h ~ 5Eh default value are download by EEPROM after the system power on

9. Power sequence.

9.1 Power on sequence



9.2 Power off sequence

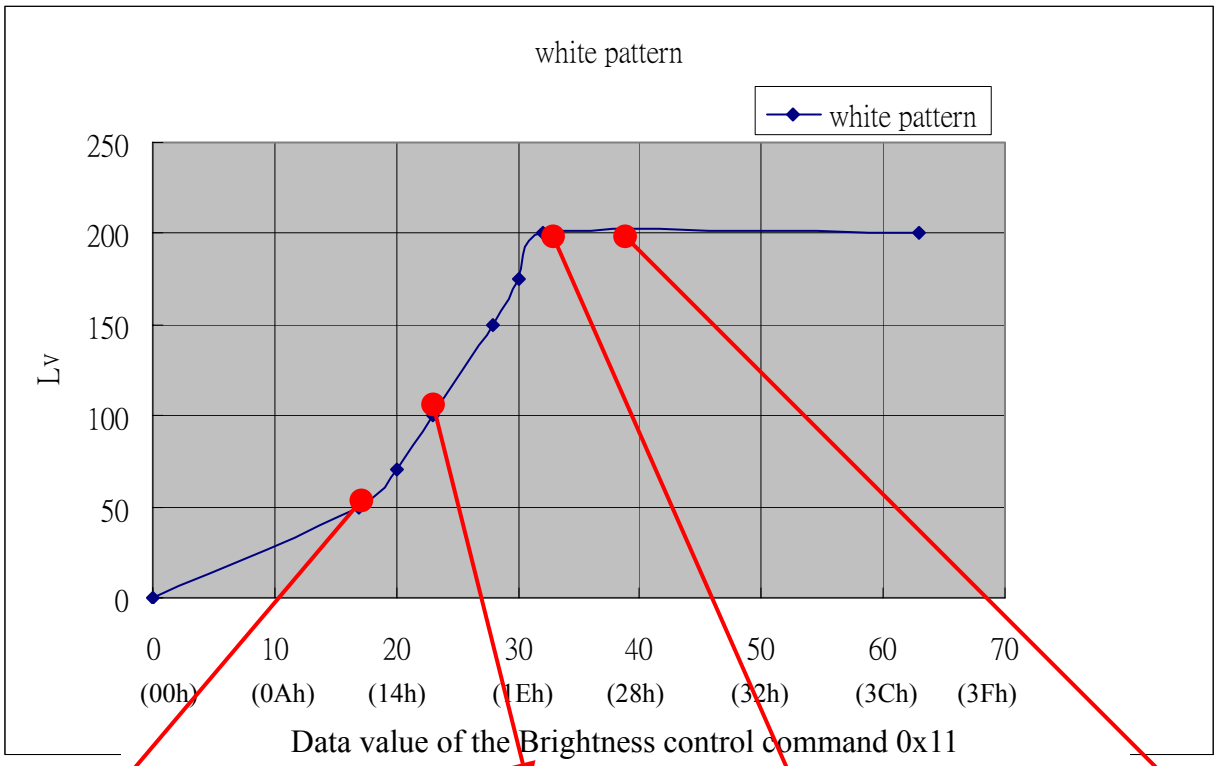


10. Brightness control

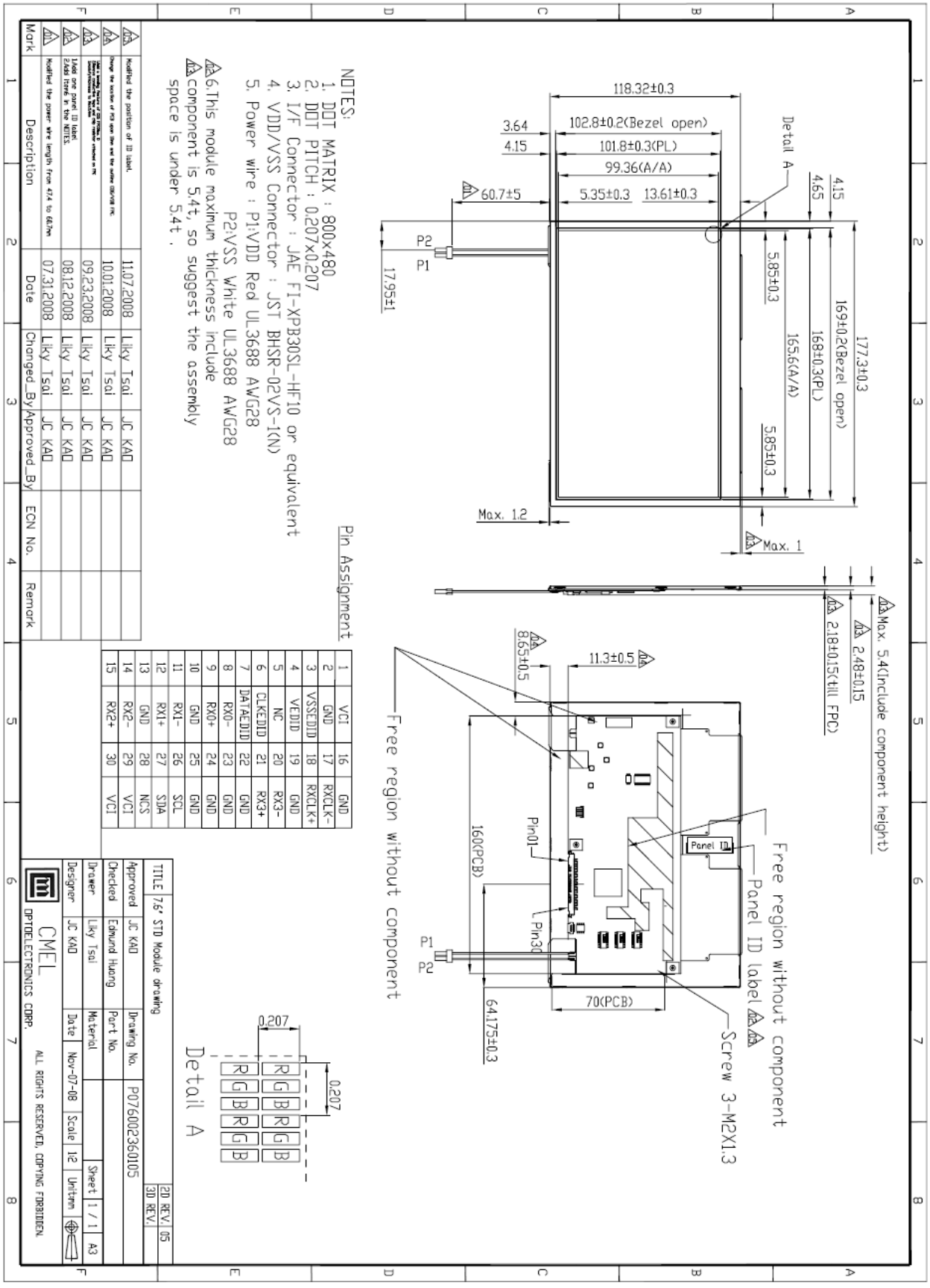
Index_out(0x11); Parameter_out(0x20); //set brightness

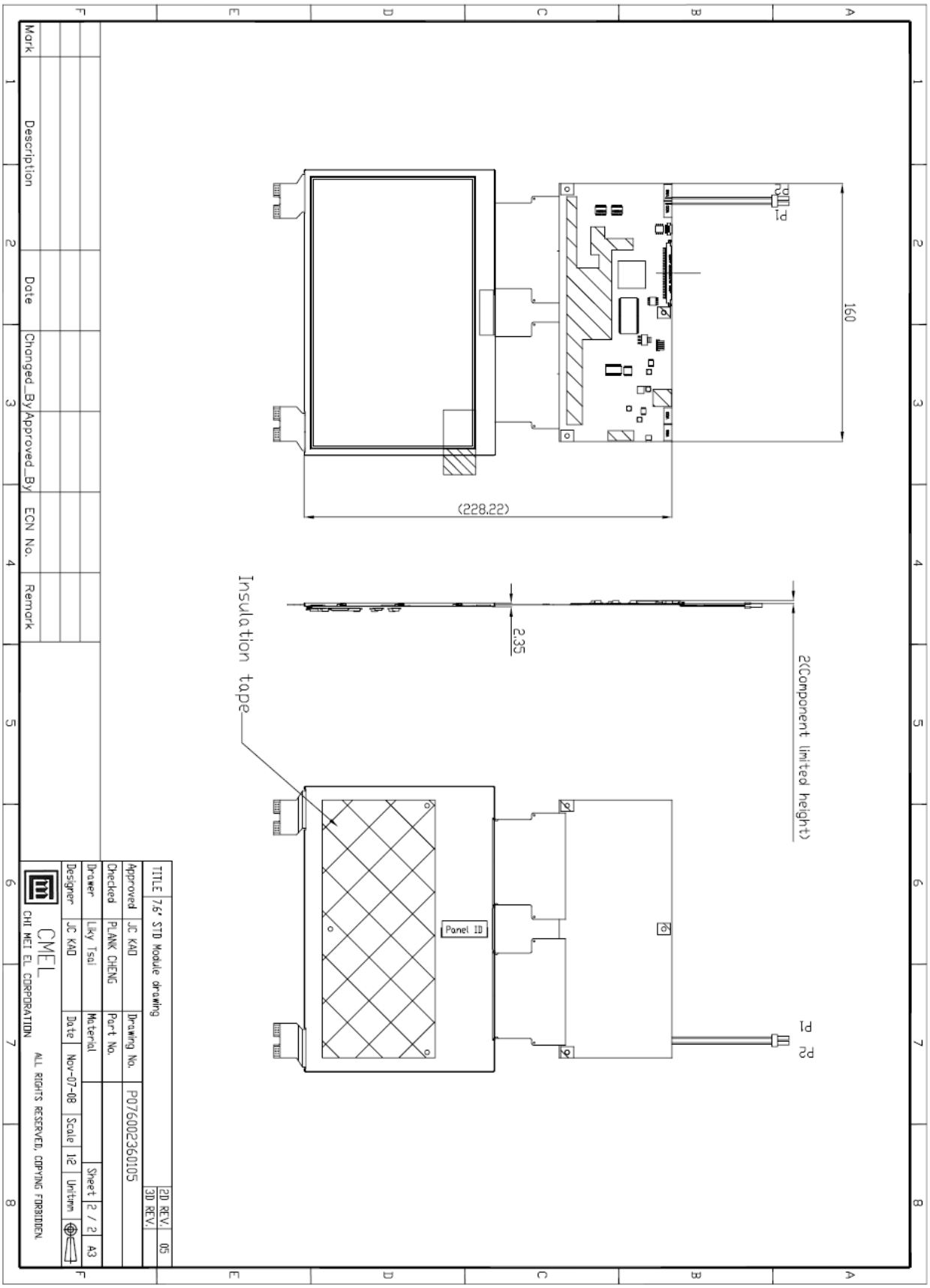
Example: if the garget specification is 200nit in white pattern.

Index_out(0x11); Parameter_out(0x20); => 200nit
Index_out(0x11); Parameter_out(0x1D); => 170nit
Index_out(0x11); Parameter_out(0x1C); => 150nit
Index_out(0x11); Parameter_out(0x19); => 125nit
Index_out(0x11); Parameter_out(0x17); => 100nit
Index_out(0x11); Parameter_out(0x14); => 75nit
Index_out(0x11); Parameter_out(0x11); => 50nit



11. External Dimension:




160
(228.22)
2.35
Insulation tape
2(Component limited height)
Panel ID
P1
P2
Mark
Description
Date
Changed_By
Approved_By
ECN No.
Remark
TITLE 7.6' STD Module drawing
Drawing No. P07600236005
2D REV. 05
3D REV.
Approved JC KAO
Checked PLANK CHENG
Drawer Liky Tsai
Designer JC KAO
Part No.
Material
Date Nov-07-08
Scale 1:2
Unit mm
Sheet 2 / 2
A3
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12. Reliability Test:

No.	Items	Specification
1	High Temp. Storage	85°C, 240hrs
2	Low Temp. Storage	-40°C, 240hrs
3	High Temp. Operation	60°C, 240hrs
4	Low Temp. Operation	-40°C, 240hrs
5	High Temp / Humidity Storage	85°C, 85%RH, 240hrs
6	High Temp / Humidity Operation	60°C, 90%RH, 240hrs
7	Thermal shock	-40°C ~85°C (-40°C /30min; transit/3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles
8	Vibration	Frequency: 5~50HZ, 0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X, Y, Z
9	Drop	Height: 76cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1
10	ESD	Air discharge model, ±8kV, 10 times

Test and measurement conditions

- All measurements shall not be started until the specimens attain to temperature stability.
- The degradation of polarizer is ignored for item 1, 5 & 6.
- The test pattern at operating condition is 30%P.C. alternating pictures.

Evaluation Criteria

- No damage to glass or encapsulation
- No drastic change to display
- Defects / Mura follow product specification
- Luminance: Within +/-50% of initial value
- Current consumption: within +/-50% of initial value

13. Handling:

13.1 Do not scratch the surface of the polarizer film as it is easily damaged.

13.2 When cleaning the display surface, use soft cloth with solvent (as recommended below) and wipe lightly

- Ethyl alcohol
- Isopropyl alcohol

13.3 Do not wipe the display surface with dry or hard materials that damage the polarizer surface.

13.4 Since this OLED panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

13.5 Do not disassemble the OLED module as it may cause permanent damage.

13.6 Hold OLED very carefully when placing OLED module into the system housing. Do not excessive stress or pressure to OLED module.

14. Storage

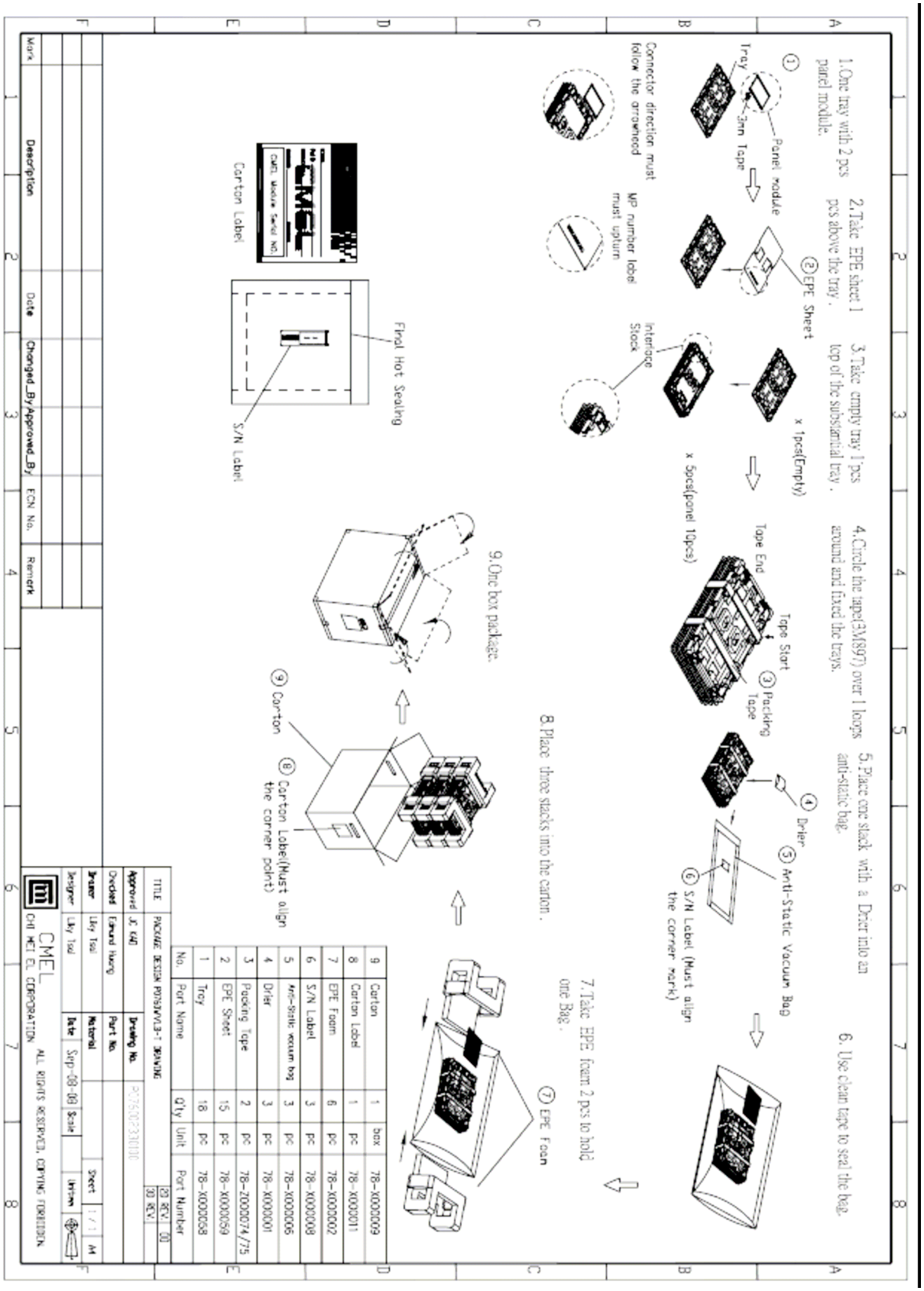
14.1 Storing in a polyethylene bag with the opening sealed.

14.2 Placing in a dark place where neither exposure to direct sunlight nor any fluorescent light is permitted and keep at room temperature & room humidity.

14.3 Storing with no contact with polarizer surface.

（It is recommended to store them in the inner container which we delivered.）

15. Package:


1.One tray with 2 pcs panel module.
2.Take EPE sheet 1 pcs above the tray.
3.Take empty tray 1 pcs top of the subsidmial tray.
4.Circle the tape(3M897) over 1 loops around and fixed the trays.
5.Place one stack with a Drier into an anti-static bag.
6. Use clean tape to seal the bag.
7.Take EPE foam 2 pcs to hold one Bag.
8.Place three stacks into the carton.
9.One box package.
Tray
3mm Tape
Panel module
②EPE Sheet
x 1pcs(Empty)
x 5pcs(panel 10pcs)
Connector direction must follow the arrowhead
MP number label must upturn
Interface Stock
Tape End
Tape Start
③ Packing Tape
④ Drier
⑤ Anti-Static Vacuum Bag
⑥ S/N Label (Must align the corner mark)
⑦ EPE Foam
⑧ Carton Label(Must align the corner point)
⑨ Carton
Carton Label
Final Hot Sealing
S/N Label
Mark
Description
Date
Changed_By
Approved_By
ECN No.
Remark
TITLE PACKAGE DESIGN P070VVL3-T DRAWING
Approved JC Cai
Checked Edmund Huang
Drawer Lily Tsai
Designer Lily Tsai
Drawing No. PK7S0P33000
Part No.
Material
Date Sep-08-06
Scale
Sheet 1 / 1
A4
Unless
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No. Part Name Q'ty Unit Part Number
9 Carton 1 box 78-X000009
8 Carton Label 1 pc 78-X000011
7 EPE Foam 6 pc 78-X000002
6 S/N Label 3 pc 78-X000008
5 Anti-Static vacuum bag 3 pc 78-X000006
4 Drier 3 pc 78-X000001
3 Packing Tape 2 pc 78-Z000074/75
2 EPE Sheet 15 pc 78-X000059
1 Tray 18 pc 78-X000058
(3) REV. 00
(0) REV.