Datasheet

Power Management IC
For Automotive R-Car Series

BD9573MUF-M

General Description

BD9573MUF-M is a Power Management Integrated Circuit (PMIC) designed specifically for use on R-Car series processor for In-Vehicle Infotainment (IVI) systems and Instrument Cluster Panel.

Features

- AEC-Q100 Qualified*(Note 1)*
- Customizable Power Up / Down Sequence and State Control
- Fewer External Components Count / Compact Size
- Power Control Logic with Processor Interface and Event Detection
- Built-in UVLO, SCP, OVP, UVP, OCP and TSD Protection

(Note 1) Grade 2

Applications

- In-Vehicle Infotainment (IVI) Systems
- Instrument Cluster Panel

Key Specifications

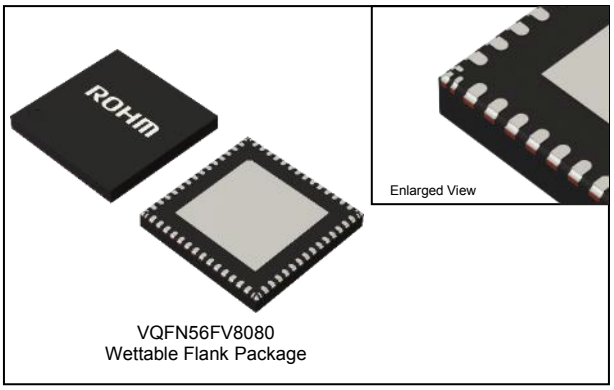
- Input Voltage Range: 3.0 V to 3.6 V
- VOUT1 (VD50) Output Voltage: 5 V (Typ)
- VOUT1 (VD50) Output Current: 0.2 A (Max)
- VOUT2 (VD18) Output Voltage: 1.8 V (Typ)
- VOUT2 (VD18) Output Current: 1.0 A (Max)
- VOUT3 (DDR) Output Voltage: 1.35 V (Typ, DDR3L)*(Note 2)* / 1.50 V (Typ, DDR3)*(Note 2)*
- VOUT3 (DDR) Output Current: 2.0 A (Max)
- VOUT4 (VD10A, VD10B) Output Voltage: 1.03 V (Typ)
- VOUT4 (VD10A, VD10B) Output Current: 5.2 A (Max)
- VOUTL1 (VL25) Output Voltage: 2.5 V (Typ)
- VOUTL1 (VL25) Output Current: 0.15 A (Max)
- VOUTS1 (VS33) Output Voltage: VIN7 = 3.3 V (Typ)
- VOUTS1 (VS33) Output Current: 0.3 A (Max)
- Operating Ambient Temperature Range: -40 °C to +105 °C

(Note 2) Select Voltage by the DDR_SEL pin.

Special Characteristics

Output Voltage:
(VOUT1 (VD50), VOUT2 (VD18), VOUT3 (DDR), VOUT4 (VD10A, VD10B), VOUTL1 (VL25), VOUTS1 (VS33))

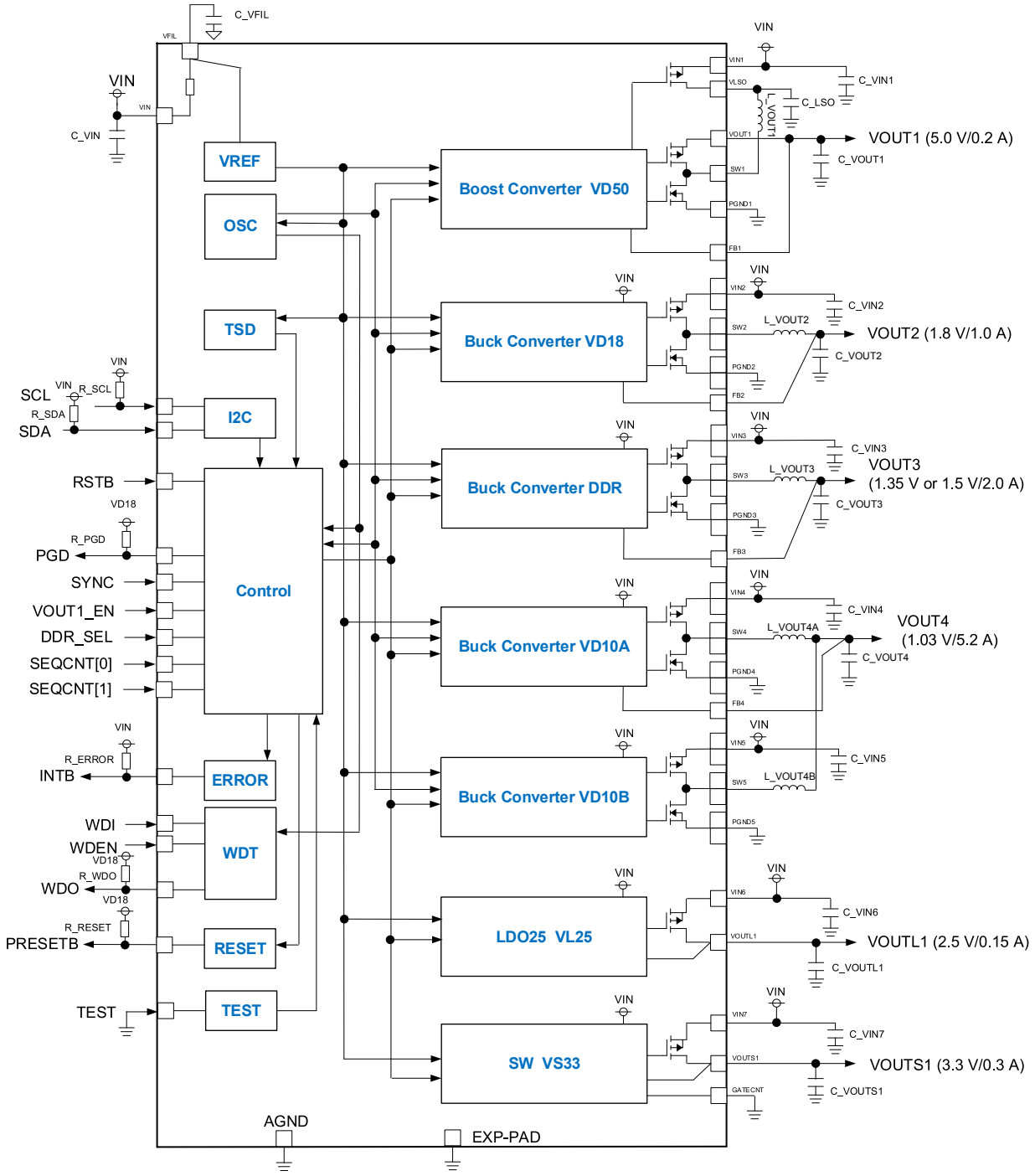
Package	W (Typ) x D (Typ) x H (Max)
VQFN56FV8080 (Wettable Flank)	8.0 mm x 8.0 mm x 1.0 mm



VQFN56FV8080
Wettable Flank Package

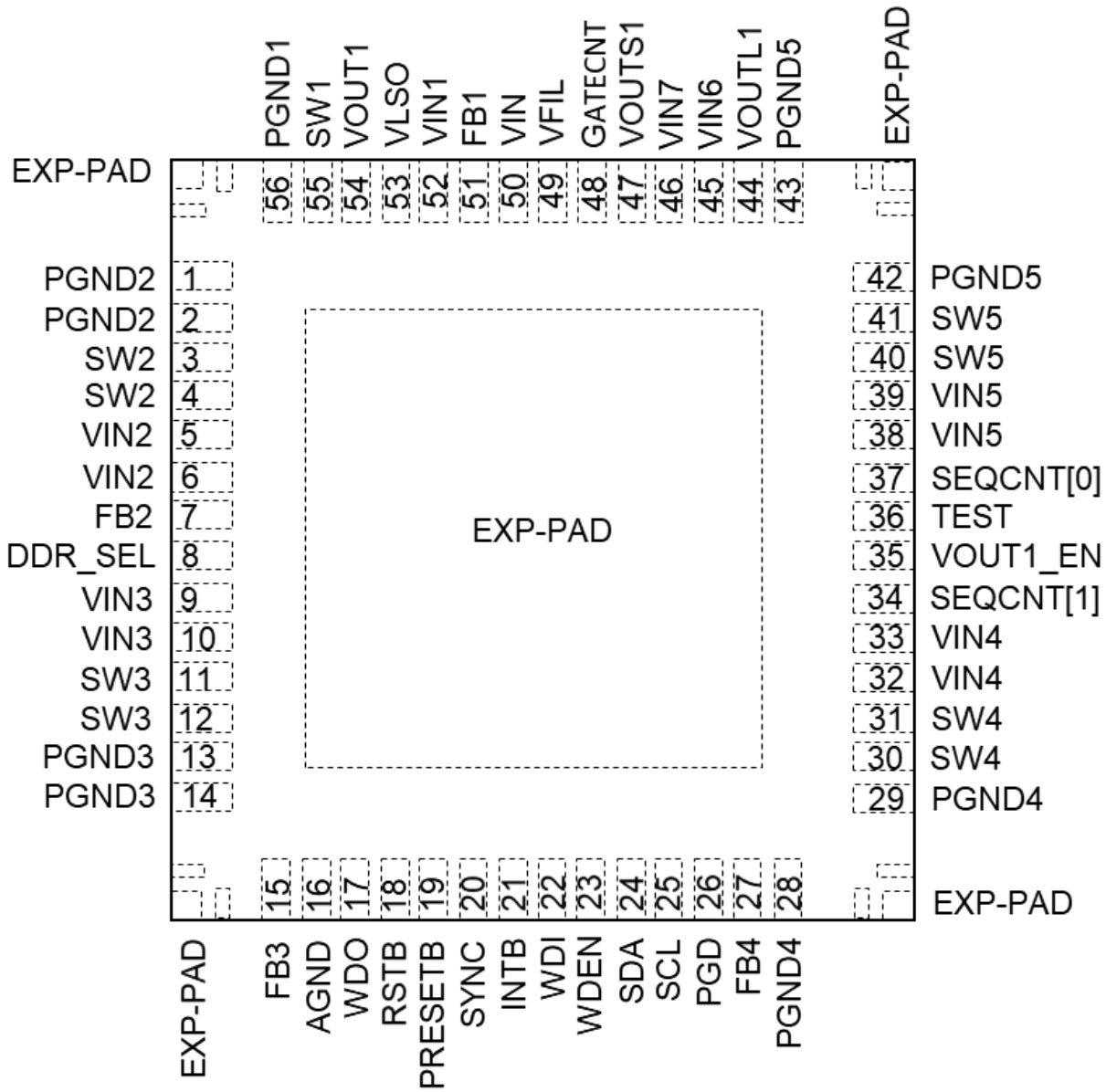
○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Block Diagram



Pin Configuration

(TOP VIEW)



Pin Description

Pin No.	Pin Name	I/O	Function
1	PGND2	-	Power GND for VOUT2
2	PGND2	-	Power GND for VOUT2
3	SW2	O	High side MOSFET source / Low side MOSFET sink pin for VOUT2
4	SW2	O	High side MOSFET source / Low side MOSFET sink pin for VOUT2
5	VIN2	I (POWER)	Power supply for VOUT2
6	VIN2	I (POWER)	Power supply for VOUT2
7	FB2	I	Feedback pin for VOUT2
8	DDR_SEL	I	VOUT3 Voltage is changed by DDR_SEL. DDR_SEL = H: 1.5 V, DDR_SEL = L: 1.35 V (internal 100 kΩ pull down)
9	VIN3	I (POWER)	Power supply for VOUT3
10	VIN3	I (POWER)	Power supply for VOUT3
11	SW3	O	High side MOSFET source / Low side MOSFET sink pin for VOUT3
12	SW3	O	High side MOSFET source / Low side MOSFET sink pin for VOUT3
13	PGND3	-	Power GND for VOUT3
14	PGND3	-	Power GND for VOUT3
15	FB3	I	Feedback pin for VOUT3
16	AGND	-	GND
17	WDO	O (O.D.)*(Note 1)*	Watchdog Timer error signal.
18	RSTB	I	Power On (internal 100 kΩ pull down)
19	PRESETB	O (O.D.)*(Note 1)*	Reset signal for SoC
20	SYNC	I	External sync for DCDC (internal 100 kΩ pull down)
21	INTB	O (O.D.)*(Note 1)*	Interrupt signal
22	WDI	I	Clock signal input as Watch Dog Timer function. (internal 100 kΩ pull down)
23	WDEN	I	Watch Dog Timer function setting ON/OFF. (internal 100 kΩ pull down)
24	SDA	I/O (O.D.)*(Note 1)*	I2C Data
25	SCL	I/O (O.D.)*(Note 1)*	I2C CLK
26	PGD	O (O.D.)*(Note 1)*	POWER Good Function
27	FB4	I	Feedback pin for VOUT4
28	PGND4	-	Power GND for VOUT4
29	PGND4	-	Power GND for VOUT4
30	SW4	O	High side MOSFET source / Low side MOSFET sink pin for VOUT4
31	SW4	O	High side MOSFET source / Low side MOSFET sink pin for VOUT4
32	VIN4	I (POWER)	Power supply for VOUT4
33	VIN4	I (POWER)	Power supply for VOUT4
34	SEQCNT[1]	I	Adjust shutdown timing of VD18. Multi-threshold PIN. (internal 2 MΩ pull down)
35	VOUT1_EN	I	Enable control pin for VOUT1 (internal 100 kΩ pull down)
36	TEST	I	Connected to AGND. TEST MODE PIN
37	SEQCNT[0]	I	Adjust start and OFF timing. Multi-threshold PIN. (internal 2 MΩ pull down)
38	VIN5	I (POWER)	Power supply for VOUT4
39	VIN5	I (POWER)	Power supply for VOUT4

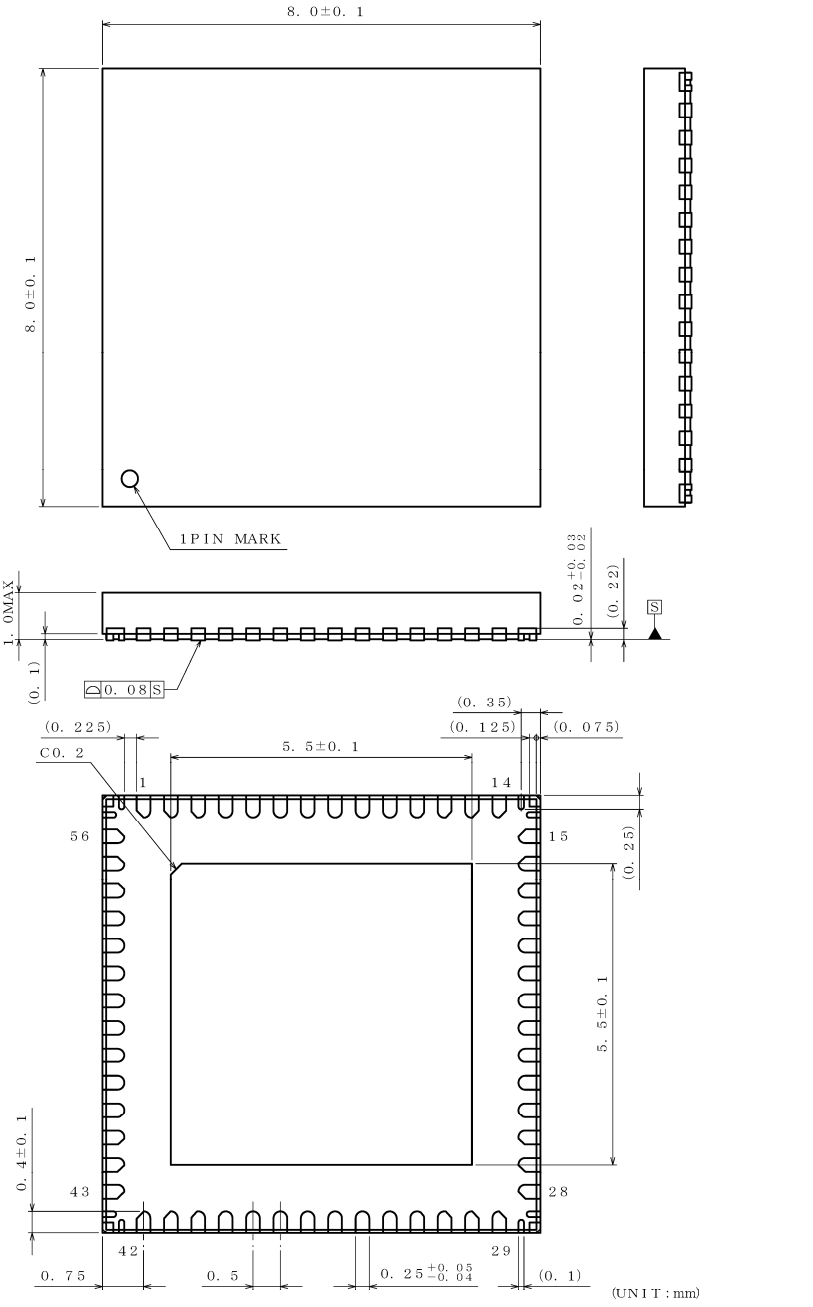
(Note 1) O.D. = Open Drain

Pin Description - continued

Pin No.	Pin Name	I/O	Function
40	SW5	O	High side MOSFET source / Low side MOSFET sink pin for VOUT4
41	SW5	O	High side MOSFET source / Low side MOSFET sink pin for VOUT4
42	PGND5	-	Power GND for VOUT4
43	PGND5	-	Power GND for VOUT4
44	VOUTL1	O	Output of VOUTL1
45	VIN6	I (POWER)	Power supply for VOUTL1
46	VIN7	I (POWER)	Power supply for VOUTS1
47	VOUTS1	O	SW Output
48	GATECNT	O	Control Gate of External PMOS SW. When use External PMOS. If External PMOS SW is not used, please connect to GND.
49	VFIL	O	Output of filtering VIN.
50	VIN	I (POWER)	Power supply for PMIC
51	FB1	I	Feedback pin for VOUT1
52	VIN1	I (POWER)	Power supply for VOUT1
53	VLSO	O	Output of LDSW
54	VOUT1	O	Output of VOUT1
55	SW1	O	High side MOSFET source / Low side MOSFET sink pin for VOUT1
56	PGND1	-	Power GND for VOUT1
-	EXP-PAD (CORNER)	-	GND (EXP-PAD (CORNER) short-circuit with EXP-PAD (CENTER) into the Package)
-	EXP-PAD (CENTER)	-	GND (Connect to common GND of PCB)

Physical Dimension and Packing Information

Package Name	VQFN56FV8080

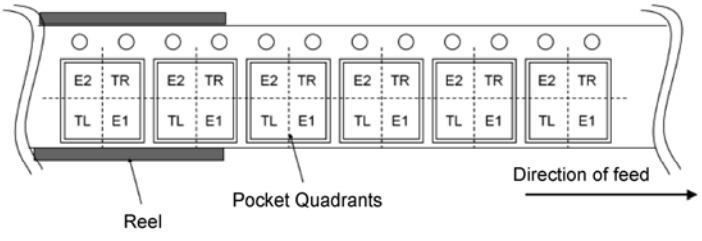


NOTE : Dimensions in ( ) for reference only.

PKG : VQFN56FV8080
Drawing No. EX409−5001−1

< Tape and Reel Information >

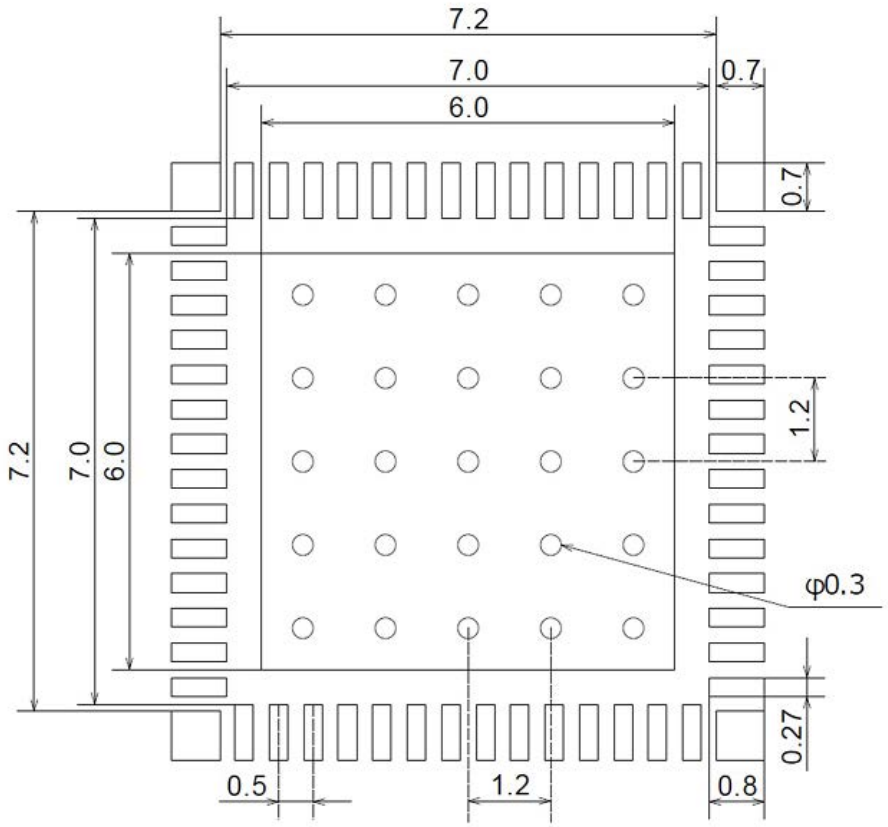
Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Footprint Dimension

Package Name	VQFN56FV8080

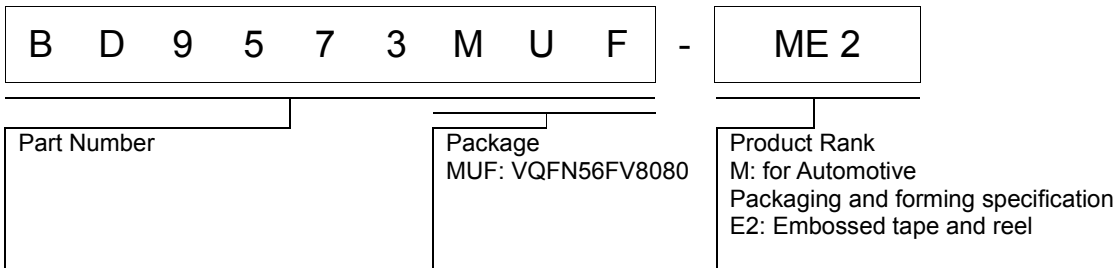
Footprint dimensions



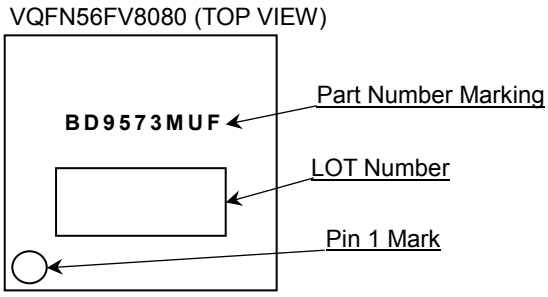
(unit:mm)

In actual design, please optimize in accordance with the situation of your board design and soldering condition.

Ordering Information



Marking Diagram



Contents

General Description 1
Features 1
Applications 1
Key Specifications 1
Special Characteristics 1
Package 1
Block Diagram 2
Pin Configuration 3
Pin Description 4
Physical Dimension and Packing Information 6
Footprint Dimension 7
Ordering Information 8
Marking Diagram 8
Contents 9
1. Device Feature 13
1.1 Output Voltage Table 13
1.2 Signal Line Diagram for PMIC 14
2. Application 15
3. Electrical Characteristics 17
3.1 Absolute Maximum Ratings 17
3.2 Thermal Resistance 18
3.3 Recommended Operating Conditions 19
3.4 DC Characteristics 20
3.5 Protection Mode (Under Voltage Lock Out) 24
3.6 Protection Mode (Thermal Shutdown) 24
3.7 Protection Mode 24
4. Function Description 25
4.1 Pin Control Function 25
4.1.1 VOUT1_EN Input 25
4.1.2 RSTB Input 25
4.1.3 PIN Setting Judge Timing 25
4.1.4 Output Power-ON / Output Power-OFF Sequence 26
4.1.5 VOUT2 (VD18) Discharge Start Timing 27
4.1.6 Countermeasures for Hang-Up 27
4.1.7 Interval Setting 28
4.1.8 Initializing Control Circuit 29
4.1.9 VOUT1 Mode Setting 29
4.1.10 State Machine 31
4.2 Whole Sequence Control 33
4.2.1 Whole Sequence (State Chart) 33
4.2.2 General Sequence Description 33
4.2.3 I2C Accessible State Condition 33
4.2.4 EEPROM Load Function and Internal OSC Stable Time 34
4.2.5 Prevention of Repetition for Protection Error, EEPROM CRC Error 34
4.3 VOUT1/VOUTL1 Disable Setting without EEPROM 35
4.4 VOUTS1 Disable Setting without EEPROM, Internal/External SW Mode Setting 36
4.5 I2C I/F 37
4.6 Interrupt Function 41
4.6.1 Interrupt Function Description 41
4.6.2 Interruption Factor 42
4.7 Power Abnormality Monitoring Function (Protection Error Detection) 45
4.8 SYNC Function 47
4.9 WDT Function 48
5. Register Specification 51
5.1 Register Map 51
5.2 Register Description 52
5.2.1 Recognition Code Indicator 52
5.2.2 FuSa Mode (Error Detection/Rectification Mode) 52
5.2.3 Spread Spectrum Clock Generation Control for Internal OSC 53
5.2.4 SMRB control Using I2C Control (Software Manual Reset for PRESETB) 54
5.2.5 Watch Dog Timer Setting 54
5.2.6 Oscillator Enable in STANDBY State 54
5.2.7 The PGD pin output assert condition Setting 55
5.2.8 PMIC Internal Status 55
5.2.9 I2C FuSa mode Error bit location 56
5.2.10 INTB Interruption Factor and Mask Condition 57
5.2.11 POW Setting 60
5.2.12 VOUT Voltage SET 63

5.2.13 VOUTS1 OCP SET 65
6. Typical Performance Curves 66
6.1 Line Regulation 66
6.2 Load Regulation 68
6.3 Power Efficiency 70
6.4 Power ON Waveform 72
6.5 Power OFF Waveform 74
6.6 Load Transient 76
7. Operational Notes 78
8. Revision History 81

Table 1: Output Voltage Table of Each State 13
Table 2: Application Circuit Components List 16
Table 3: Absolute Maximum Ratings 17
Table 4: Recommended Operating Conditions 19
Table 5: DC Characteristics (Unless otherwise specified, Tj = -40 °C to +150 °C, VIN = 3.3 V) 20
Table 6: Logic Characteristics (Unless otherwise specified, Tj = -40 °C to +150 °C, VIN = 3.3 V) 23
Table 7: Protection Mode (General) 24
Table 8: Protection Mode (VD50, DDR, VD18, VD10) 24
Table 9: Protection Mode (VL25) 24
Table 10: Protection Mode (VS33) 24
Table 11: SEQCNT[0] Operation Mode 28
Table 12: SEQCNT[1] Operation Mode 28
Table 13: Initializing Control Circuit 29
Table 14: I2C Accessible Condition 33
Table 15: Interruption at Primary Level 43
Table 16: Interruption at Secondary Level 2 44
Table 17: WDT setting (NG_RATIO[1:0] = “00”) 49
Table 18: WDT setting (NG_RATIO[1:0] = “01”) 49
Table 19: WDT setting (NG_RATIO[1:0] = “10”) 49
Table 20: WDT setting (NG_RATIO[1:0] = “11”) 49
Table 21: I2C I/F Register Map 51
Table 22: PMIC Internal State 55
Table 23: PON/POFF Trigger Signal 61
Table 24: PON/POFF Interval 62
Table 25: VOUT1 Tuning Voltage 63
Table 26: VOUT2 Tuning Voltage 63
Table 27: VOUT3 Tuning Voltage 64
Table 28: VOUT4 Tuning Voltage 64
Table 29: VOUTL1 Tuning Voltage 65
Table 30: VOUTS1 OCP Current (Internal) and Voltage (External) 65
Figure 1. An Example of Signal Line Diagram for PMIC 14
Figure 2. Application Circuit 15
Figure 3. Application Circuit (External MOS) 15
Figure 4. RSTB Operation Timing Chart 25
Figure 5. Output Power-ON Operation Timing Chart (Default Register Setting) 26
Figure 6. Output Power-OFF Operation Timing Chart (Default Register Setting) 26
Figure 7. VOUT2 Discharge Start Timing 27
Figure 8. SEQCNT Circuit 28
Figure 9. Whole Sequence1 (Mode B) 29
Figure 10. Whole Sequence2 (Mode B) 29
Figure 11. Error Case (Mode B) 30
Figure 12. Main State Machine 31
Figure 13. Sub State Machine 32
Figure 14. Whole Sequence (State Chart) 33
Figure 15. Sequence at Protection Error Occurrence (Timing Chart) 34
Figure 16. VOUT1 Disable Setting without EEPROM 35
Figure 17. VOUTL1 Disable Setting without EEPROM 35
Figure 18. VOUT1 and VOUTL1 OFF Circuit 35
Figure 19. VOUTS1 Disable Setting without EEPROM 36
Figure 20. VOUTS1 Internal/External Setting 36
Figure 21. VOUTS1 OFF Circuit and SW Mode Selection 36
Figure 22. I2C Basic Protocol 37
Figure 23. I2C Protocol (Each Access Mode) 37
Figure 24. I2C Protocol (FuSa Mode) 38
Figure 25. I2C Data Format (FuSa Mode type2 = ECC at Calculation) 40
Figure 26. Error Detection Judgement by ECC Calculation 40
Figure 27. Error Correction Calculation 40
Figure 28. Interruption Factor/Mask/Request 41
Figure 29. Interrupt Function Description 41
Figure 30. System Diagram of Interruption Function 42
Figure 31. Power Abnormality Monitoring Circuit 45
Figure 32. Timing Chart when Protection Error Factor Occur 1 45
Figure 33. Timing Chart when Protection Error Factor Occur 2 46
Figure 34. WDT Function 48
Figure 35. WDT NG RATIO 48
Figure 36. WDT Detection Time when NG_RATIO[1:0] = “00” 50
Figure 37. WDT Detection Time when NG_RATIO[1:0] = “01” 50
Figure 38. Modulation Waveform of SSCG 53
Figure 39. VOUT1 Output Voltage vs VIN 66
Figure 40. VOUT2 Output Voltage vs VIN 66

Figure 41. VOUT3 Output Voltage vs VIN (VOUT3 = 1.35 V Setting)....66
Figure 42. VOUT3 Output Voltage vs VIN (VOUT3 = 1.5 V Setting)....66
Figure 43. VOUT4 Output Voltage vs VIN....67
Figure 44. VOUTL1 Output Voltage vs VIN....67
Figure 45. VOUT1 Output Voltage vs IOUT....68
Figure 46. VOUT2 Output Voltage vs IOUT....68
Figure 47. VOUT3 Output Voltage vs IOUT (VOUT3 = 1.35 V Setting)....68
Figure 48. VOUT3 Output Voltage vs IOUT (VOUT3 = 1.5 V Setting)....68
Figure 49. VOUT4 Output Voltage vs IOUT....69
Figure 50. VOUTL1 Output Voltage vs IOUT....69
Figure 51. VOUT1 Power Efficiency vs IOUT....70
Figure 52. VOUT2 Power Efficiency vs IOUT....70
Figure 53. VOUT3 Power Efficiency vs IOUT (VOUT3 = 1.35 V Setting)....70
Figure 54. VOUT3 Power Efficiency vs IOUT (VOUT3 = 1.5 V Setting)....70
Figure 55. VOUT4 Power Efficiency vs IOUT....71
Figure 56. VOUT1 Power ON Waveform....72
Figure 57. VOUT2 Power ON Waveform....72
Figure 58. VOUT3 Power ON Waveform (VOUT3 = 1.35 V Setting)....72
Figure 59. VOUT3 Power ON Waveform (VOUT3 = 1.5 V Setting)....72
Figure 60. VOUT4 Power ON Waveform....73
Figure 61. VOUTL1 Power ON Waveform....73
Figure 62. VOUTS1 Power ON Waveform....73
Figure 63. VOUT1 Power OFF Waveform....74
Figure 64. VOUT2 Power OFF Waveform....74
Figure 65. VOUT3 Power OFF Waveform (VOUT3 = 1.35 V Setting)....74
Figure 66. VOUT3 Power OFF Waveform (VOUT3 = 1.5 V Setting)....74
Figure 67. VOUT4 Power OFF Waveform....75
Figure 68. VOUTL1 Power OFF Waveform....75
Figure 69. VOUTS1 Power OFF Waveform....75
Figure 70. VOUT1 Load Transient (IOUT = 0 A to 100 mA (SR = 100 mA/µs))....76
Figure 71. VOUT2 Load Transient (IOUT = 0 A to 0.5 A (SR = 1 A/µs))....76
Figure 72. VOUT3 Load Transient (VOUT3 = 1.35 V Setting, IOUT = 0 A to 1 A (SR = 1 A/µs))....76
Figure 73. VOUT3 Load Transient (VOUT3 = 1.5 V Setting, IOUT = 0 A to 1 A (SR = 1 A/µs))....76
Figure 74. VOUT4 Load Transient (IOUT = 0 A to 2.05 A (SR = 1 A/µs))....77
Figure 75. VOUTL1 Load Transient (IOUT = 0 A to 75 mA (SR = 100 mA/µs)....77
Figure 76. Example of Monolithic IC Structure....79

1. Device Feature

1.1 Output Voltage Table

Table 1: Output Voltage Table of Each State

Channel	Rail name	Output [V]	Iomax [A]	STANDBY	ACTIVE
VD50	VOUT1	5.0	0.2	OFF	ON
VD18	VOUT2	1.8	1.0	OFF	ON
DDR	VOUT3	1.35 (DDR3L) 1.50 (DDR3)	2.0	OFF	ON
VD10A VD10B	VOUT4	1.03	5.2	OFF	ON
VL25	VOUTL1	2.50	0.15	OFF	ON
VS33	VOUTS1	VIN7 (Analog Switch)	0.3	OFF	ON

1. Device Feature - continued

1.2 Signal Line Diagram for PMIC

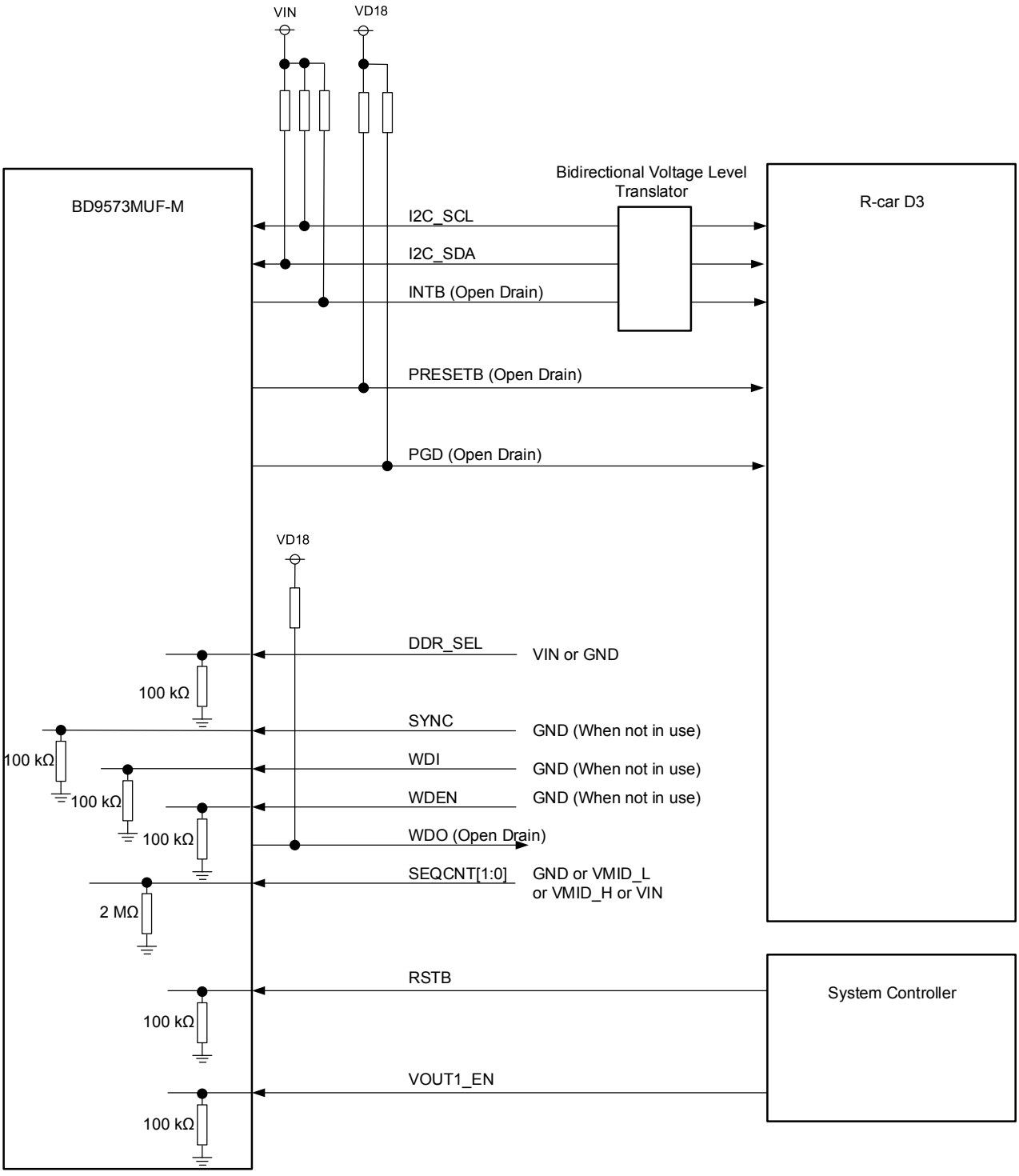


Figure 1. An Example of Signal Line Diagram for PMIC

2. Application

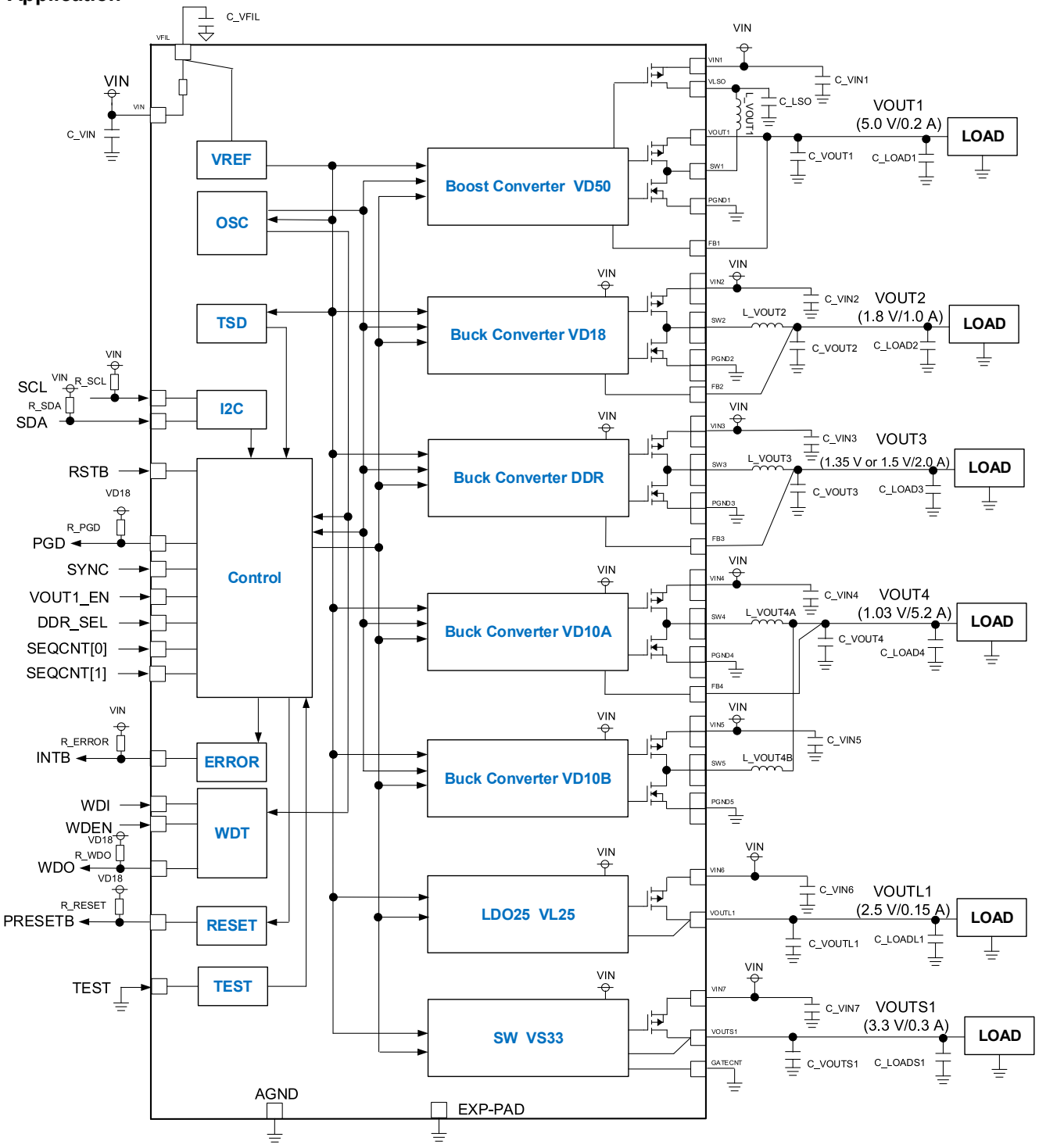


Figure 2. Application Circuit

Figure 3 shows the case of external FET for VOUTS1.
When output current is over 0.3 A or more, external FET is used.

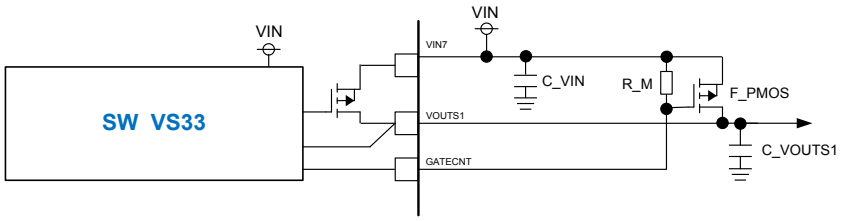


Figure 3. Application Circuit (External MOS)

2. Application - continued

Table 2: Application Circuit Components List

Parts Name	Value			Unit	Vendor	Parts Number	Size (mm)
	Min(Note 1)	Typ	Max				
C_VINx	-	10	-	µF	MURATA	GCM21BR70J106KE22	2012
C_VFIL	-	1	-	µF	MURATA	GCM188R71C105KA64	1608
C_LSO	-	10 x 2	-	µF	MURATA	GCM21BR70J106KE22	2012
C_VOUT1	-	22	-	µF	MURATA	GCM31CR71A226KE02	3216
C_LOAD1	22	-	-	µF	MURATA	GCM31CR71A226KE02	3216
L_VOUT1	-	2.2	-	µH	TDK	TFM252012ALMA2R2MTAA	2520
L_VOUT2	-	0.22	-	µH	TDK	TFM252012ALMAR22MTAA	2520
C_VOUT2	-	22	-	µF	MURATA	GCM31CR70J226KE26	3216
	-	or 22	-	µF	TDK	CGA4J1X7T0J226M	2012
C_LOAD2	22 x 2	-	-	µF	MURATA	GCM31CR70J226KE26	3216
	or 22 x 2	-	-	µF	TDK	CGA4J1X7T0J226M	2012
L_VOUT3	-	0.33	-	µH	TDK	TFM252012ALMAR33MTAA	2520
C_VOUT3	-	22	-	µF	MURATA	GCM31CR70J226KE26	3216
	-	or 22	-	µF	TDK	CGA4J1X7T0J226M	2012
C_LOAD3	22 x 3	-	-	µF	MURATA	GCM31CR70J226KE26	3216
	or 22 x 3	-	-	µF	TDK	CGA4J1X7T0J226M	2012
L_VOUT4A	-	0.22	-	µH	TDK	TFM252012ALMAR22MTAA	2520
L_VOUT4B	-	0.22	-	µH	TDK	TFM252012ALMAR22MTAA	2520
C_VOUT4	-	47 x 2	-	µF	MURATA	GCM32ER70J476KE19	3225
	-	or 22 x 4	-	µF	TDK	CGA4J1X7T0J226M	2012
C_LOAD4	47 x 4	-	-	µF	MURATA	GCM32ER70J476KE19	3225
	or 22 x 8	-	-	µF	TDK	CGA4J1X7T0J226M	2012
C_VOUTL1	-	10	-	µF	MURATA	GCM21BR70J106KE22	2012
C_LOADL1	1	-	300	µF	-	-	-
C_VOUTS1	-	10	-	µF	MURATA	GCM21BR70J106KE22	2012
C_LOADS1	1	-	300	µF	-	-	-
F_PMOS	-	-	-	-	ROHM	RQ1A070ZPHZG	TSMT8
R_M	-	100	-	kΩ	ROHM	MCR01MZPF1003	1005
R_PGD	-	10	-	kΩ	ROHM	MCR01MZPF1002	1005
R_EEROR	-	10	-	kΩ	ROHM	MCR01MZPF1002	1005
R_RESET	-	10	-	kΩ	ROHM	MCR01MZPF1002	1005
R_SDA	-	1	-	kΩ	ROHM	MCR01MZPF1001	1005
R_SCL	-	1	-	kΩ	ROHM	MCR01MZPF1001	1005
R_WDO	-	10	-	kΩ	ROHM	MCR01MZPF1002	1005

(*Note 1*) Please set in consideration of temperature properties and DC bias properties not to become less than the minimum.
Please consider it based on enough evaluations with the actual model.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage 1	VIN, VIN1, VIN2, VIN3, VIN4, VIN5, VIN6, VIN7	-0.3 to +7.0	V
Input Voltage 2	FB1, FB2, FB3, FB4	-0.3 to +7.0	V
Output Voltage 1	VFIL	-0.3 to VIN+0.3	V
Output Voltage 2	VLSO	-0.3 to VIN1+0.3	V
Output Voltage 3	VOUT1	-0.3 to +7.0	V
Output Voltage 4	VOUTL1, VOUTS1	-0.3 to VINx+0.3	V
Output Voltage 5	GATECNT	-0.3 to +7.0	V
SW to GND Voltage 1	SW2, SW3, SW4, SW5	-0.3 to VINx+0.3	V
SW to GND Voltage 2	SW1	-0.3 to +10.0	V
Logic Input Voltage 1	RSTB, SDA, SCL	-0.3 to +7.0	V
Logic Input Voltage 2	SYNC, WDI, WDEN, VOUT1_EN, DDR_SEL	-0.3 to VIN+0.3	V
Logic Input Voltage 3	SEQCNT[0], SEQCNT[1]	-0.3 to VIN+0.3	V
Logic Output Voltage 1	INTB, PGD, WDO	-0.3 to +7.0	V
Logic Output Voltage 2	PRESETB	-0.3 to VIN+0.3	V
Logic Output Pin Current Low 1	PRESETB, INTB, PGD, WDO	-3.0	mA
Logic Output Pin Current Low 2	SDA, SCL	-20.0	mA
Storage Temperature Range	Tstg	-55 to +150*(Note 1)*	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Operation is not guaranteed.

3. Electrical Characteristics - continued

3.2 Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN56FV8080				
Junction to Ambient	θ_{JA}	59.8	22.2	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	4.0	2.0	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

3. Electrical Characteristics - continued

3.3 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VIN	3.0	3.3	3.6	V
Power Supply Voltage 1	VIN1	3.0	3.3	3.6	V
Power Supply Voltage 2	VIN2	3.0	3.3	3.6	V
Power Supply Voltage 3	VIN3	3.0	3.3	3.6	V
Power Supply Voltage 4	VIN4	3.0	3.3	3.6	V
Power Supply Voltage 5	VIN5	3.0	3.3	3.6	V
Power Supply Voltage 6	VIN6	3.0	3.3	3.6	V
Power Supply Voltage 7	VIN7	3.0	3.3	3.6	V
Logic Input Voltage Low 1	RSTB, SYNC, WDI, WDEN, VOUT1_EN, DDR_SEL	-0.3	-	+0.5	V
Logic Input Voltage High 1	RSTB, SYNC, WDI, WDEN, VOUT1_EN, DDR_SEL	1.2	-	VIN + 0.3	V
Logic Input Voltage Low 2	SCL, SDA	-0.3	-	+0.5	V
Logic Input Voltage High 2	SCL, SDA	1.2	-	VIN + 0.3	V
Input Voltage Low 3	SEQCNT[0], SEQCNT[1]	-0.3	-	VIN x 0.1	V
Input Voltage Middle Low 3	SEQCNT[0], SEQCNT[1]	VIN x 0.2	-	VIN x 0.5	V
Input Voltage Middle High 3	SEQCNT[0], SEQCNT[1]	VIN x 0.6	-	VIN x 0.8	V
Input Voltage High 3	SEQCNT[0], SEQCNT[1]	VIN x 0.9	-	VIN x 0.3	V
SYNC Input Frequency Range	SYNC	1.8	2.0	2.2	MHz
SYNC Input Pulse Duty Range	SYNC	45	50	55	%
Operating Ambient Temperature	Ta	-40	25	+105	°C
Operating Junction Temperature	Tj	-40	25	+150	°C

3. Electrical Characteristics - continued

3.4 DC Characteristics

Table 5: DC Characteristics (Unless otherwise specified, Tj = -40 °C to +150 °C, VIN = 3.3 V)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[General]						
Bias Current 1	ICC_1	-	0.5	-	mA	STANDBY (VIN, VIN1 to VIN7 total)
Bias Current 2	ICC_2	-	6	12	mA	ACTIVE (VIN, VIN1 to VIN7 total, Switching stop)
VFIL UVLO Threshold Voltage	VFIL_UVLO	2.7	2.8	2.9	V	VFIL: Sweep down
VFIL UVLO Hysteresis Voltage	dVFIL_UVLO	-	0.1	-	V	VFIL: Sweep up
VIN1 to VIN7 UVP Threshold Voltage	VIN1-7_UVP	2.6	2.7	2.8	V	VIN1 to VIN7: Sweep down
VIN1 to VIN7 UVP Hysteresis Voltage	dVIN1-7_UVP	-	0.1	-	V	VIN1 to VIN7: Sweep up
VFIL Resistance	R_VFIL	-	10	-	Ω	-
[VOUT1 (VD50)]						
Output Voltage	VOUT1	4.91	5.00	5.09	V	Io = 0 mA
Switching Frequency	Fosc_VOUT1	1.912	2.250	2.588	MHz	SSCG = OFF
Synchronization Frequency	Fsync_VOUT1	1.8	2.0	2.2	MHz	SYNC = 2 MHz
Soft-Start Time Rate	Tssr_VOUT1	-	4.2	-	V/ms	VIN to VOUT1 (DCDC converter Soft-start time rate)
VOUT1 Soft Start time	Tss_VOUT1	-	1.57	-	ms	0 V to 5 V (Include LDSW on time)
Upper-Side ON Resistance	Ronh_VOUT1	-	250	500	mΩ	-
Lower-Side ON Resistance	Rohl_VOUT1	-	200	400	mΩ	-
Over Current Protection	OCP_VOUT1	1.2	-	-	A	Detect a peak current flowing in Low-side FET
SCP Detecting Voltage	SCP_VOUT1	VOUT1 x 0.7	VOUT1 x 0.8	VOUT1 x 0.9	V	-
OVP Detecting Voltage	OVP_VOUT1	VOUT1 x 1.13	VOUT1 x 1.2	VOUT1 x 1.27	V	-
Load Switch ON Resistance	Ron_LS	-	200	400	mΩ	-
Load Switch Over Current Protection	OCP_LDSW	2.2	-	-	A	-
Output Discharge Resistance	Rdis_VOUT1	-	25	50	Ω	VOUT1 Discharge
[VOUT2 (VD18)]						
Output Voltage	VOUT2	1.7676	1.8000	1.8324	V	Io = 0 mA
Switching Frequency	Fosc_VOUT2	1.912	2.250	2.588	MHz	SSCG = OFF
Synchronization Frequency	Fsync_VOUT2	1.8	2.0	2.2	MHz	SYNC = 2 MHz
Soft-Start Time Rate	Tss_VOUT2	-	1.0	-	V/ms	-
Upper-Side ON Resistance	Ronh_ VOUT2	-	160	320	mΩ	-
Lower-Side ON Resistance	Rohl_VOUT2	-	100	200	mΩ	-
Over Current Protection	OCP_VOUT2	2.5	-	-	A	Detect a peak current flowing in High-side FET
SCP Detecting Voltage	SCP_VOUT2	VOUT2 x 0.73	VOUT2 x 0.80	VOUT2 x 0.87	V	-
OVP Detecting Voltage	OVP_VOUT2	VOUT2 x 1.13	VOUT2 x 1.2	VOUT2 x 1.27	V	-
Output Discharge Resistance	Rdis_VOUT2	20	55	150	Ω	FB2 Discharge

3.4 DC Characteristics - continued

(Unless otherwise specified, Tj = -40 °C to +150 °C, VIN = 3.3 V)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[VOUT3 (DDR)]						
Output Voltage 1	VOUT3_1	1.3257	1.3500	1.3743	V	Io = 0 mA DDR_SEL = L
Output Voltage 2	VOUT3_2	1.473	1.500	1.527	V	Io = 0 mA DDR_SEL = H
Switching Frequency	Fosc_VOUT3	1.912	2.250	2.588	MHz	SSCG = OFF
Synchronization Frequency	Fsync_VOUT3	1.8	2.0	2.2	MHz	SYNC = 2 MHz
Soft-Start Time Rate	Tss_VOUT3	-	1.0	-	V/ms	-
Upper-Side ON Resistance	Ronh_VOUT3	-	100	200	mΩ	-
Lower-Side ON Resistance	Rohl_VOUT3	-	70	140	mΩ	-
Over Current Protection	OCP_VOUT3	3.6	-	-	A	Detect a peak current flowing in High-side FET
SCP Detecting Voltage	SCP_VOUT3	VOUT3 x 0.73	VOUT3 x 0.80	VOUT3 x 0.87	V	-
OVP Detecting Voltage	OVP1_VOUT3	VOUT3 x 1.13	VOUT3 x 1.2	VOUT3 x 1.27	V	-
Output Discharge Resistance	Rdis_VOUT3	20	40	80	Ω	FB3 Discharge
[VOUT4 (VD10A, VD10B)]						
Output Voltage	VOUT4	1.0115	1.0300	1.0485	V	Io = 0 mA
Switching Frequency	Fosc_VOUT4	1.912	2.250	2.588	MHz	SSCG = OFF
Synchronization Frequency	Fsync_VOUT4	1.8	2.0	2.2	MHz	SYNC = 2 MHz
Soft-Start Time Rate	Tss_VOUT4	-	1.0	-	V/ms	-
Upper-Side ON Resistance	Ronh_VOUT4A Ronh_VOUT4B	-	100	200	mΩ	-
Lower-Side ON Resistance	Rohl_VOUT4A Rohl_VOUT4B	-	70	140	mΩ	-
Over Current Protection	OCP_VOUT4A OCP_VOUT4B	3.6	-	-	A	Detect a peak current flowing in High-side FET
SCP Detecting Voltage	SCP_VOUT4	VOUT4 x 0.73	VOUT4 x 0.80	VOUT4 x 0.87	V	-
OVP Detecting Voltage	OVP_VOUT4	VOUT4 x 1.07	VOUT4 x 1.14	VOUT4 x 1.21	V	-
Output Discharge Resistance	Rdis_VOUT4	15	30	60	Ω	FB4 Discharge

3.4 DC Characteristics - continued

(Unless otherwise specified, Tj = -40 °C to +150 °C, VIN = 3.3 V)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[VOUTL1 (VL25)]						
Output Voltage	VOUTL1	2.455	2.500	2.545	V	Io = 0 mA
Soft-Start Time Rate	Tss_VOUTL1	-	1.0	-	V/ms	-
On Resistance	Ron_VOUTL1	-	-	2	Ω	Ids = 50 mA
Over Current Protection	OCP_VOUTL1	350	-	-	mA	-
SCP Detecting Voltage	SCP_ VOUTL1	VOUTL1 x 0.73	VOUTL1 x 0.8	VOUTL1 x 0.87	V	-
OVP Detecting Voltage	OVP_ VOUTL1	VOUTL1 x 1.13	VOUTL1 x 1.2	VOUTL1 x 1.27	V	-
Output Discharge Resistance	Rdis_ VOUTL1	75	150	300	Ω	VOUTL1 Discharge
[VOUTS1 (VS33)]						
Soft-Start Time Rate	Tss_VOUTS1	-	1	-	V/ms	-
Output Discharge Resistance	Rdis_VOUTS1	15	30	50	Ω	VOUTS1 Discharge
SW ON Resistance	Ron_VOUTS1	100	250	450	mΩ	-
GATECNT ON Resistance	Ron_GATECNT	10	25	50	Ω	GATECNT = 0.5 V
GATECNT Pull Up Resistance	Rup_GATECNT	-	2	-	MΩ	-
SW OCP Detecting Current (Internal)	OCP_VOUTS1_IN	510	-	-	mA	-
SW OCP Detecting Voltage (External)	OCP_VOUTS1_EX	60	90	120	mV	ΔV = VIN7-VOUTS1

3.4 DC Characteristics - continued

Table 6: Logic Characteristics (Unless otherwise specified, Tj = -40 °C to +150 °C, VIN = 3.3 V)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
[Logic Block]						
[Logic Input 1] (RSTB, SYNC, WDI, WDEN, VOUT1_EN, DDR_SEL)						
Input Voltage Low 1	VIL1	-0.3	-	+0.5	V	-
Input Voltage High 1	VIH1	1.2	-	VIN+0.3	V	-
Pull down Resistance 1	RIN1	-	100	-	kΩ	-
[Logic Input 2] (SDA, SCL)						
Input Voltage Low 2	VIL2	-0.3	-	+0.5	V	-
Input Voltage High 2	VIH2	1.2	-	VIN+0.3	V	-
Input Current 2	IIN2	-1	0	+1	μA	-
Acknowledge ON Voltage	VACK	-0.3	-	+0.4	V	Iload = -20 mA
[Logic Input 3] (SEQCNT[0], SEQCNT[1])						
Input Voltage Low 3	VIL3	-0.3	-	VIN x 0.1	V	-
Input Voltage Middle Low 3	VIML3	VIN x 0.2	-	VIN x 0.5	V	-
Input Voltage Middle High 3	VIMH3	VIN x 0.6	-	VIN x 0.8	V	-
Input Voltage High 3	VIH3	VIN x 0.9	-	VIN x 0.3	V	-
Pull down Resistance 3	RIN3	-	2	-	MΩ	-
[Logic Output Voltage Low1] (Open Drain Output)						
INTB, PGD, WDO	Logic_out_low1	-0.3	-	+0.7	V	Iload = -3 mA
[Logic Output Voltage Low2] (Open Drain Output)						
PRESETB	Logic_out_low2	-0.3	-	+0.5	V	Iload = -3 mA

3. Electrical Characteristics - continued

3.5 Protection Mode (Under Voltage Lock Out)

All power supply shuts down at the same time when the VFIL UVLO signal is detected. There is no sequence in this shutdown mode and the BD9573MUF-M cannot receive any external signals during this time.

3.6 Protection Mode (Thermal Shutdown)

Built-in internal Thermal Shutdown (TSD) circuit is provided to protect IC from heat destruction. Operation usage should stay within the allowable loss range. Continuous use beyond this range can cause chip temperature Tj to increase and consequently activate the TSD circuit. Threshold is 175 °C (Typ). TSD over 10 µs shuts down all power supplies at the same time. Please consider the set design not to exceed TSD for safety use.

3.7 Protection Mode

Table 7: Protection Mode (General)

Protection Mode	SW	Output	Function
UVLO Protection (VFIL)	Hi-Z	Low (Discharge)	PMIC is shut down immediately. All Registers are reset.
Thermal Shutdown	Hi-Z	Low (Discharge)	PMIC is shut down immediately. Some registers (SEQ reset Register) are reset.

Table 8: Protection Mode (VD50, DDR, VD18, VD10)

Protection Mode	SW	Output	Function
Under Voltage Protection[UVP] (VIN1 to VIN5)*(Note 1)*	Hi-Z	Low (Discharge)	PMIC is shut down immediately. Some registers (SEQ reset Register) are reset.
Short Circuit Protection	Hi-Z	Low (Discharge)	Timer latch (1 ms). PMIC is shut down. Some registers (SEQ reset Register) are reset.
Over Voltage Protection	Hi-Z	Low (Discharge)	PMIC is shut down immediately. Some registers (SEQ reset Register) are reset.
Over Current Protection	Hi-Z	Low (Discharge)	Duty is restricted. Timer latch (1 ms). PMIC is shut down. Some registers (SEQ reset Register) are reset.

(Note 1) VOUT1 or VOUTL1 output can be set to disable by connecting the VIN1 pin or the VIN6 pin to GND.
Please refer to section 4.3 VOUT1/VOUTL1 Disable Setting without EEPROM.

Table 9: Protection Mode (VL25)

Protection Mode	Output	Function
Under Voltage Protection[UVP] (VIN6)*(Note 1)*	Low (Discharge)	PMIC is shut down immediately. Some registers (SEQ reset Register) are reset.
Short Circuit Protection	Low (Discharge)	Timer latch (1 ms). PMIC is shut down. Some registers (SEQ reset Register) are reset.
Over Voltage Protection	Low (Discharge)	PMIC is shut down immediately. Some registers (SEQ reset Register) are reset.

(Note 1) VOUT1 or VOUTL1 output can be set to disable by connecting the VIN1 pin or the VIN6 pin to GND.
Please refer to section 4.3 VOUT1/VOUTL1 Disable Setting without EEPROM.

Table 10: Protection Mode (VS33)

Protection Mode	Output	Function
Under Voltage Protection[UVP] (VIN7)	Low (Discharge)	PMIC is shut down immediately. Some registers (SEQ reset Register) are reset.
Over Current Protection	Low (Discharge)	Timer latch (1 ms). PMIC is shut down. Some registers (SEQ reset Register) are reset.

4. Function Description

4.1 Pin Control Function

4.1.1 VOUT1_EN Input

VOUT1 Mode is selected by VOUT1_EN (pin) condition at UVLO release timing.
At the judgement timing, VOUT1 output voltage is
Mode A: controlled sequentially by the register setting. (VOUT1_EN (pin) = H at UVLO release timing).
Mode B: controlled by VOUT1_EN (pin) individually, and register setting is ignored.
(VOUT1_EN (pin) = L at UVLO release timing).

(Note) Most of timing charts in this data sheet are based on Mode A. Regarding Mode B, please refer to section 4.1.9 VOUT1 Mode Setting.

4.1.2 RSTB Input

The RSTB pin input is control signal to start Output Power-ON / Output Power-OFF.
Output Power-ON starts by inputting RSTB = H level and Output Power-OFF starts by inputting RSTB = L level.
Between the completion of Output Power-OFF and beginning of Output Power-ON (STANDBY state), internal functions (except particular functions) are initialized and stops the circuit oscillator for low power consumption with OSC_EN register = “0” setting.
Even though in STANDBY state, circuit oscillation starts with OSC_EN register = “1” setting.

(Note) In case RSTB = L level is detected during Power-ON Sequence, Power-OFF sequence starts immediately.

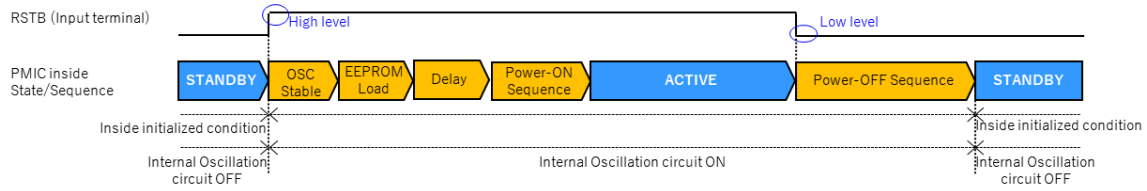


Figure 4. RSTB Operation Timing Chart

4.1.3 PIN Setting Judge Timing

The SEQCNT[1:0] pin (Select Power-ON / Power-OFF interval) and the DDR_SEL pin (select DDR output voltage) settings are judged just before EEPROM Load.

4.1 Pin Control Function – continued

4.1.4 Output Power-ON / Output Power-OFF Sequence

Output Power-ON starts by input of RSTB = H level.
In Output Power-ON operation,
(1) Internal Oscillation Operation (OSC Stable), (2) EEPROM Load, (3) Delay and (4) Power-ON sequence are consecutively activated as shown in the following figure.
Regarding the interval T1 and T4, please refer to section 4.1.7 Interval Setting.

(1) Internal Oscillation Operation: BD9573MUF-M waits 110 µs (Max) for stable oscillation internally.
(2) EEPROM Load: Some of the functions can be selected by EEPROM setting value (Max 2 ms).
(3) Delay: BD9573MUF-M execute delay for internal setting (Max 2 ms) before Power-ON.
(4) Power-ON sequence: Activates Output Power-ON and PRESETB = H negate in order and with interval as in following figure. PGD is asserted when all output voltage levels are over 75 % (Typ) x V_{OUT}.

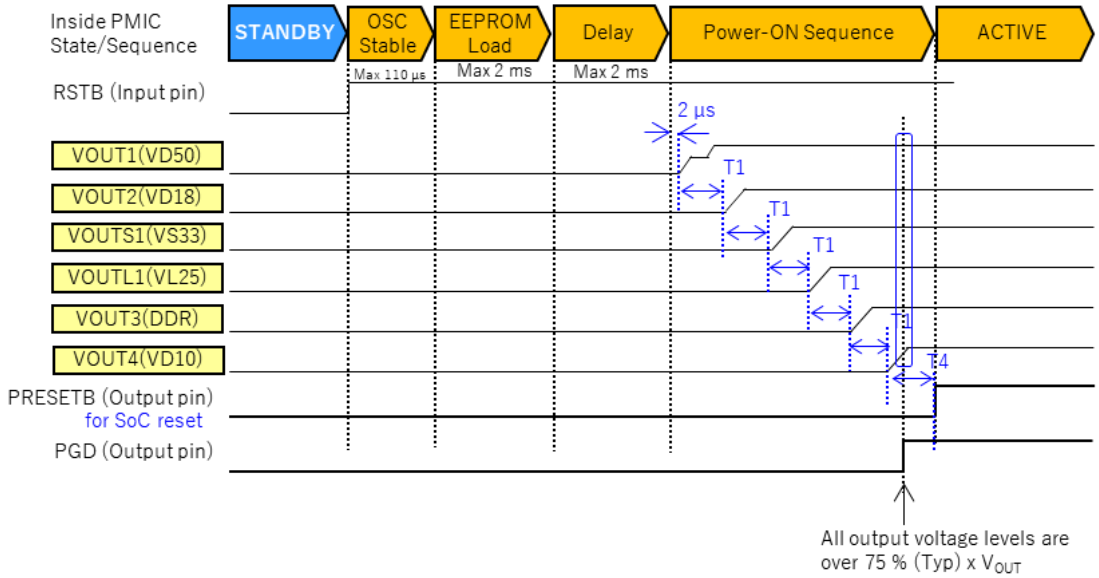


Figure 5. Output Power-ON Operation Timing Chart (Default Register Setting)

Output Power-OFF starts by input of RSTB = L level.
For Output Power-OFF operation, Power-OFF sequence activates as in following figure.
Regarding the interval T2 and T3, please refer to section 4.1.7 Interval Setting.
PGD is negated when one of the output power starts discharging.
Power-OFF operation is completed when all SHDN (= output voltage levels are under 200 mV (Typ)) is asserted.

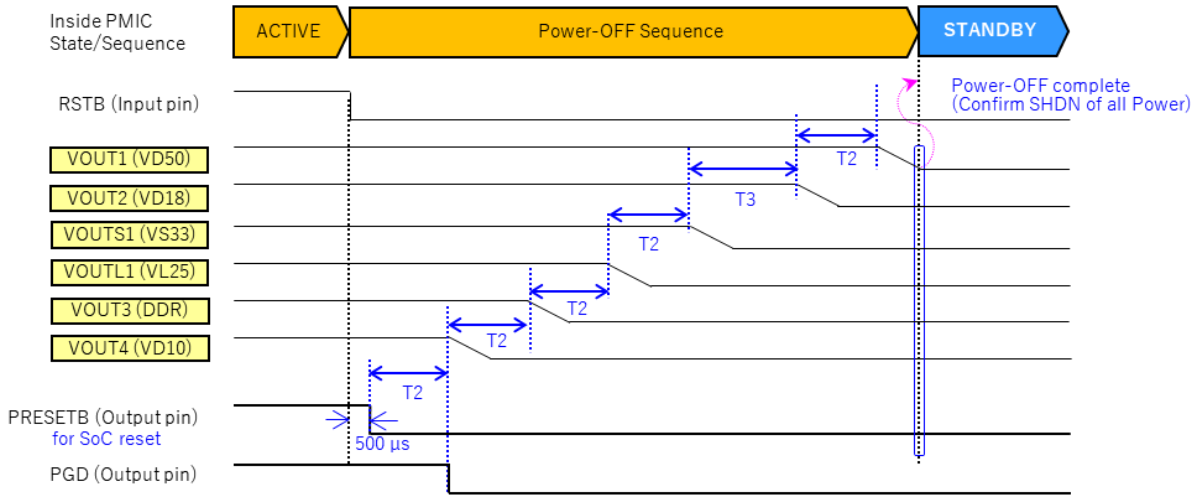


Figure 6. Output Power-OFF Operation Timing Chart (Default Register Setting)

4.1 Pin Control Function – continued

4.1.5 VOUT2 (VD18) Discharge Start Timing

In case all previous output's SHDN is not asserted after the interval T3, VOUT2 output does not start discharging until all previous output's SHDN assertion.

4.1.6 Countermeasures for Hang-Up

In case any SHDN signal keeps low (shutdown is not detected) during Power-Off sequence, the sequence is never completed and sequence cannot shift to next. As countermeasure for this Hang-Up situation, Hang-Up Timer is implemented.
Hang-Up Timer counts the time of Power-OFF Sequence, and if it continues over 400 ms, internal state transitions to STANDBY automatically. In Mode B, VOUT1 also has Hang-Up Timer individually. If VOUT1 Power-OFF Sequence continues over 100 ms, internal state transitions to STANDBY automatically.

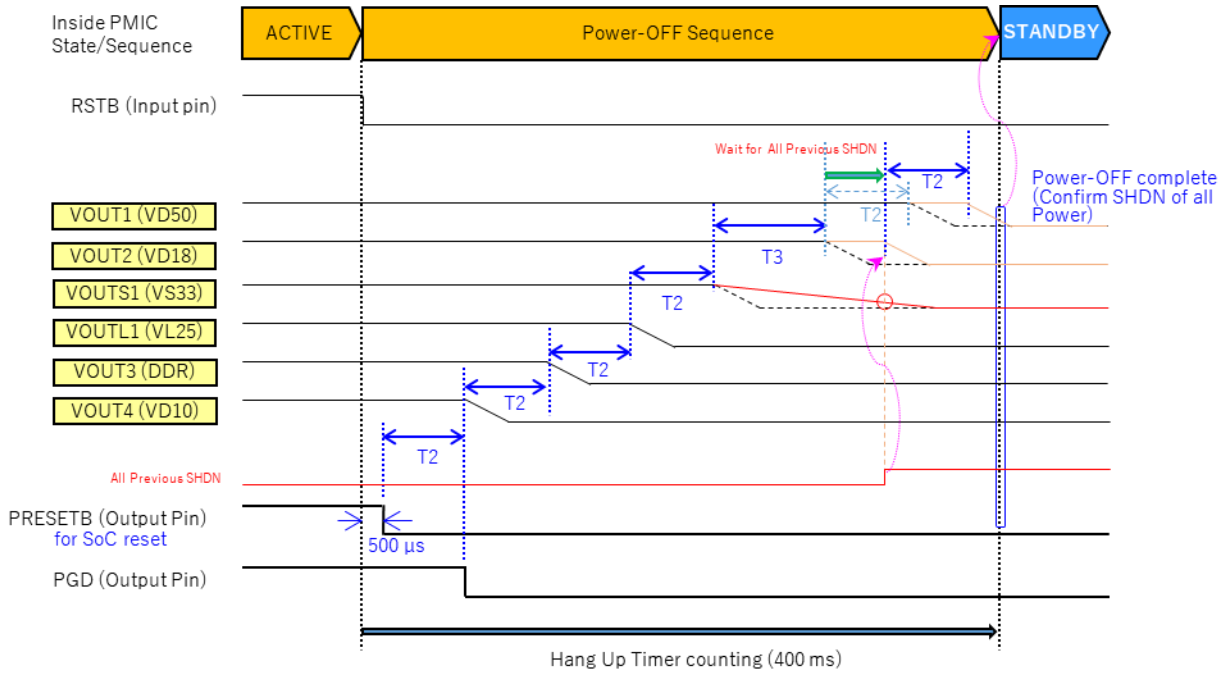


Figure 7. VOUT2 Discharge Start Timing

4.1 Pin Control Function – continued

4.1.7 Interval Setting

Regarding the interval T1, T2, T3 and T4, they are set by the voltage setting of the SEQCNT[0] pin and the SEQCNT[1] pin.
The SEQCNT[1:0] pin input value is judged just before EEPROM Load. If EEPROM connection is detected in the state of EEPROM Load, interval setting by the SEQCNT[1:0] pin is discarded and the setting by EEPROM is used.
If I2C write command to POW Trigger VOUTx (VOUTx = VOUT1 to VOUT4, VOUTL1, VOUTS1) or POW Wait VOUTx registers is detected, interval setting by the SEQCNT[1:0] pin is discarded and the setting by I2C write command is used. Also in this case, by EEPROM connection interval setting by the SEQCNT[1:0] pin or I2C write command are discarded and the setting by EEPROM is used.

Table 11: SEQCNT[0] Operation Mode

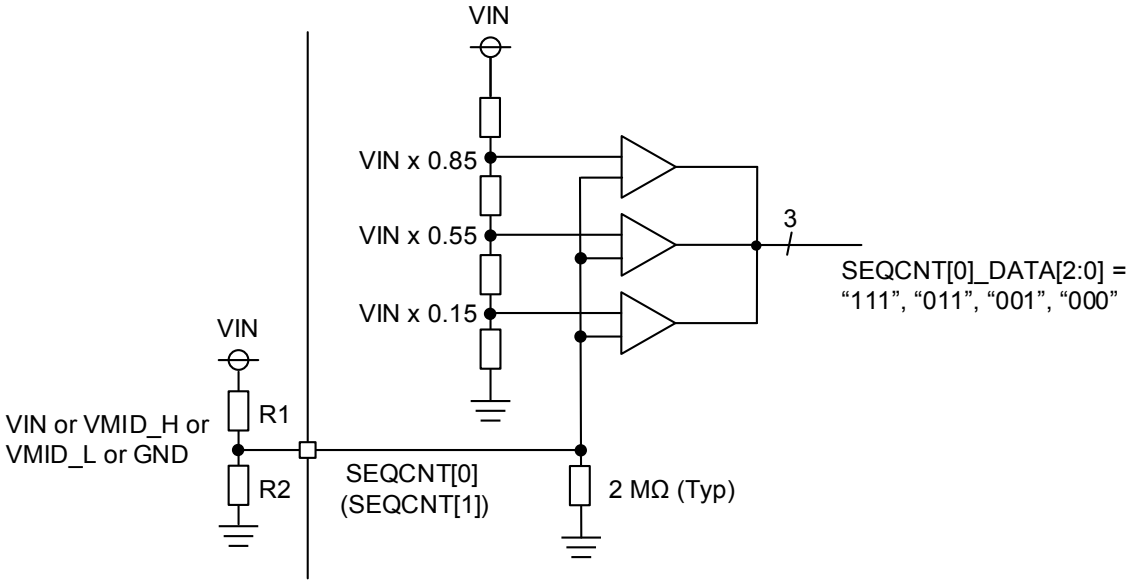
SEQCNT[0]	SEQCNT[0]_DATA[2:0]	T1	T2	T4
VIN	“111”	10 ms	10 ms	25 ms
VMD_H *(Note 1)*	“011”	8 ms	8 ms	15 ms
VMD_L *(Note 2)*	“001”	4 ms	4 ms	10 ms
GND	“000”	2 ms	2 ms	8 ms

(Note 1) VMD_H: VIN x 0.55 < Input Voltage < VIN x 0.85
(Note 2) VMD_L: VIN x 0.15 < Input Voltage < VIN x 0.55

Table 12: SEQCNT[1] Operation Mode

SEQCNT[1]	SEQCNT[1]_DATA[2:0]	T3
VIN	“111”	50 ms
VMD_H *(Note 1)*	“011”	40 ms
VMD_L *(Note 2)*	“001”	30 ms
GND	“000”	20 ms

(Note 1) VMD_H: VIN x 0.55 < Input Voltage < VIN x 0.85
(Note 2) VMD_L: VIN x 0.15 < Input Voltage < VIN x 0.55



Ex)
VMID_H (SEQCNT_DATA[2:0] = “011”) : R1 = 24 kΩ, R2 = 52 kΩ → VIN x 0.68
VMID_L (SEQCNT_DATA[2:0] = “001”) : R1 = 45 kΩ, R2 = 24 kΩ → VIN x 0.35
Please connect resistors of the total less than 200 kΩ.

Figure 8. SEQCNT Circuit

4.1 Pin Control Function – continued

4.1.8 Initializing Control Circuit

There are 2 initialize conditions. Details of the initializing conditions are shown in following table.

Table 13: Initializing Control Circuit

Reset Name	Initializing Condition	Initializing Target Circuit
VDD reset	UVLO of VFIL	Every Control Circuit
SEQ reset	state transition to STANDBY state	Every Control Circuit except some I2C registers. In more detail, please refer Table 21 I2C I/F Register Map.

4.1.9 VOUT1 Mode Setting

In Mode B, VOUT1 is managed in Sub State. Regarding Main State and Sub State, please refer State Machine. VOUT1 Sub State is activated only in limited Main State. Regarding the “limited Main State”, and Sub State, please refer Figure 12 Main State Machine and Figure 13 Sub State Machine.

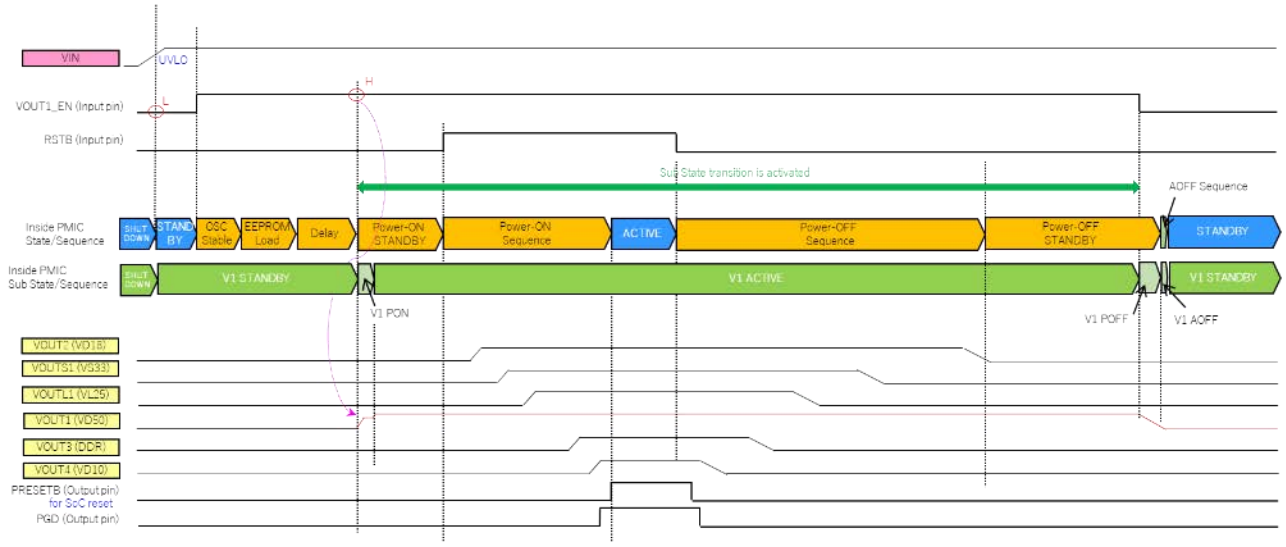


Figure 9. Whole Sequence1 (Mode B)

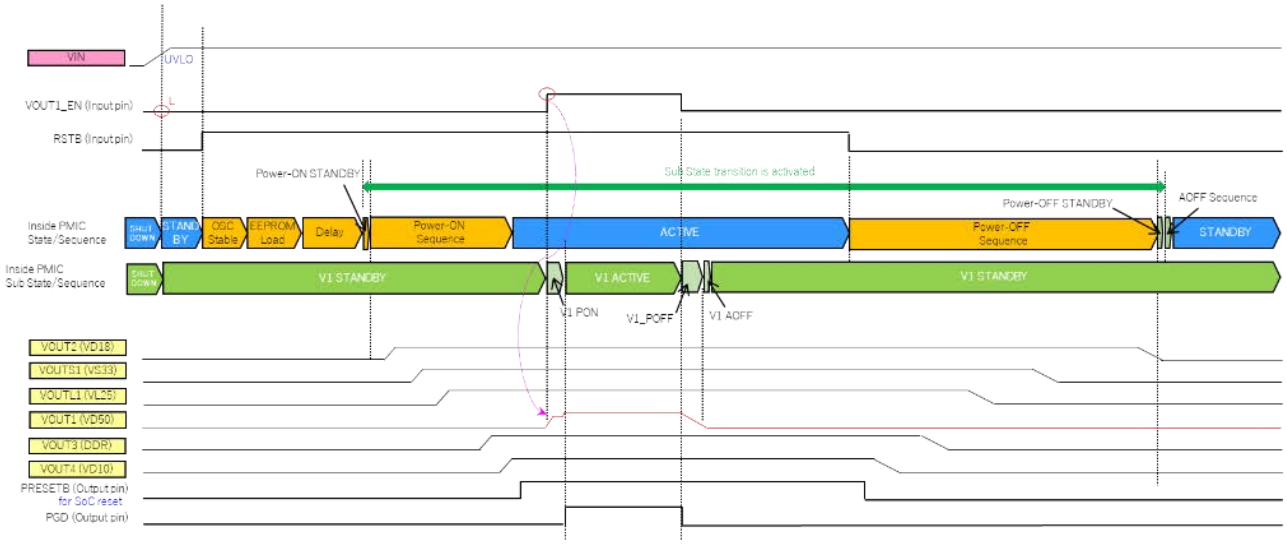


Figure 10. Whole Sequence2 (Mode B)

4.1.9 VOUT1 Mode Setting – continued

When protection error or Hang Up Timer Overflow occurs, all outputs start to Power-OFF at the same time regardless the error is due to VOUT1 or other channels. In this case, VOUT1_EN (pin) = L and RSTB (pin) = L is needed to Re Power-ON.

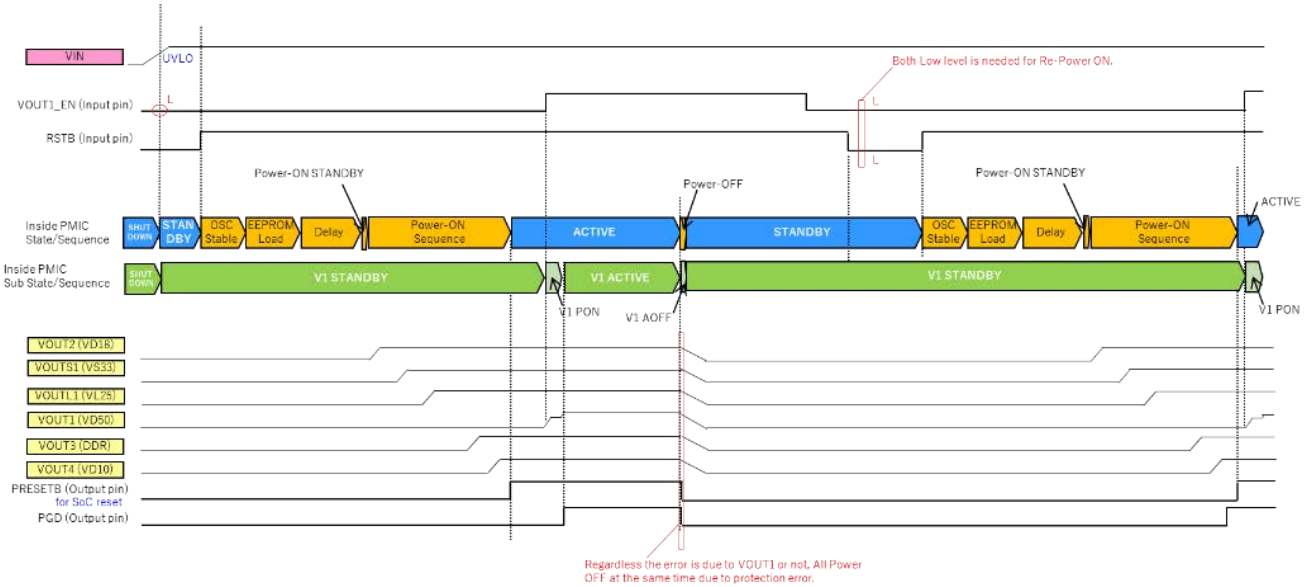


Figure 11. Error Case (Mode B)

4.1 Pin Control Function – continued

4.1.10 State Machine

BD9573MUF-M has two State Machine, Main and Sub. Sub State Machine is for VOUT1 individual control in Mode B.

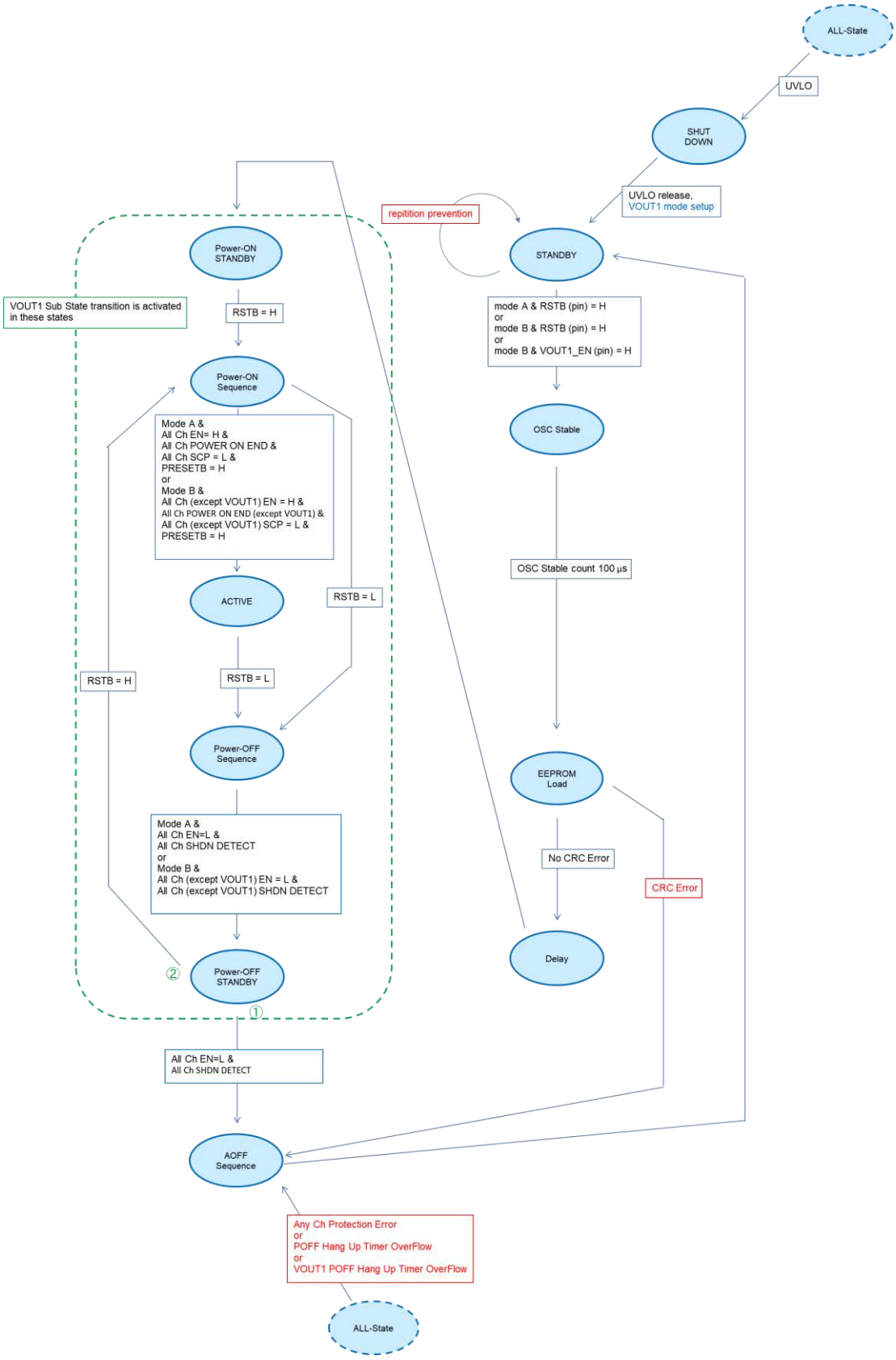


Figure 12. Main State Machine

4.1.10 State Machine - continued

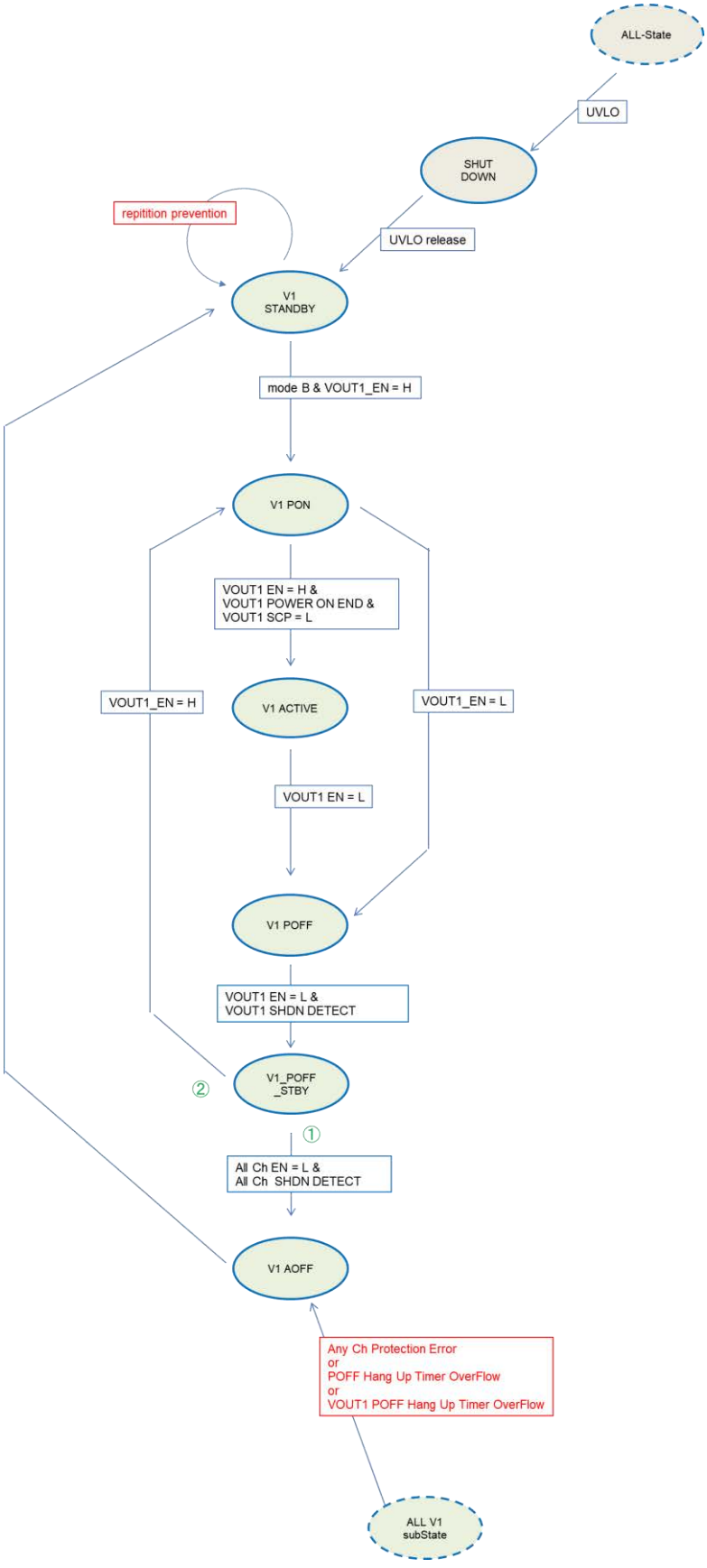


Figure 13. Sub State Machine

4. Function Description – continued

4.2 Whole Sequence Control

4.2.1 Whole Sequence (State Chart)

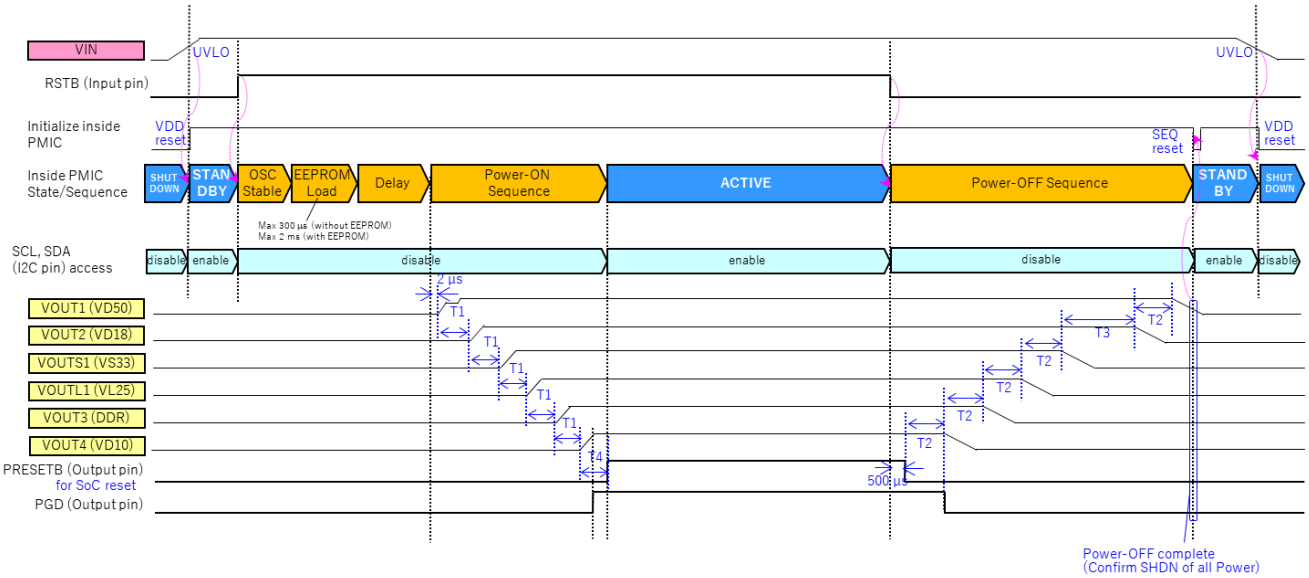


Figure 14. Whole Sequence (State Chart)

4.2.2 General Sequence Description

(SHUTDOWN to STANDBY)

BD9573MUF-M is in SHUTDOWN state during VIN Power off.
After the input of VIN power, internal state starts transition from SHUTDOWN to STANDBY.
In STANDBY state,
Case1: OSC disable (OSC_EN register = "0" setting)
Case2: OSC enable (OSC_EN register = "1" setting)
In Case2, I2C write in STANDBY state is possible since OSC clock is supplied.

[Output Power-ON] (STANDBY to ACTIVE)

By the input of RSTB (pin) = H level, internal state starts transition from STANDBY to ACTIVE, and it initiate Output Power-ON. PGD (pin) output is asserted when all output voltage levels are over 75 % (Typ) x V_{OUT}. PRESETB (pin) is asserted with the interval setting. Then, the transition to ACTIVE state is completed.

[Output Power-OFF] (ACTIVE to STANDBY)

By the input of RSTB (pin) = L level, internal state starts transition from ACTIVE to STANDBY and it initiate Output Power-OFF.
After Power-OFF sequence is completed, BD9573MUF-M is initialized and stops OSC, then completes transition to STANDBY state.

(STANDBY to SHUTDOWN)

UVLO of VFIL becomes effective during VIN power OFF.

4.2.3 I2C Accessible State Condition

I2C accessibility is restricted to only in STANDBY state and ACTIVE state.

Table 14: I2C Accessible Condition

Internal State	I2C read	I2C write
STANDBY	Enable	Disable (with OSC_EN register = "0") / Enable (with OSC_EN register = "1")
EEPROM Load	Disable	Disable
Power-ON STANDBY, ACTIVE, Power-OFF STANDBY	Enable	Enable
Other	Enable	Disable

(Note) Only OSC_EN register can be written without OSC_EN register = "1" setting in STANDBY State.
Some register I2C read value in STANDBY State are 0x00 (initial value), and they may differ from the value after Power-ON.

4.2 Whole Sequence Control – continued

4.2.4 EEPROM Load Function and Internal OSC Stable Time

By connecting external EEPROM to I2C I/F pin (I2C_SCL, I2C_SDA), functions can be customized by the parameters written in EEPROM.
EEPROM load operates before Power-ON sequence started by RSTB = H level.
If EEPROM is connected, 2 ms (Max) EEPROM load time is needed.

Case1: with EEPROM and correct response from EEPROM, EEPROM parameters are loaded.
Case2: with EEPROM and no response (not Acknowledgement) from EEPROM, initial value is used.
Case3: with EEPROM and can not read check code (CON_CHK_CODE is not 0x8E), initial value is used.
Case4: with EEPROM and CRC error has occurred, internal state returns to STANDBY.

In Case2 and Case3, NO_EEP register is set to “1”.
In Case4, EEP_CRC_ERR register is set to “1”.

Regarding “CON_CHK_CODE” and detailed EEPROM setting, please refer to BD9573MUF-M EEPROM setting sheet.

4.2.5 Prevention of Repetition for Protection Error, EEPROM CRC Error

When Protection Function is activated by VR (Voltage Regulator)’s malfunction, every output power is turned off at once and transitions to STANDBY state. In this case, there is a possibility that RSTB = H level is maintained and internal state starts transition from STANDBY to ACTIVE. At that time, every output power is turned off at once again and it may be repeated if the factor of malfunction is not removed.
This kind of repetition is also concerned for EEPROM CRC Error case.
To prevent this repetition, state transition from STANDBY does not start until the input of RSTB = L level.

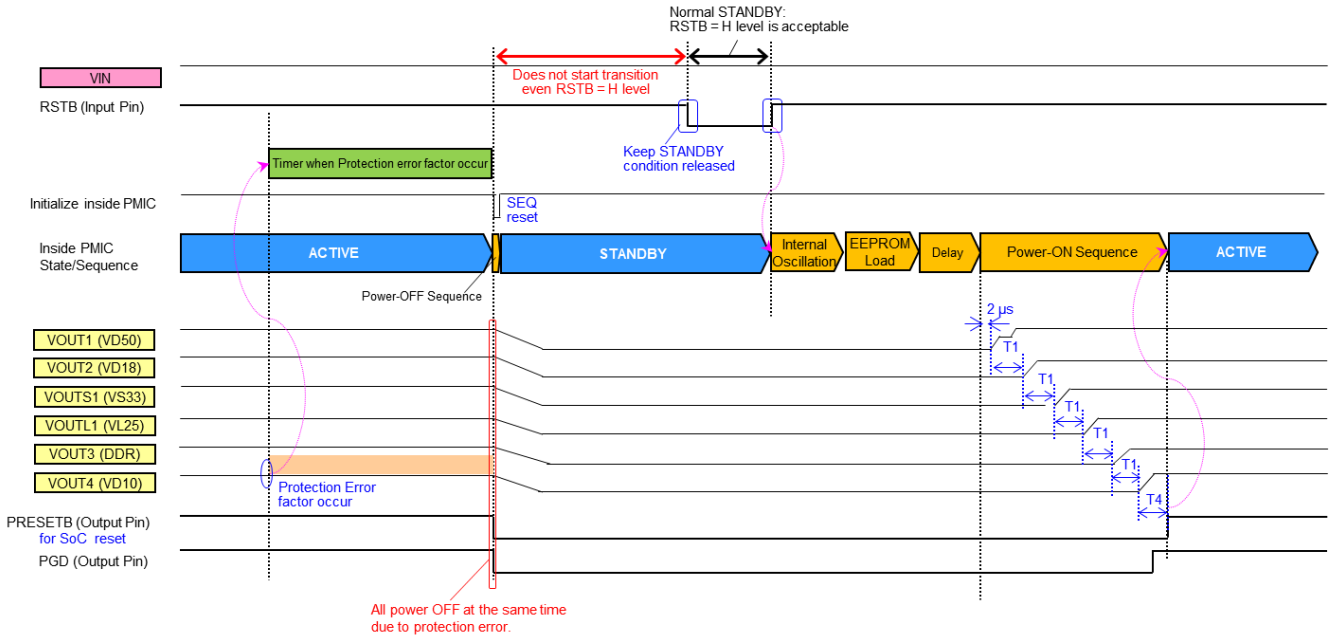


Figure 15. Sequence at Protection Error Occurrence (Timing Chart)

4. Function Description - continued

4.3 VOUT1/VOUTL1 Disable Setting without EEPROM

Without EEPROM setting, VOUT1 or VOUTL1 output can be set to disable by connecting VIN1 or VIN6 to GND. In this case, disable setting outputs are excluded from the Power-ON / Power-OFF sequence automatically. VOUT1 and VOUTL1 disable setting is judged just before EEPROM Load.

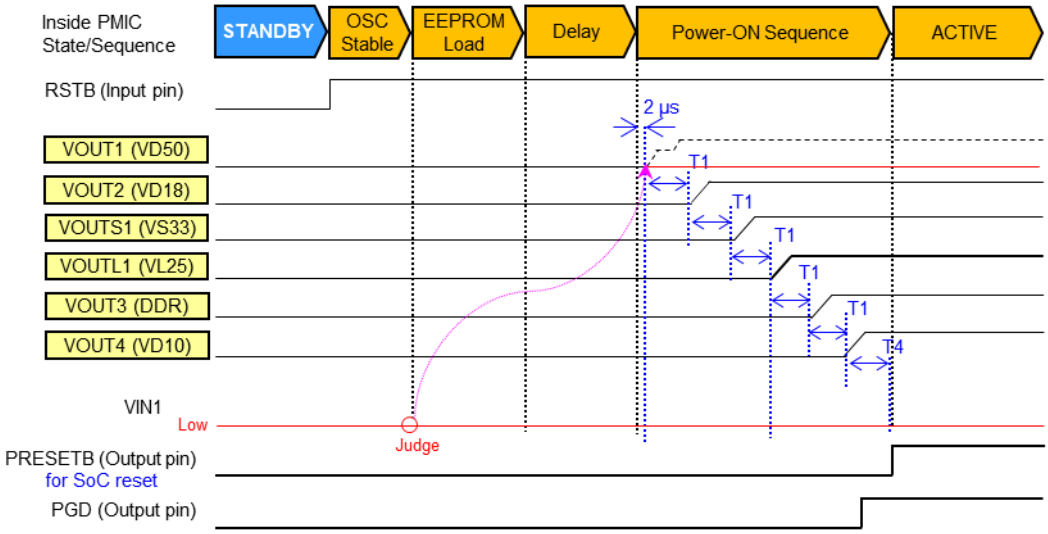


Figure 16. VOUT1 Disable Setting without EEPROM

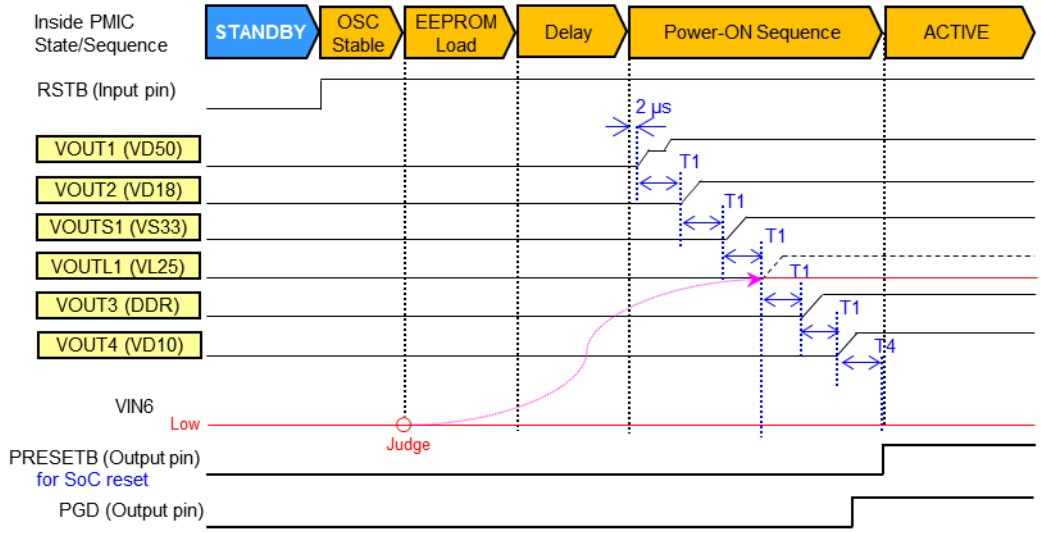


Figure 17. VOUTL1 Disable Setting without EEPROM

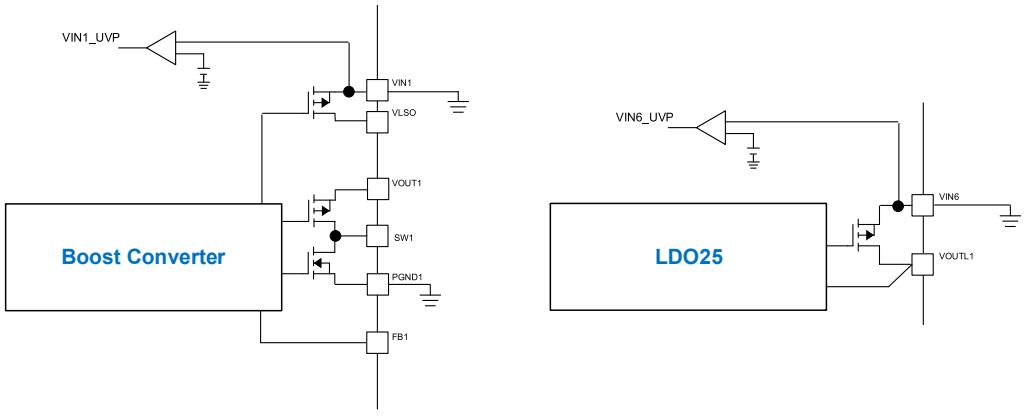


Figure 18. VOUT1 and VOUTL1 OFF Circuit

4. Function Description - continued

4.4 VOUTS1 Disable Setting without EEPROM, Internal/External SW Mode Setting

VOUTS1 output mode is selected by GATECNT (pin).
Mode1: Using VOUTS1 internally (GATECNT = L)
Mode2: Using VOUTS1 externally (GATECNT = H)
Without EEPROM setting, VOUTS1 output can be set to disable by connecting VIN7 and GATECNT to GND.
In this case, disable setting outputs are excluded from the Power-ON / Power-OFF sequence automatically.
Internal/External setting is judged at the end of Self Diagnosis, and Disable setting is judged just before EEPROM Load.
When Power-On, VOUTS1 is used as internal SW for 4.1 ms (±15 %). VOUTS1 changes to external SW after POWER-ON completion. Therefore, voltage drop may occur in VOUTS1 when big current is loaded from VOUTS1 before POWER-ON completion.

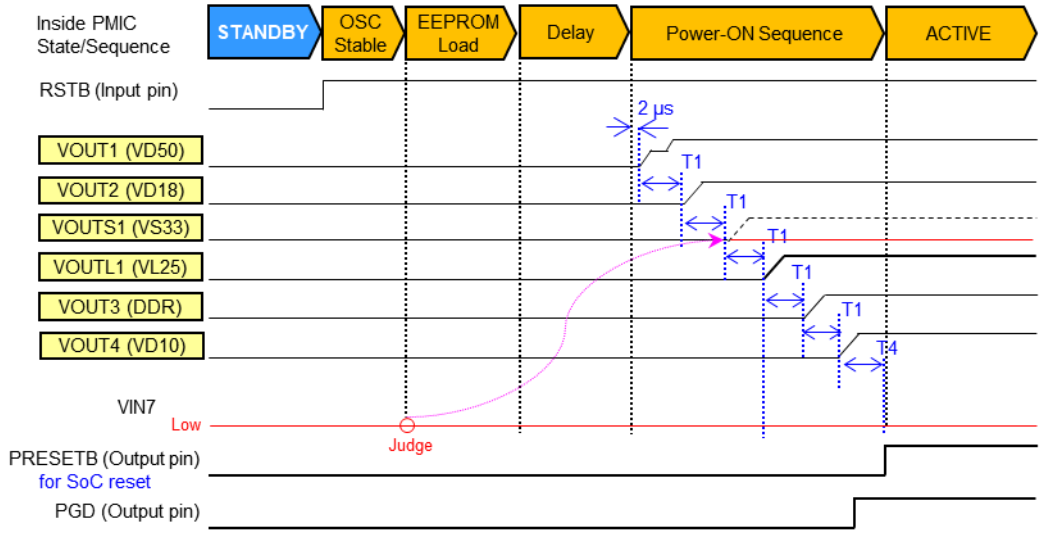


Figure 19. VOUTS1 Disable Setting without EEPROM

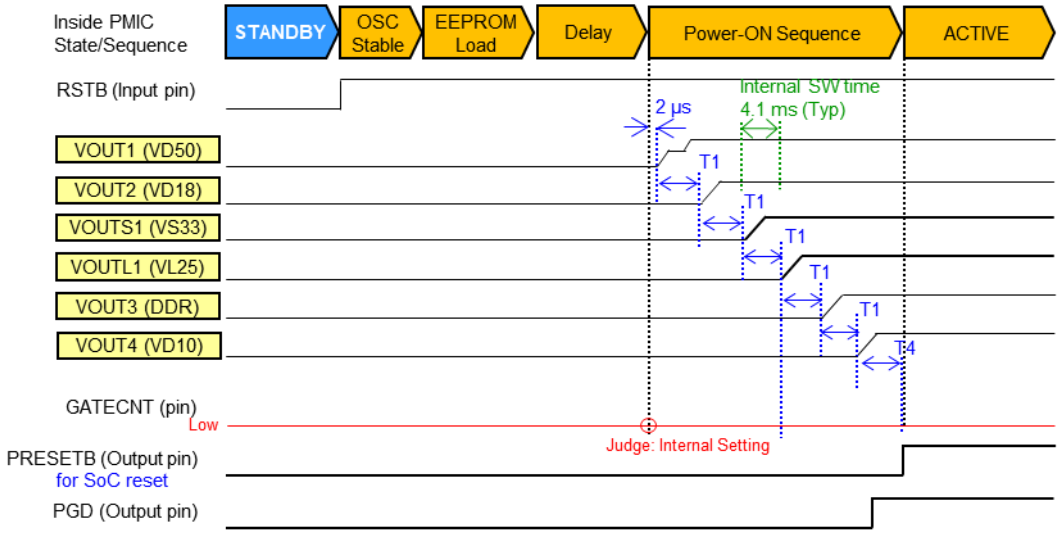


Figure 20. VOUTS1 Internal/External Setting

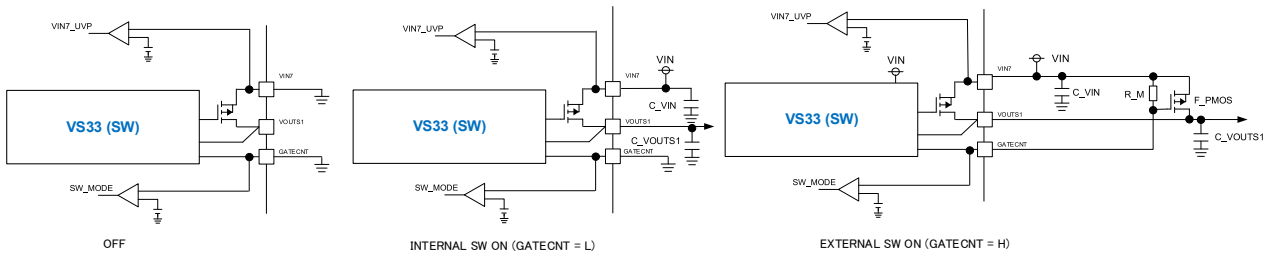


Figure 21. VOUTS1 OFF Circuit and SW Mode Selection

4. Function Description - continued

4.5 I2C I/F

I2C Slave Interface of 1ch is installed in BD9573MUF-M.

I2C Protocol

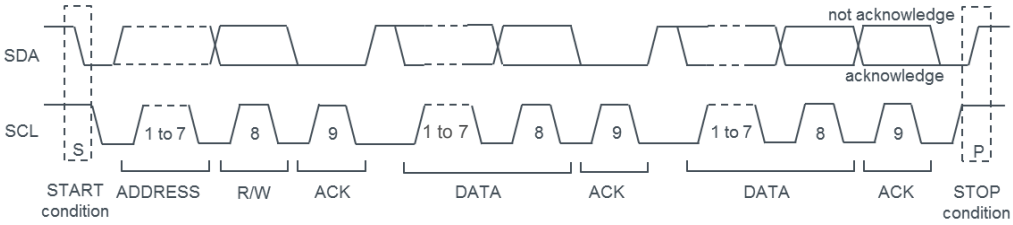


Figure 22. I2C Basic Protocol

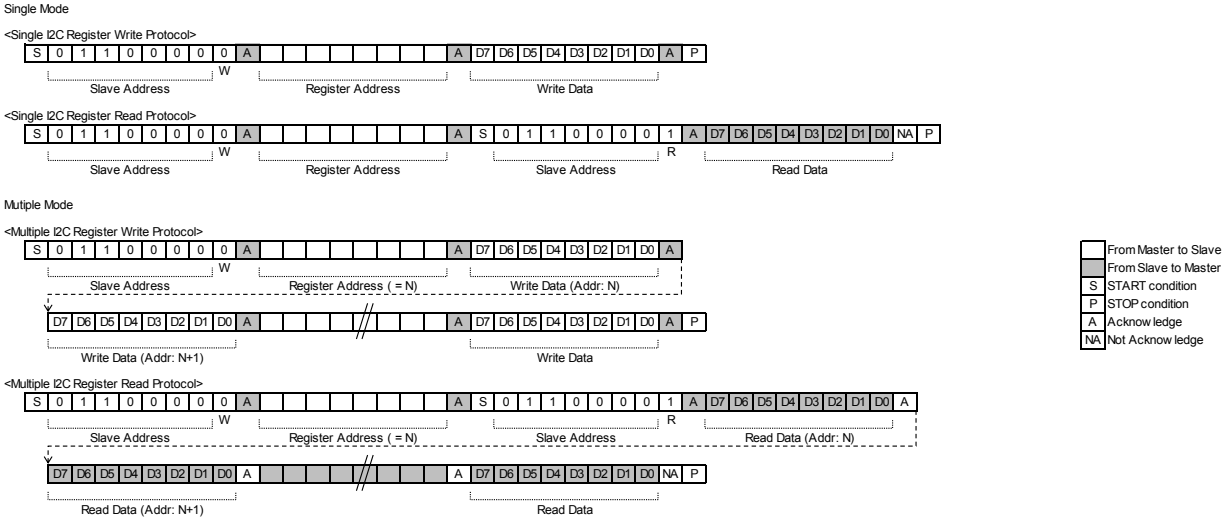


Figure 23. I2C Protocol (Each Access Mode)

Slave Address
Support 7 bit Address mode
Slave Address: 0x30 (When 8 bit description, it is 0x60 in Write mode and 0x61 in Read mode)

Speed Mode
(1) Fast mode
(2) Fast mode plus

Frequency
(1) Fast mode: 400 kHz (Max)
(2) Fast mode plus: 1 MHz (Max)

I2C accessible State condition
(1) I2C read condition: except EEPROM Load state
(2) I2C write condition: In STANDBY state (with OSC_EN register = “1” setting) or ACTIVE state

(Note) For I2C write condition in STANDBY state, 110 µs (Max) wait time after OSC_EN register = “1” is needed.

ACK/NACK Criterion
NACK is output when the Slave Address is not set to 0x30.
NACK is output without the I2C accessible State condition.
ACK is output even with read/write access to register address that is not being used.
ACK is output even with write access to RO attribute register.

Bus Clear
If the data line (SDA) is stuck LOW, please send 18 clock pulses. SDA bus is released by this procedure.
If not, then use the Hardware reset or cycle power to clear the bus.

4.5 I2C I/F – continued

FuSa Mode (Error Detection / Rectification Mode)

FuSa (Functional Safety) mode is a function to detect/rectify transfer error. The 2nd byte of writing data at I2C transfer is given as a FuSa byte to confirm.

Normal I2C mode or FuSa mode (type1 and type2) is selectable by I2C FuSa mode register.

The transfer protocol for this uses the same conventional I2C protocol.
Continuous data write with register address increment is supported.
(Odd-bytes of writing data are the actual data and even-bytes are FuSa byte for confirmation. Address increments every 2 bytes.)
(If FuSa byte returns with error, then the corresponding byte is not written. If the FuSa byte returns without error, then the corresponding byte is written).
FuSa Mode is applied not only write data but also read data by I2C FuSa mode register setting.
Mode switching is valid from the next transferred byte after settings are changed.

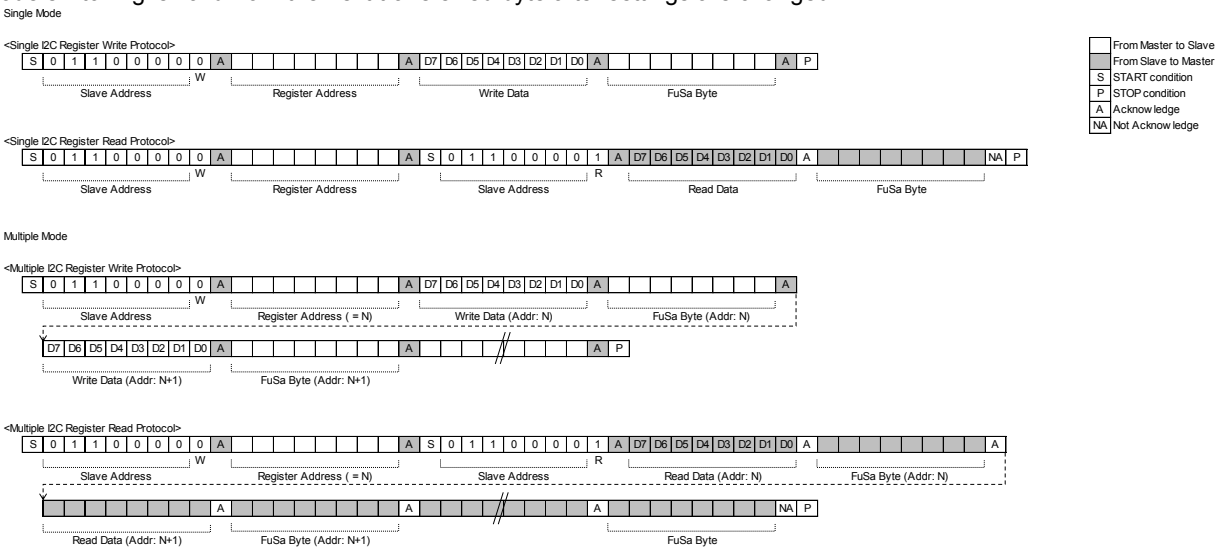
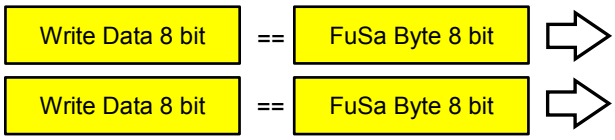


Figure 24. I2C Protocol (FuSa Mode)

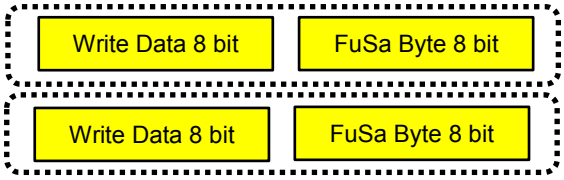
[FuSa Mode Type1 : Compare Write Data and FuSa Byte]



Writes properly to register.

(1) Does not write in register.
(2) Asserts interrupt while changing bit of I2C / Thermal Error Status register. (MD1 interrupt)
I2C_IMASK = “1” (Mask setting)
=> Do no assert
I2C_IMASK = “0” (Mask released)
=> Assert the INTB pin output
MD1 bit is cleared by writing in “1”.

[FuSa Mode Type2 : Error Correction by FuSa Byte (1 bit error)]



ECC Calculation (1 bit error)

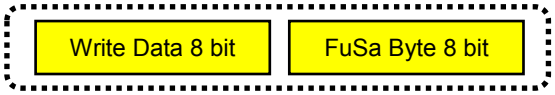
Writes properly to register.

(1) Rectify with FuSa Byte and writes to register.
(2) Asserts interrupt while changing bit of I2C / Thermal Error Status register. (MD2_E1 interrupt)
I2C_IMASK = “1” (Mask setting)
=> Do not assert the INTB pin output
I2C_IMASK = “0” (Mask released)
=> Assert the INTB pin output
MD2_E1 bit is cleared by writing in “1”.
(3) The cause of error is indicated in the I2C MD2_E1 Bit1 register by asserting the corresponding bit.
This is indicated in I2C MD2_E1 Bit2 register if P[4:0] has an error. (Error rectification is unnecessary.)

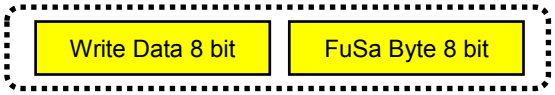
4.5 I2C I/F – continued

[FuSa Mode Type2: Error Correction by FuSa Byte (Error more than 2 bit)]

ECC Calculation (No error)



Writes properly to register.



ECC Calculation (2 bit error)

(1) Does not write in register.
(2) Asserts interrupt while changing bit of I2C / Thermal Error Status register. (MD2_E2 interrupt)
I2C_IMASK = “1” (Mask setting)
=> Do not assert the INTB pin output
I2C_IMASK = “0” (Mask released)
=> Assert the INTB pin output
MD2_E2 bit is cleared by writing in “1”.

4.5 I2C I/F – continued

ECC Calculation Specification

Arrange and add P[4:0] on LSB as FuSa byte[7:0] for FuSa mode type2.

I2C Data Stream

D7	D6	D5	D4	D3	D2	D1	D0	A	0	0	0	P4	P3	P2	P1	P0
Write Data (Addr: N)									FuSa byte (Addr: N)							

Figure 25. I2C Data Format (FuSa Mode type2 = ECC at Calculation)

Transmitter [Encode]

Calculation method of P[4:0] added to DI[7:0] data ("^" means XOR calculation)

```
P[0] =          DI[0] ^ DI[1] ^          DI[3] ^ DI[4]      ^      DI[6]
P[1] =          DI[0] ^          DI[2] ^ DI[3] ^          DI[5] ^ DI[6]
P[2] =                 DI[1] ^ DI[2] ^ DI[3] ^                          DI[7]
P[3] =                                        DI[4] ^ DI[5] ^ DI[6] ^ DI[7]
P[4] =          DI[0] ^ DI[1] ^ DI[2] ^ DI[3] ^ DI[4] ^ DI[5] ^ DI[6] ^ DI[7] ^ P[0] ^ P[1] ^ P[2] ^ P[3]
```

Receiver [Decode]

Error detecting and rectifying method by ECC Factor, receiving DI[7:0] and P[4:0].

ECC Factor Calculation Method
=> Error Detection Judgment/Error

```
ECC[0] = P[0] ^ DI[0] ^ DI[1] ^          DI[3] ^ DI[4] ^          DI[6]
ECC[1] = P[1] ^ DI[0] ^          DI[2] ^ DI[3] ^          DI[5] ^ DI[6]
ECC[2] = P[2] ^          DI[1] ^ DI[2] ^ DI[3] ^                          DI[7]
ECC[3] = P[3] ^                                  DI[4] ^ DI[5] ^ DI[6] ^ DI[7]
ECC[4] =        DI[0] ^ DI[1] ^ DI[2] ^ DI[3] ^ DI[4] ^ DI[5] ^ DI[6] ^ DI[7] ^ P[0] ^ P[1] ^ P[2] ^ P[3] ^ P[4]
```

(1) Error Detection Judgment
Error Detection Judgment based on ECC Factor

Parity Check	Error Codes	Bit in Error	PMIC behavior	
ECC[4]	ECC[3:0]		Error Processing	Flagged Register
0	0000	No error	-	-
0	0001	Multi-bit	Error Detection	MD2_E2_INT
0	0010	Multi-bit	Error Detection	MD2_E2_INT
0	0011	Multi-bit	Error Detection	MD2_E2_INT
0	0100	Multi-bit	Error Detection	MD2_E2_INT
0	0101	Multi-bit	Error Detection	MD2_E2_INT
0	0110	Multi-bit	Error Detection	MD2_E2_INT
0	0111	Multi-bit	Error Detection	MD2_E2_INT
0	1000	Multi-bit	Error Detection	MD2_E2_INT
0	1001	Multi-bit	Error Detection	MD2_E2_INT
0	1010	Multi-bit	Error Detection	MD2_E2_INT
0	1011	Multi-bit	Error Detection	MD2_E2_INT
0	1100	Multi-bit	Error Detection	MD2_E2_INT
0	1101	Multi-bit	Error Detection	MD2_E2_INT
0	1110	Multi-bit	Error Detection	MD2_E2_INT
0	1111	Multi-bit	Error Detection	MD2_E2_INT

Parity Check	Error Codes	Bit in Error	PMIC behavior	
ECC[4]	ECC[3:0]		Error Processing	Flagged Register
1	0000	P4	-	MD2_E1_INT
1	0001	P0	-	MD2_E1_INT
1	0010	P1	-	MD2_E1_INT
1	0011	D0	Error Correction	MD2_E1_INT
1	0100	P2	-	MD2_E1_INT
1	0101	D1	Error Correction	MD2_E1_INT
1	0110	D2	Error Correction	MD2_E1_INT
1	0111	D3	Error Correction	MD2_E1_INT
1	1000	P3	-	MD2_E1_INT
1	1001	D4	Error Correction	MD2_E1_INT
1	1010	D5	Error Correction	MD2_E1_INT
1	1011	D6	Error Correction	MD2_E1_INT
1	1100	D7	Error Correction	MD2_E1_INT
1	1101	Multi-bit	Error Detection	MD2_E2_INT
1	1110	Multi-bit	Error Detection	MD2_E2_INT
1	1111	Multi-bit	Error Detection	MD2_E2_INT

for displaying error bit position: I2C MD2_E1 Bit 1 register, I2C MD2_E1 Bit 2 register

Figure 26. Error Detection Judgement by ECC Calculation

(2) Error Rectification
Error Correction is operated by following calculation for Single bit Error.

```
DO[0] = DI[0] ^ (    ECC[0] &    ECC[1] & ~ECC[2] & ~ECC[3] &    ECC[4] )
DO[1] = DI[1] ^ (    ECC[0] & ~ECC[1] &    ECC[2] & ~ECC[3] &    ECC[4] )
DO[2] = DI[2] ^ ( ~ECC[0] &    ECC[1] &    ECC[2] & ~ECC[3] &    ECC[4] )
DO[3] = DI[3] ^ (    ECC[0] &    ECC[1] &    ECC[2] & ~ECC[3] &    ECC[4] )
DO[4] = DI[4] ^ (    ECC[0] & ~ECC[1] & ~ECC[2] &    ECC[3] &    ECC[4] )
DO[5] = DI[5] ^ ( ~ECC[0] &    ECC[1] & ~ECC[2] &    ECC[3] &    ECC[4] )
DO[6] = DI[6] ^ (    ECC[0] &    ECC[1] & ~ECC[2] &    ECC[3] &    ECC[4] )
DO[7] = DI[7] ^ ( ~ECC[0] & ~ECC[1] &    ECC[2] &    ECC[3] &    ECC[4] )
```

Figure 27. Error Correction Calculation

4. Function Description - continued

4.6 Interrupt Function

4.6.1 Interrupt Function Description

Interruptions are notified from the INTB pin when interruption requests are enabled by any interruption factors.
The meaning of the words relevant to interruption are defined as followed.

"Interruption Factor": Factor of any condition where an interruption is made.
"Interruption Mask": Controls which interruption factors cause an interruption to occur.
(Masked: No interruption / No Mask: interruption occurs).
"Interruption Request": Interruption request only becomes active when the interruption factor is active and the interruption is not masked.

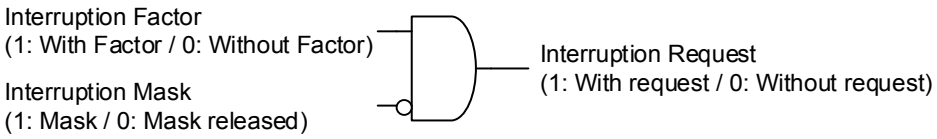


Figure 28. Interruption Factor/Mask/Request

Each factor can be masked, read or cleared by I2C. Also, INTB utilizes active-low pin operation.

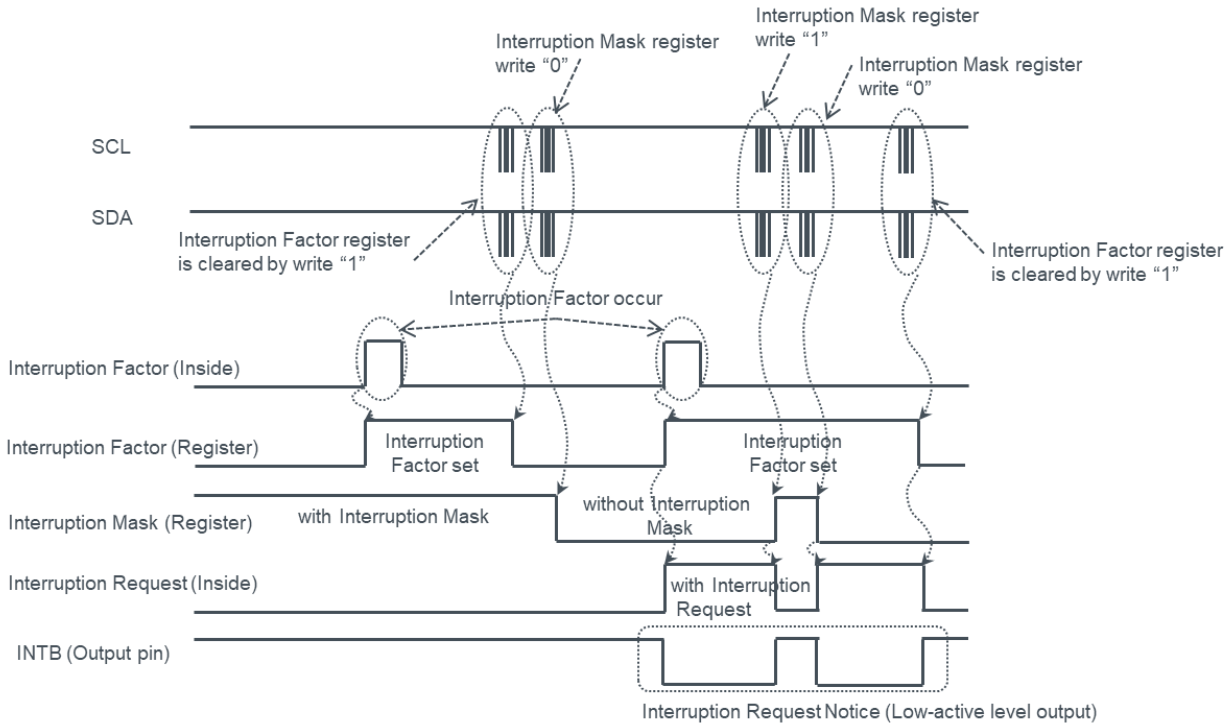


Figure 29. Interrupt Function Description

4.6 Interrupt Function – continued

4.6.2 Interruption Factor

Interruption request notice function is implemented in 2 levels for the factor.

(1) Primary level interruption register of final stage
(2) Interruption register in secondary level of each function block stage

Following figure shows the logical flowchart of Interruption Factor/Mask/Request implemented in BD9573MUF-M.

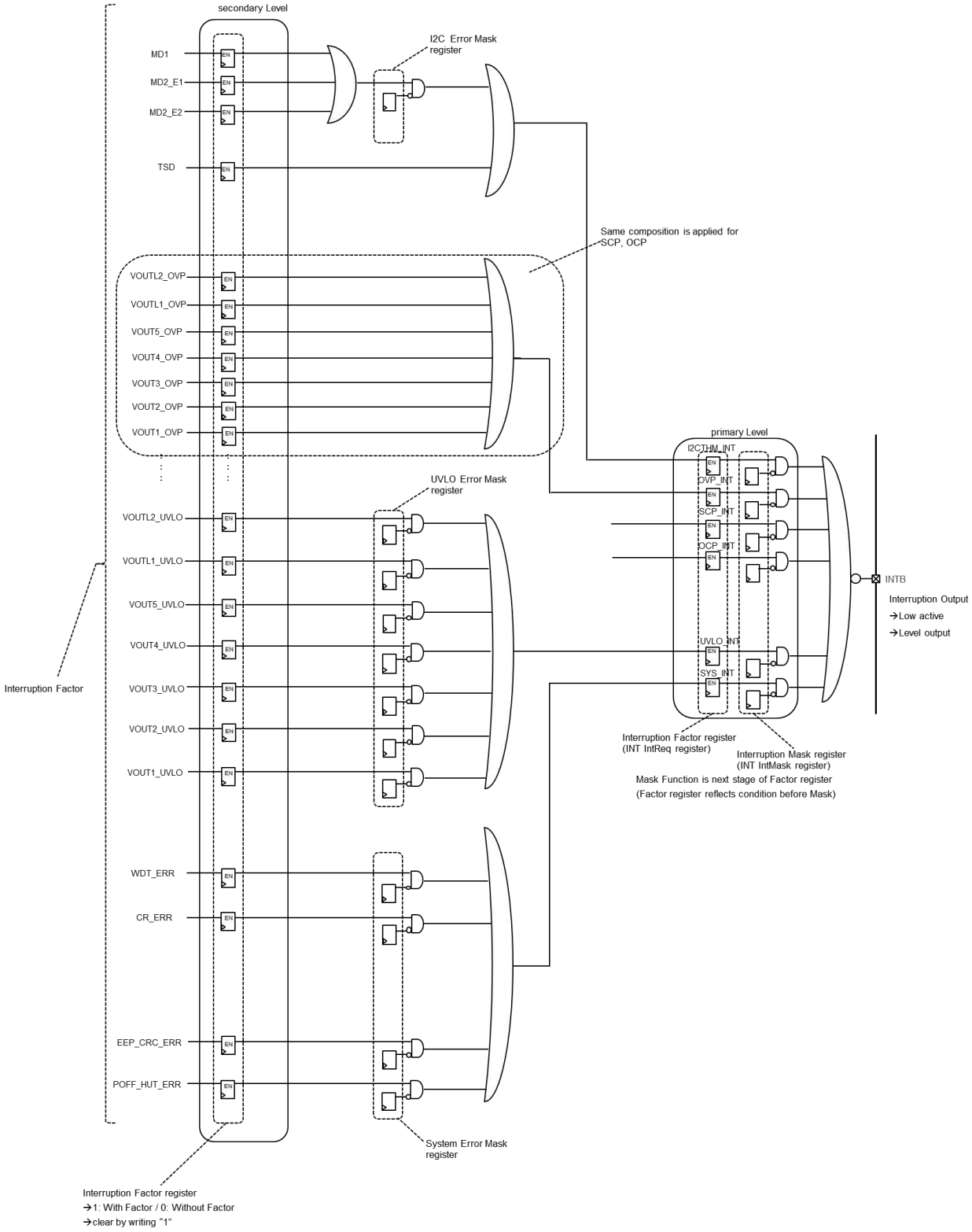


Figure 30. System Diagram of Interruption Function

4.6.2 Interruption Factor – continued

Following Shows All Interruption Factors.

(A) Interruption in Primary level

Interruption Factor register: INT IntReq register
Interruption Mask register: INT IntMask register

Table 15: Interruption at Primary Level

Interruption Factor (INT IntReq Register)	Interruption Mask (INT IntMask Register)	Detail of Interruption Factor	Active Condition of Interruption Factor
I2CTHM_INT	I2CTHM_IMASK	I2C Transfer Error, Thermal Error (TSD)	Error judged at writing register, Thermal Error detection
OVP_INT	OVP_IMASK	OVP Error Status	OVP detection
SCP_INT	SCP_IMASK	SCP Error Status	SCP detection
OCP_INT	OCP_IMASK	OCP Error Status	OCP detection
UVP_INT	UVP_IMASK	UVP Error Status	UVP detection
SYS_INT	SYS_IMASK	System Error Status	System Error detection

(B) Interruption in Secondary Level

Regarding factors in Secondary Level, please refer the next page.

4.6.2 Interruption Factor – continued

Table 16: Interruption at Secondary Level 2

Interruption Request	Interruption Mask	Detail of Interruption Factor
MD1	I2C_IMASK	FuSa Mode Type1 error
MD2_E1		FuSa Mode Type2 error 1 bit
MD2_E2		FuSa Mode Type2 error more than 2 bit
TSD	-	Thermal Shutdown
VOUT1_OVP	-	VD50 power Output over voltage protection
VOUT2_OVP		VD18 power Output over voltage protection
VOUT3_OVP		DDR power Output over voltage protection
VOUT4_OVP		VD10 power Output over voltage protection
VOUTL1_OVP		VL25 power Output over voltage protection
VOUT1_OCP	-	VD50 power Output over current protection
VOUT2_OCP		VD18 power Output over current protection
VOUT3_OCP		DDR power Output over current protection
VOUT4A_OCP		VD10A power Output over current protection
VOUT4B_OCP		VD10B power Output over current protection
VOUTS1_OCP		VS33 power Output over current protection
LDSW_OCP		LDSW power Output over current protection
VOUT1_SCP	-	VD50 power Output short circuit protection
VOUT2_SCP		VD18 power Output short circuit protection
VOUT3_SCP		DDR power Output short circuit protection
VOUT4_SCP		VD10 power Output short circuit protection
VOUTL1_SCP		VL25 power Output short circuit protection
VIN1_UVP	-	VD50 power Input under voltage protection
VIN2_UVP		VD18 power Input under voltage protection
VIN3_UVP		DDR power Input under voltage protection
VIN4_UVP		VD10A power Input under voltage protection
VIN5_UVP		VD10B power Input under voltage protection
VIN6_UVP		VL25 power Input under voltage protection
VIN7_UVP		VS33 power Input under voltage protection
WDT_ERR	WDT_E_IMASK	WDI Input Clock Frequency Error
EEP_CRC_ERR	EEPCRC_E_IMASK	CRC Error during EEPROM Load
EEP_END	EEP_END_IMASK	EEPROM Load End
POFF_HUT_ERR	POFFHUT_E_IMASK	Hang-Up Timer counts over 400 ms
V1_HUT_ERR	V1_HUT_E_IMASK	Hang-Up Timer for VOUT1 (only for Mode B), 100 ms

4. Function Description – continued

4.7 Power Abnormality Monitoring Function (Protection Error Detection)

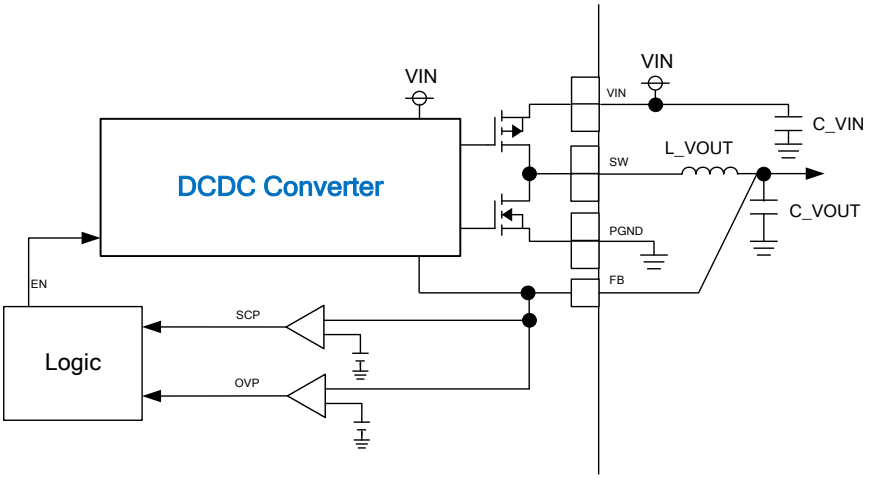


Figure 31. Power Abnormality Monitoring Circuit

Power Abnormality Monitoring Function for SCP and OCP work as follows:
LDSW_OCP function is excluded.

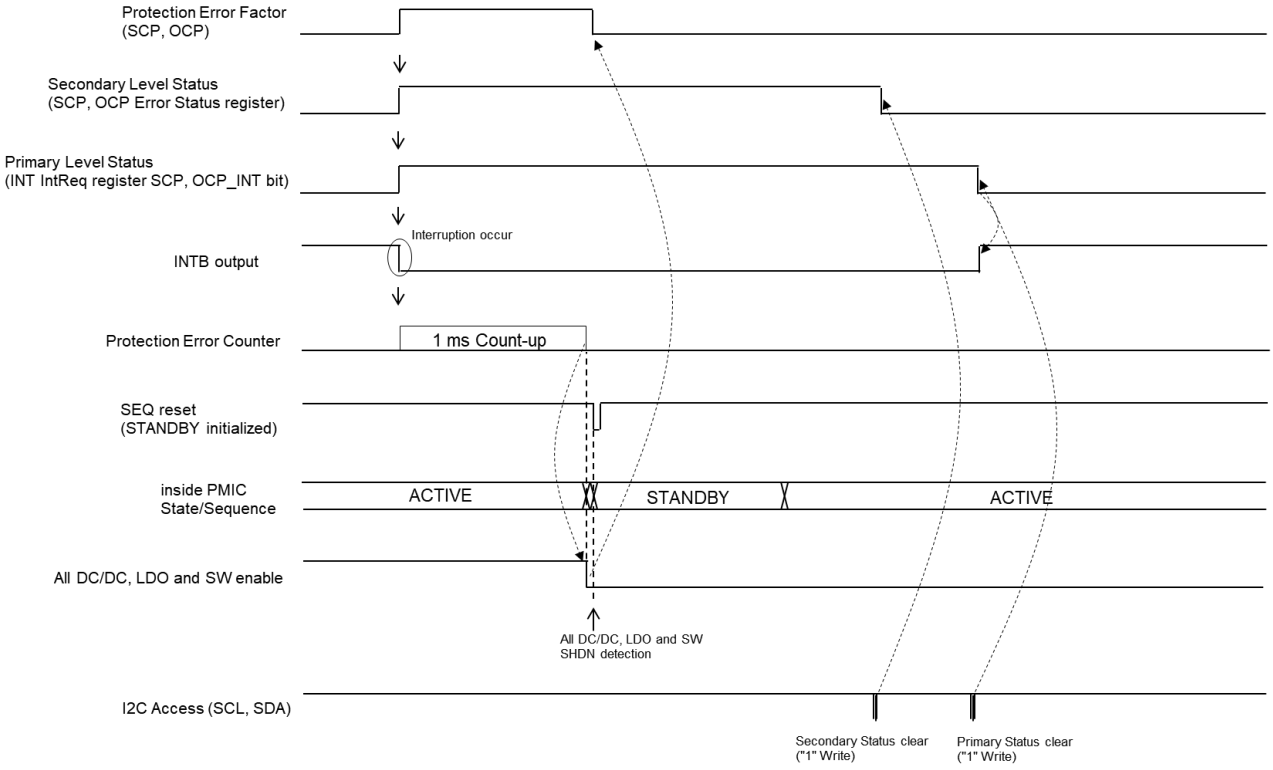


Figure 32. Timing Chart when Protection Error Factor Occur 1

4.7 Power Abnormality Monitoring Function (Protection Error Detection) – continued

Power Abnormality Monitoring Function for OVP and TSD work as follows:

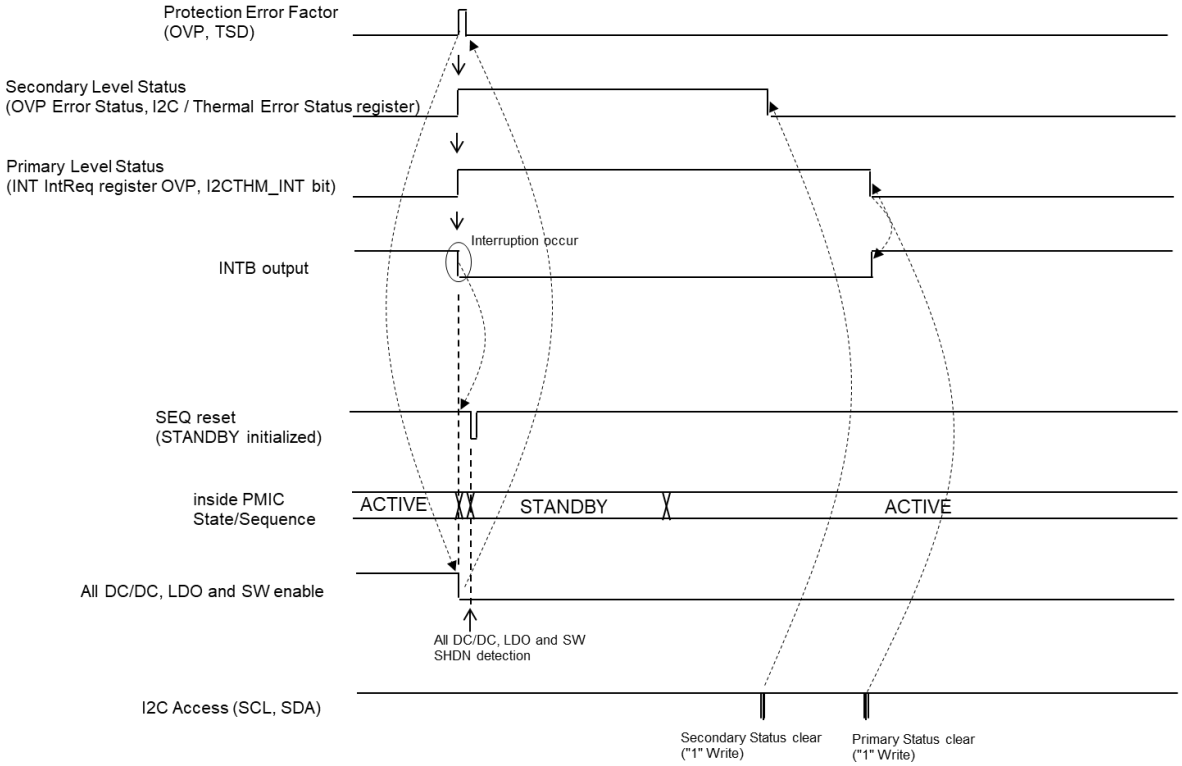


Figure 33. Timing Chart when Protection Error Factor Occur 2

4. Function Description – continued

4.8 SYNC Function

The SYNC pin is used to synchronize the DC/DC switching frequency with external pulse clock signal.
SYNC input frequency range is from 1.8 MHz to 2.2 MHz, and SYNC input pulse duty range is from 45 % to 55 %.
Entering abnormal clock through the SYNC pin (e.g. out of range signal) may cause malfunction.

The external pulse clock signal is reflected in ACTIVE mode. This pin can be remained open if synchronization is not needed. The SYNC pin needs 10 kΩ external pull down resistor when synchronization signal is supplied from R-car SoC.

4. Function Description – continued

4.9 WDT Function

Watch Dog Timer (WDT) monitors the WDI pin input by detecting the rising edge of WDI input pulse.
This function is enabled by WDEN (pin) = H in ACTIVE state. If WDT Error is detected, the WDO pin output is negated.

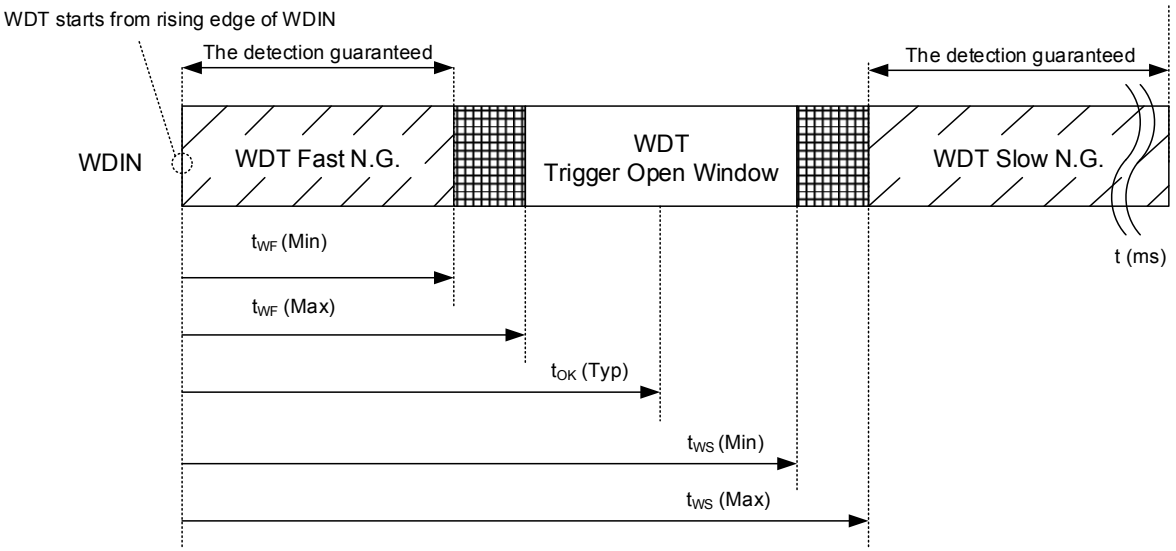


Figure 34. WDT Function

WDT FAST N.G. Detection

1. WDI input signal is ignored when WDEN = L or internal state is not ACTIVE. WDT is activated when WDEN = H.
2. For the initial duration just after WDEN goes to high, only SLOW N.G. time detection works and FAST N.G. does not work. If rise edge of WDI comes within SLOW N.G. time, then
   (1) both FAST N.G. and SLOW N.G. time detections start to work. (TYPE register (0x16[5]) = H)
   (2) only SLOW N.G. time detection starts to work. (TYPE register (0x16[5]) = L)
3. These time detection monitors the time until next rising edge and when it detects WDI edge within FAST N.G. time (t_{WF}), WDO becomes LOW. WDO goes back to High after 100 ms (Typ) delay.
4. When WDO becomes High, WDT is activated again and operation resumes.
   Only SLOW N.G. time detection works until the next first rising edge, and both SLOW and FAST N.G. starts at the first rising edge like state 1.

When WDEN is Low, WDO becomes H and WDT is disabled. During this period, WDI input signal is ignored and WDO output is not affected.
Regarding WDI input signal, over 200 µs H level is required to be detected as “H” level.

FAST/SLOW N.G. Detection Area is determined by FAST_NG[2:0] and NG_RATIO[1:0] register setting.
WDIN input clock duration is set by FAST_NG[2:0] register value.

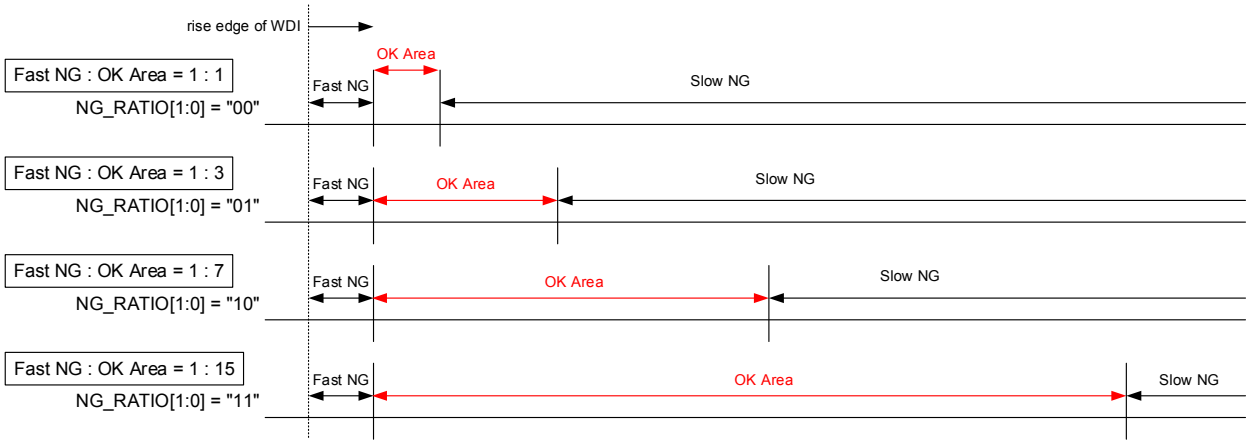


Figure 35. WDT NG RATIO

4.9 WDT Function – continued

Table 17: WDT setting (NG_RATIO[1:0] = “00”)

FAST_NG[2:0]	Fast NG Detection (ms)		t_{OK} (ms) (Typ)	Slow NG Detection (ms)	
	t_{WF} (Min)	t_{WF} (Max)		t_{WS} (Min)	t_{WS} (Max)
“000”	1.7	2.3	3.0	3.6	4.6
“001”	3.4	4.6	6.0	7.4	9.2
“010”	6.8	9.2	12.0	14.5	18.5
“011”	13.5	18.5	24.0	29.5	36.5
“100”	27.5	36.5	48.0	59.5	73.0
“101”	55.0	73.0	96.0	119.0	146.0
“110”	110.0	146.0	192.0	238.0	292.0
“111”	220.0	292.0	384.0	476.0	583.0

Table 18: WDT setting (NG_RATIO[1:0] = “01”)

FAST_NG[2:0]	Fast NG Detection (ms)		t_{OK} (ms) (Typ)	Slow NG Detection (ms)	
	t_{WF} (Min)	t_{WF} (Max)		t_{WS} (Min)	t_{WS} (Max)
“000”	1.7	2.3	4.8	7.2	9.2
“001”	3.4	4.6	9.7	14.8	18.4
“010”	6.8	9.2	19.0	29.0	37.0
“011”	13.5	18.5	39.0	59.0	73.0
“100”	27.5	36.5	78.0	119.0	146.0
“101”	55.0	73.0	156.0	238.0	292.0
“110”	110.0	146.0	311.0	476.0	584.0
“111”	220.0	292.0	622.0	952.0	1166.0

Table 19: WDT setting (NG_RATIO[1:0] = “10”)

FAST_NG[2:0]	Fast NG Detection (ms)		t_{OK} (ms) (Typ)	Slow NG Detection (ms)	
	t_{WF} (Min)	t_{WF} (Max)		t_{WS} (Min)	t_{WS} (Max)
“000”	1.7	2.3	8.4	14.4	18.4
“001”	3.4	4.6	17.0	29.6	36.8
“010”	6.8	9.2	33.5	58.0	74.0
“011”	13.5	18.5	68.0	118.0	146.0
“100”	27.5	36.5	137.0	238.0	292.0
“101”	55.0	73.0	275.0	476.0	584.0
“110”	110.0	146.0	550.0	952.0	1168.0
“111”	220.0	292.0	1100.0	1904.0	2332.0

Table 20: WDT setting (NG_RATIO[1:0] = “11”)

FAST_NG[2:0]	Fast NG Detection (ms)		t_{OK} (ms) (Typ)	Slow NG Detection (ms)	
	t_{WF} (Min)	t_{WF} (Max)		t_{WS} (Min)	t_{WS} (Max)
“000”	1.7	2.3	15.5	28.8	36.8
“001”	3.4	4.6	32.0	59.2	73.6
“010”	6.8	9.2	63.0	116.0	148.0
“011”	13.5	18.5	127.0	236.0	292.0
“100”	27.5	36.5	256.0	476.0	584.0
“101”	55.0	73.0	512.0	952.0	1168.0
“110”	110.0	146.0	1025.0	1904.0	2336.0
“111”	220.0	292.0	2050.0	3808.0	4664.0

4.9 WDT Function – continued

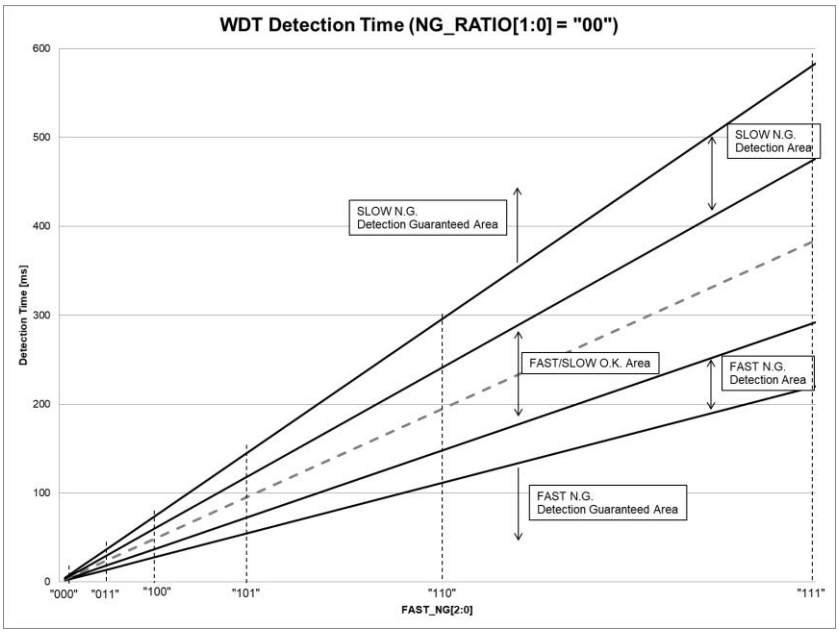


Figure 36. WDT Detection Time when NG_RATIO[1:0] = “00”

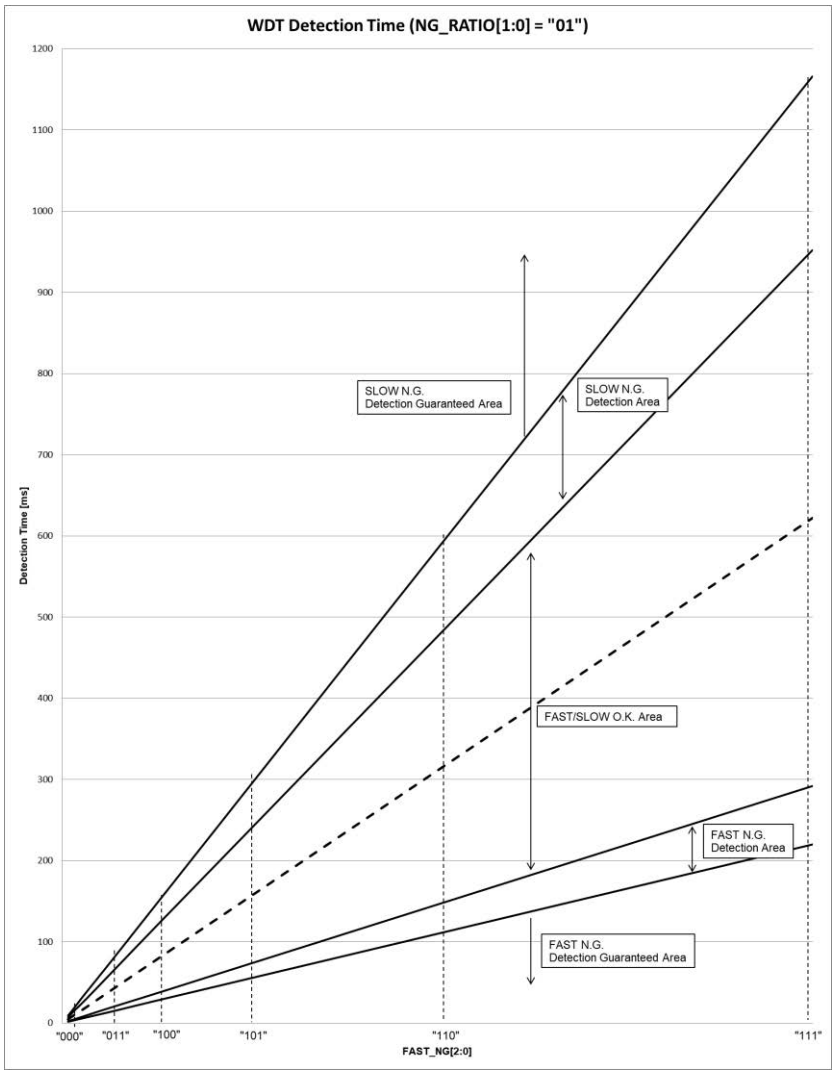


Figure 37. WDT Detection Time when NG_RATIO[1:0] = “01”

5. Register Specification

5.1 Register Map

…Initializes at either VIN reset (VFIL UVLO) or SEQ reset (STANDBY transition)

…Initializes only at VIN reset (VFIL UVLO)

Table 21: I2C I/F Register Map

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default	
0x00	Vendor Code	1	1	0	1	1	0	1	1	RO	0xDB	
0x01	Product Code	0	1	1	1	0	0	1	1	RO	0x73	
0x02	Product Revision	0	0	0	0	0	0	0	1	RO	0x01	
-	-	-	-	-	-	-	-	-	-	-	-	
0x10	I2C FuSa Mode	-	-	-	SMOD_read	-	-	I2C_SMOD[1:0]		R/W	0x00	
0x11	-	-	-	-	-	-	-	-	-	R/W	0x00	
0x12	-	-	-	-	-	-	-	-	-	R/W	0x03	
0x13	SSCG Cnt	-	SSCG_PERI	SSCG_FORM[1:0]		-	-	-	SSCG_EN	R/W	0x00	
0x14	SMRB Write Protect	SMRB_WP[7:0]								R/W	0x00	
0x15	SMRB Cnt	-	-	-	SMRB_hist	-	-	-	SMRB_asrt	R/W	0x01	
0x16	Watch Dog Timer setting	-	-	TYPE	NG_RATIO[1:0]		FAST_NG[2:0]			R/W	0x20	
0x17	OSC Enable	-	-	-	-	-	-	-	OSC_EN	R/W	0x00	
0x18	PGD Setting	-	-	PGD_SETTING[5:0]						R/W	0x3F	
-	-	-	-	-	-	-	-	-	-	-	-	
0x20	PMIC Internal Status	-	-	-	NO_EEP	PMIC_STATE[3:0]				RO	0x00	
0x21	I2C MD2_E1 Bit 1	I2C_MD2_E1_BIT[7:0]								RO	0x00	
0x22	I2C MD2_E1 Bit 2	-	-	-	I2C_MD2_E1_BIT_P[4:0]					RO	0x00	
0x23	I2C / Thermal Error Status	-	-	-	TSD	-	MD2_E2	MD2_E1	MD1	R/W	0x00	
0x24	I2C / Thermal Error Mask	-	-	-	-	-	-	-	I2C_IMASK	R/W	0x00	
0x25	OVP Error Status	-	-	VOUTL1_OVP	-	VOUT4_OVP	VOUT3_OVP	VOUT2_OVP	VOUT1_OVP	R/W	0x00	
0x26	SCP Error Status	-	-	VOUTL1_SCP	-	VOUT4_SCP	VOUT3_SCP	VOUT2_SCP	VOUT1_SCP	R/W	0x00	
0x27	OCP Error Status	LDSW_OCP	VOUTS1_OCP	-	VOUT4B_OCP	VOUT4A_OCP	VOUT3_OCP	VOUT2_OCP	VOUT1_OCP	R/W	0x00	
0x28	-	-	-	-	-	-	-	-	-	R/W	0x00	
0x29	-	-	-	-	-	-	-	-	-	R/W	0x00	
0x2A	UVP Error Status	-	VIN7_UVP	VIN6_UVP	VIN5_UVP	VIN4_UVP	VIN3_UVP	VIN2_UVP	VIN1_UVP	R/W	0x00	
0x2B	System Status	V1_HUT_ERR	HUT_ERR	EEP_END	EEP_CRC_ERR	-	-	WDT_ERR	-	R/W	0x00	
0x2C	System Status Mask	V1_HUT_E_IMASK	HUT_E_IMASK	EEP_END_IMASK	EEPCRC_E_IMASK	-	-	WDT_E_IMASK	-	R/W	0x20	
-	-	-	-	-	-	-	-	-	-	-	-	
-	-	-	-	-	-	-	-	-	-	-	-	
0x30	INT IntReq	SYS_INT	UVP_INT	-	-	OCP_INT	SCP_INT	OVP_INT	I2CTHM_INT	R/W	0x00	
0x31	INT IntMask	SYS_IMASK	UVP_IMASK	-	-	OCP_IMASK	SCP_IMASK	OVP_IMASK	I2CTHM_IMASK	R/W	0x00	
-	-	-	-	-	-	-	-	-	-	-	-	
0x40	POW Write Protect	POW_WP[7:0]								R/W	0x00	
0x41	POW Trigger VOUT1	POFF_TRG_VOUT1[3:0]				PON_TRG_VOUT1[3:0]				R/W	0x20	
0x42	POW Trigger VOUT2	POFF_TRG_VOUT2[3:0]				PON_TRG_VOUT2[3:0]				R/W	0x61	
0x43	POW Trigger VOUT3	POFF_TRG_VOUT3[3:0]				PON_TRG_VOUT3[3:0]				R/W	0x45	
0x44	POW Trigger VOUT4	POFF_TRG_VOUT4[3:0]				PON_TRG_VOUT4[3:0]				R/W	0x73	
0x45	POW Trigger VOUTL1	POFF_TRG_VOUTL1[3:0]				PON_TRG_VOUTL1[3:0]				R/W	0x36	
0x46	POW Trigger VOUTS1	POFF_TRG_VOUTS1[3:0]				PON_TRG_VOUTS1[3:0]				R/W	0x52	
0x47	POW Trigger PRESETB	POFF_TRG_PRESETB[3:0]				PON_TRG_PRESETB[3:0]				R/W	0x04	
0x48	POW Wait VOUT1	POFF_WAIT_VOUT1[3:0]				PON_WAIT_VOUT1[3:0]				R/W	0x00	
0x49	POW Wait VOUT2	POFF_WAIT_VOUT2[3:0]				PON_WAIT_VOUT2[3:0]				R/W	0x00	
0x4A	POW Wait VOUT3	POFF_WAIT_VOUT3[3:0]				PON_WAIT_VOUT3[3:0]				R/W	0x00	
0x4B	POW Wait VOUT4	POFF_WAIT_VOUT4[3:0]				PON_WAIT_VOUT4[3:0]				R/W	0x00	
0x4C	POW Wait VOUTL1	POFF_WAIT_VOUTL1[3:0]				PON_WAIT_VOUTL1[3:0]				R/W	0x00	
0x4D	POW Wait VOUTS1	POFF_WAIT_VOUTS1[3:0]				PON_WAIT_VOUTS1[3:0]				R/W	0x00	
0x4E	POW Wait PRESETB	POFF_WAIT_PRESETB[3:0]				PON_WAIT_PRESETB[3:0]				R/W	0x00	
-	-	-	-	-	-	-	-	-	-	-	-	
0x50	VOUT1 TUNE	V1_SIGN	-	-	-	-	VOUT1_TUNE[2:0]			RO	0x00	
0x51	-	-	-	-	-	-	-	-	-	R/W	0x43	
0x52	-	-	-	-	-	-	-	-	-	R/W	0x43	
0x53	VOUT2 TUNE	V2_SIGN	-	-	-	-	VOUT2_TUNE[2:0]			RO	0x00	
0x54	-	-	-	-	-	-	-	-	-	R/W	0x37	
0x55	-	-	-	-	-	-	-	-	-	R/W	0x37	
0x56	VOUT3 TUNE	V3_SIGN	-	-	VOUT3_TUNE[4:0]					RO	0x00	
0x57	-	-	-	-	-	-	-	-	-	R/W	0x3E/0x27	(Note 1)
0x58	-	-	-	-	-	-	-	-	-	R/W	0x23/0x27	(Note 2)
0x59	VOUT4 TUNE	V4_SIGN	-	-	VOUT4_TUNE[4:0]					RO	0x00	
0x5A	-	-	-	-	-	-	-	-	-	R/W	0x19	
0x5B	-	-	-	-	-	-	-	-	-	R/W	0x19	
0x5C	VOUTL1 TUNE	VL1_SIGN	-	-	-	-	VOUTL1_TUNE[2:0]			RO	0x00	
0x5D	-	-	-	-	-	-	-	-	-	R/W	0x40	
0x5E	-	-	-	-	-	-	-	-	-	R/W	0x40	
0x5F	-	-	-	-	-	-	-	-	-	R/W	0x10/0x06	(Note 3)
0x60	VOUTS1 OCP	-	-	VOUTS1_OCP[5:0]						R/W	0x16/0x08	(Note 4)
0x61	-	-	-	-	-	-	-	-	-	R/W	0x33	

(Note) Please do not access to the address except above.

(Note 1) DDR_SEL (pin) = L: Default value is 0x3E.
DDR_SEL (pin) = H: Default value is 0x27.

(Note 2) DDR_SEL (pin) = L: Default value is 0x23.
DDR_SEL (pin) = H: Default value is 0x27.

(Note 3) GATECNT (pin) = L: Default value is 0x10.
GATECNT (pin) = H: Default value is 0x06.

(Note 4) GATECNT (pin) = L: Default value is 0x16.
GATECNT (pin) = H: Default value is 0x08.

5. Register Specification – continued

5.2 Register Description

5.2.1 Recognition Code Indicator

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
Vendor Code	0x00	1	1	0	1	1	0	1	1	RO	0xDB

Vendor Recognition Code
0xDB: Rohm

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
Product Code	0x01	0	1	1	1	0	0	1	1	RO	0x73

Product Recognition Code
0x73: BD9573MUF-M

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
Product Revision	0x02	0	0	0	0	0	0	0	1	RO	0x01

Product Revision Recognition Code
0x01: Rev.1 Sample

5.2.2 FuSa Mode (Error Detection / Rectification Mode)

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
I2C FuSa Mode	0x10	-	-	-	SMOD_read	-	-	I2C_SMOD[1:0]		R/W	0x00

I2C_SMOD[1:0] FuSa Mode Setting

"00": General mode (NO FuSa mode) => Normal I2C format without FuSa byte.

"01": FuSa mode type1
FuSa byte = Write data. (No error if 2 transferring data bytes are the same value.)
When error is detected
=> Do not execute writing and assert MD1 Interruption Factor bit of I2C / Thermal Error Status register.
(Assert the INTB pin output if I2C_IMASK mask is released by I2C / Thermal Error Mask register.)

"10": FuSa mode type2
FuSa byte = ECC data. (Refer to section 4.5 I2C I/F for details regarding ECC mathematical operation specification)
As a result of ECC mathematical operation,
At 1 bit Error (Rectify error of relevant bit)
=> Execute rectification writing and assert MD2_E1 Interruption Factor bit of I2C / Thermal Error Status register.
(Assert the INTB pin output if I2C_IMASK mask is released by I2C / Thermal Error Mask register, and also indicate location of relevant bit on I2C MD2_E1 Bit1 register and I2C MD2_E1 Bit2 register (for P[4:0])).
At 2 bit Error (Error Detection)
=> Do not execute writing and assert MD2_E2 Interruption Factor bit of I2C / Thermal Error Status register.
(Assert the INTB pin output if I2C_IMASK mask is released by I2C / Thermal Error Mask register.)

"11": Reserved

SMOD_read FuSa Mode Read Setting

0: FuSa Mode is applied only for I2C write data.
1: FuSa Mode is applied not only I2C write data, but also I2C read data.

5.2 Register Description – continued

5.2.3 Spread Spectrum Clock Generation Control for Internal OSC

BD9573MUF-M has built-in SSCG (Spread Spectrum Clock Generator) with center spread.

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
SSCG Cnt	0x13	-	SSCG_ PERI	SSCG_ FORM[1:0]		-	-	-	SSCG_ EN	R/W	0x00

SSCG_EN Enable signal of SSCG
0: SSCG Disable
1: SSCG Enable

SSCG_FORM[1:0] Selection of SSCG modulation waveform
"00": Normal Triangle
"01": Original waveform1 (A:B:C = 4:1:4)
"10": Original waveform2 (A:B:C = 3:3:3)
"11": Original waveform3 (A:B:C = 2:5:2)

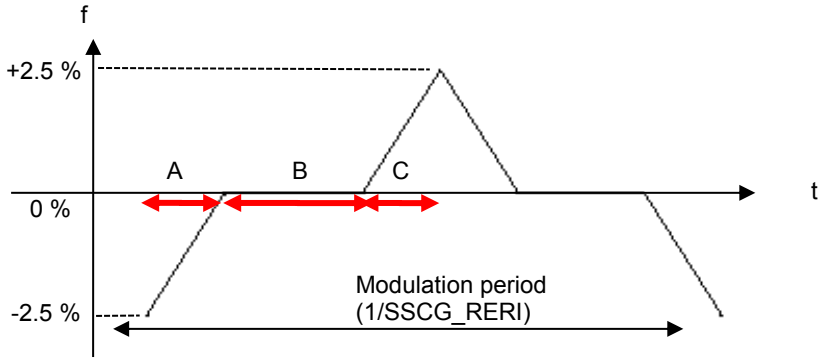


Figure 38. Modulation Waveform of SSCG

SSCG_PERI
0: 122 Hz
1: 7.813 kHz

5.2 Register Description – continued

5.2.4 SMRB control Using I2C Control (Software Manual Reset for PRESETB)

The PRESETB pin output can be controlled by these registers.

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
SMRB Write Protect	0x14	SMRB_WP[7:0]								R/W	0x00

SMRB_WP[7:0] Protection register for SMRB_asrt (Software Manual Reset for PRESETB)
0x9D: SMRB assert is enabled.
Others: SMRB assert is disabled.

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
SMRB Cnt	0x15	-	-	-	SMRB_ hist	-	-	-	SMRB_ asrt	R/W	0x01

SMRB_asrt SMRB assert register
When this register is set to “0”, PRESETB is asserted to L. After 5ms, this register value is reset to “1” and PRESETB is negated to H automatically.

SMRB_hist SMRB status register
If SMRB assert is occurred, this register is set to “1”. Register value does not be initialized during STANDBY state transition. Clear condition is I2C writing “1” or UVLO.

5.2.5 Watch Dog Timer Setting

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
Watch Dog Timer setting	0x16	-	-	TYPE	NG_RATIO[1:0]		FAST_NG[2:0]			R/W	0x20

FAST_NG[2:0], NG_RATIO[1:0] WDT N.G. detection area setting
Regarding these registers’ function, please refer to section 4.9 WDT Function.

TYPE WDT detecting type setting
0: timeout detection (SLOW N.G.)
1: window detection (FAST/SLOW N.G.)

(Note) I2C write to Watch Dog Timer setting register when the WDEN pin H level is prohibited.

5.2.6 Oscillator Enable in STANDBY State

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
OSC Enable	0x17	-	-	-	-	-	-	-	OSC_ EN	R/W	0x00

OSC_EN Oscillator Enable/Disable Selection in STANDBY state
0: Oscillator Disable in STANDBY state
1: Oscillator Enable in STANDBY state

(Note) For I2C write condition in STANDBY state, 110 µs (Max) wait time after OSC_EN register = “1” is needed.

5.2 Register Description – continued

5.2.7 The PGD pin output assert condition Setting

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
PGD Setting	0x18	-	-	PGD_SETTING[5:0]						R/W	0x3F

PGD_SETTING[5:0] The PGD pin output assert condition
PGD_SETTING[0] = 0: VOUT1 PGD is not the factor of the PGD pin output,
1: VOUT1 PGD is the factor of the PGD pin output.
PGD_SETTING[1] = 0: VOUT2 PGD is not the factor of the PGD pin output,
1: VOUT2 PGD is the factor of the PGD pin output.
PGD_SETTING[2] = 0: VOUT3 PGD is not the factor of the PGD pin output,
1: VOUT3 PGD is the factor of the PGD pin output.
PGD_SETTING[3] = 0: VOUT4 PGD is not the factor of the PGD pin output,
1: VOUT4 PGD is the factor of the PGD pin output.
PGD_SETTING[4] = 0: VOUTL1 PGD is not the factor of the PGD pin output,
1: VOUTL1 PGD is the factor of the PGD pin output.
PGD_SETTING[5] = 0: VOUTS1 PGD is not the factor of the PGD pin output,
1: VOUTS1 PGD is the factor of the PGD pin output.

For example, the PGD pin output is asserted by VOUT1, VOUT2, VOUT3 and VOUT4 PGD when PGD_SETTING[5:0] = 0x0F.
In this case, the PGD pin output is negated at any one of VOUT1, VOUT2, VOUT3 or VOUT4 discharge start timing.

5.2.8 PMIC Internal Status

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
PMIC Internal Status	0x20	-	-	-	NO_EEP	PMIC_STATE[3:0]				RO	0x00

PMIC_STATE[3:0] PMIC Internal State
PMIC Internal State is shown in the following table.

Table 22: PMIC Internal State

PMIC_STATE[3:0] Setting Value	PMIC Internal State
0x0	SHUTDOWN
0x1	STANDBY
0x2	OSC Stable
0x3	Delay
0x4	Power-ON STANDBY
0x5	Power-ON
0x6	ACTIVE
0x7	Power-OFF
0x8	Power-OFF STANDBY
0x9 to 0xF	State transition

NO_EEP Judgement for EEPROM installation
0: With ACK from EEPROM (EEPROM is installed)
1: Without ACK from EEPROM (EEPROM is not installed)

5.2 Register Description – continued

5.2.9 I2C FuSa mode Error bit location

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
I2C MD2_E1 Bit 1	0x21	I2C_MD2_E1_BIT[7:0]								RO	0x00

I2C_MD2_E1_BIT[7:0] Error bit location at FuSa mode type2

Set “1” to the bit location where error is detected and rectified in FuSa mode type2.

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
I2C MD2_E1 Bit 2	0x22	-	-	-	I2C_MD2_E1_BIT_P[4:0]					RO	0x00

I2C_MD2_E1_BIT_P[4:0] Error bit location (P code) at FuSa mode type2

Set “1” to the bit (P code value) location where error is detected and rectified in FuSa mode type2.

5.2 Register Description – continued

5.2.10 INTB Interruption Factor and Mask Condition

(Note) Clear condition of Status registers is I2C writing "1" or UVLO.

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
I2C / Thermal Error Status	0x23	-	-	-	TSD	-	MD2_E2	MD2_E1	MD1	R/W	0x00

MD1 I2C Write Error Status in FuSa Mode Type1
0: No Interruption Factor
1: with Interruption Factor

MD2_E1 I2C Write Error Status in FuSa Mode Type2 with 1 bit error
0: No Interruption Factor
1: with Interruption Factor

MD2_E2 I2C Write Error Status in FuSa Mode Type2 with more than 2 bit error
0: No Interruption Factor
1: with Interruption Factor

TSD Thermal Shutdown Detection
0: No Interruption Factor
1: with Interruption Factor

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
I2C / Thermal Error Mask	0x24	-	-	-	-	-	-	-	I2C_IMASK	R/W	0x00

I2C_IMASK FuSa Mode Error (MD1, MD2_E1, MD2_E2) Interruption Factor Mask
0: Mask Disable
1: Mask Enable

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
OVP Error Status	0x25	-	-	VOUTL1_OVP	-	VOUT4_OVP	VOUT3_OVP	VOUT2_OVP	VOUT1_OVP	R/W	0x00

VOUTx_OVP (x = 1 to 4 and L1) Over Voltage Protection Detection
0: No Interruption Factor
1: with Interruption Factor

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
SCP Error Status	0x26	-	-	VOUTL1_SCP	-	VOUT4_SCP	VOUT3_SCP	VOUT2_SCP	VOUT1_SCP	R/W	0x00

VOUTx_SCP (x = 1 to 4 and L1) Short Circuit Protection Detection
0: No Interruption Factor
1: with Interruption Factor

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
OCP Error Status	0x27	LDSW_OCP	VOUTS1_OCP	-	VOUT4B_OCP	VOUT4A_OCP	VOUT3_OCP	VOUT2_OCP	VOUT1_OCP	R/W	0x00

VOUTx_OCP (x = 1 to 3, 4A, 4B and S1), LDSW_OCP Over Current Protection Detection
0: No Interruption Factor
1: with Interruption Factor

5.2.10 INTB Interruption Factor and Mask Condition - continued

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
UVP Error Status	0x2A	-	VIN7_UVP	VIN6_UVP	VIN5_UVP	VIN4_UVP	VIN3_UVP	VIN2_UVP	VIN1_UVP	R/W	0x00

VINx_UVP (x = 1 to 7) Under Voltage Protection
0: No Interruption Factor
1: with Interruption Factor

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
System Status	0x2B	V1_HUT_ERR	HUT_ERR	EEP_END	EEP_CRC_ERR	-	-	WDT_ERR	-	R/W	0x00

WDT_ERR Watch Dog Timer Error
0: No Interruption Factor
1: with Interruption Factor

EEP_CRC_ERR CRC Error during EEPROM Load
0: No Interruption Factor
1: with Interruption Factor

EEP_END Notification of EEPROM Load Internal State completion
0: Before EEPROM Load Completion
1: EEPROM Load is completed

HUT_ERR Power-OFF Sequence Hang-Up Timer counts over 400 ms
0: No Interruption Factor
1: with Interruption Factor

V1_HUT_ERR V1 Power-OFF Hang-Up Timer counts over 100 ms
0: No Interruption Factor
1: with Interruption Factor

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
System Status Mask	0x2C	V1_HUT_E_IMASK	HUT_E_IMASK	EEP_END_IMASK	EEPCRC_E_IMASK	-	-	WDT_E_IMASK	-	R/W	0x20

WDT_E_IMASK Watch Dog Timer Error Interruption Factor Mask
0: Mask Disable
1: Mask Enable

EEPCRC_E_IMASK CRC Error during EEPROM Load Interruption Factor Mask
0: Mask Disable
1: Mask Enable

EEP_END_IMASK Notification of EEPROM Load Internal State completion Interruption Factor Mask
0: Mask Disable
1: Mask Enable

HUT_E_IMASK Hang-Up Timer Interruption Factor Mask
0: Mask Disable
1: Mask Enable

V1_HUT_E_IMASK V1 Hang-Up Timer Interruption Factor Mask
0: Mask Disable
1: Mask Enable

5.2.10 INTB Interruption Factor and Mask Condition - continued

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
INT IntReq	0x30	SYS_INT	UVP_INT	-	-	OCP_INT	SCP_INT	OVP_INT	I2CTHM_INT	R/W	0x00

I2CTHM_INT Primary Level Interruption Factor of I2C / Thermal Error Status Register
0: No Interruption Factor
1: with Interruption Factor

OVP_INT Primary Level Interruption Factor of OVP Error Status Register
0: No Interruption Factor
1: with Interruption Factor

SCP_INT Primary Level Interruption Factor of SCP Error Status Register
0: No Interruption Factor
1: with Interruption Factor

OCP_INT Primary Level Interruption Factor of OCP Error Status Register
0: No Interruption Factor
1: with Interruption Factor

UVP_INT Primary Level Interruption Factor of UVP Error Status Register
0: No Interruption Factor
1: with Interruption Factor

SYS_INT Primary Level Interruption Factor of System Status Register
0: No Interruption Factor
1: with Interruption Factor

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
INT IntMask	0x31	SYS_IMASK	UVP_IMASK	-	-	OCP_IMASK	SCP_IMASK	OVP_IMASK	I2CTHM_IMASK	R/W	0x00

I2CTHM_IMASK Primary Level Interruption Factor of I2C / Thermal Error Status Register Mask
0: Mask Disable
1: Mask Enable

OVP_IMASK Primary Level Interruption Factor of OVP Error Status Register Mask
0: Mask Disable
1: Mask Enable

SCP_IMASK Primary Level Interruption Factor of SCP Error Status Register Mask
0: Mask Disable
1: Mask Enable

OCP_IMASK Primary Level Interruption Factor of OCP Error Status Register Mask
0: Mask Disable
1: Mask Enable

UVP_IMASK Primary Level Interruption Factor of UVP Error Status Register Mask
0: Mask Disable
1: Mask Enable

SYS_IMASK Primary Level Interruption Factor of System Status Register Mask
0: Mask Disable
1: Mask Enable

5.2 Register Description – continued

5.2.11 POW Setting

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW WriteProtect	0x40	POW_WP[7:0]								R/W	0x00

POW_WP[7:0] Protection register for POW Trigger and POW Wait
0xAB: Access for POW registers is enabled.
Others: Access for POW registers is disabled.

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Trigger VOUT1	0x41	POFF_TRG_VOUT1				PON_TRG_VOUT1				R/W	0x20

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Trigger VOUT2	0x42	POFF_TRG_VOUT2				PON_TRG_VOUT2				R/W	0x61

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Trigger VOUT3	0x43	POFF_TRG_VOUT3				PON_TRG_VOUT3				R/W	0x45

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Trigger VOUT4	0x44	POFF_TRG_VOUT4				PON_TRG_VOUT4				R/W	0x73

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Trigger VOUTL1	0x45	POFF_TRG_VOUTL1				PON_TRG_VOUTL1				R/W	0x36

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Trigger VOUTS1	0x46	POFF_TRG_VOUTS1				PON_TRG_VOUTS1				R/W	0x52

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Trigger PRESETB	0x47	POFF_TRG_PRESETB				PON_TRG_PRESETB				R/W	0x04

PON_TRG_VOUTx*(Note 1)* Trigger Signal Setting in Power-ON Sequence

POFF_TRG_VOUTx*(Note 1)* Trigger Signal Setting in Power-OFF Sequence

The Order of Power-ON Sequence and Power-OFF Sequence is selected by POW Trigger VOUTx*(Note 1)* registers. POW Trigger VOUTx*(Note 1)* registers' value can be changed by EEPROM. Regarding default value of each registers, please refer register map.

(e.g.)
By setting PON_TRG_VOUT2 = 0x1 (VOUT1 Enable Signal), VOUT2 starts Power-ON after VOUT1.
By setting POFF_TRG_VOUTL1 = 0x03 (VOUT3 Enable Signal), VOUTL1 starts Power-OFF after VOUT3.
By setting PON_TRG_VOUTL1 = 0xFF (Always OFF Setting), VOUTL1 never Power-ON. In this case, VOUTL1 is excluded from the Power-ON / Power-OFF sequence automatically.
Setting over 2 signals triggering one Enable Signal is prohibited.

(Note 1) VOUTx = VOUT1 to VOUT4, VOUTL1 and VOUTS1

5.2.11 POW Setting – continued

Table 23: PON/POFF Trigger Signal

PON_TRG_VOUTx(Note 1) / POFF_TRG_VOUTx(Note 1) PON_TRG_PRESETB / POFF_TRG_PRESETB	Trigger Signal
0x0	RSTB (pin) = H level (Power-ON) / L level (Power-OFF)
0x1	VOUT1 Enable Signal
0x2	VOUT2 Enable Signal
0x3	VOUT3 Enable Signal
0x4	VOUT4 Enable Signal
0x5	VOUTL1 Enable Signal
0x6	VOUTS1 Enable Signal
0x7	PRESETB (pin)
0x8 to 0xF	Always OFF Setting

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Wait VOUT1	0x48	POFF_WAIT_VOUT1				PON_WAIT_VOUT1				R/W	0x00

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Wait VOUT2	0x49	POFF_WAIT_VOUT2				PON_WAIT_VOUT2				R/W	0x00

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Wait VOUT3	0x4A	POFF_WAIT_VOUT3				PON_WAIT_VOUT3				R/W	0x00

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Wait VOUT4	0x4B	POFF_WAIT_VOUT4				PON_WAIT_VOUT4				R/W	0x00

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Wait VOUTL1	0x4C	POFF_WAIT_VOUTL1				PON_WAIT_VOUTL1				R/W	0x00

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Wait VOUTS1	0x4D	POFF_WAIT_VOUTS1				PON_WAIT_VOUTS1				R/W	0x00

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
POW Wait PRESETB	0x4E	POFF_WAIT_PRESETB				PON_WAIT_PRESETB				R/W	0x00

PON_WAIT_VOUTx(Note 1) Interval Setting in Power-ON Sequence

POFF_WAIT_VOUTx(Note 1) Interval Setting in Power-OFF Sequence

The Interval of Power-ON Sequence and Power-OFF Sequence is selected by POW Wait VOUTx(Note 1) registers. POW Wait VOUTx(Note 1) registers' value can be changed by EEPROM. Regarding default value of each registers, please refer register map.

(Note 1) VOUTx = VOUT1 to VOUT4, VOUTL1 and VOUTS1

5.2.11 POW Setting – continued

Table 24: PON/POFF Interval

PON_WAIT_VOUTx*(Note 1)* / POFF_WAIT_VOUTx*(Note 1)* PON_WAIT_PRESETB / POFF_WAIT_PRESETB	Interval
0x0	2 µs
0x1	500 µs
0x2	1 ms
0x3	2 ms
0x4	4 ms
0x5	5 ms
0x6	8 ms
0x7	10 ms
0x8	15 ms
0x9	20 ms
0xA	25 ms
0xB	30 ms
0xC	40 ms
0xD	45 ms
0xE	50 ms
0xF	60 ms

Please set Power-OFF interval not to exceed totally 400 ms (Power-OFF Sequence Hang Up Timer).

(Note 1) VOUTx = VOUT1 to VOUT4, VOUTL1 and VOUTS1

5.2 Register Description – continued

5.2.12 VOUT Voltage SET

These VOUT voltage tuning registers are set via external EEPROM.

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
VOUT1 TUNE	0x50	V1_ SIGN	-	-	-	-	VOUT1_TUNE[2:0]			RO	0x00

V1_SIGN VOUT1 Sign Bit
0: Plus
1: Minus

VOUT1_TUNE[2:0] VOUT1 Tuning Bit
VOUT1 output voltage is tuned from default value (5.0 V) by these registers. Step: 100 mV.

Table 25: VOUT1 Tuning Voltage

VOUT1_TUNE[2:0]	Tuning Voltage (mV)
0x0	0
0x1	100
0x2	200
0x3	300
0x4	400
0x5	500
0x6	Clipped to 500
0x7	Clipped to 500

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
VOUT2 TUNE	0x53	V2_ SIGN	-	-	-	-	VOUT2_TUNE[2:0]			RO	0x00

V2_SIGN VOUT2 Sign Bit
0: Plus
1: Minus

VOUT2_TUNE[2:0] VOUT2 Tuning Bit
VOUT2 output voltage is tuned from default value (1.8 V) by these registers. Step: 20 mV.

Table 26: VOUT2 Tuning Voltage

VOUT2_TUNE[2:0]	Tuning Voltage (mV)
0x0	0
0x1	20
0x2	40
0x3	60
0x4	80
0x5	100
0x6	120
0x7	140

5.2.12 VOUT Voltage SET – continued

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
VOUT3 TUNE	0x56	V3_ SIGN	-	-	VOUT3_TUNE[4:0]					RO	0x00

V3_SIGN VOUT3 Sign Bit
0: Plus
1: Minus

VOUT3_TUNE[4:0] VOUT3 Tuning Bit
VOUT3 output voltage is tuned from default value (1.35 V, 1.5 V) by these registers. Step: 10 mV.

Table 27: VOUT3 Tuning Voltage

VOUT3_TUNE[4:0]	Tuning Voltage (mV)
0x0	0
0x1	10
0x2	20
……	……
……	……
0x1D	290
0x1E	300
0x1F	310

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
VOUT4 TUNE	0x59	V4_ SIGN	-	-	VOUT4_TUNE[4:0]					RO	0x00

V4_SIGN VOUT4 Sign Bit
0: Plus
1: Minus

VOUT4_TUNE[4:0] VOUT4 Tuning Bit
VOUT4 output voltage is tuned from default value (1.03 V) by these registers. Step: 10 mV.

Table 28: VOUT4 Tuning Voltage

VOUT4_TUNE[4:0]	Tuning Voltage (mV)
0x0	0
0x1	10
0x2	20
……	……
……	……
0x1D	290
0x1E	300
0x1F	310

5.2.12 VOUT Voltage SET – continued

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
VOUTL1 TUNE	0x5C	VL1_ SIGN	-	-	-	-	VOUTL1_TUNE[2:0]			RO	0x00

VL1_SIGN VOUTL1 Sign Bit
0: Plus
1: Minus

VOUTL1_TUNE[2:0] VOUTL1 Tuning Bit
VOUTL1 output voltage is tuned from default value (2.5 V) by these registers. Step: 40 mV.

Table 29: VOUTL1 Tuning Voltage

VOUTL1_TUNE[2:0]	Tuning Voltage (mV)
0x0	0
0x1	40
0x2	80
0x3	120
0x4	160
0x5	200
0x6	240
0x7	280

5.2.13 VOUTS1 OCP SET

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0	R/W	Default
VOUTS1 OCP	0x60	-	-	VOUTS1_OCP[5:0]						R/W	0x16/ 0x08

VOUTS1_OCP[5:0] VOUTS1 OCP setting. Step: 50 mA (Internal Mode), 10 mV (External Mode)
Default value is determined by GATECNT (pin) condition.
GATECNT (pin) = L: Default value is 0x16 (Internal: 1100 mA).
GATECNT (pin) = H: Default value is 0x08 (External: 90 mV).

Table 30: VOUTS1 OCP Current (Internal) and Voltage (External)

VOUTS1_OCP_SET[5:0]	Internal OCP Current (mA)	External OCP Voltage (mV)
0x00	Function Disable	Function Disable
0x00 to 0x05	Clipped to 300	Clipped to 70
0x06	300	70
0x07	350	80
0x08	400	90
……	……	……
0x16	1100	230
……	……	……
0x1B	1350	280
0x1C to 0x3F	Clipped 1350	Clipped to 280

Internal OCP Current has ±50 % of deviation.
This is because it depends on Ron of internal SW.

6. Typical Performance Curves

Unless otherwise specified: VIN = 3.3 V, Ta = 25 °C, IOUT = 0 A

6.1 Line Regulation

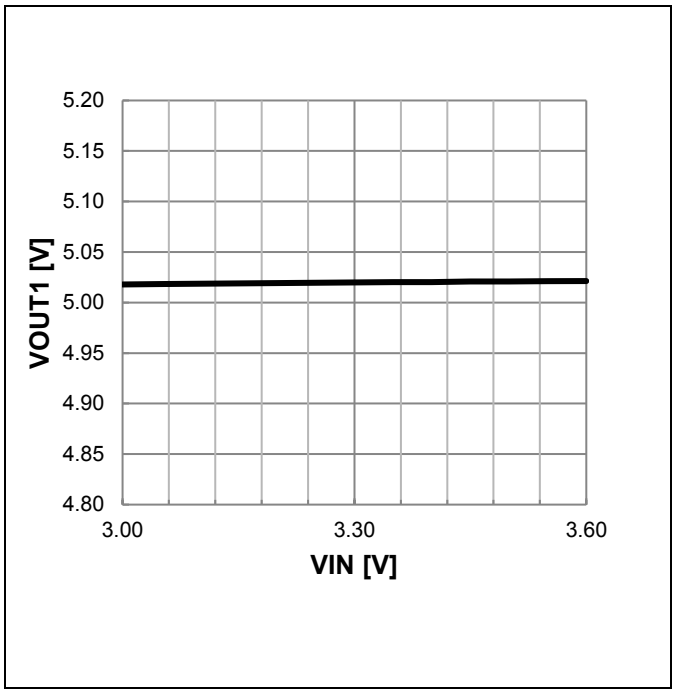


Figure 39. VOUT1 Output Voltage vs VIN

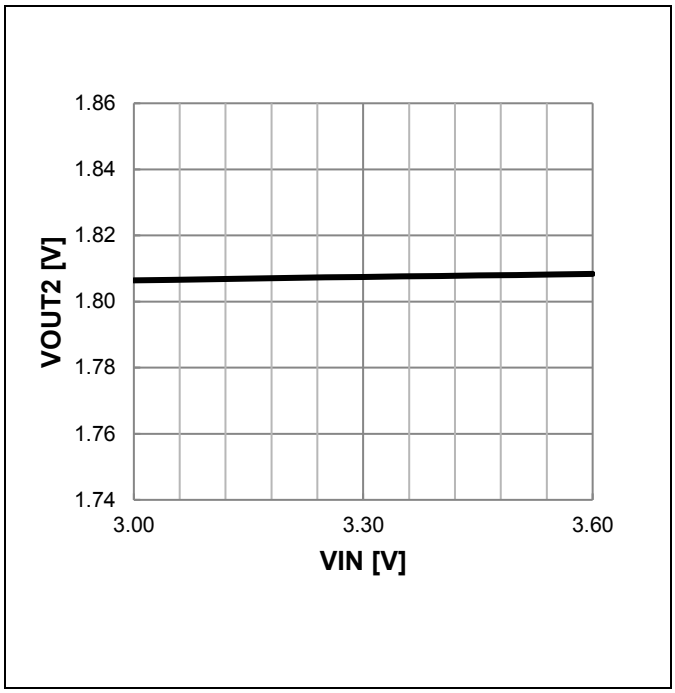


Figure 40. VOUT2 Output Voltage vs VIN

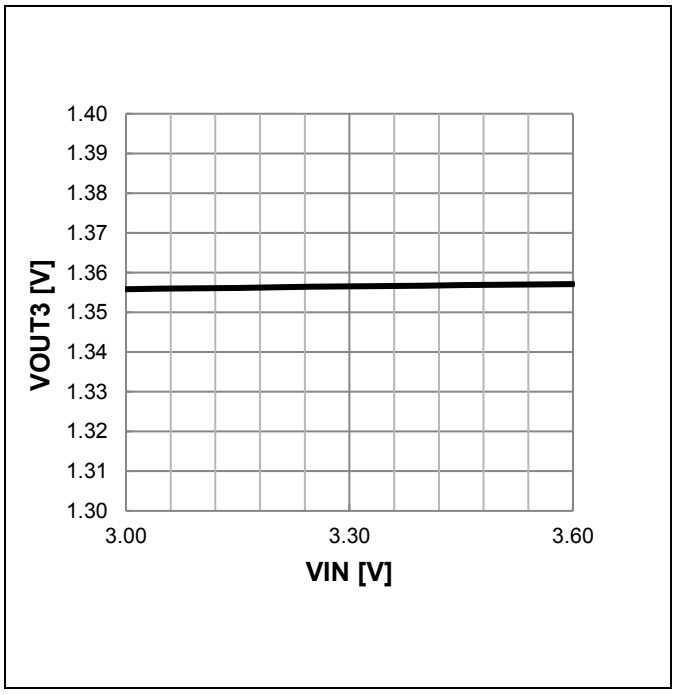


Figure 41. VOUT3 Output Voltage vs VIN
(VOUT3 = 1.35 V Setting)

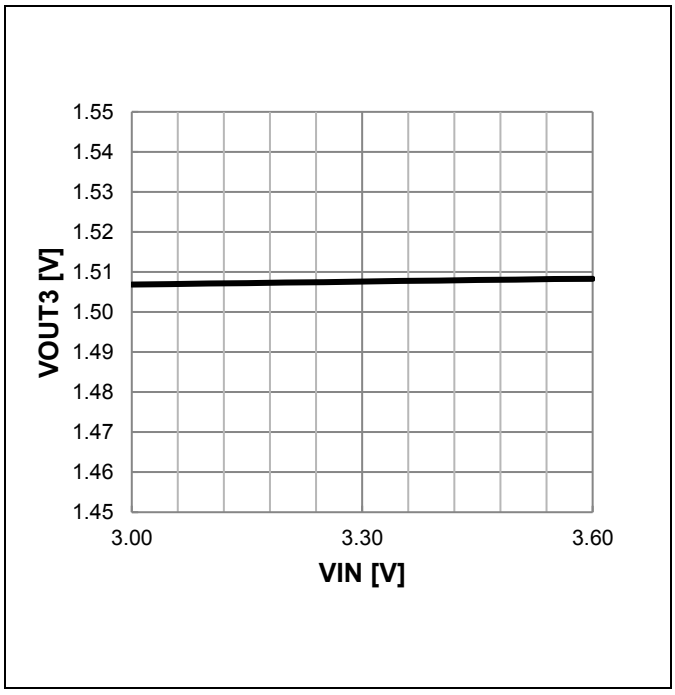


Figure 42. VOUT3 Output Voltage vs VIN
(VOUT3 = 1.5 V Setting)

6.1 Line Regulation - continued

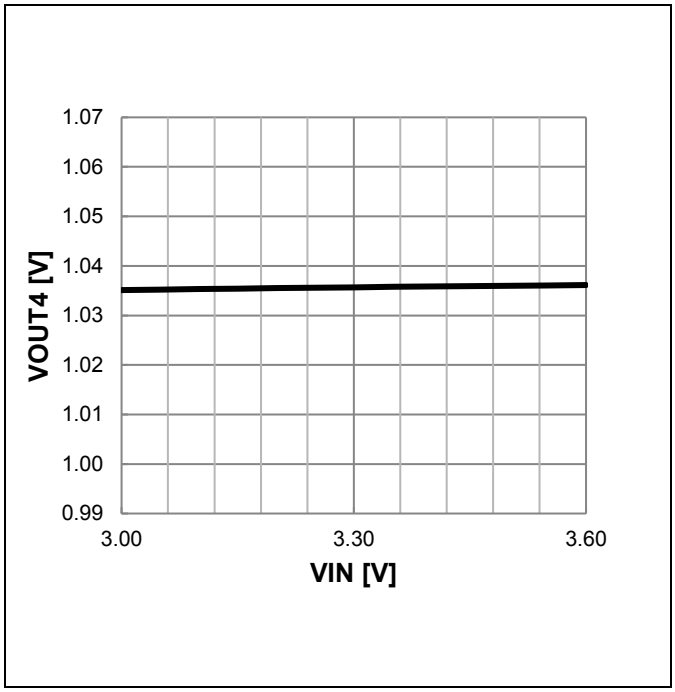


Figure 43. VOUT4 Output Voltage vs VIN

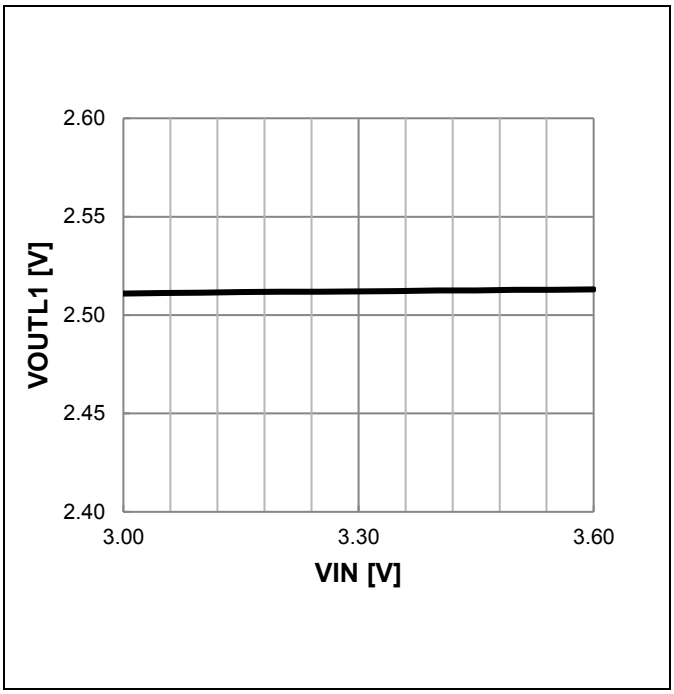


Figure 44. VOUTL1 Output Voltage vs VIN

6. Typical Performance Curves – continued

6.2 Load Regulation

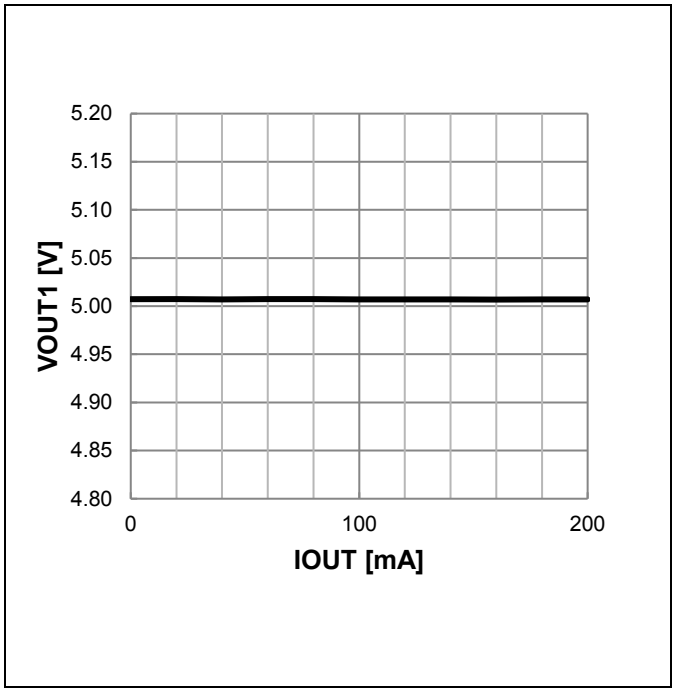


Figure 45. VOUT1 Output Voltage vs IOUT

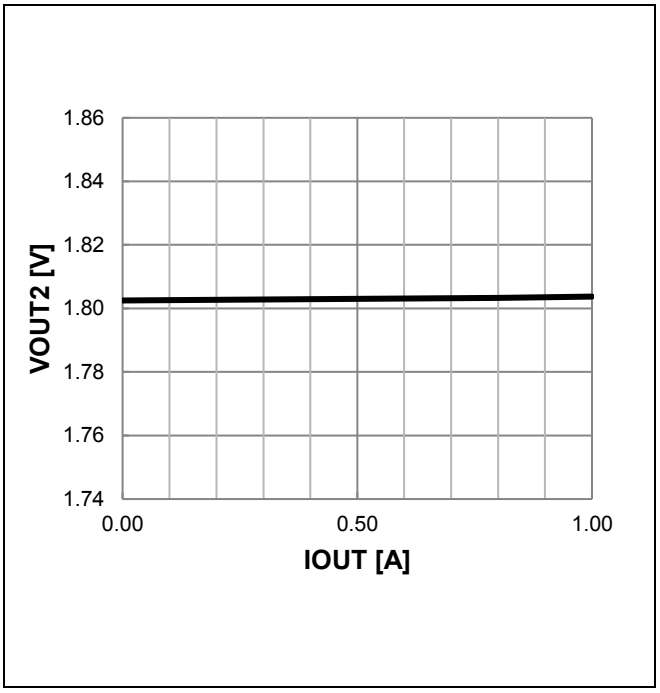


Figure 46. VOUT2 Output Voltage vs IOUT

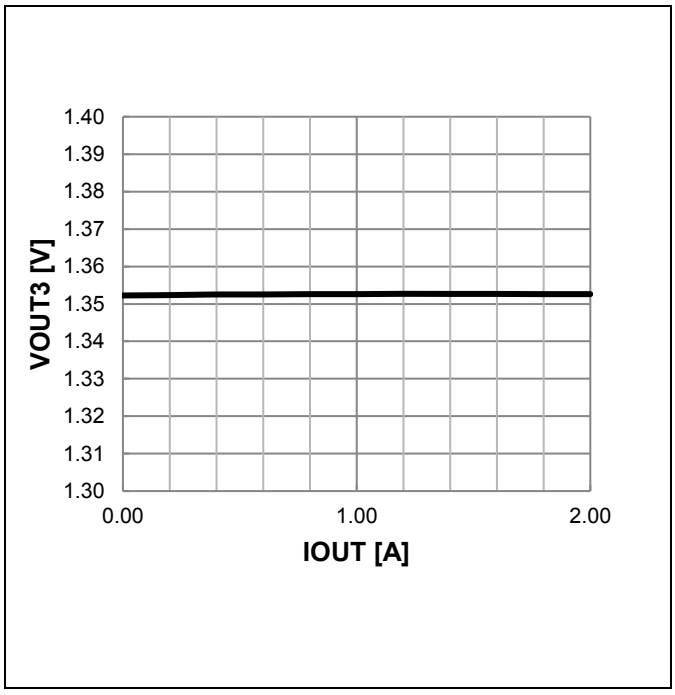


Figure 47. VOUT3 Output Voltage vs IOUT
(VOUT3 = 1.35 V Setting)

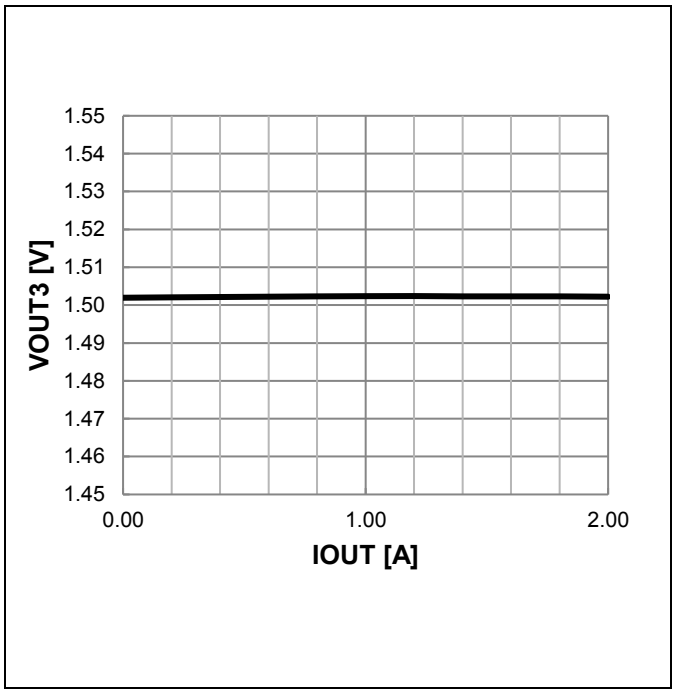


Figure 48. VOUT3 Output Voltage vs IOUT
(VOUT3 = 1.5 V Setting)

6.2 Load Regulation - continued

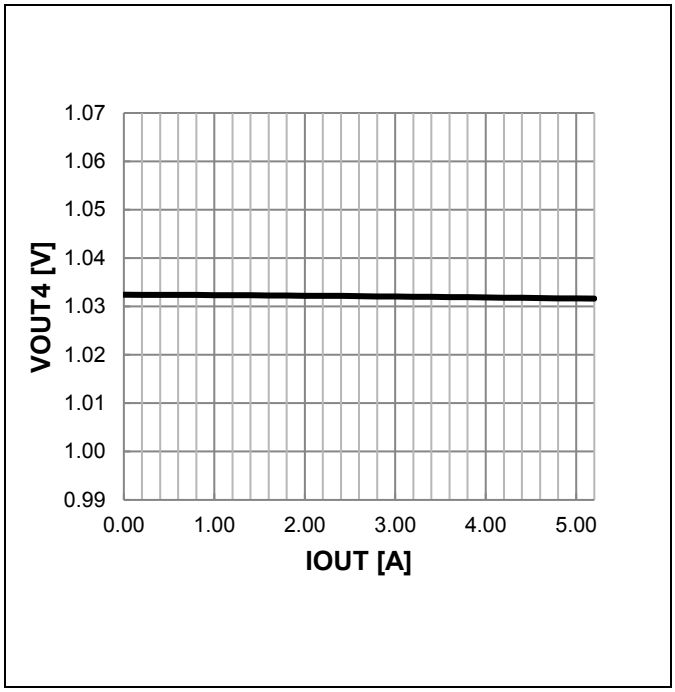


Figure 49. VOUT4 Output Voltage vs IOUT

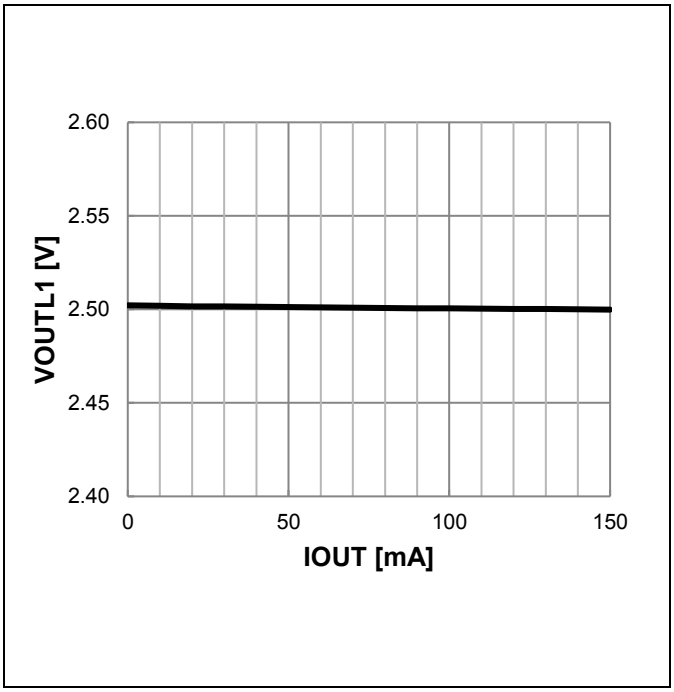


Figure 50. VOUTL1 Output Voltage vs IOUT

6. Typical Performance Curves – continued

6.3 Power Efficiency

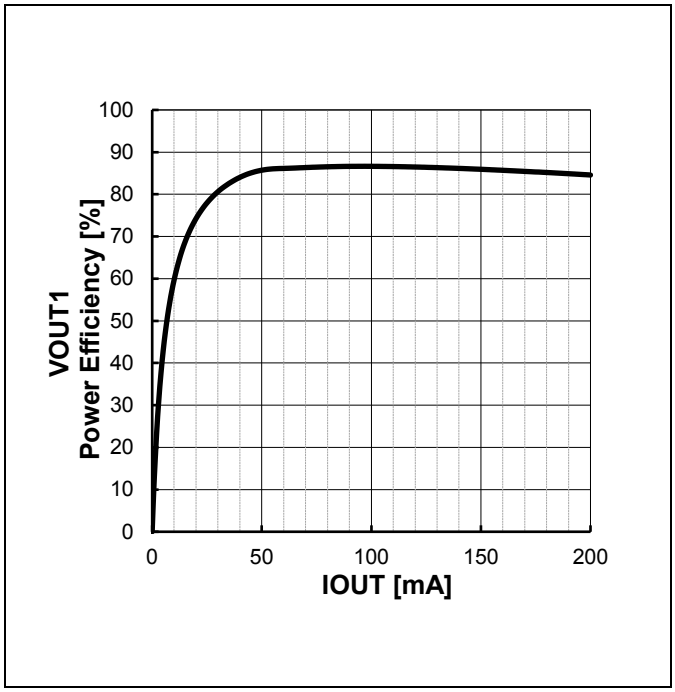


Figure 51. VOUT1 Power Efficiency vs IOUT

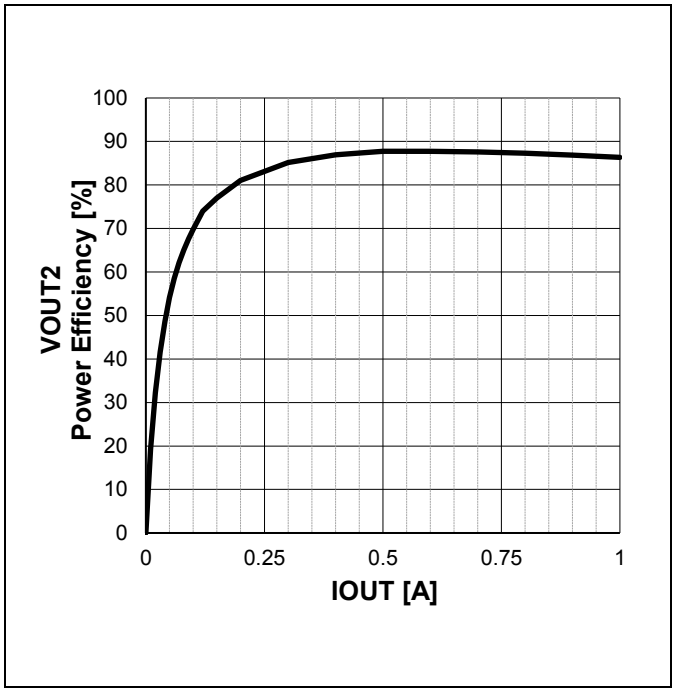


Figure 52. VOUT2 Power Efficiency vs IOUT

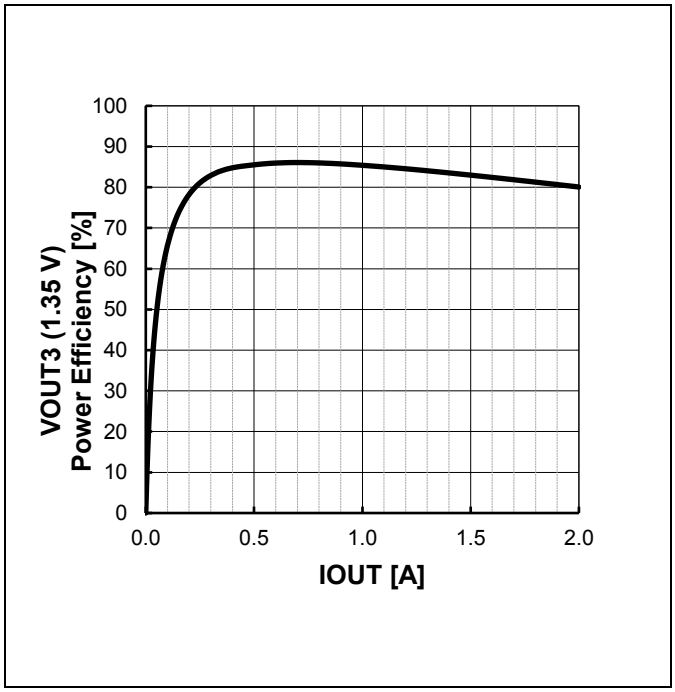


Figure 53. VOUT3 Power Efficiency vs IOUT
(VOUT3 = 1.35 V Setting)

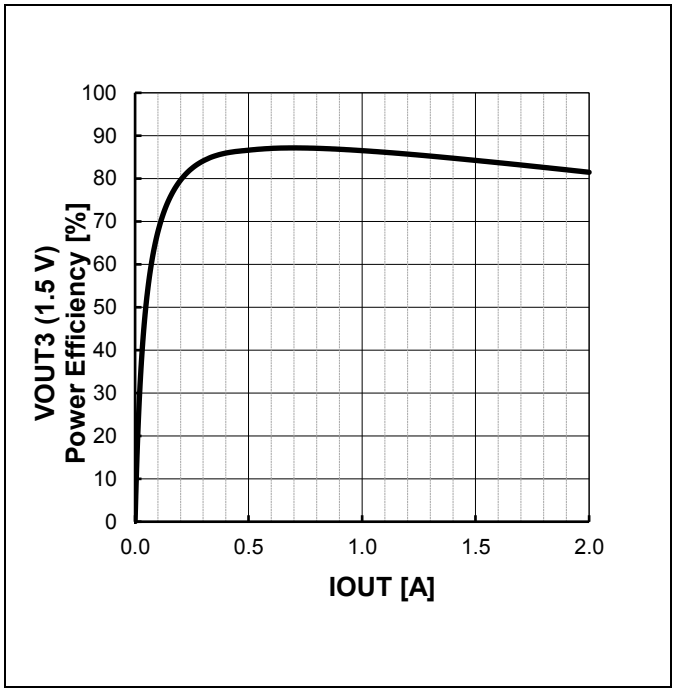


Figure 54. VOUT3 Power Efficiency vs IOUT
(VOUT3 = 1.5 V Setting)

6.3 Power Efficiency -continued

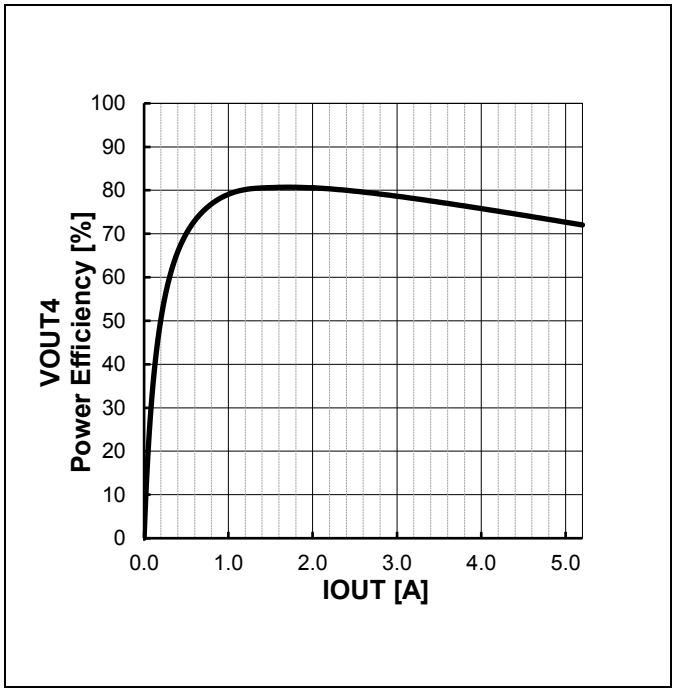


Figure 55. VOUT4 Power Efficiency vs IOUT

6. Typical Performance Curves – continued

6.4 Power ON Waveform

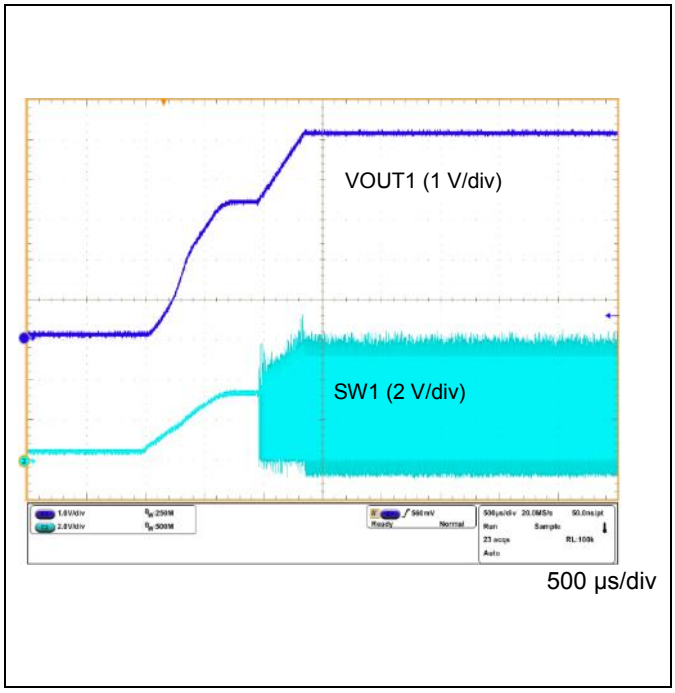


Figure 56. VOUT1 Power ON Waveform

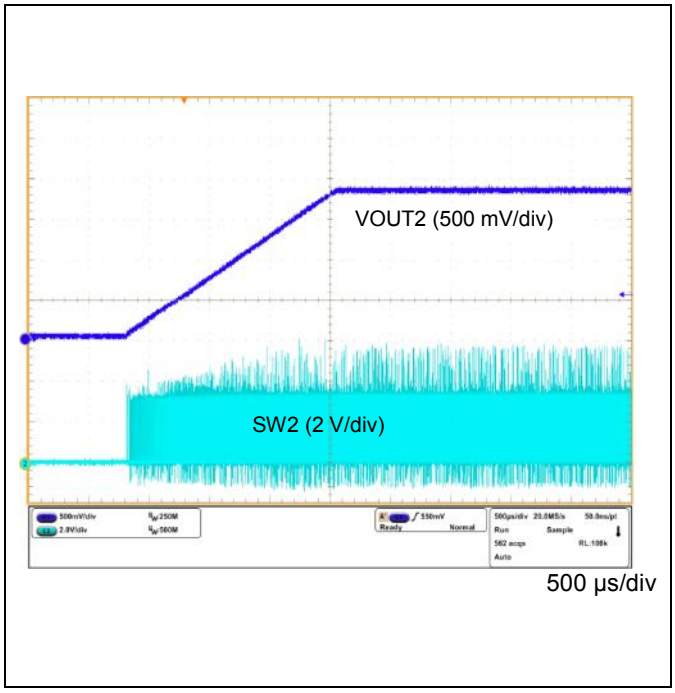


Figure 57. VOUT2 Power ON Waveform

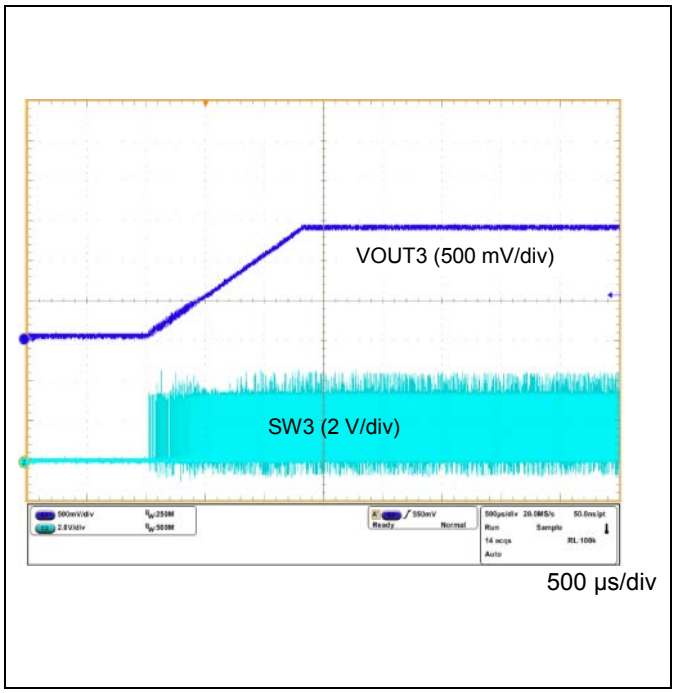


Figure 58. VOUT3 Power ON Waveform
(VOUT3 = 1.35 V Setting)

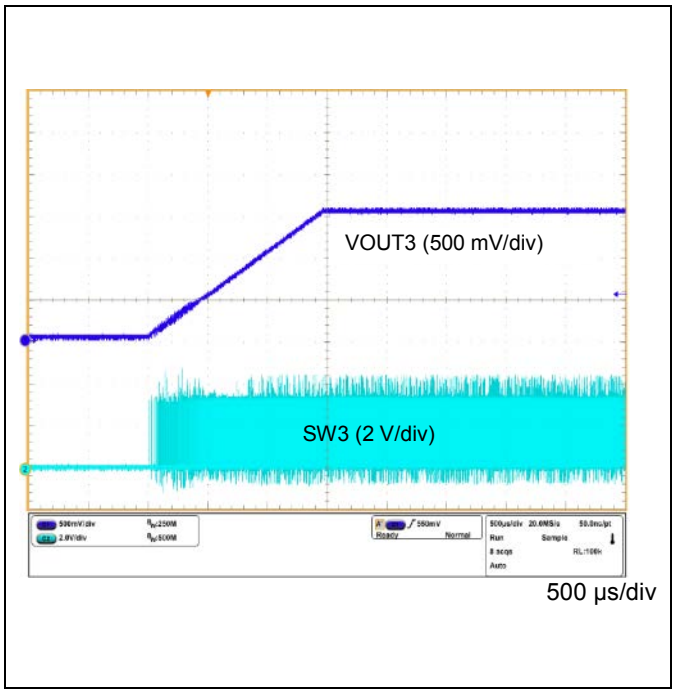


Figure 59. VOUT3 Power ON Waveform
(VOUT3 = 1.5 V Setting)

6.4 Power ON Waveform- continued

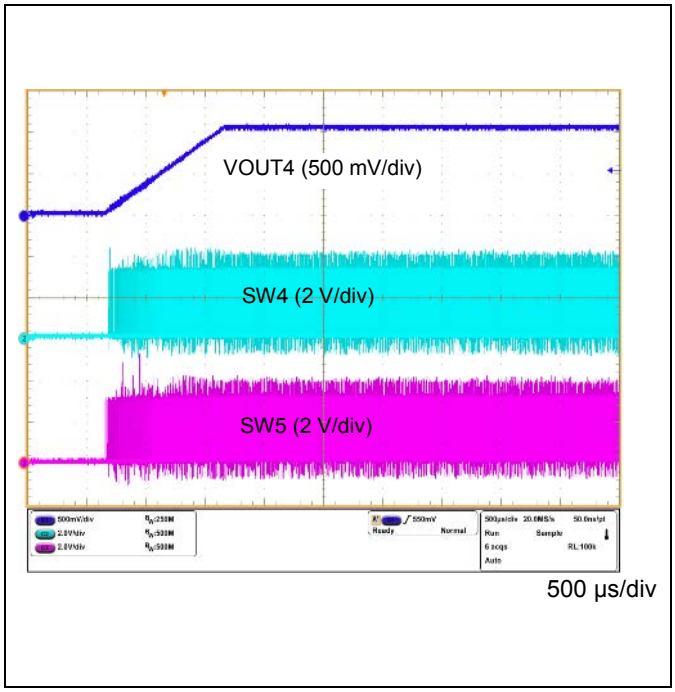


Figure 60. VOUT4 Power ON Waveform

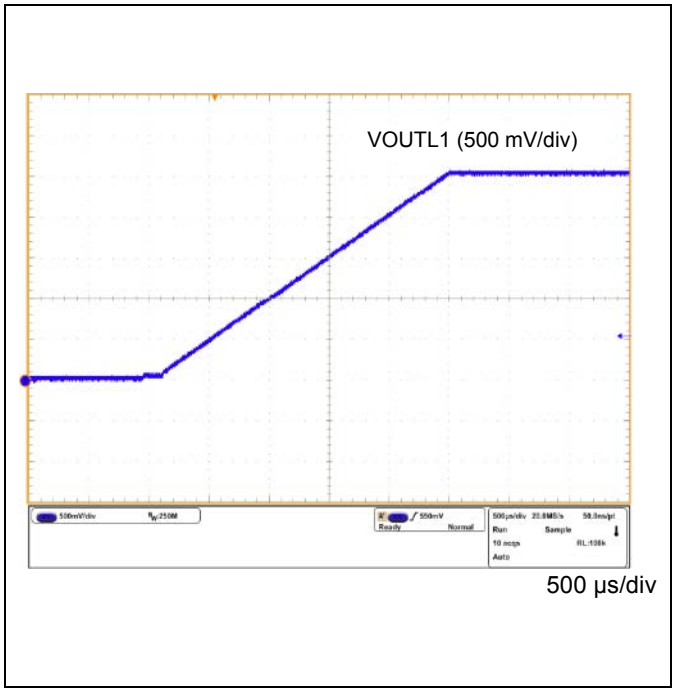


Figure 61. VOUTL1 Power ON Waveform

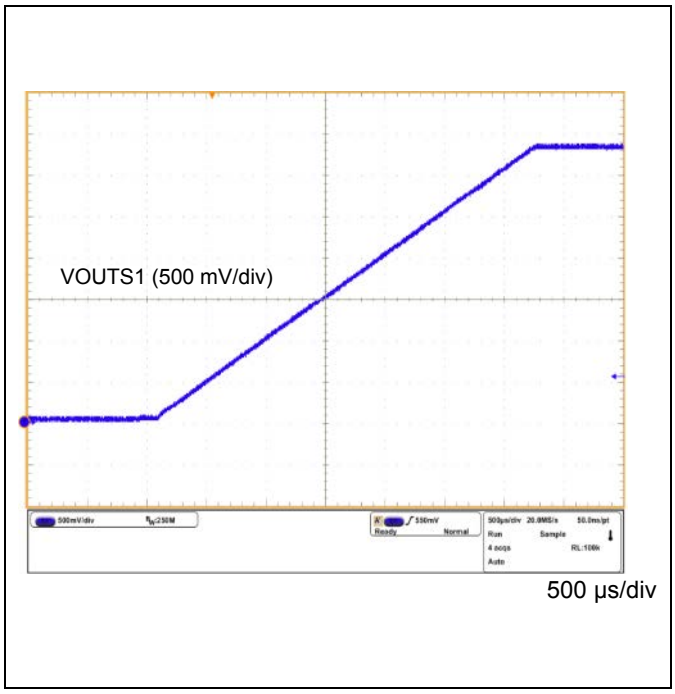


Figure 62. VOUTS1 Power ON Waveform

6. Typical Performance Curves – continued

6.5 Power OFF Waveform

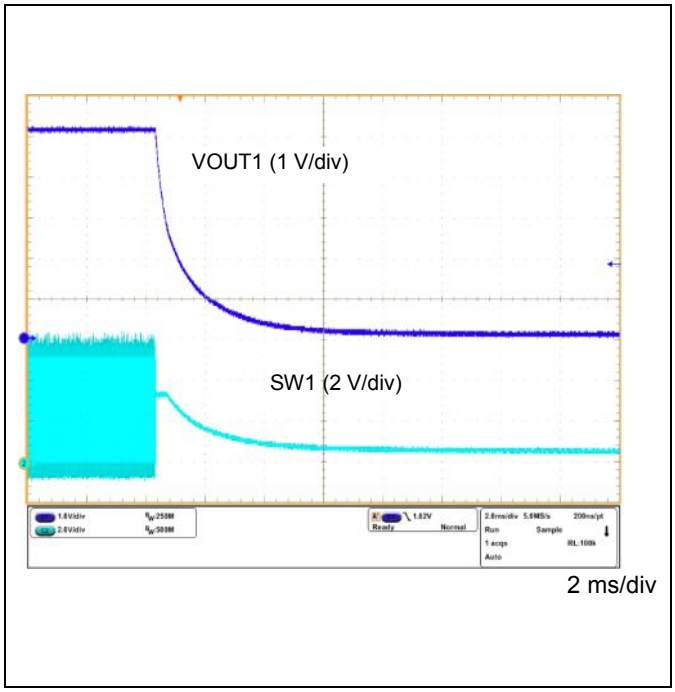


Figure 63. VOUT1 Power OFF Waveform

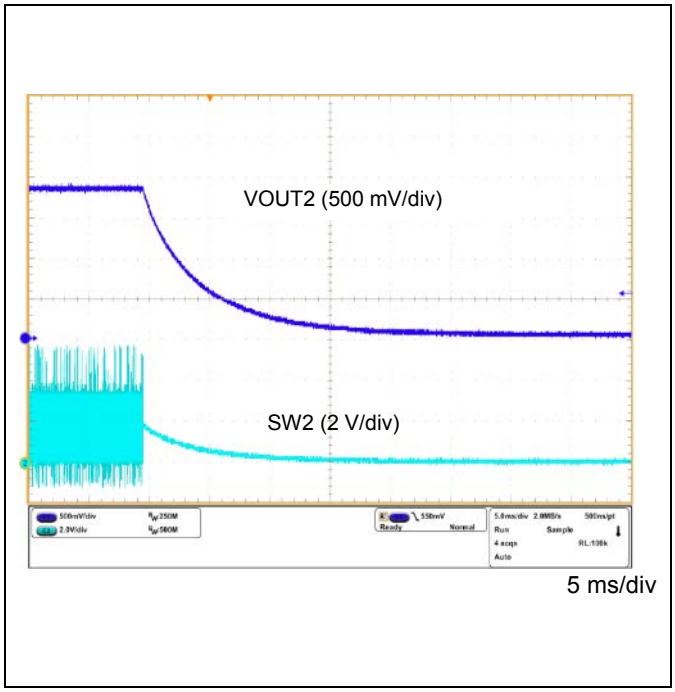


Figure 64. VOUT2 Power OFF Waveform

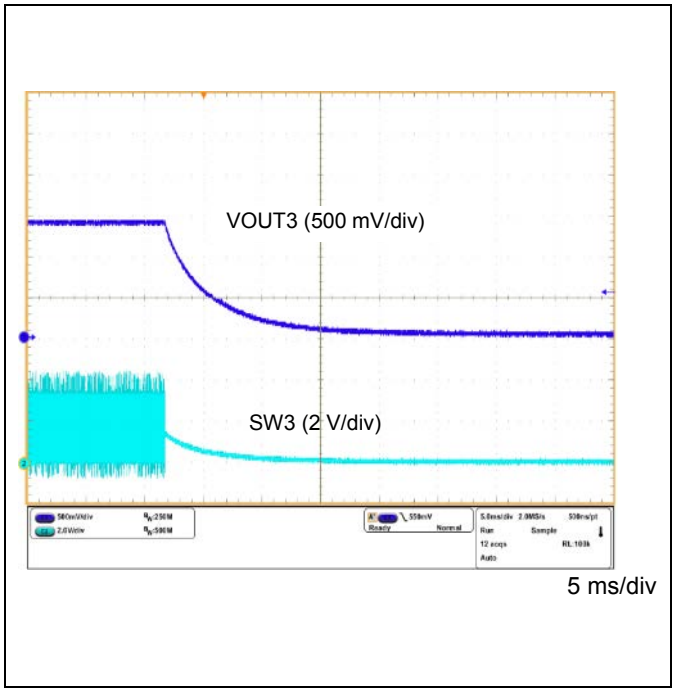


Figure 65. VOUT3 Power OFF Waveform
(VOUT3 = 1.35 V Setting)

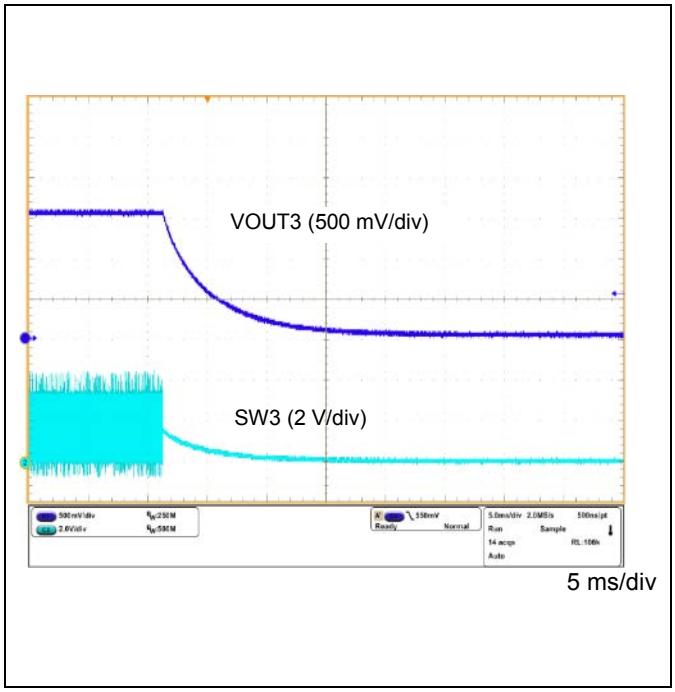


Figure 66. VOUT3 Power OFF Waveform
(VOUT3 = 1.5 V Setting)

6.5 Power OFF Waveform- continued

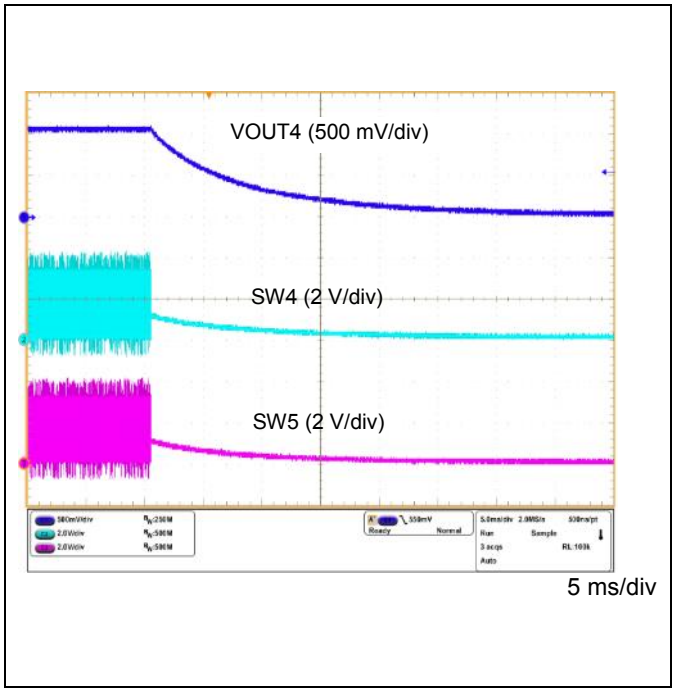


Figure 67. VOUT4 Power OFF Waveform

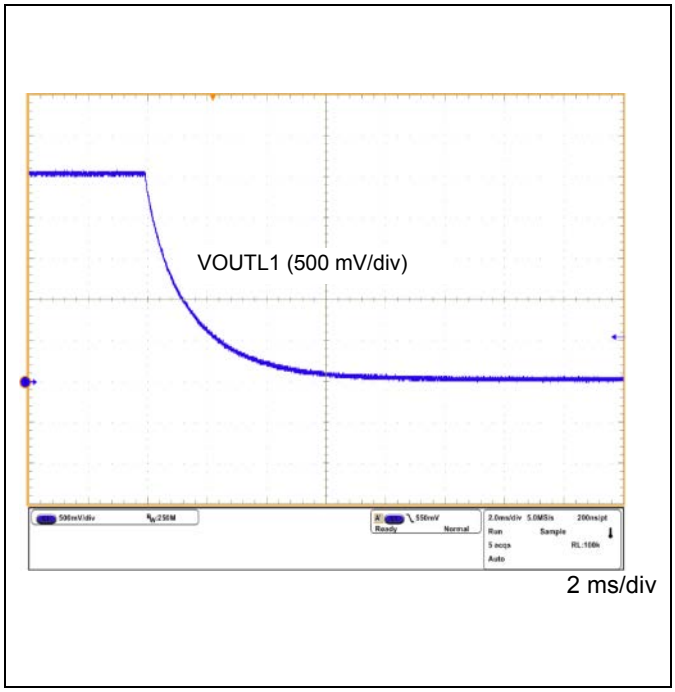


Figure 68. VOUTL1 Power OFF Waveform

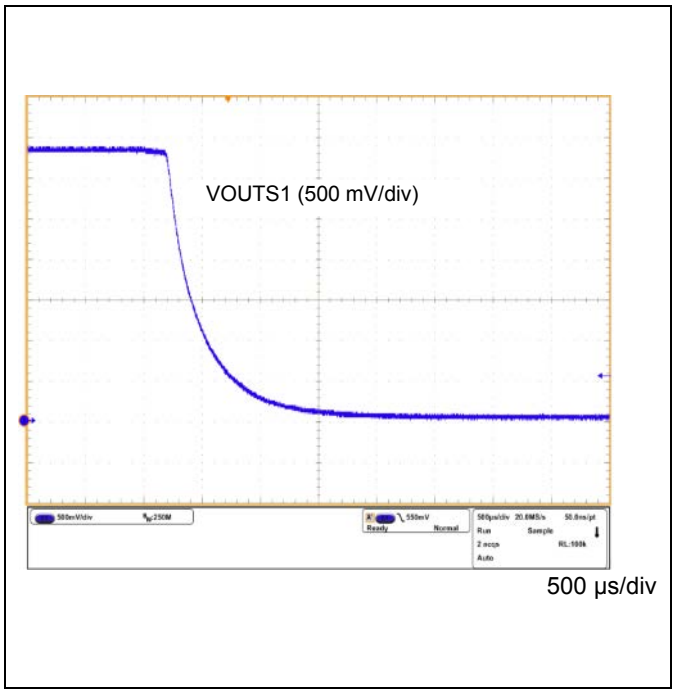


Figure 69. VOUTS1 Power OFF Waveform

6. Typical Performance Curves – continued

6.6 Load Transient

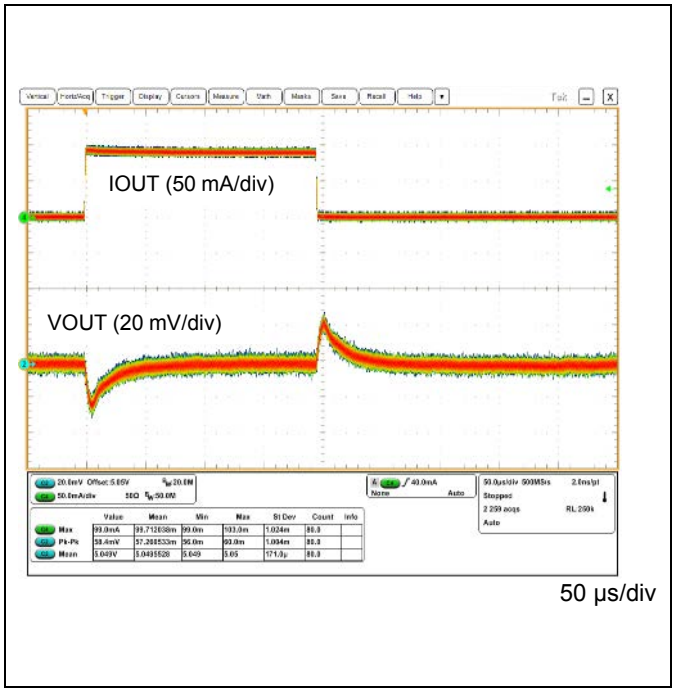


Figure 70. VOUT1 Load Transient
(IOUT = 0 A to 100 mA (SR = 100 mA/µs))

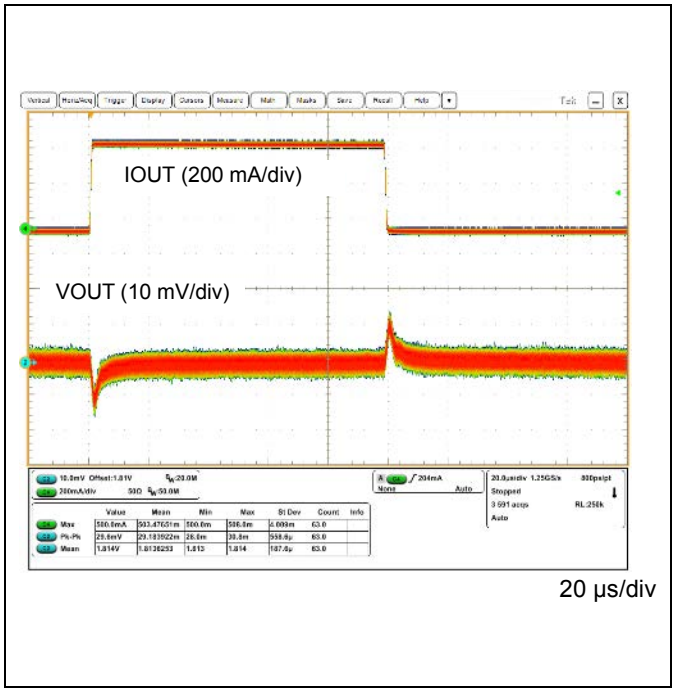


Figure 71. VOUT2 Load Transient
(IOUT = 0 A to 0.5 A (SR = 1 A/µs))

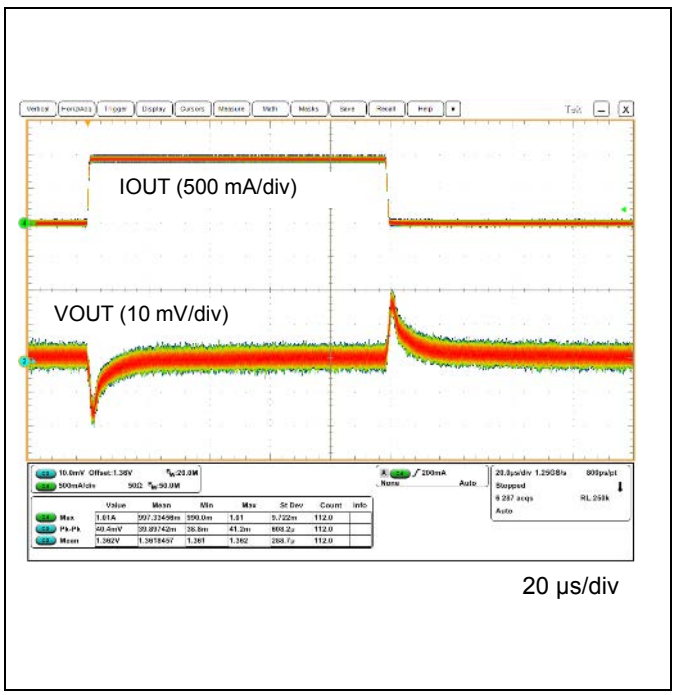


Figure 72. VOUT3 Load Transient
(VOUT3 = 1.35 V Setting, IOUT = 0 A to 1 A (SR = 1 A/µs))

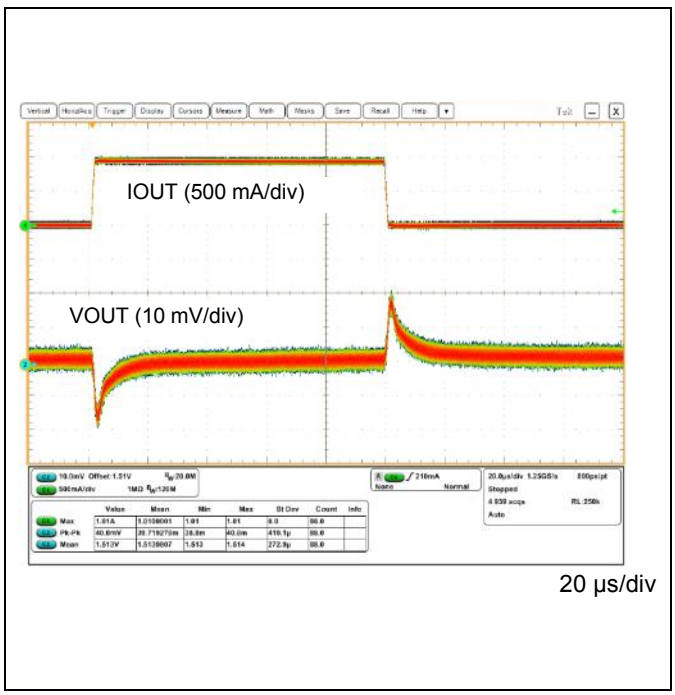


Figure 73. VOUT3 Load Transient
(VOUT3 = 1.5 V Setting, IOUT = 0 A to 1 A (SR = 1 A/µs))

6.6 Load Transient- continued

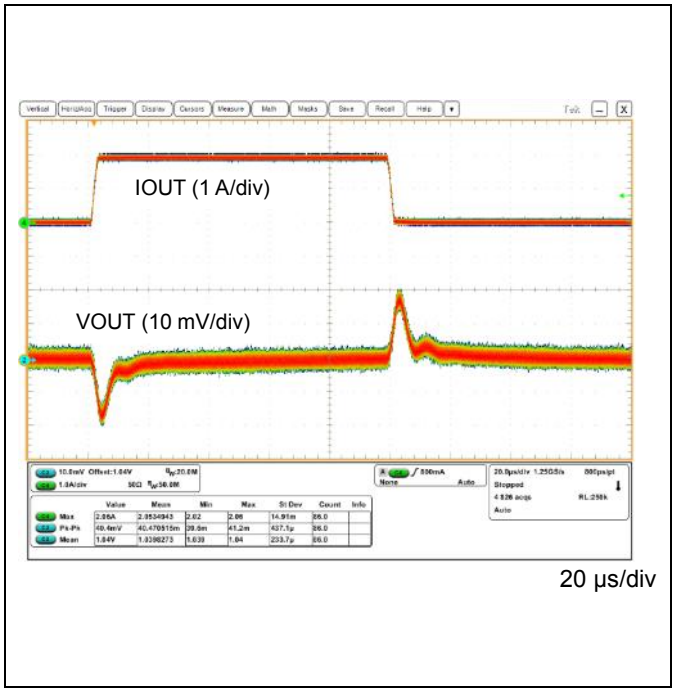


Figure 74. VOUT4 Load Transient
(IOUT = 0 A to 2.05 A (SR = 1 A/µs))

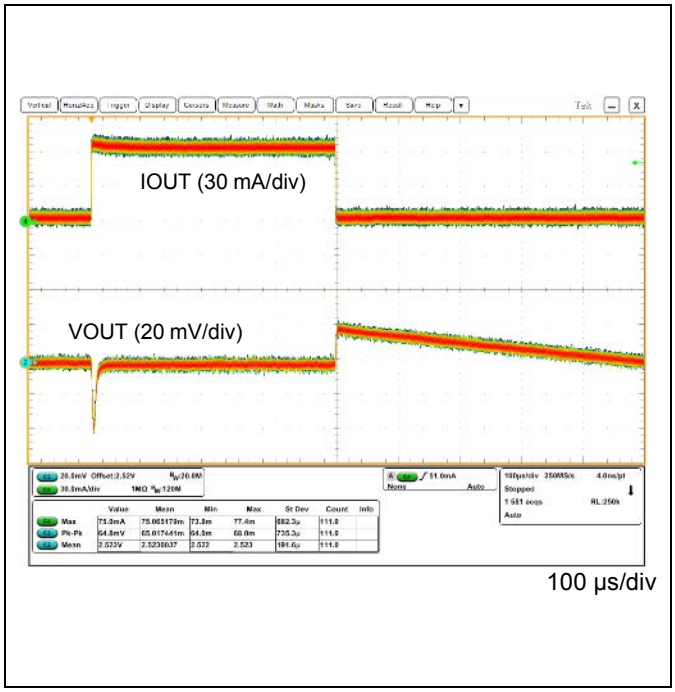


Figure 75. VOUTL1 Load Transient
(IOUT = 0 A to 75 mA (SR = 100 mA/µs)

7. Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

7. Operational Notes – continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

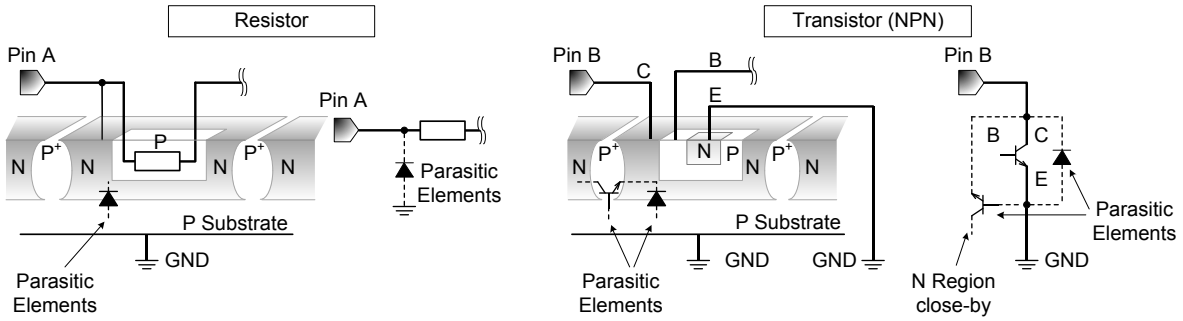


Figure 76. Example of Monolithic IC Structure

7. Operational Notes – continued

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the Tj falls below the TSD threshold.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

8. Revision History

Date	Revision	Changes
29.May.2020	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.