

# Product Change Notification / SYST-10CZPR378

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11-Nov-2021

# **Product Category:**

8-bit Microcontrollers

# **PCN Type:**

Silicon Die Revision

# **Notification Subject:**

ERRATA - PIC1615225/45 Silicon Errata and Data Sheet Clarifications

# **Affected CPNs:**

SYST-10CZPR378\_Affected\_CPN\_11112021.pdf SYST-10CZPR378\_Affected\_CPN\_11112021.csv

### **Notification Text:**

SYST-10CZPR378

Microchip has released a new Product Documents for the PIC1615225/45 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at PIC1615225/45 Silicon Errata and Data Sheet Clarifications.

**Notification Status: Final** 

Description of Change: 1) Added new silicon rev. B1. 2) Updated Table 2. 3) Added silicon erratum items 1.1.1, 1.2.1, 1.3.1,

and 1.4.1.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Estimated First Ship Date: 11 Nov 2021

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices: Traceability Code

Attachments:
PIC1615225/45 Silicon Errata and Data Sheet Clarifications
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### SYST-10CZPR378 - ERRATA - PIC1615225/45 Silicon Errata and Data Sheet Clarifications

# Affected Catalog Part Numbers (CPN)

PIC16F15225-E/MG

PIC16F15225-E/P

PIC16F15225-E/SL

PIC16F15225-E/ST

PIC16F15225-I/MG

PIC16F15225-I/P

PIC16F15225-I/SL

PIC16F15225-I/ST

PIC16F15225T-I/SL

PIC16F15245-E/P

PIC16F15245-E/REB

PIC16F15245-E/SO

PIC16F15245-E/SS

PIC16F15245-I/P

PIC16F15245-I/REB

PIC16F15245-I/SO

PIC16F15245-I/SS

PIC16F15245-I/SSVAO

PIC16F15245T-I/REB

PIC16F15245T-I/SSVAO

# PIC16F15225/45

# PIC16F15225/45 Silicon Errata and Data Sheet Clarifications

The PIC16F15225/45 devices that you have received conform functionally to the current device data sheet (DS20006389**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC16F15225/45 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

**Table 1. Silicon Device Identification** 

Part Number	Device ID	Revision ID	
Fait Nullibel	Device iD	В0	
PIC16F15225	0x30EF	0x2040	
PIC16F15245	0x30F0	0x2040	



Important: Refer to the **Device/Revision ID** section in the current "**PIC16F152xx Family Programming Specification**" (DS40002149) for more detailed information on Device Identification and Revision IDs for a specific device.

**Table 2. Silicon Issue Summary** 

Madula	Facture	Itam Na	la a constant a consta	Affected	Revisions
Module	Feature	Item No.	Issue Summary	В0	B1
Pulse-Width Modulation (PWM)	PWM Mode	1.1.1	Duty cycle values are incorrect	x	х
Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)	Transmit Mode	1.2.1	Possible duplicate byte transmitted	Х	X
Host Synchronous Serial Port (MSSP)	Start and Stop Interrupt Function	1.3.1	A race condition can cause the Start and/or Stop flags to be set when I <sup>2</sup> C is enabled	x	х
Development Support	Low-Voltage Programming	1.4.1	Low-Voltage Programming is not possible when V <sub>DD</sub> is below BORV while BOR is enabled	X	x
Note: Only those issues	indicated in the last colu	mn annly to	o the current silicon revision		

**Note:** Only those issues indicated in the last column apply to the current silicon revision.

### 1. Silicon Errata Issues



**Notice:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

## 1.1 Module: Pulse-Width Modulation (PWM)

### 1.1.1 Wrong Duty Cycle for CCP Module

While in PWM mode and the Timer2 prescaler is configured to 1:1, the duty cycle of the PWM output is as expected. When the Timer2 prescaler is changed to a value other than 1:1, while T2PR = 0 (PWM resolution of two bits), the expected duty cycle is wrong. The corrected duty cycle values are shown in the table below.

Table 1-1. Corrected Duty Cycle Values

Prescaler/CCPR	0	1	2	3	4
1:1	0%	25%	50%	75%	100%
1:2	50%	75%	50%	75%	100%
1:41:128	75%	75%	75%	75%	100%

#### Work around

None.

#### **Affected Silicon Revisions**

В0	B1			
X	X			

# 1.2 Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

#### 1.2.1 Double Byte Transmit

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

#### Work around

Method 1: Monitor the Transmit Interrupt Flag (TXIF) bit. Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty. If using this method, ensure that the second byte is filled in the TXREG before bit 6 of the first byte is transmitted. If the delay is more than six bit times, there is a possibility of double byte transmission.

Method 2: Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty. This work around can be applied if back-to-back transmissions are not necessary.

#### **Affected Silicon Revisions**

В0	B1			
X	X			

#### 1.3 Module: Host Synchronous Serial Port (MSSP)

#### I<sup>2</sup>C Start and/or Stop Flags May Be Set When I<sup>2</sup>C Is Enabled 1.3.1

When I<sup>2</sup>C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I<sup>2</sup>C interrupts if enabled.

#### Work around

Use the following procedure to correctly detect the Start and Stop conditions:

- Disable the Start and Stop conditions interrupt functions.
- Enable the I<sup>2</sup>C module.
- Wait 250 ns+ six instructions cycles (F<sub>OSC</sub>/4).
- Clear the Start and Stop conditions interrupt flags.
- Enable the Start and Stop conditions interrupt functions if used.

```
SSPxCON3bits.SCIE = 0;
                                       // Disable Start condition interrupt
SSPxCON3bits.PCIE = 0;
                                       // Disable Stop condition interrupt
                                       // Enable I2C
SSPxCON1bits.SSPEN = 1;
                                       // Wait for 250 ns + 6 instruction cycles (F_{OSC}/4)
Delay();
PIRxbits.SSPxIF = 0;
                                       // Clear the MSSP interrupt flag
SSPxCON3bits.SCIE = 1;
                                       // Enable Start condition interrupt if used
SSPxCON3bits.PCIE = 1;
                                       // Enable Stop condition interrupt if used
```

#### Affected Silicon Revisions

В0	B1			
X	X			

#### Module: Low-Voltage In-Circuit Serial Programming<sup>™</sup> (LVP) 1.4

#### 1.4.1 Low-Voltage Programming Not Possible

Low-Voltage Programming is not possible when V<sub>DD</sub> is below the selected BORV voltage level, while BOR is enabled.

#### Work around

Method 1: Disable BOR to use Low-Voltage Programming.

Method 2: Raise V<sub>DD</sub> above the selected BORV level while using Low-Voltage Programming.

#### **Affected Silicon Revisions**

В0	B1			
X	X			

**Errata** 

# 2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (20006389**C**):

#### Note:

Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.

# 2.1 None

There are no known data sheet clarifications as of this publication date.

**Errata** 

# 3. Appendix A: Revision History

Doc Rev.	Date	Comments
В	10/2021	Updated Table 2. Added silicon erratum items 1.1.1, 1.2.1, 1.3.1, and 1.4.1. Added new silicon Rev B1.
Α	11/2020	Initial document release

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