



Product Change Notification / ALAN-15FPNL260

Date:

14-Dec-2021

Product Category:

General Purpose FPGAs, Radiation Tolerant FPGAs, System On Chip FPGAs

PCN Type:

Document Change

Notification Subject:

eSign# E000077600 Final Notice: Implement change of memory density from 4GB to 2GB on selected Microsemi M2GLxx, RT4Gxx and 5962-16xx device families available in various packages.

Affected CPNs:

[ALAN-15FPNL260_Affected_CPN_12142021.pdf](#)
[ALAN-15FPNL260_Affected_CPN_12142021.csv](#)

Notification Text:

PCN Status:Final Notification

PCN Type:Document Change

Microchip Parts Affected:Please open one of the files found in the Affected CPNs section.
Note: For your convenience Microchip includes identical files in two formats (.pdf and .xls)

Description of Change:Implement change of memory density from 4GB to 2GB on selected Microsemi M2GLxx, RT4Gxx and 5962-16xx device families available in various packages.

Pre and Post Change Summary:

	Pre Change	Post Change
Memory Density	4GB is originally documented in the RTG4, IGLOO2 and SmartFusion2	2GB will be documented in the RTG4, IGLOO2 and SmartFusion2 Product

Product briefs and the DDR Memory Controller User Guides as well as supported by Libero SoC software

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CN: RTG4, SmartFusion2, and IGLOO2 DDR Controller Memory Density Support can be view on the link below: <https://www.microchip.com/product-change-notifications/Data/ALAN-15FPNL260/RTG4,%20SmartFusion2,%20and%20IGLOO2%20DDR%20Controller%20Memory%20Density%20Support.pdf>

Impacts to Data Sheet:None

Change Impact:None

Reason for Change:To improve productivity by implementing change of memory density from 4GB to 2GB.

Change Implementation Status:In Progress

Estimated Implementation Date:

December 16, 2021 (date code: 2151)

Time Table Summary:

	December 2021				
Workweek	4 9	5 0	5 1	5 2	5 3
Final PCN Issue Date			X		
Estimated Implementation Date			X		

Method to Identify Change:Traceability code

Qualification Report:Not applicable

Revision History:

December 16, 2021: Issued final notification.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachments:

[RTG4, SmartFusion2, and IGLOO2 DDR Controller Memory Density Support.pdf](#)

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Affected Catalog Part Numbers (CPN)

M2S060T-1FGG676I
M2S060T-1FGG676S0013
M2S060T-1FGG676S0015
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M2S060T-1FGG676S0024
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M2GL090-FGG676



Customer Notification (CN)

Subject: RTG4, SmartFusion2, and IGLOO2 DDR Controller Memory Density Support

Nov 1, 2021

Description:

This customer notification **is to inform of a decrease to** the memory density supported by the RTG4, IGLOO2 and SmartFusion2 Fabric Double-Data Rate (FDDR) controller from 4GB to 2GB. Similarly, the memory density supported by the SmartFusion2 MSS Double-Data Rate (MDDR) controller is decreased from 4GB to 2GB. Specific to RTG4, this change also applies to both East and West FDDR controllers with each limited to 2GB address access.

Reason for Change:

A functional issue has been identified where the FDDR/MDDR configured to support 4GB was unable to access the entire 32-bit AXI address range. Analysis of the FDDR/MDDR hard-IP block design has determined the LPDDR/DDR2/DDR3 Row, Bank, Column address space is limited to 2GB and not 4GB as originally indicated in Libero SoC Software and documented in the RTG4, IGLOO2 and SmartFusion2 Product Briefs and DDR Memory Controller User Guides.

FDDR/MDDR that are configured to access a 4GB DDR memory space (that configures MSB of the 32-bit AXI address to the 4GB DDR memory address) will generate incorrect DDR memory addresses whenever the MSB of the AXI address is asserted. This scenario will result in functional errors in simulation and hardware testing. Designs must not use a DDR memory organization that will exceed a 2GB AXI address to access the entire memory space.

Application Impact:

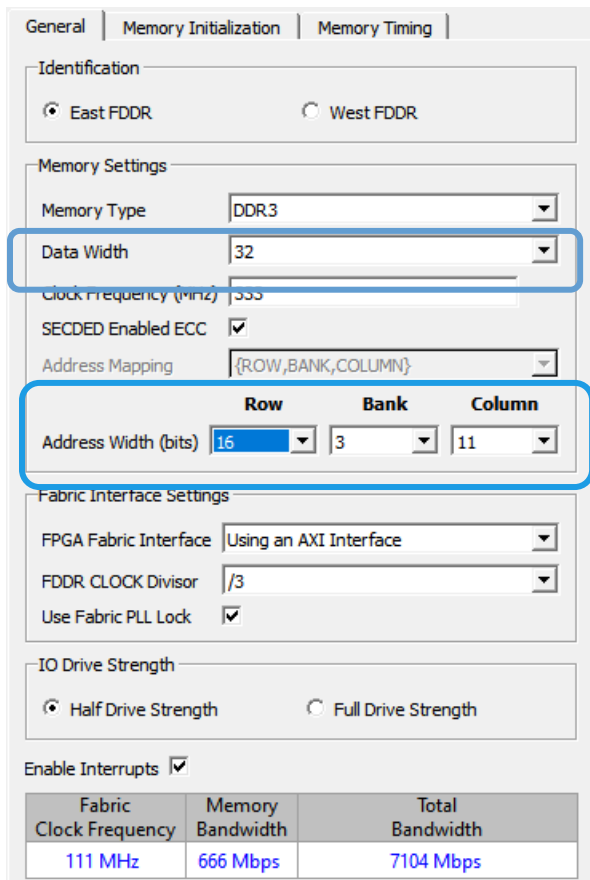
FDDR/MDDR configurations that do not map the MSB of the 32-bit AXI address to the DDR memory address are not affected. In other words, if the AXI address does not exceed a 2GB address space, there is no application impact. Designs with memories greater than 2GB can only access up to 2GB of the memory.



How to assess if configuration of memory controller is addressing more than 2GB.

From the Libero Configurator, below

- Total LPDDR/DDR2/DDR3 address bits = Row+ Bank + Column
- Total LPDDR/DDR2/DDR3 addressable data bits = $2^{\text{address bits}} * \text{(word size aka Data Width)}$
- Total LPDDR/DDR2/DDR3 addressable bytes = $(\text{addressable data bits})/8$

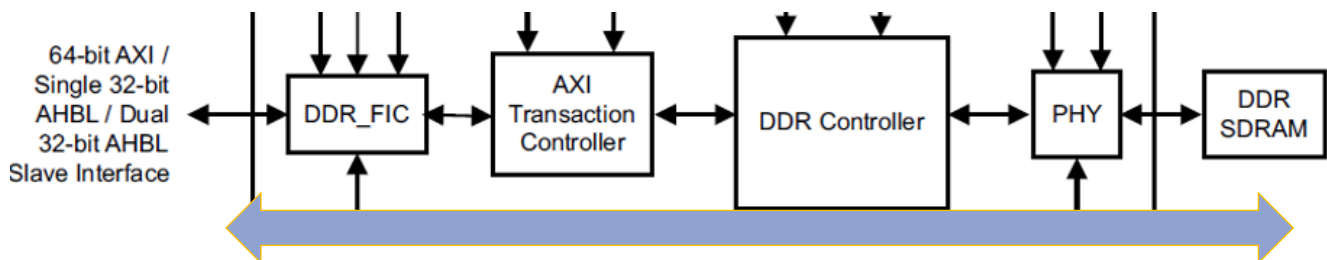


Example: Row = 16, Bank = 3, Column = 11

Total LPDDR/DDR2/DDR3 address bits = 30

Total LPDDR/DDR2/DDR3 addressable data bits = $2^{30} * 32 = 34,359,738,368$

Total LPDDR/DDR2/DDR3 addressable bytes = $34,359,738,368/8 = 4,294,967,296 = 4GB$





Required Action:

No action is required for designs that do not address more than 2GB with the FDDR/MDDR controller hard-IP blocks in RTG4, IGLOO2, and SmartFusion2.

For designs experiencing the functional issue described above, or those planning to address more than 2GB, the following conditions must be reviewed:

- Ensure that the Libero FDDR/MDDR configuration does not map the AXI address to a 4GB DDR memory address.

- Designs with memories greater than 2GB can only access up to 2GB of the memory.

Contact Information:

If you have any questions about this subject, contact Microchip FPGA-BU Technical Support at the web portal below:

<http://www.microchip.com/support>

Regards,

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