Figure 1. FRDMGD31RPEVM
2 Important notice

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3 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

The tool summary page for FRDMGD31RPEVM is at http://www.nxp.com/FRDMGD31RPEVM. The overview tab provides an overview of the device, product features, a description of the kit contents, a list of (and links to) supported devices, a list of (and links to) any related products, and a Get Started section.

The Get Started section provides links to everything needed to start using the device and contains the most relevant, current information applicable to the FRDMGD31RPEVM.

1. Go to http://www.nxp.com/FRDMGD31RPEVM.
2. On the Overview tab, locate the Jump To navigation feature on the left side of the window.
3. Select the Get Started link, review each entry, and download an entry by clicking the title.
4. After reviewing the Overview tab, visit the other product-related tabs for additional information:
   • Documentation: download current documentation
   • Software & Tools: download current hardware and software tools
   • Buy/Parametrics: purchase the product and view the product parametrics

After downloading files, review each file, including the user guide, which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the Get Started section of the Overview tab.

3.1 Kit contents/packing list

The FRDMGD31RPEVM kit contents include:

• Assembled and tested FRDMGD31RPEVM board in an anti-static bag
• 3.3 V to 5.0 V translator board (KITGD3160TREVB) connected to FRDM-KL25Z
• USB cable, type A male/type mini B male, 3 ft
• Quick start guide
3.2 Required equipment

To use this kit, you need:

- Compatible SiC RoadPak module
- DC link capacitor compatible with the SiC RoadPak module
- 1.27 mm jumpers for configuration (included with kit)
- 30 µH to 50 µH, high current air core inductor for double pulse testing
- HV power supply with protection shield and hearing protection
- 25 V, 1.0 A DC power supply
- 500 MHz 2.5 GS/s 4-channel oscilloscope
- Rogowski coil, PEM Model CWT Mini HF60R, or CTW MiniHF30 (smaller diameter)
- Isolated high-voltage probe (CAL Test Electric CT2593-1, LeCroy AP030)
- Digital voltmeter

3.3 System requirements

The kit requires the following to function properly with the software:

- Windows 7 or higher operating system

4 Getting to know the hardware

4.1 Overview

The FRDMGD31RPEVM is a half-bridge evaluation kit populated with two GD3100 single channel gate drive devices. The kit includes the Freedom KL25Z microcontroller hardware for interfacing a PC installed with FlexGUI software for communication to the serial peripheral interface (SPI) registers on the GD3100 gate drive devices in either daisy chain or standalone configuration.

The KITGD3160TREV host board is used to translate 3.3 V signals to 5.0 V signals between the MCU and GD3100 gate drivers. The evaluation kit can be connected to a compatible insulated gate bipolar transistor (IGBT) or SiC module for half-bridge evaluations and applications development.

4.2 Board features

- Capability to connect to RoadPak SiC module for half-bridge evaluations
- Negative VEE gate low drive level (−3.9 V DC)
- VCCREG regulated high gate drive level (+15 V DC)
- Jumper configurable for disabling dead time fault protection when short-circuit testing
- Easy access power, ground, and signal test points
- Easy to install and use FlexGUI for interfacing via SPI through PC; software includes double pulse and short-circuit testing capability
- DC link bus voltage monitor on low-side driver via AMUXIN and AOUT
- Negative temperature coefficient (NTC) connection and configurable for monitoring module temperature
4.3 Device features

Table 1. Device features

<table>
<thead>
<tr>
<th>Device</th>
<th>Description</th>
<th>Features</th>
</tr>
</thead>
</table>
| GD3100 | The GD3100 is an advanced single channel gate driver for IGBTs. | • Compatible with current sense and temp sense IGBTs  
• DESAT detection capability for detecting $V_{CE}$ desaturation condition  
• Fast short-circuit protection for IGBTs with current sense feedback  
• Compliant with automotive safety integrity level (ASIL) C/D ISO 26262 functional safety requirements  
• SPI interface for safety monitoring, programmability, and flexibility  
• Integrated galvanic signal isolation  
• Integrated gate drive power stage capable of 10 A peak source and sink  
• Interrupt pin for fast response to faults  
• Compatible with negative gate supply  
• Compatible with 200 V to 1700 V IGBTs, power range > 125 kW |

4.4 Board description

The FRDMGD31RPEVM is a half-bridge evaluation board populated with two GD3100 single channel IGBT or SiC gate drive devices. The board supports connection to an FRDM-KL25Z microcontroller for SPI communication configuration programming and monitoring. The board includes DESAT circuitry for short-circuit detection and implementation of GD3100 shutdown protection capabilities.

The evaluation board is designed to connect to a RoadPak SiC metal-oxide-semiconductor field-effect transistor (MOSFET) for evaluation of the GD3100 performance and capabilities.
4.4.1 Low-voltage logic and control connector

Low-voltage domain is 12 V VSUP domain that interfaces with the MCU and GD3100 control registers through the 24-pin connector interface.

Low-side driver and high-side driver domains are driver control interfaces to RoadPak module single phase connections and test points.
Table 2. Low-voltage domain 24-pin connector definitions

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AOUTL</td>
<td>analog output duty cycle encoded signal (low side) for reading temperature via TSENSEA or voltage via AMUXIN</td>
</tr>
<tr>
<td>2</td>
<td>n.c.</td>
<td>not connected</td>
</tr>
<tr>
<td>3</td>
<td>CSBL</td>
<td>chip select bar (low side)</td>
</tr>
<tr>
<td>4</td>
<td>n.c.</td>
<td>not connected</td>
</tr>
<tr>
<td>5</td>
<td>PWML</td>
<td>pulse width modulation (PWM) input (low side)</td>
</tr>
<tr>
<td>6</td>
<td>INTBL</td>
<td>interrupt bar (low side)</td>
</tr>
<tr>
<td>7</td>
<td>MOSIL</td>
<td>master out slave in (low side)</td>
</tr>
<tr>
<td>8</td>
<td>SCLK</td>
<td>serial clock input</td>
</tr>
<tr>
<td>9</td>
<td>MISOL</td>
<td>master in slave out (low side)</td>
</tr>
<tr>
<td>10</td>
<td>n.c.</td>
<td>not connected</td>
</tr>
<tr>
<td>11</td>
<td>FSSTATEL</td>
<td>fail-safe state (low side)</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>ground</td>
</tr>
<tr>
<td>13</td>
<td>FSENB</td>
<td>fail-safe enable (high side and low side)</td>
</tr>
<tr>
<td>14</td>
<td>MISOH</td>
<td>master in slave out (high side)</td>
</tr>
</tbody>
</table>
Table 2. Low-voltage domain 24-pin connector definitions...

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>n.c.</td>
<td>not connected</td>
</tr>
<tr>
<td>16</td>
<td>MOSIH</td>
<td>master out slave in (high side)</td>
</tr>
<tr>
<td>17</td>
<td>n.c.</td>
<td>not connected</td>
</tr>
<tr>
<td>18</td>
<td>CSBH</td>
<td>chip select bar (high side)</td>
</tr>
<tr>
<td>19</td>
<td>LED_PWR</td>
<td>USB 3.3 V power for INTB LEDs (high side and low side)</td>
</tr>
<tr>
<td>20</td>
<td>AOUTH</td>
<td>duty cycle encoded signal (high side)</td>
</tr>
<tr>
<td>21</td>
<td>PWMH</td>
<td>PWM input (high side)</td>
</tr>
<tr>
<td>22</td>
<td>FSSTATEH</td>
<td>fail-safe state (high side)</td>
</tr>
<tr>
<td>23</td>
<td>GND</td>
<td>ground</td>
</tr>
<tr>
<td>24</td>
<td>INTBH</td>
<td>interrupt bar (high side)</td>
</tr>
</tbody>
</table>

4.4.2 Test point definitions

All test points are clearly marked on the evaluation board. Figure 4 shows the location of various test points.

Figure 4. Key test point locations
<table>
<thead>
<tr>
<th>Test point</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Low-voltage domain</strong></td>
<td></td>
</tr>
<tr>
<td>VSUP</td>
<td>DC voltage source connection point for VSUP power input of GD3100 devices. Typically supplied by vehicle battery +12 V DC.</td>
</tr>
<tr>
<td>GND1</td>
<td>grounding points for low-voltage domain</td>
</tr>
<tr>
<td>INTBL</td>
<td>interrupt bar low-side test point</td>
</tr>
<tr>
<td>INTBH</td>
<td>interrupt bar high-side test point</td>
</tr>
<tr>
<td><strong>Low-side driver domain</strong></td>
<td></td>
</tr>
<tr>
<td>VCCL</td>
<td>positive voltage supply test point for isolated circuitry and low-side driver domain</td>
</tr>
<tr>
<td>DSTL</td>
<td>( V_{CE} ) desaturation test point connected to low-side driver DESAT pin and circuitry</td>
</tr>
<tr>
<td>VEEL</td>
<td>negative voltage supply test point for low-side driver gate of IGBT or SiC module</td>
</tr>
<tr>
<td>VDC</td>
<td>DC link voltage test point at voltage divider</td>
</tr>
<tr>
<td>VRFL</td>
<td>5.0 V reference test point for isolated analog circuitry on low-side driver</td>
</tr>
<tr>
<td>GNDISOL</td>
<td>low-side driver grounding points</td>
</tr>
<tr>
<td>GL</td>
<td>module gate test point on low-side driver domain which is the charging pin of gate; including MMCX probe connection</td>
</tr>
<tr>
<td>COLL</td>
<td>collector test point/connection terminal on low side</td>
</tr>
<tr>
<td><strong>High-side driver domain</strong></td>
<td></td>
</tr>
<tr>
<td>VCCH</td>
<td>positive voltage supply test point for isolated circuitry and high-side driver domain</td>
</tr>
<tr>
<td>DSTH</td>
<td>( V_{CE} ) desaturation test point connected to high-side driver DESAT pin and circuitry</td>
</tr>
<tr>
<td>VEEH</td>
<td>negative voltage supply test point for high-side driver gate of IGBT or SiC module</td>
</tr>
<tr>
<td>AMXH</td>
<td>analog MUX input test point for high-side driver</td>
</tr>
<tr>
<td>VRFH</td>
<td>5.0 V reference test point for isolated analog circuitry on high-side driver</td>
</tr>
<tr>
<td>TSNS1</td>
<td>NTC1 test point at module and TSENSEH high-side</td>
</tr>
<tr>
<td>TSNS2</td>
<td>NTC2 test point at module and GNDISOH</td>
</tr>
<tr>
<td>GNDISOH</td>
<td>high-side driver grounding points</td>
</tr>
<tr>
<td>GH</td>
<td>module gate test point on high-side driver domain which is the charging pin of gate; including MMCX probe connection</td>
</tr>
<tr>
<td>COLH</td>
<td>collector test point/connection high side</td>
</tr>
</tbody>
</table>
4.4.3 Power supply and jumper configuration

**Table 4. Jumper definitions**

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Position</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWMHSEL (J10)</td>
<td>1-2</td>
<td>dead time fault protection enabled (high side)</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>dead time fault protection disabled (use for short-circuit testing)</td>
</tr>
<tr>
<td>PWMLSEL (J9)</td>
<td>1-2</td>
<td>dead time fault protection enabled (low side)</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>dead time fault protection disabled (use for short-circuit testing)</td>
</tr>
</tbody>
</table>
4.4.4 Bottom view

Figure 6. Evaluation board bottom view

4.4.5 Gate drive resistors

- RGH - gate high resistor in series with the GH pin at the output of the GD3100 gate high driver and RoadPak module gate that controls the turn-on current for SiC MOSFET gate.
- RGL - gate low resistor in series with the GL pin at the output of the GD3100 gate low driver and RoadPak module gate that controls the turn-off current for SiC MOSFET gate.
- RAMC - series resistor between RoadPak module gate and AMC input pin of the GD3100 driver for gate sensing and active Miller clamping.
4.4.6 LED interrupt indicators

Figure 7. Gate drive resistors

Figure 8. LED interrupt indicators
Table 5. LED interrupt indicators

<table>
<thead>
<tr>
<th>LED</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-side INTB</td>
<td>connected to the INTB output pin of low-side driver indicating reported</td>
</tr>
<tr>
<td></td>
<td>fault status when on (active LOW)</td>
</tr>
<tr>
<td>High-side INTB</td>
<td>connected to the INTB interrupt output pin of high-side driver indicating</td>
</tr>
<tr>
<td></td>
<td>reported fault status when on (active LOW)</td>
</tr>
</tbody>
</table>

4.5 Kinetis KL25Z Freedom board

The Freedom KL25Z is an ultra low-cost development platform for Kinetis L series MCU built on Arm Cortex-M0+ processor.
4.6 3.3 V to 5.0 V translator board

KITGD3160TREVB translator enables level shifting of signals from MCU 3.3 V to 5.0 V SPI communication.

Table 6. Translator board jumper definitions

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Position</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCSEL (J3)</td>
<td>1-2</td>
<td>selects 5.0 V for 5.0 V compatible gate drive</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>selects 3.3 V for 3.3 V compatible gate drive</td>
</tr>
<tr>
<td>PWMH_SEL (J4)</td>
<td>1-2</td>
<td>selects PWM high-side control from KL25Z MCU</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>selects PWM high-side control from fiber optic receiver inputs</td>
</tr>
<tr>
<td>PWML_SEL (J5)</td>
<td>1-2</td>
<td>selects PWM low-side control from KL25Z MCU</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>selects PWM low-side control from fiber optic receiver inputs</td>
</tr>
</tbody>
</table>

5 Configuring the hardware

FRDMGD31RPEVM is connected to compatible SiC MOSFET RoadPak module with a DC link capacitor as shown in Figure 11. Double pulse and short-circuit testing can be conducted utilizing Windows based PC with FlexGUI software.
Suggested equipment needed for test:

- Rogowski coil high-current probe
- High-voltage differential voltage probe
- High sample rate digital oscilloscope with probes
- DC link capacitor (power ring 700D407 425 μF, 900 V DC)
- SiC MOSFET RoadPak module
- Windows based PC
- High-voltage DC power supply for DC link voltage
- Low-voltage DC power supply for VSUP
  - +12 V DC gate drive board low-voltage domain
- Voltmeter for monitoring high-voltage DC link supply
- Load coil for double pulse and short-circuit testing

Figure 11. Evaluation board and system setup

6 Installation and use of software tools

Software for FRDMGD31RPEVM is distributed with the FlexGUI tool (available on NXP.com). Necessary firmware comes pre-installed on the FRDM-KL25Z with the kit.

Even if the user intends to test with other software or PWM, it is recommended to install this software as a backup or to help debugging.
6.1 Installing FlexGUI on your computer

The latest version of FlexGUI supports the GD3100 and GD3160. It is designed to run on any Windows 10 or Windows 8 based operating system. To install the software, do the following:

1. Go to [www.nxp.com/FlexGUI](http://www.nxp.com/FlexGUI) and click Download.
2. When the FlexGUI software page appears, click Download and select the version associated with your PC operating system.
3. FlexGUI wizard creates a shortcut, an NXP FlexGUI icon appears on the desktop. By default, the FlexGUI executable file is installed at `C:\flexgui-app-des-gd31xx.exe`. Installing the device drivers overwrites any previous FlexGUI installation and replaces it with a current version containing the GD31xx drivers. However, configuration files (.spi) from the previous version remain intact.

6.2 Configuring the FRDM-KL25Z microcode

![Figure 12. FRDM-KL25Z setup and interface](aaa-038800)

By default, the FRDM-KL25Z delivered with this kit is preprogrammed with the current and most up-to-date firmware available for the kit.

A way to check quickly that the microcode is programmed and the board is functioning properly, is to plug the KL25Z into the computer, open FlexGUI, and verify that the software version at the bottom is 6.4 or later (see Figure 13).

If a loss of functionality following a board reset, reprogramming, or a corrupted data issue, the microcode may be rewritten per the following steps:

1. To clear the memory and place the board in boot loader mode, hold down the reset button while plugging a USB cable into the OpenSDA USB port.
2. Verify that the board appears as a BOOTLOADER device and continue with step 3. If the board appears as KL25Z, you may go to step 6.
3. Download the Firmware Apps .zip archive from the PEmicro OpenSDA webpage (http://www.pemicro.com/opensda/). Validate your email address to access the files.
4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA and copy/drag-and-drop into the BOOTLOADER device.
5. Reboot the board by unplugging and replugging the connection to the OpenSDA port. Verify now that the device appears as a KL25Z device to continue.

6. Locate the most recent KL25Z firmware; which is distributed as part of the FlexGUI package.
   a. From the FlexGUI install directory, which is located in the flexgui-app-des-gd31xx\bin folder and is named in the form "flexgui-fw-KL25Z_usb_hid_gd31xxC_vx.x.x.bin".
   b. This .bin file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the translator board as part of FRDMGD31RPEVM.

7. With the KL25Z still plugged through the OpenSDA port, copy/drag-and-drop the .bin file into the KL25Z device memory. Once done, disconnect the USB and plug into the other USB port, labeled KL25Z.
   a. The device may not appear as a distinct device to the computer while connected through the KL25Z USB port, this is normal.

8. The FRDM-KL25Z board is now fully set up to work with FRDMGD31RPEVM and the FlexGUI.
   a. There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in non-volatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplugging event.

6.3 Using the FlexGUI

The FlexGUI is available from [http://www.nxp.com/FlexGUI](http://www.nxp.com/FlexGUI) as an evaluation tool demonstrating GD31xx-specific functionality, configuration, and fault reporting. FlexGUI also includes basic capacity for the FRDMGD31RPEVM to control an IGBT or SiC module, enabling double pulse or short-circuit testing.

SPI messages can be realized graphically or in hexadecimal format. CSB is selectable to address one or both GD31xx on the board via daisy chain. See Figure 13 to Figure 32 for FlexGUI for GD31xx internal register read and write access.

Starting FlexGUI for GD31xx

- FlexGUI install program (flexgui-app-des-gd31xx-0.x.x.exe)
- Download FlexGUI and run the install program on your PC.
- When you start the application, Figure 13 allows you to select the target application board, feature set (standard or daisy chain), target MCU, and USB interface. Leave all settings as shown.
FlexGUI settings

- Access settings by selecting Settings from the File menu
• The Loader and Logs settings are shown below:

![Loader settings](image1)

**Figure 15. Loader settings**

![Logs settings](image2)

**Figure 16. Logs settings**
• Access settings by selecting Settings from the File menu.
• The Register Map and Tabs settings are shown below:

Figure 17. Register map settings

Figure 18. Tabs settings
Command Log window

- The Command Log area informs the user about application events.

![Command Log area](image)

**Figure 19. Command Log area**

Global workspace controls

- Always visible in the lower left corner of the main application window.
  - GD3160 tab functionality
    - Switch modes between run and configuration mode
    - Set SPI frequency

![Device pins settings and status menus](image)

**Figure 20. Device pins settings and status menus**
• Pins tab functionality
  – Set control levels. Default values are shown.
  – Read and automatically poll INTB pins (INTA pins are added for GD3160).
  – Control pins set values to a default to a functional state.
    – FSENB - enable/disable fail-safe enable
    – EN_PS - enables flyback supply on EVB at 17 V VCC on high side and low side
    – FSSTATEL and FSSTATEH set the fail-safe state when FSENB is enabled
    – PWML and PWMH set the default state PWM inputs for high side and low side

Figure 21. Pins tab functionality

• Status tab functionality
  – Monitors Status 1 and Status 2 fault bits. Bits that are set are shown in red.
  – Ability to clear all faults and automatically poll status registers.

Figure 22. Status tab functionality
• Analog tab functionality
  – Read and poll ADC values from the high-voltage domain
  – Displays raw ADC and converted values

![Analog tab functionality](image1.png)

Figure 23. Analog tab functionality

Register map

• Registers are grouped according to function; independent lines to read and write the registers
• Individual registers can be read by clicking the R button and can be written by using the W button.
• Copy button to copy the read values to the write line; can be set to copy automatically
• Reset button to undo the changes on the write line and reset to the previous value
• Global register controls perform the selected command on all registers with the checkbox selected.

![Register map](image2.png)

Figure 24. Register map
Gate Drive tab
- Allows setting of parameters related to the gate drive; controls are disabled when not in config mode
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

Figure 25. Gate drive tab

Current Sense tab
- Allows setting of parameters related to current sense
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.
DESAT & Seg Drive tab

- Allows setting of parameters related to desat and segmented drive
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.
Overtemperature tab

- Allows setting of parameters related to overtemperature and overtemperature warning thresholds
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

Undervoltage threshold tab

- Allows setting of parameters related to undervoltage threshold
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.
Measurements tab

- Allows monitoring and graphing of ADC and temperature values

![Measurements tab diagram]

Figure 30. Measurements tab

Status tab

- Allows monitoring of Status 1, Status 2, and Status 3 register values
- Status 1 and Status 2 faults can be cleared
- Status mask registers can be modified when in configuration mode
Pulse tab

- Used for double pulse, short circuit, and PWM testing
- Select desired T1, T2, and T3 timings for each test type; select enable then generate pulses

6.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debug may be needed.
<table>
<thead>
<tr>
<th>Problem</th>
<th>Evaluation</th>
<th>Explanation</th>
<th>Corrective action(s)</th>
</tr>
</thead>
</table>
| No PWM output (no fault reported) | Check PWM jumper position on translator board | Incorrect PWM jumpers obstruct signal path but not report fault | Set PWMH_SEL (J4) and PWML_SEL (J5) jumpers properly, for desired control method:  
- 3.3 V to 5.0 V translator board reviewed in Section 4.6 |
| | Check PWM control signal | Ensure that proper PWM signal is reaching GD3100 | Monitor EXT_PWML (TP14) and EXT_PWMMH (TP15) for commanded PWM state |
| | Check FSENB status (see GD3100 pin 15, STATUS5) | PWM is disabled when FSENB = LOW | Set pin FSENB = HIGH (pin 15) to continue |
| | Check CONFIG_EN bit (MODE2) | PWM is disabled when CONFIG_EN is logic 1 | Write CONFIG_EN = logic 0 to continue |
| No PWM output (fault reported) | Check VGE fault (VGE_FLT) | A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate. | Clear VGE_FLT bit (STATUS2) to continue, increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault. |
| | Check for short-circuit fault (SC) in STATUS1 register | SC is a severe fault that disables PWM. SC fault cannot be masked | Clear SC fault to continue. Consider adjusting SC fault settings on GD3100:  
- Adjust short-circuit threshold setting (CONFIG2)  
- Adjust short-circuit filter setting (CONFIG2) |
| PWM output is good, but with persistent fault reported | Check for dead time fault (DTFLT) in STATUS2 register | Dead time is enforced, but fault indicates that PWM controls signals are in violation | Clear DTFLT fault bit (STATUS2), Check PWMHSEL (J10) and PWMLSEL (J9) are configured to bypass dead time faults. Consider adjusting dead time settings on GD3100:  
- Change mandatory PWM dead time setting (CONFIG5)  
- Mask dead time fault (MSK2) |
| | Check for overcurrent (OC) fault in STATUS1 register | OC fault latches, but does not disable PWM. OC fault cannot be masked. | Clear OC fault bit (STATUS1), Adjust OC fault detection settings on GD3100:  
- Adjust overcurrent threshold setting (CONFIG1)  
- Adjust overcurrent filter setting (CONFIG1) |
| PWM or FSSTATE rising edge has longer delay than falling edge | Check translator output voltage versus GD3100 VDD voltage | Low translator output voltage (compared with correct VDD at GD3100) causes the high threshold at the GD3100 pin to be crossed later than commanded | Check translator output voltage selection (J233) is configured to the same level as the GD3100 VDD. Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/pulldown |
| WDOG_FLT reported on startup | Check VSUP and VCC are powered | On initialization, watchdog fault is reported when one die is powered up before the other | Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue. |
| SPIERR reported on startup | Check KL25Z/translator connection | On initialization, SPIERR can occur when the SPI bus is open, or when GD3100 IC is powered up before the translator (which provides CSB). | Clear SPIERR fault to continue. Reinitialize power to GD3100 after translator is powered (over USB). |
## Problem

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<th>Explanation</th>
<th>Corrective action(s)</th>
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<td>SPIERR reported after SPI message</td>
<td>Check bit length of message sent</td>
<td>There is SPIERR if SCLK does not see a n’24 multiple of cycles</td>
<td>Use 24-bit message length for SPI messages</td>
</tr>
<tr>
<td></td>
<td>Check CRC</td>
<td>SPIERR faults if CRC provided in sent message is not good</td>
<td>Use FlexGUI to generate commands with valid CRC. The command can be copied in binary or hexadecimal and sent from another program.</td>
</tr>
<tr>
<td></td>
<td>Check for sufficient dead time between SPI messages</td>
<td>SPIERR fault bit is set when the time between SPI messages (txfer_delay) received is too short. Minimum required delay time is 19 µs.</td>
<td>Check time between CSB rising edge (old message end) and CSB falling edge (new message start) during normal SPI read, and ensure transfer delay dead time check. SPIERR can also be cleared in BIST.</td>
</tr>
<tr>
<td>VCCREGUV reported on startup</td>
<td>Check VCCREG potential</td>
<td>Caused by low VCC</td>
<td>Clear VCCREGUV fault bit (STATUS1). Tune VCC-GNDISO potential with power supply set resistor (R20).</td>
</tr>
<tr>
<td>VREFUV reported on startup</td>
<td>Check HV domain is powered correctly</td>
<td>Related to slow rise time of VCC supply on HV domain, or failed VREF regulator</td>
<td>Clear VREFUV bit (STATUS2). Reset HV domain supply if fault bit does not clear.</td>
</tr>
<tr>
<td></td>
<td>Check VCC for undervoltage condition</td>
<td>Low VCC is visible indirectly through other HV domain faults</td>
<td>Tune VCC-GNDISO using R20 feedback</td>
</tr>
<tr>
<td>VCCOV fault reported on startup</td>
<td>Check VEE level on suspect domain.</td>
<td>If VEE level is not at desired negative voltage it could cause excessive VCC level.</td>
<td>Check Zener diode in power supply circuit for proper value in setting VEE level. Clear VCCOV bit (STATUS1) to continue.</td>
</tr>
<tr>
<td></td>
<td>Check VCC-GNDISO potential</td>
<td>PWM is disabled during a VCC overvoltage (20 V nom.)</td>
<td>Tune VCC-GNDISO potential to suitable level with power supply set resistor (R22). Clear VCCOV bit (STATUS1) to continue.</td>
</tr>
<tr>
<td>No PWM during short circuit test</td>
<td>Check PWMxSEL jumpers</td>
<td>Incorrect configuration of PWMALT pins prevent short-circuit test by enforcing dead time</td>
<td>For short-circuit test, set PWMLSEL (J9) and PWMHSEL (J10) to bypass dead time. See Section 4.4.3 for details.</td>
</tr>
<tr>
<td>Bad SPI data, appears to repeat previous response</td>
<td>Check VSUP/VDD for undervoltage condition</td>
<td>VDD_UV latches SPI buffer contents, preventing updated fault reporting.</td>
<td>Check voltage provided at VDD pin (pin 3). On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive). Read multiple addresses to ensure a good comparison.</td>
</tr>
<tr>
<td></td>
<td>Check PS_EN is set to HIGH in FlexGUI; see Figure 21</td>
<td>VCC/VEE can be enabled/disabled in software.</td>
<td>Enable VCC/VEE from FlexGUI</td>
</tr>
<tr>
<td></td>
<td>Check VCC for undervoltage</td>
<td>Unpowered VCC prevents HV domain from updating data</td>
<td>Tune VCC-GNDISO using R22 feedback</td>
</tr>
</tbody>
</table>

### 7 Schematics, board layout, and bill of materials


### 8 References


## 9 Revision history

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<tr>
<td>v.2</td>
<td>20210122</td>
<td>Section 6.2 list item 6a: changed FlexGUI version</td>
</tr>
<tr>
<td>v.1</td>
<td>20200803</td>
<td>initial version</td>
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